Practical Aspect in Mixed Signal Circuits

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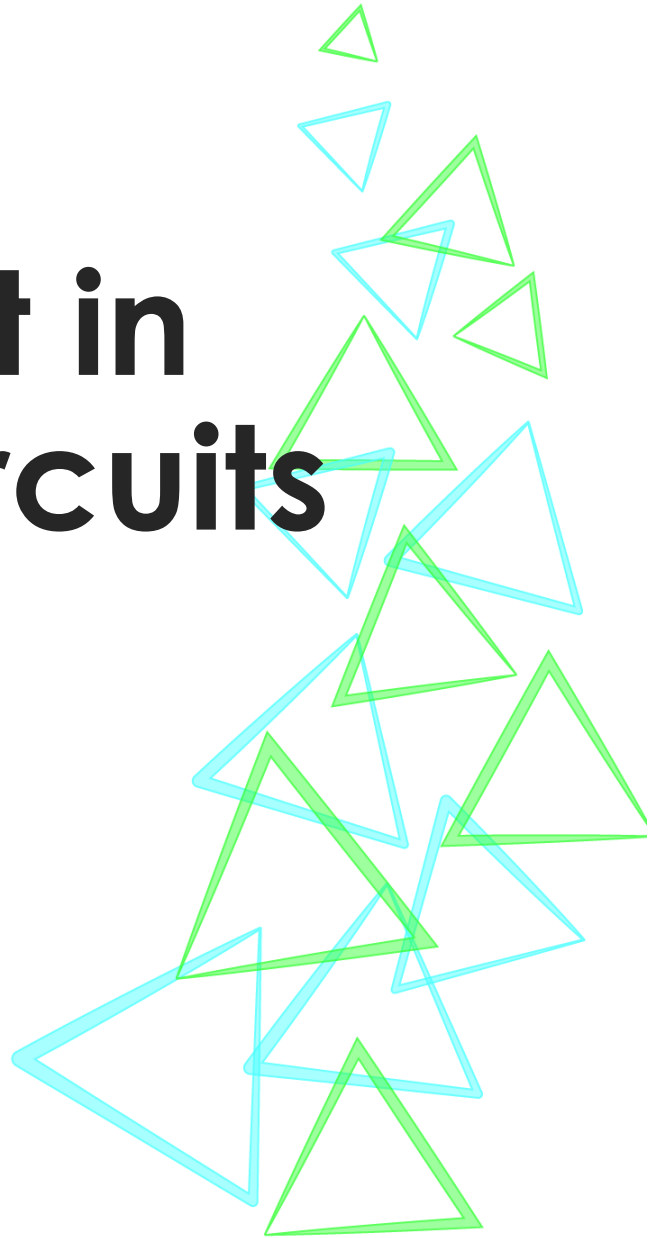
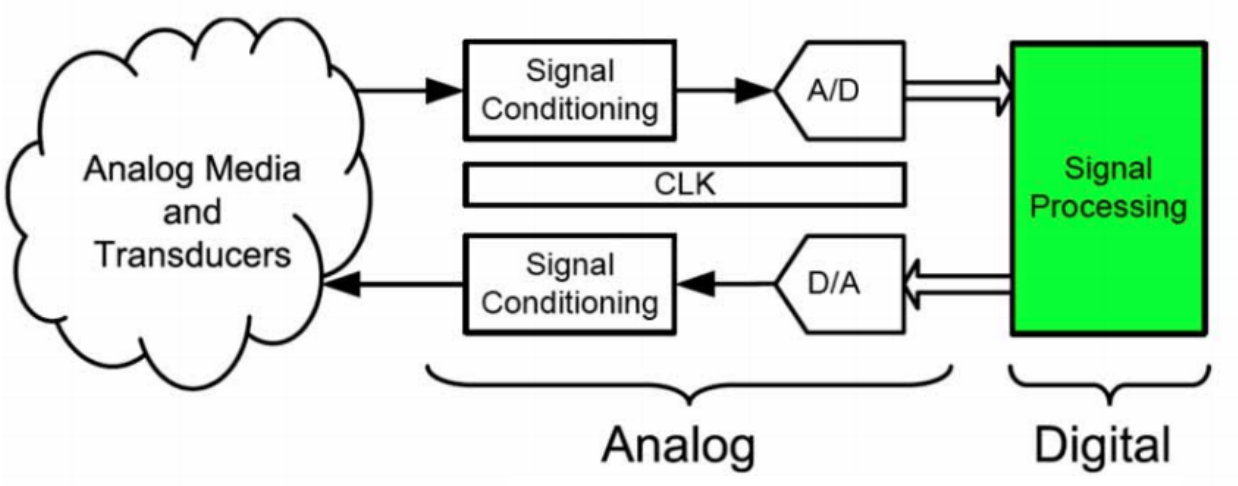
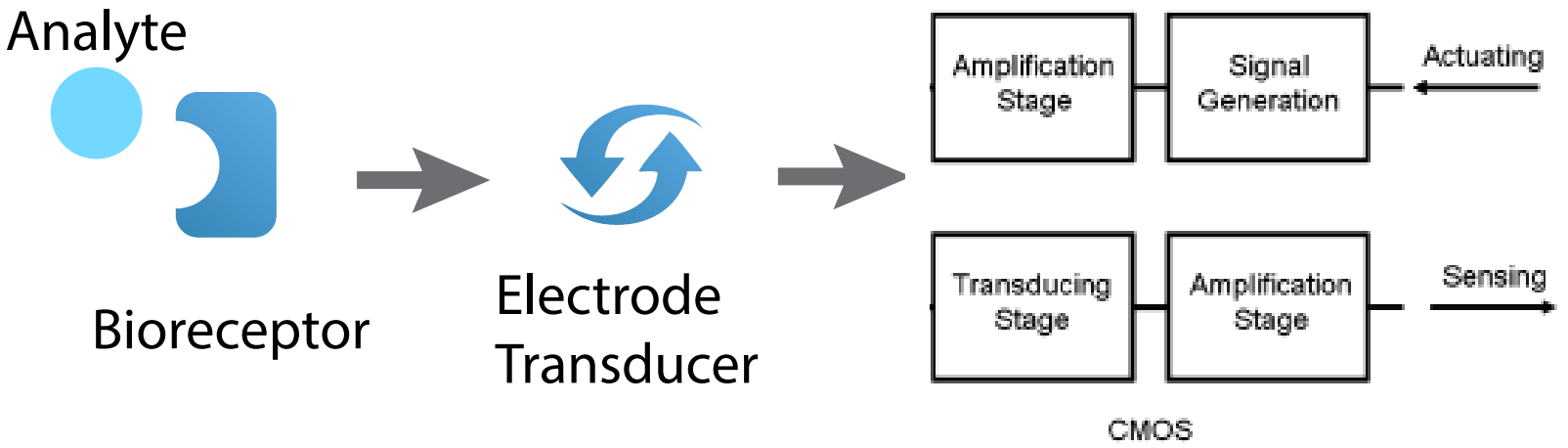


ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

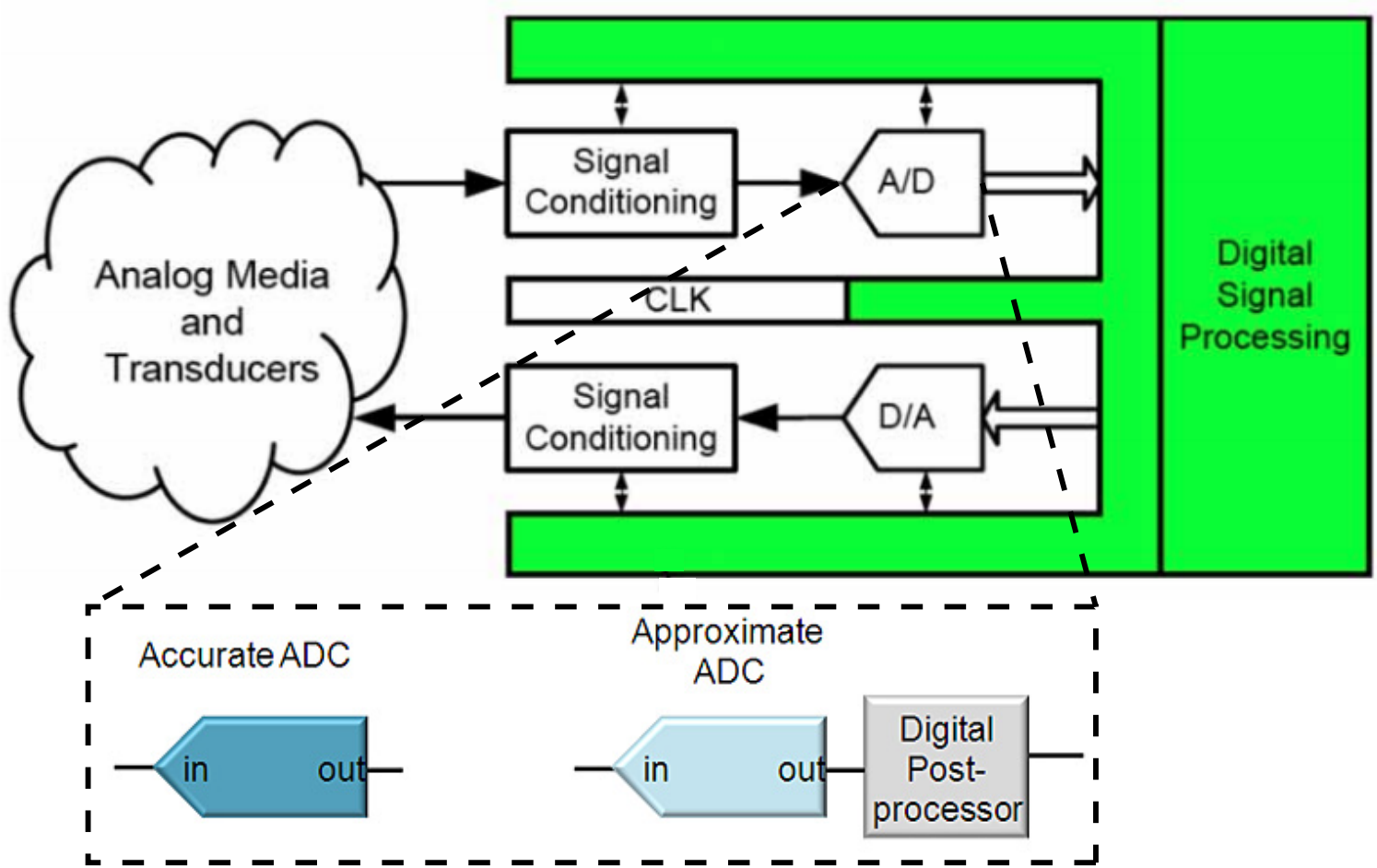
LSI
Integrated Systems Laboratory

Parallelism: mixed signal & biosensor

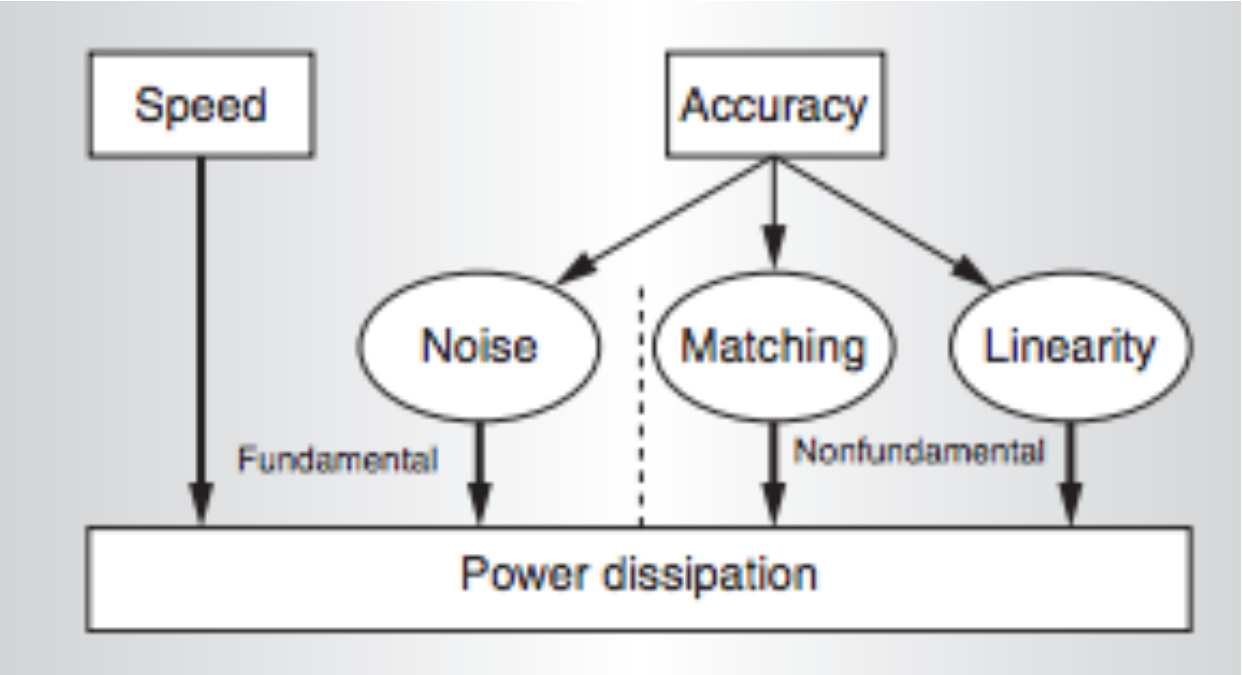




Digital Assisted Analog (DDA)



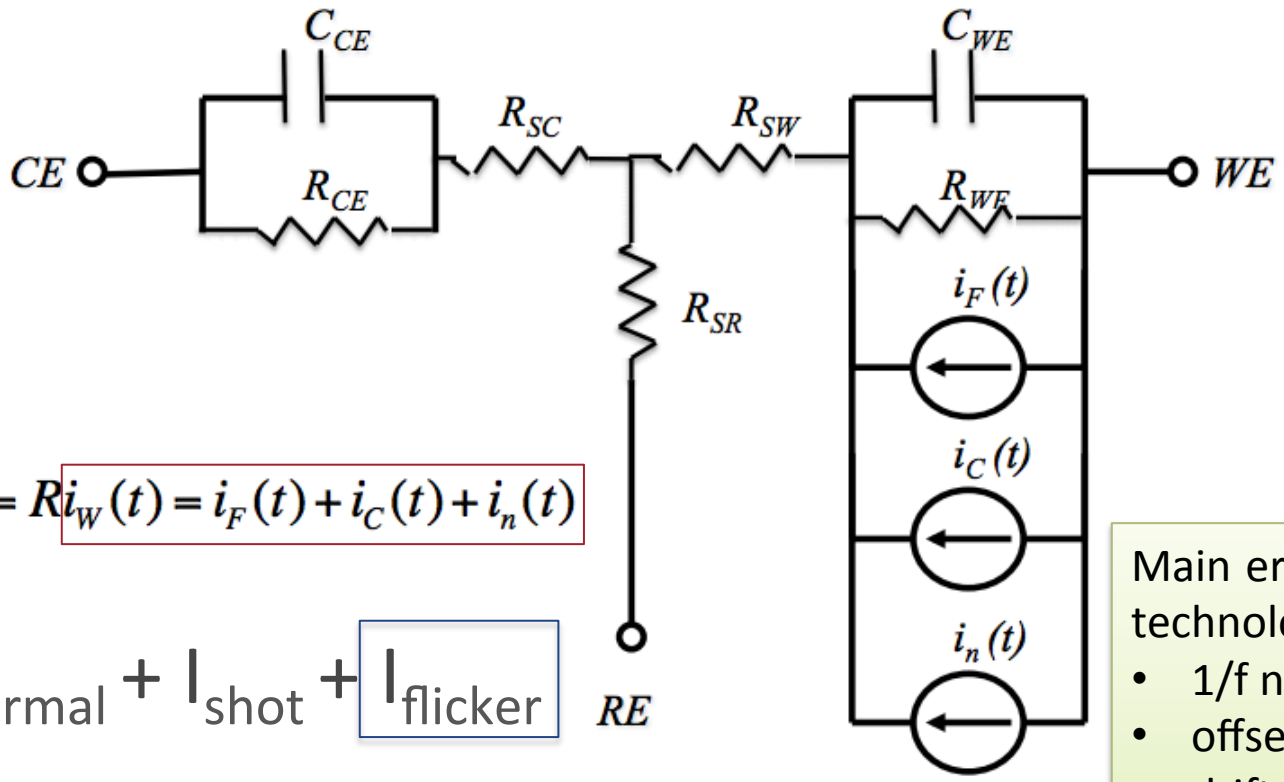
Analog Circuit Trade-off



- Power tends to increase linearly with speed
- Precision is affected by:
  1. thermal noise (caused by random carrier motion),
  2. component matching (inversely proportional to component area),
  3. high linear amplification (sub-optimal in terms of speed and noise).

Total noise in Bio-Application

$$I_w = I_f + I_c + I_n$$



$$V_{out} = R i_W(t) = i_F(t) + i_C(t) + i_n(t)$$

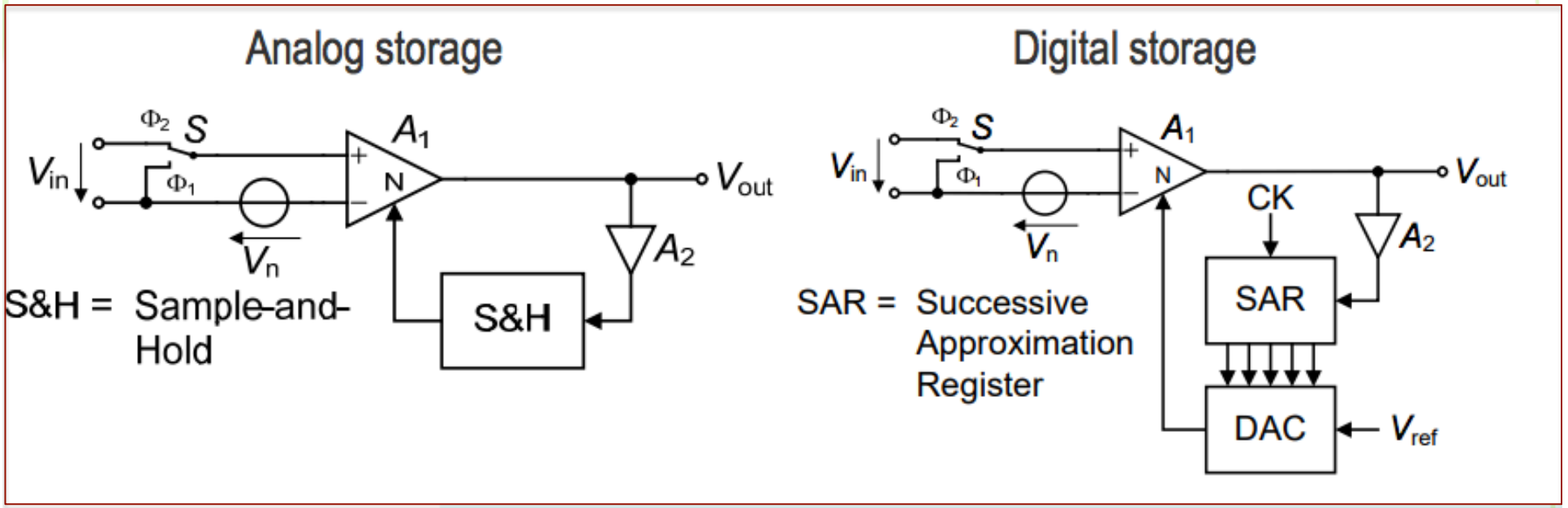
$$I_n = I_{thermal} + I_{shot} + I_{flicker}$$

Main errors in CMOS technology (opAmp)

- 1/f noise
- offset
- drift

Offset Cancellation

- Trimming usually performed during production.
- AutoZeroing (AZ)
- Chopper Stabilization (CS)



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- Trimming
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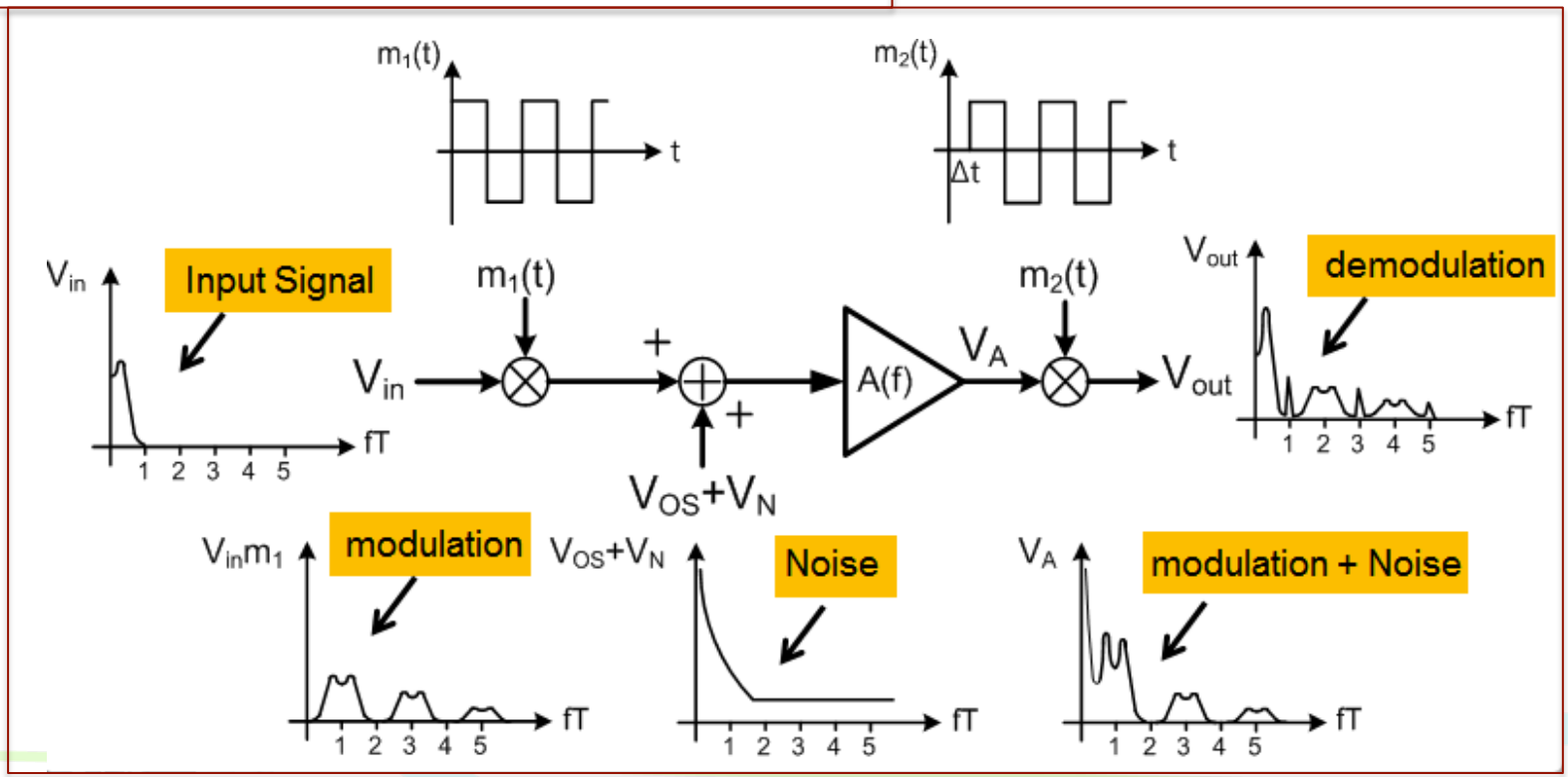
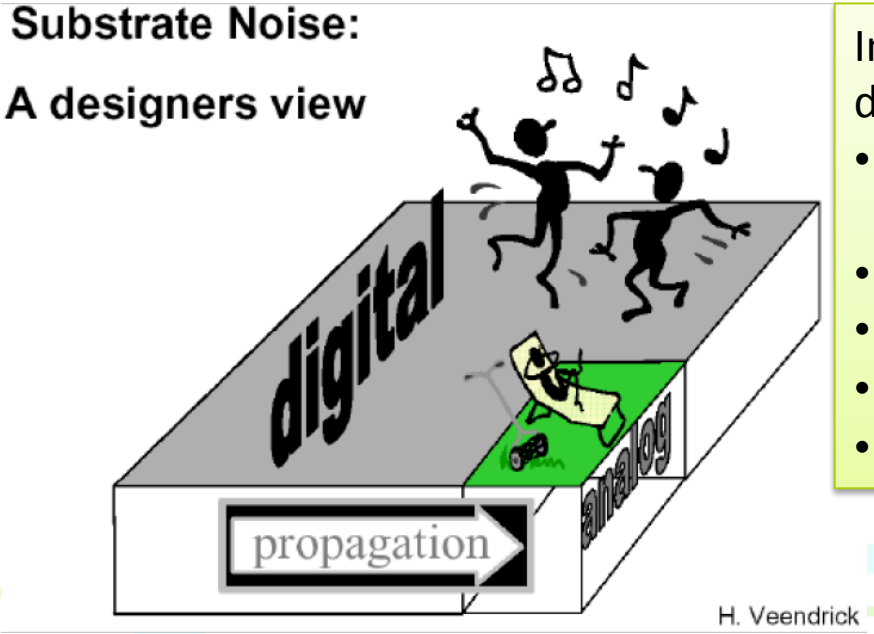


Generalize good co-designing

- **Quiet the talker** (reduce noise generation)
- **Isolate the listener** (sensitive circuit by shielding, guarding rings etc)
- **Close the listener's ears** (make more noise-tolerant)



Important to make right decisions regarding

- placement of components,
- I/Os
- Routing
- Powering
- Decoupling…

ElectroMagnetic Compatibility EMC

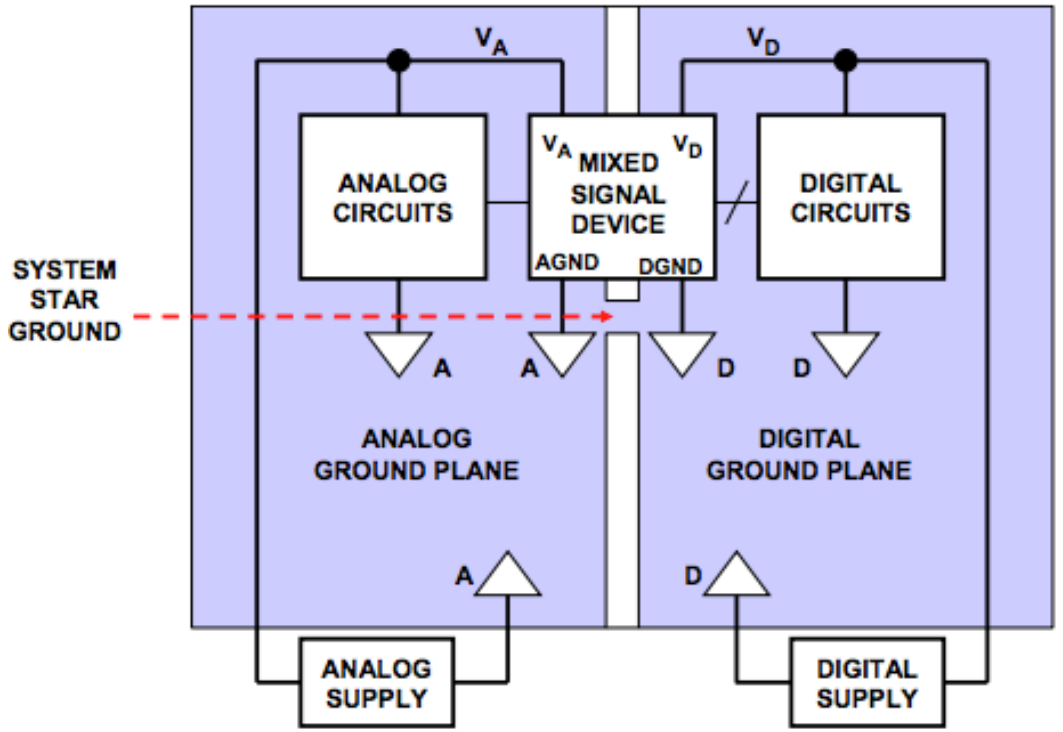
Two main pricinples

1. Current should be returned to their sources locally to avoid loop-antenna.
2. A system should have only one reference plane to not create dipole antenna.

Grounding

PCB Grounding

- **split analog (AGND) and digital ground (DGND)**, not overlapping each other (to minimize coupling)
- connect the GND plane to a single point, normally the power supply -> **STAR GND configuration**



Routing Suggestions

- **minimize** long parallel lines and close proximity of signal traces to reduce inductive coupling,
- minimize long traces on adjacent layer to prevent capacitive coupling,
- route on separate layers signal traces requiring high isolation. If not possible, make them run orthogonally to one another with GND plane in between to minimize capacitive coupling (GND acts as shielding).

Circuit decoupling:
Power Supply Rejection Ration (PSRR)

PSRR = sensitivity of an analog circuit to power supply variations

- Check the **application section in the datasheet** of each component to follow power supply decoupling recommendations.
- Main rules are:
  - **large electrolytic C** (10-100µF) close to chip (reservoir)
  - **small C** (0.01-0.1µF) physically close to power pins (short the high f away from chip),
  - decoupling Cs connected to a large-area low-impedance GND plane through via or short trace,
  - **Optional:** small ferrite bead in series with supply pin (localize the noise, keep external high f noise, keep internally generated noise from propagation to the rest of circuit).

ElectroStatic Discharge (ESD)

Typically a 3000 volt discharge cannot be felt.

If you see a spark the discharge is at least 10,000 volts.

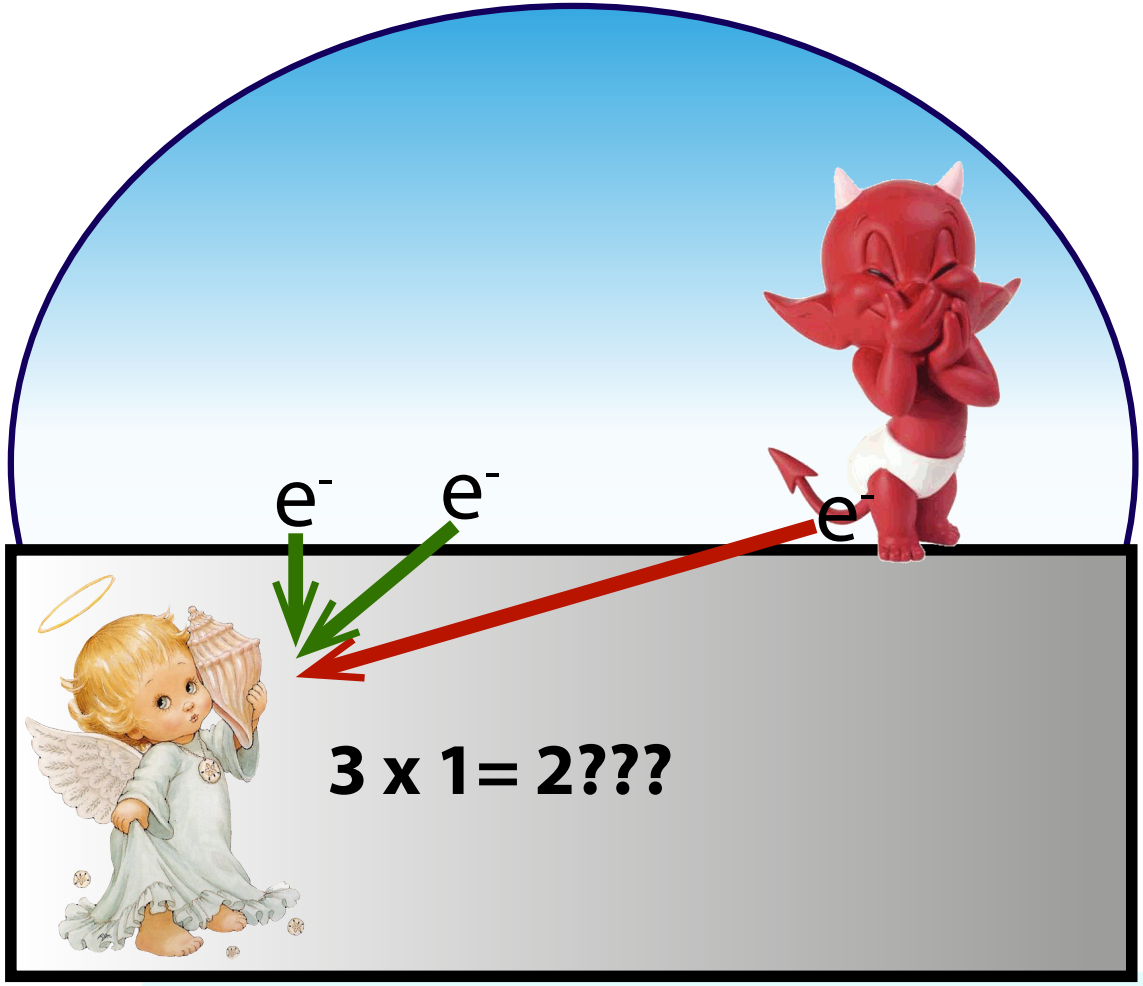
Damage is usually worse to a part not attached to a card/board/system yet!

1kV is new Industry Target for IC protection based on product assembly/manufacturing

ESD Discharge from a person to a device

A person's body obtains a Charge relative to an IC and the Electro Static Discharge equalizes the charge difference.

keep care ☺



References

- Sandro Carrara. Bio/cmos interfaces in constant bias. In Bio/CMOS Interfaces and
- Co-Design, pages 185–205. Springer, 2013.
- QiWang. What is digitally assisted analog design?, 2012.
- Boris Murmann and Bernhard Boser. Digitally assisted analog integrated circuits.
- Queue, 2(1):64, 2004.
- Jan M. Rabaey. The analog to digital tradeoff. 2017.
- Boris Murmann. Digitally assisted analog circuits. IEEE Micro, 26(2):38–47, 2006.
- Christian C Enz and Gabor C Temes. Circuit techniques for reducing the effects of
- op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization.
- Proceedings of the IEEE, 84(11):1584–1614, 1996.
- Christian Enz and Assim Boukhayma. Recent trends in low-frequency noise reduction
- techniques for integrated circuits. In Noise and Fluctuations (ICNF), 2015 International
- Conference on, pages 1–6. IEEE, 2015.
- [Qinwen Fan, Kofi AA Makinwa, and Johan H Huijsing. The chopping technique. In
- Capacitively-Coupled Chopper Amplifiers, pages 11–27. Springer, 2017.
- Tim Schmerbeck. Noise coupling in mixed-mode ics. 2017.
- Sanjay Pithadia and Shridhar More. Grounding in mixed-signal systems demystified,
- part 1. Analog Applications, 2013.
- Walt Kester, James Bryant, and Mike Byrne. Grounding data converters and solving
- the mystery of" agnd" and" dgnd. Analog Devices Tutorial, 2006.
- John Ardizzoni. A practical guide to high-speed printed-circuit-board layout. Analog
- Dialogue, 39(9):1–6, 2005.
- WHAT IS PROPER DECOUPLING and WHYISIT NECESSARY. Decoupling techniques.
- Mini Circuits. The prevention and control of electrostatic discharge (esd). 2015.
- Sanjay Pithadia, and Shridhar More, Grounding in mixed-signal systems demystified, Part 1-2, Analog Applications Journal Texas Instruments Incorporated, 2013.
- Analog Devices, MT-101 TUTORIAL Decoupling techniques: What is proper decoupling and why is it necessary?, 2009.
- Walt Kester, James Bryant, and Mike Byrne , Grounding Data Converters and Solving the Mystery of "AGND" and "DGND", 2009.
- e2v Semiconductors, Design Considerations for Mixed-Singnal How to Design a PCB Layout, 2009.
- John Ardizzoni, A practical guide to High Speed Printed Circuit Board Layout, 2005.
- John R. Barnes dBi Corporation, Designing Electronic Systems For ESD Immunity:Here's A Comprehensive Checklist To Ensure That Your System Is Properly Protected, 2003.
- Partitioning and Layout of a Mixed-Signal PCB, Henry W. Ott, 2001