Solution 11

Exercise 1: AMOLED Pixel Driver Circuits

a) T_2 is easily identifiable as most of the current is passing through it, it is also the biggest structure.

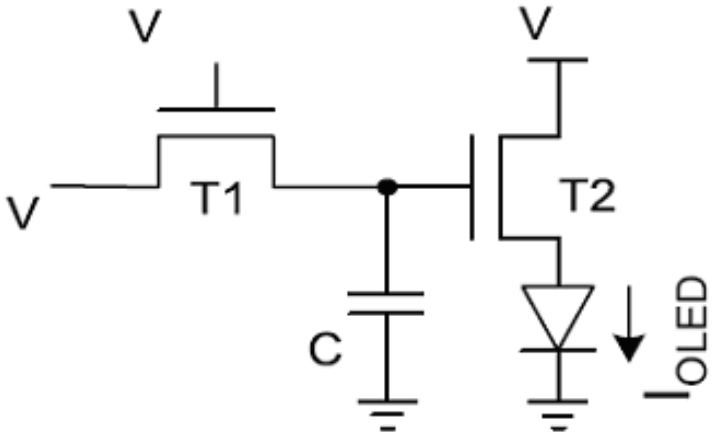


Figure 1: 2-transistors circuit.

From the above circuit, the solution is then given in the following figure. The OLED is the whole black surface, connected via T_2.

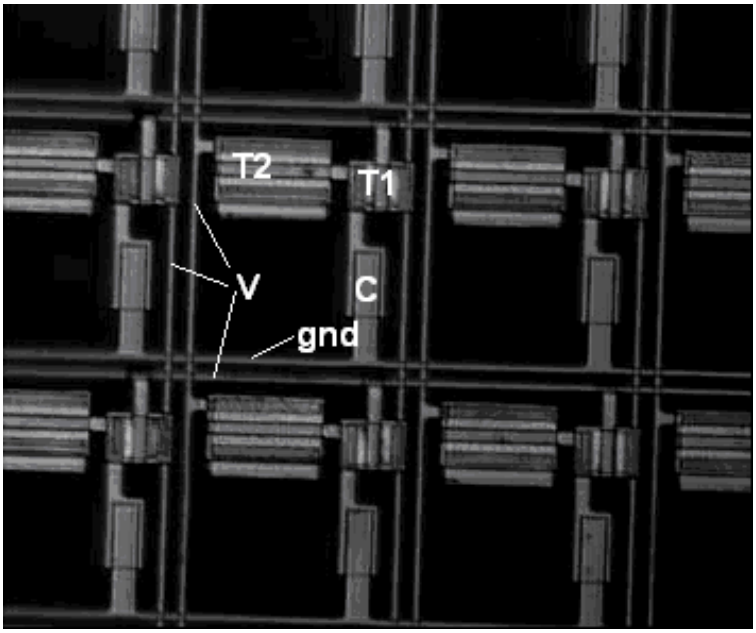
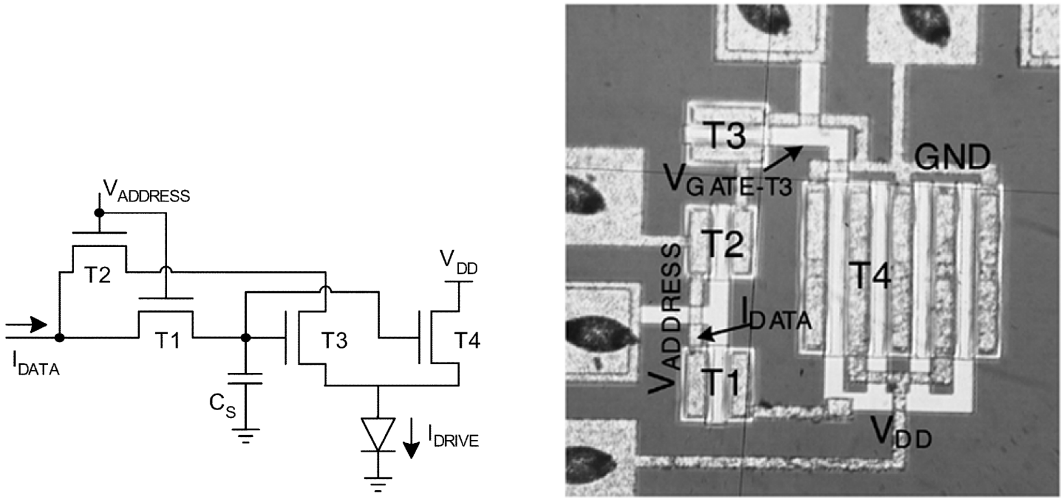


Figure 2: AMOLED pixel circuit.

b) The solution is given by:

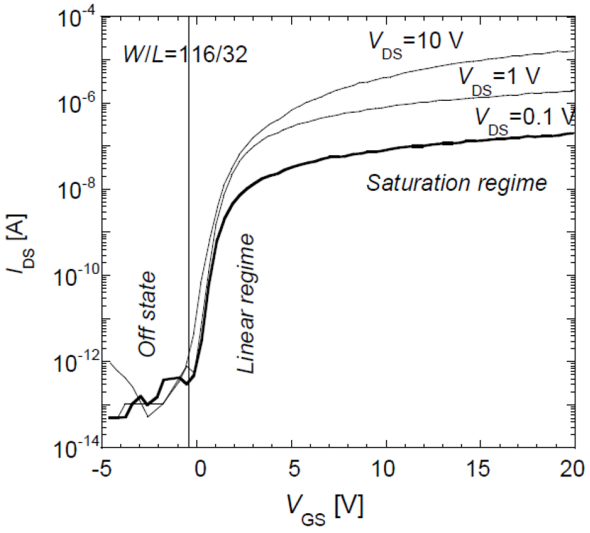


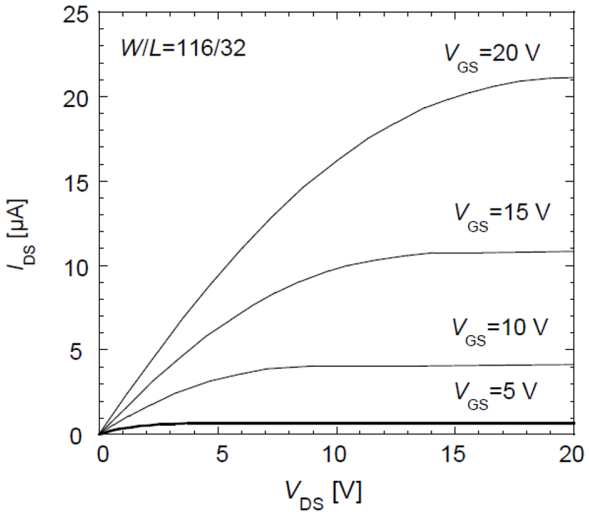
(a) (b)

Figure 3: More details can be found in: K. Sakariya et al., IEEE Transactions on electron. devices, Vol. 51 **(12)**, Dec. 2004.

Exercise 2: Given are the following a-Si:H TFT characteristics:

a) In `p-Thin-film transistors and flat panel displays`, slide 36, the following for-





mula is given for the estimation of the field effect mobility:

$$\mu_n^{\mathrm{FET}} \left[\frac{\mathrm{cm}^2}{\mathrm{V\,s}}\right] = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{G}}} \cdot \frac{L}{W \cdot C'_{\mathrm{SiN_x}} \cdot V_{\mathrm{ds}}}, \tag{1}$$

which is valid in the linear regime. Here $C'_{\mathrm{SiN_x}}$ denotes a surface normalized capacitance, otherwise above equation would not be correct. Every information can be extracted from the upper left figure (also given in `p-Thin-film transistors and flat panel displays`, slide 34), except the capacitance due to the insulating layer, which will be approximated with a parallel plate capacitor, given by

$$\frac{C}{A} = \frac{\epsilon_0 \epsilon_r}{d} \cong 2.66 \times 10^{-8}\,\mathrm{F\,cm^{-2}}, \tag{2}$$

where d is typically 250 nm (`p-Thin-film transistors and flat panel displays`, slide 27) , $\epsilon_0 = 8.85 \times 10^{-14}\,\mathrm{F\,cm^{-1}}$ and $\epsilon_r = 7.5$.

By using values in the linear range (approximatively between 2 V and 4 V, be careful of the logarithmic scale!)

$$\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{G}}} \cong \frac{3 \times 10^{-7}\,\mathrm{A} - 2 \times 10^{-8}\,\mathrm{A}}{4\,\mathrm{V} - 2\,\mathrm{V}} \cong 1.4 \times 10^{-7}\,\mathrm{A\,V^{-1}} \tag{3}$$

for $V_{\mathrm{ds}} = 10\,\mathrm{V}$, $W = 116\,\mu\mathrm{m}$ and $L = 32\,\mu\mathrm{m}$, we obtain $\mu_n^{\mathrm{FET}} \cong 0.15\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is in the same order as the values given in `p-Thin-film transistors and flat panel displays`, slide 26.

b) By assuming a uniform distribution along the channel of the effective mobility and using the first equation on slide 29, the ratio of free to trapped charge is given by

$$\frac{\mu_n^0}{\mu_n^{\mathrm{FET}}} = \frac{n_f + n_t}{n_f} \tag{4}$$

with $\mu_n^0 \cong 10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, leading to

$$\frac{n_t}{n_f} \cong \frac{10}{0.15} - 1 \cong 66. \tag{5}$$

c) In the case of an illuminated layer of a-Si:H (so no field effect in that case), this ratio is very approximately given by the ratio of the drift mobility to the band mobility (see e.g. the lecture on band tails in a-Si:H, `e-conductivity_band-tails, slide 11`), that is

$$\frac{\mu_n^{\mathrm{drift}}}{\mu_n^0} = \frac{n_f}{n_f + n_t}, \tag{6}$$

leading to

$$\frac{n_t}{n_f} = \frac{\mu_n^0}{\mu_n^{\mathrm{drift}}} - 1 \cong \frac{10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}}{1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}} - 1 \cong 9. \tag{7}$$

Both values were expected to be approximately the same: in both cases there is a thermodynamical equilibrium between trapped and free states (above the Quasi-Fermi level and within the band tails). Our estimation for the FET mobility is a bit too high but with the given graphs, it is quite difficult to make an exact estimation.