Stability Analysis of Current Programmed a-Si:H AMOLED Pixel Circuits

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***Abstract*—In this paper, we present self-compensating current mirror-based pixel circuits, and analyze basic stability issues to provide a deeper understanding of circuit operation, and the impact of thin film transistor bias nonidealities, which can lead to the long-term (and gradual) instabilities in pixel drive current. The analysis also provides the circuit designer a means to tailor the pixel drive current stability to the long-term brightness degradation characteristics of the organic light-emitting diode.**

***Index Terms*—Active matrix, amorphous silicon, current programmed pixel circuit, organic light emitting diode (OLED), thin-film transistor (TFT), threshold voltage shift.**

I. Introduction

THE a-Si:H thin-film transistor (TFT) technology is mature and well suited to produce active matrix display [1] and imaging [2] backplanes in view of its low fabrication costs over large areas, good process uniformity, adequate switching speed, and the option of a low-temperature process that allows the fabrication of TFTs and circuits on mechanically flexible substrates [3]. However, the material does have the drawback of defect metastability, causing threshold voltage (V_T) shifts in the TFT over time thus reducing the drive current, which is already constrained by the low material mobility. In contrast to active matrix liquid crystal displays (AMLCD) where the pixel comprises of only one TFT, which is used as a switch, TFTs in active matrix organic light-emitting diode (AMOLED) pixel circuits are used as both switches and analog current sources. As a result, AMOLED pixel circuits, particularly in amorphous silicon (a-Si:H) technology, are highly susceptible to long-term performance degradation caused by V_T metastability. The problem of instability can be overcome through the use of appropriate circuit design techniques along with current programming [4].

The simplest possible pixel driver circuit for active matrix OLED displays is the conventional two-TFT voltage-driven circuit shown in Fig. 1, [1].

The gate drivers are connected to the V_{ADDRESS} line, and the source drivers supply data to the source of T1 in each pixel circuit. After data has been written to the pixel, the V_{ADDRESS} line is switched to low, the voltage stored in C_S remains constant, except for the initial drop due to charge feed-through stemming from the C_{GS} of T1 when it turns off.

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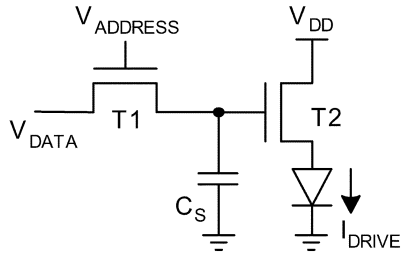

Fig. 1. Conventional voltage programmed two-TFT OLED pixel driver circuit.

The OLED current is controlled by the drive TFT, T2. In the saturation region of T2, the current is given by [5]

$$I_{\mathrm{OLED}} = \frac{\mu_{\mathrm{eff}}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{\mathrm{eff}}}\gamma_{\mathrm{sat}}(V_{\mathrm{GS}}-V_T)^{\alpha} = K'(V_{\mathrm{GS}}-V_T)^{\alpha} \quad (1)$$

where μ_{eff} is the effective device mobility, ζ is an amorphous silicon material parameter, C_i the gate dielectric capacitance, α a coefficient that ranges between 2 and 2.4 (see [5]), $\gamma_{\mathrm{sat}} = (1+\lambda)V_{\mathrm{DS}}$, and λ the channel length modulation parameter.

The issue with the two-TFT circuit is that the threshold voltage V_T of the drive TFT T2 increases during operation. The direct consequence of the increasing V_T, following (1), is a decreasing OLED drive current for the same input data voltage. As a result, the pixel brightness gradually diminishes up to a point where the pixel essentially turns off. Hence, for reliable OLED operation, some form of compensation is required to maintain a constant current through the OLED.

In this paper, we show a four-TFT current programmed current mirror-based ΔV_T compensating pixel circuit, and demonstrate its superiority over the conventional two-TFT voltage-programmed circuit. This paper builds on the preliminary results presented in [4], which described the transfer characteristics of the various four-TFT circuits that were presented. In particular, this paper assesses the theoretical stability of the four-TFT circuit, analyzes the operation of the TFTs in the circuit, and examines the effect of the ΔV_T of the various TFTs on the OLED drive current. The analysis presented here can be applied to all current mirror-based AMOLED pixel circuits.

II. ΔV_T Compensating Current Programmed Pixel Circuit

The current mirror architecture is inherently independent of the V_T of the two transistors, and hence it is an excellent

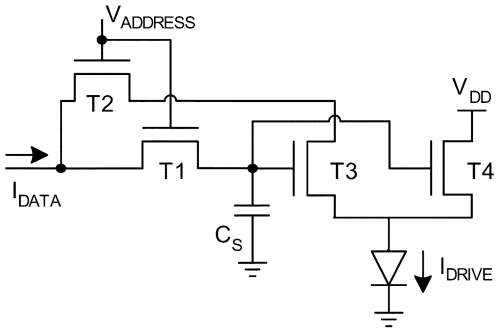

Fig. 2. A V_T-shift compensating four-TFT current programmed circuit.

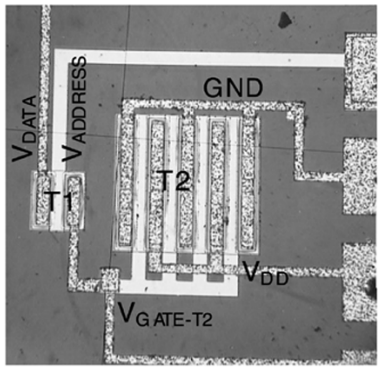

Fig. 3. Micrograph of the voltage programmed two-TFT circuit.

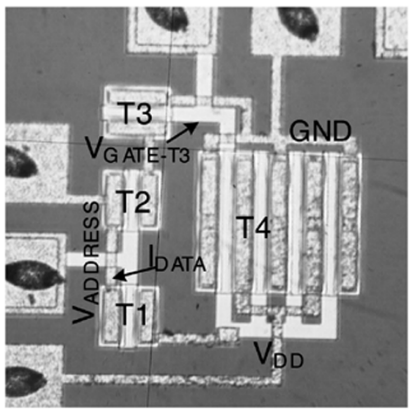

Fig. 4. Micrograph of the V_T-shift compensating four-TFT current programmed circuit.

building block for designing self-compensating pixel circuits. A capacitor at the common gate terminal can store the gate voltage (which, in turn, sets the output current). For pixel programming, we need a minimum of two switches to isolate the pixel capacitor so that its charge cannot leak out during the frame time. Based on this, a four-TFT current programmed V_T-shift invariant pixel circuit has been developed, and is shown in Fig. 2.

When programming the circuit, $V_{\rm ADDRESS}$ is high, and a current $I_{\rm DATA}$ is applied. This current initially flows through transistor T1 and charges capacitor C_S. As the capacitor voltage rises, T3 begins to turn on and $I_{\rm DATA}$ starts to flow through T2 and T3 to ground. The capacitor voltage stabilizes at the point when all of $I_{\rm DATA}$ flows through T2 and T3, and none through T1. This process is independent of the V_T of transistors T3 and T4.

The gates of T3 and T4 are connected, so the current flowing through T3 is mirrored in T4. This topology allows us to have on-pixel current gain or attenuation depending on the sizing of T3 and T4, so that the respective data current can be proportionately smaller or larger than the OLED current. Since the OLED current is dependent on $V_{\rm DD}$ even in the saturation region due to the low output resistance of TFTs, there is a deviation from the ideal gain. However, this deviation is known a priori and can be incorporated in the external gamma correction circuit.

In an active matrix array, pixels are scanned and programmed in a row-by-row fashion. The time taken to scan all rows (one frame) is called the frame time. During array operation, the switching TFTs (T1 and T2) are on only once in the frame time. If the refresh rate is 60 frames/s and there are 240 rows in the array, the switches are on for 70 μs/frame. For this array size, the duty cycle will be only 0.42%, thus the V_T shift in the switches will be minimal. Moreover, it may possible to reduce the switch V_T if their gate voltages are set to a negative value when they are off.

Both the simple voltage programmed two-TFT and current programmed four-TFT circuits were fabricated in a-Si:H, using a tri-layer inverted-staggered TFT process at 260 °C. Figs. 3 and 4 show the micrographs of the two-TFT and four-TFT circuits, respectively, from which we can see that the four-TFT circuit does not occupy significantly more area. The parameters for the TFTs in the circuits are given in Table I. To bring the V_T of all TFTs to an initial known level, we annealed the circuits at 175 °C for 3 h, and allowed them to cool down for another 3 h. This annealing process was repeated before any experiment was performed on the circuits.

A 12-h lifetime comparison was done on both pixel circuits, the results of which are shown in Fig. 5. To avoid any OLED-related degradation issues, this test was performed without connecting the OLED (i.e., we directly connected the source terminals of T3 and T4 to ground). Also, to reduce the complexity of the experimental setup, the pixel was continuously stressed by leaving the switching TFTs on all the time. Here, for the two-TFT circuit, the input data voltage was held at a constant value for the duration of the test, while for the four-TFT circuit, the input data current was held constant. The initial drive currents of both the two-TFT and four-TFT circuits were comparable.

From the experiment results, we can see that the four-TFT circuit is far more stable than the two-TFT circuit. Over the 12-h period, the two-TFT circuit drive current falls by almost 30%, while the drive current provided by the four-TFT circuit does not degrade. To the contrary, we observe a distinct rise in the drive current. After an initial rapid current rise for about 2 h, the drive current rises slowly but steadily (reasons for which will be discussed in Section III). Indeed, this is totally unexpected since in a balanced current mirror with both T3 and T4 in the saturation region, the output current should only depend on the input (i.e., reference) current, and hence in principle it should be constant.

TABLE I
TFT SIZES AND ON-RESISTANCES IN two-TFT AND four-TFT PIXEL CIRCUITS

a-Si:H TFT Parameters				
Initial V_T	**μ_{eff}**	**C_i**	**α**	**Leakage Current (at V_{GS}=-5 V)**
3.65 V	**0.45 cm^2/Vs**	**19 nF/cm^2**	**2.27**	**0.3 pA (for 100um/23um TFT)**

Pixel Circuit Parameters		
	2-TFT Pixel Circuit (Figure 1)	**4-TFT Pixel Circuit (Figure 2)**
TFT Sizes	T1: 100μm / 23μm T2: 1000μm / 23μm	T1,T2,T3: 100μm / 23μm T4: 1000μm / 23μm
R_{ON} at V_{GS}=20V	T1: 1.79 MΩ T2: 0.176 MΩ	T1,T2,T3: 1.79 MΩ T4: 0.176 MΩ

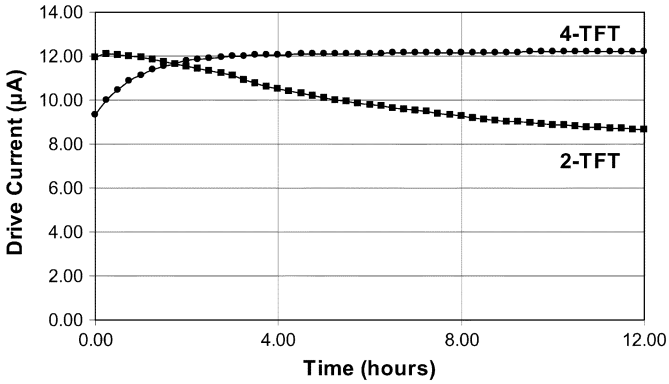

Fig. 5. Lifetime comparison of the two-TFT and four-TFT pixel circuits.

III. CURRENT STABILITY ANALYSIS

The basic requirement for a current mirror to work accurately (i.e., replicate the input or reference current at the output) is that the $V_{\rm GS} - V_T$ of the two transistors should be equal at all times, and both transistors should always be in the saturation region of operation. This means that in the four-TFT pixel circuit, we have to ensure that the initial V_T of T3 and T4 are equal, the magnitudes and rates of rise in V_T are equal, and finally, both T3 and T4 stay in saturation. The output drive current can vary if any of these conditions are not satisfied. In particular, we have identified the following three distinct mechanisms that can cause current variations in the four-TFT pixel circuit:

- switch TFT (T2) degradation;
- differential V_T shift between T3 and T4, caused by:
  - T3 operating in linear and T4 in saturation region;
  - other possible mismatches;
- initial V_T mismatch between T3 and T4.

The general time dependence of the drive current can be quantitatively determined as follows. Assuming a constant $V_{\rm DD}$ and $I_{\rm DATA}$, and a fixed $V_{\rm ADDRESS}$ voltage in the four-TFT circuit, and noting that T1 does not pass any current in the steady state, the drive current provided by T4 (in saturation) is given by

$$\begin{aligned} I_{\rm DRIVE}(t) &= G \cdot K'[V_{{\rm GS}-T4}(t) - V_{T-T4}(t)]^{\alpha} \\ &= f[V_{{\rm GS}-T4}(t), V_{T-T4}(t)] \end{aligned} \tag{2}$$

where K' is defined by (1), G is the gain of the current mirror (W_{T4}/W_{T3}), and

$$V_{{\rm GS}-T4}(t) = I_{\rm DATA} \cdot R_{{\rm ON}-T2}(t) + V_{{\rm DS}-T3}. \tag{3}$$

TFT T3 is in saturation, thus, we need to incorporate the channel length modulation parameter λ in order to determine $V_{{\rm DS}-T3}$. This gives us

$$V_{{\rm DS}-T3} = \frac{I_{\rm DATA}}{\lambda K'[V_{{\rm GS}-T4}(t) - V_{T-T3}(t)]^{\alpha}} - \frac{1}{\lambda}. \tag{4}$$

Now, T2 is in the linear region of operation, and is governed by the following [6]:

$$\begin{aligned} I_{{\rm DS}-T2} = \mu_{\rm eff}\zeta C_i^{\alpha-1}\frac{W}{L_{\rm eff}}[&V_{\rm ADDRESS} - V_{{\rm DS}-T3} \\ &- V_{T-T2}(t)]^{\alpha-1}V_{{\rm DS}-T2}. \end{aligned} \tag{5}$$

Its on resistance is given by [6]

$$\begin{aligned} &R_{{\rm ON}-T2}(t) \\ &\quad = \frac{1}{\mu_{\rm eff}\zeta C_i^{\alpha-1}\frac{W}{L_{\rm eff}}[V_{\rm ADDRESS}\text{-}V_{{\rm DS}\text{-}T3}\text{-}V_T\text{-}T2(t)]^{\alpha-1}}. \end{aligned} \tag{6}$$

Using (2)–(6), the change in the drive current with respect to time can be written as

$$\begin{aligned} \frac{dI_{\rm DRIVE}(t)}{dt} = &\frac{\partial f}{\partial V_{{\rm GS}-T4}} \cdot \frac{\partial V_{{\rm GS}-T4}}{\partial R_{{\rm ON}-T2}} \\ &\cdot \frac{\partial R_{{\rm ON}-T2}}{\partial V_{T-T2}} \cdot \frac{dV_{T-T2}}{dt} \\ &+ \frac{\partial f}{\partial V_{{\rm GS}-T4}} \cdot \frac{\partial V_{{\rm GS}-T4}}{\partial R_{{\rm ON}-T2}} \\ &\cdot \frac{\partial R_{{\rm ON}-T2}}{\partial V_{T-T3}} \cdot \frac{dV_{T-T3}}{dt} \\ &+ \frac{\partial f}{\partial V_{{\rm GS}-T4}} \cdot \frac{\partial V_{{\rm GS}-T4}}{\partial V_{T-T3}} \\ &\cdot \frac{dV_{T-T3}}{dt} + \frac{\partial f}{\partial V_{T-T4}} \cdot \frac{dV_{T-T4}}{dt}. \end{aligned} \tag{7}$$

From the above equation, we can see that the root cause of drive current instability is the V_T-shift in T2, T3, and T4. The first two terms represent the degradation of switch TFT T2 due to an increase in the V_T of T2 and T3, and the third and fourth

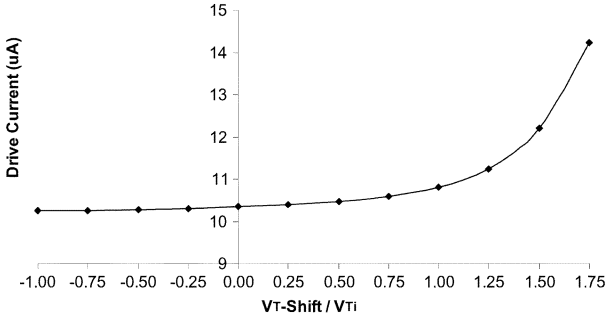

Fig. 6. Simulation of the effect of switch TFT (T1 and T2) degradation on the OLED current.

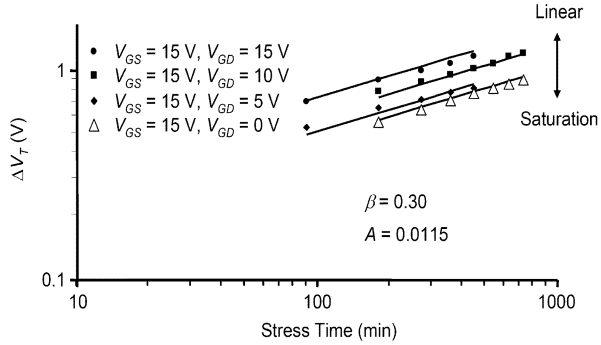

Fig. 7. Dependence of ΔV_T on $V_{\rm GS}$ and $V_{\rm GD}$ of a TFT. The value extracted for β is 0.3. The solid lines represent the model shown in (4).

terms together represent the differential V_T-shift in T3 and T4. The effect of any initial mismatch in V_T of T3 and T4 is also predicted by (7).

A. Switch TFT Degradation

The function of the switching TFTs T1 and T2 in the four-TFT circuit is to isolate the pixel once it has been programmed. As such, the TFTs are required to have very low leakage current in the off state, and a very low on resistance $(R_{\rm ON})$ in the on state. The leakage current requirement is easily achievable with inverted-staggered TFTs since it is of the order of 10–100 fA at the vicinity of $V_{\rm GS} = -5$ V. However, the on resistance is usually in the range of $M\Omega$, and is defined by (6). Despite the low duty cycle in typical QVGA operation, the switches also degrade because their on resistance increases over time as V_T increases, making their behavior far from ideal.

In the four-TFT circuit, the current path from the input through T2 and T3 to ground causes the voltage at the current input terminal to rise. Since no current flows through T1, the voltage at the gate of T3 is the same as that of the data input terminal. Now, when the resistance of the T2 switch increases, the voltage at the input terminal rises, and the gate voltage of T3 correspondingly rises. Since the gates of T3 and T4 are connected, the output drive current provided by T4 also rises. Thus, even if T3 and T4 are perfectly matched in geometry, bias/operation, and V_T, the degradation of the switches can cause the circuit to over-compensate, leading to a rise in the output drive current.

Fig. 6 shows a simulation of the effect of switch degradation on the OLED drive current. For this simulation, T3 and T4 are assumed to have the same and constant V_T and hence $R_{\rm ON}$. The graph shows that for large increases in the V_T of T2, the OLED drive current rises significantly. However, the OLED current is affected to a much lesser extent in the case of decreasing V_T in T2. This behavior arises because T3 moves from saturation (less sensitive drain voltage) to the linear region (highly sensitive to drain voltage) as the V_T of T2 increases.

B. Differential V_T Shift Between T3 and T4

It is not immediately obvious that T3 and T4 in the four-TFT circuit would not experience the same V_T shift, since they are subjected to identical $V_{\rm GS}$ (as shown in the V_T model presented in [7]). However, when the pixel circuit is not being programmed (i.e., during most of the frame time), T1 and T2 are off, hence T3 is in the linear mode of operation with $V_{\rm DS} = 0$, while T4 remains in saturation.

The effect of drain voltage on TFT metastability cannot be ignored. Experiments investigating the dependence of ΔV_T on $V_{\rm GS}$ and $V_{\rm GD}$ show that the ΔV_T for a TFT entering saturation is smaller than that in the linear mode at the same gate bias voltage, as shown in Fig. 7, [8]. Driving the TFT deeper into saturation (i.e., $V_{\rm DS} > V_{\rm GS} - V_T$ or as $V_{\rm GD} < V_T$) appears to have little effect on ΔV_T. These observations can be explained if we consider the defect pool model [9] Assuming that the ΔV_T is proportional to the number of carriers in the conduction band tail states, the decrease in TFT channel charge in saturation helps explain the smaller ΔV_T as compared to that in the linear region. Further, since once the TFT is saturated, there is no significant change in the concentration of channel charge as the TFT is driven further into saturation, the change in ΔV_T is negligible. We also have to note that carrier trapping in the gate nitride is not significant at the indicated bias voltages.

Since ΔV_T appears to vary with the density and distribution of the induced channel charge, simple MOS equations for channel charge are employed to develop a rudimentary ΔV_T model for a TFT operating under gate and drain bias voltages. Following the observed dependences of ΔV_T on TFT drain bias, ΔV_T equations developed by Powell *et al.* [9] can be suitably modified to include the effect of drain voltage by determining the ratio of the channel charge for given $V_{\rm GD}$ and $V_{\rm GS}$ bias values to that in the linear mode of operation [8]. Thus

$$\Delta V_T(t) = \left(\frac{Q_G}{Q_{G0}}\right) A(V_{\rm GS} - V_{\rm Ti})t^{\beta} \tag{8}$$

where

$$Q_{G0} = C_G.W.L(V_{\rm GS} - V_{\rm Ti})$$

$$Q_G = \left(\frac{\alpha}{\alpha+1}\right) C_G W L \times \frac{(V_{\rm GS} - V_{\rm Ti})^{\alpha+1} - (V_{\rm GD} - V_{\rm Ti})^{\alpha+1}}{(V_{\rm GS} - V_{\rm Ti})^{\alpha} - (V_{\rm GD} - V_{\rm Ti})^{\alpha}}$$

and $V_{\rm Ti}$ is the initial V_T of the TFT.

This can be simplified to

$$\Delta V_T(t) = A\left(\frac{\alpha}{\alpha+1}\right) \times \frac{(V_{\rm GS} - V_{\rm Ti})^{\alpha+1} - (V_{\rm GD} - V_{\rm Ti})^{\alpha+1}}{(V_{\rm GS} - V_{\rm Ti})^{\alpha} - (V_{\rm GD} - V_{\rm Ti})^{\alpha}} t^{\beta}. \tag{9}$$

Since ΔV_T is proportional to the normalized channel charge, the maximum (in linear mode) and minimum (in saturation mode) values for channel charge set the upper and lower limits of ΔV_T at a given $V_{\rm GS}$.

In our current mirror-based four-TFT circuit, T3 and T4 experience different drain voltages. Assuming that $V_{\rm DD}$ is large, T4 always remains deep in saturation. However, T3 is in the linear mode of operation for most of the frame time. As predicted by the model in (9), the V_T-shift is higher in T3 in comparison to T4, which pulls the floating gate of T3 to a higher voltage resulting in an over-compensation, and leads to a gradual rise in OLED current.

To show this mathematically, we can derive the equation for $I_{\rm DRIVE}$ of the four-TFT circuit when the V_T of T3 and T4 are not matched. This can by done using (1) with $\alpha = 2$, and ignoring the switch resistances

$$I_{\rm DRIVE} = G \cdot I_{\rm DATA} + G \cdot K'(V_{T,T3} - V_{T,T4})^2 + 2G(V_{T,T3} - V_{T,T4})\sqrt{K' \cdot I_{\rm DATA}} \quad (10)$$

where G is the ratio of (W/L)s of T4 and T3 (i.e., the gain/attenuation of the current mirror).

Now, from (8), we can write

$$\Delta V_{T-T3}(t) = A(V_{\rm GS} - V_{\rm Ti})t^{\beta} \quad \text{and} \quad (11)$$

$$\Delta V_{T-T4}(t) = \frac{2}{3}A(V_{\rm GS} - V_{\rm Ti})t^{\beta}. \quad (12)$$

Thus

$$\Delta V_{T-T3}(t) - \Delta V_{T-T4}(t) = \frac{A}{3}(V_{\rm GS} - V_{\rm Ti})t^{\beta}. \quad (13)$$

Using this result in (10) and assuming that the initial V_T of T3 and T4 are identical, we can derive the time dependence of $I_{\rm DRIVE}$ caused by differential V_T-shift in T3 and T4

$$I_{\rm DRIVE}(t) = G \cdot I_{\rm DATA} + G \cdot K' \left[\frac{A}{3}(V_{\rm GS} - V_{\rm Ti})t^{\beta}\right]^2 + 2G\left[\frac{A}{3}(V_{\rm GS} - V_{\rm Ti})t^{\beta}\right]\sqrt{K' \cdot I_{\rm DATA}}. \quad (14)$$

The above derivation can be made more accurate if we include the effect of the drain voltage on the V_T-shift of the TFTs as shown in (9), however this has to be done numerically. This is shown in Fig. 8, where the solid lines are the expected values based on the model. The model agrees very well with measurements of ΔV_T in T3 and T4, and the corresponding OLED current increase. In this differential V_T-shift experiment, we pulsed T1 and T2 at a 0.42% duty cycle, thereby minimizing the impact of switch degradation on the voltage of the floating T3 gate node.

C. Combined Effect of Switch Degradation and Differential V_T-Shift

Switch degradation is a major reason for OLED current rise when T1 and T2 are always on (static operation). In such operating conditions, switch degradation also leads to differential V_T-shift, because when the voltage drop across T2 exceeds

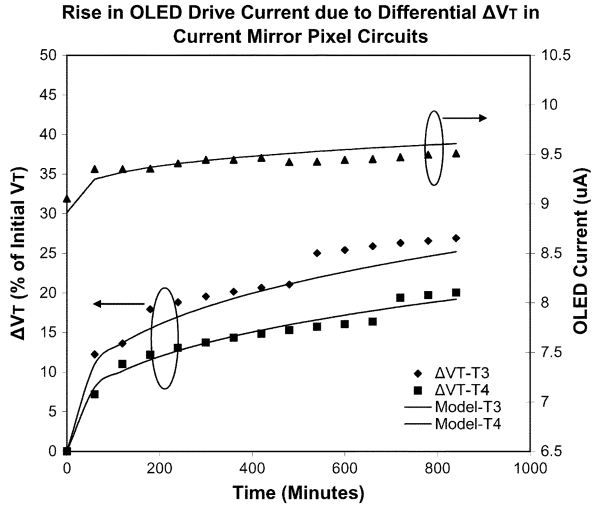

Fig. 8. Differential V_T-shift in T3 and T4 leading to a gradual rise in OLED current. The solid lines represent expected values based on models.

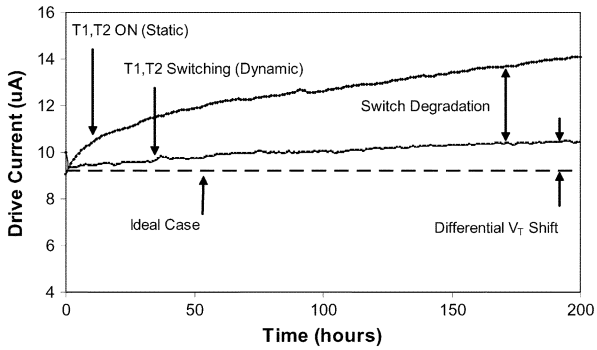

Fig. 9. A 200-h stress test on four-TFT current programmed pixel circuit.

the V_T of T3, T3 will move into the linear region of operation. Meanwhile, T4 continues to be in saturation, thus creating the $V_{\rm DS}$ mismatch that leads to different ΔV_T in T3 and T4. Thus, during static operation, OLED current rise is due to the combined effects of switch degradation and differential ΔV_T.

In contrast, under dynamic operation of the pixel circuit (T1 and T2 switched with a 0.42% duty cycle), switch degradation is minimal, and the dominant mechanism is differential V_T-shift. This distinction can be used to investigate the relative magnitudes of current rise due to each of the two effects. Fig. 9 shows 200-h measurements on the four-TFT pixel circuit in both static and dynamic operation. The dotted line is the ideal pixel where there is no current increase. The graph demonstrates that the magnitude of current rise due to switch degradation is about three times that due to differential V_T-shift over a 200-h period of operation.

D. Initial V_T Mismatch Between T3 and T4

Another effect that is present current-mirror circuits like the four-TFT circuit is the initial mismatch in V_T of T3 and T4. Despite the excellent uniformity of the various layers in the amorphous silicon TFT process, the mismatch in V_T of TFTs using an industrial process on a 320- $\times$ 400-mm glass can be about 6% (from data presented in [10]), and up to about 25% with a research process (from data presented in [11]). The behavior

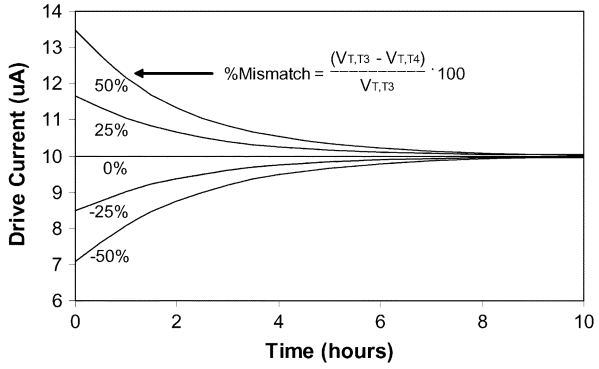

Fig. 10. Current stabilization after initial V_T mismatch between T3 and T4.

of the circuit in the presence of such mismatches is determined below.

From (10), we can see that a mismatch in V_T leads to an OLED current that is higher (when $V_{T,T3} > V_{T,T4}$) or lower (when $V_{T,T3} < V_{T,T4}$) than the desired current. This equation can also be used to demonstrate the effects of a mismatch in the initial V_T of those TFTs. The effective gate voltage $V_{\rm GS}$–V_T experienced by T3 is different from that of T4, which leads to a higher V_T-shift in the TFT that started off with the lower initial V_T. This is a self-stabilizing mechanism, whereby after a few h the V_T of T3 and T4 will become equal. This effect can be demonstrated mathematically by using (9) to predict the V_T shift of T3 (in linear) and T4 (in saturation) with the additional constraint that the initial V_T of T3 and T4 are different, and using that in (10) to obtain the time varying OLED current. The resulting equation is best solved numerically.

Fig. 10 shows this variation in the OLED current due to initial V_T mismatches of -50% to 50%. From the graph, we see that OLED current settles to the desired value in about 6 to 8 h. This graph shows that even in the presence of a current mirror mismatch, the circuit will adjust to stabilize the current. In Fig. 5, the initial V_T mismatch can be one of the causes of the initial rise in OLED current over the first few hours of operation. This effect is also compounded by the a current transient created when traps in the a-Si:H channel are filled during TFT operation.

IV. Discussion

The previous section explained how three distinct effects, namely switch TFT degradation, differential V_T-shift, and initial V_T mismatch, cause long term instability in the OLED drive current of current programmed four-TFT circuit. From the analysis, we can see that by controlling the magnitude of these three effects, the designer can customize the rate of change of the drive current. For example, the designer can choose the amplitude and duty-cycle of $V_{\rm ADDRESS}$ to achieve the desired switch TFT degradation rate, or judiciously select the sizes of the four TFTs to obtain the desired differential V_T-shift. Moreover, it is even possible to adjust the initial rise/fall of the drive current by deliberately introducing a mismatch in the V_T of T3 and T4, though this may be difficult to do in an industrial process. This is a unique and powerful feature of this circuit since it allows the drive current instability to be tailored to the OLED brightness instability (which generally falls over time), resulting in constant brightness throughout the life of the display.

V. Conclusion

This work analyzed the long-term stability of the current mirror-based current programmed four-TFT circuit. It addressed the issue of the gradual rise in the OLED drive current that is observed in the circuit, which can be explained by three mechanisms: switch degradation, differential V_T-shift, and initial V_T mismatch in the current mirror. Using models and simulations to determine the magnitude of the observed effects of each mechanism, this paper demonstrates that it is possible by circuit design to control the OLED drive current instability in the circuit. Most importantly, the analysis presented here can be applied to all other current mirror-based a-Si:H circuits, and presents the circuit designer with an innovative and unique method to tailor the drive current increase to the OLED brightness degradation characteristics.

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