An ASIC for High-resolution Capacitive Microaccelerometers

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Abstract

An ASIC (application specific integrated circuit) for high-resolution capacitive accelerometers using switched-capacitor techniques is presented The circuit, realized in a 3 μm CMOS process, is suited for the measurement of the differential capacitance of any capacitor bridge and features a maximum output noise density of -110 dB V/$\sqrt{\text{Hz}}$ The cut-off frequency of its first-order low-pass filter characteristic is determined by an external filter capacitor and the sampling rate

Introduction

Capacitive silicon pressure sensors or accelerometers [1] have very interesting properties such as high sensitivity, good linearity and low fabrication cost A drawback of this type of sensor is the increased complexity of the measurement electronics The goal of this work was to study, design and realize an ASIC for the measurement of the plate deflection of a capacitive accelerometer [2]

The main problems to be addressed were a good linearity with respect to the plate deflection and a high dynamic range They could only be solved if the technique used to measure the plate deflection created low and symmetrical electrostatic forces on the capacitor plates and if the electronic circuit was optimized with respect to its offset and output noise Different measurement principles have been studied in the course of this project [3] and the self-balancing bridge has been found to be the optimum solution

The Self-balancing Capacitor Bridge

The acceleration sensor consists of a movable plate with a fixed electrode on each side (Fig 1) Together the three electrodes form the capacitors C_1 and C_2 The plate deflection Δd normalized with respect to the distance d_0 between the fixed electrodes, may be expressed in terms of the capacitances C_1 and C_2 by

$$x = \frac{\Delta d}{d_0} = \frac{C_1 - C_2}{C_1 + C_2} \tag{1}$$

A measurement scheme resulting in an output voltage proportional to $(C_1 - C_2)/(C_1 + C_2)$ leads to a linear relationship between the plate deflection and the output voltage Such a measurement scheme is realized with the self-balancing capacitor bridge shown in Fig 1

The fixed electrodes of the capacitors C_1 and C_2 are periodically switched between a reference voltage V_0 and the output voltage V_m The resulting charge transfers Q_1 and Q_2 on capacitors C_1 and C_2, respectively, as well as their difference $(\Delta Q = Q_1 - Q_2)$ are given by

$$\Delta Q = Q_1 - Q_2 = C_1(V_0 - V_m) - C_2(V_0 + V_m) \tag{2}$$

The electronic measurement circuit samples ΔQ from the movable center plate and integrates it on a filter capacitor, thereby generating the output voltage V_m, that is fed back to the excitation network in order to establish the equilibrium condition $\Delta Q = 0$ From eqns (1) and (2) one can derive that *the output voltage of the balanced bridge is proportional to the deflection* of the movable center plate

$$V_m = \frac{C_1 - C_2}{C_1 + C_2} V_0 = xV_0 \tag{3}$$

Functional Description of the Circuit

The schematic of the self-balancing capacitor bridge is shown in Fig 2 The circuit consists of a

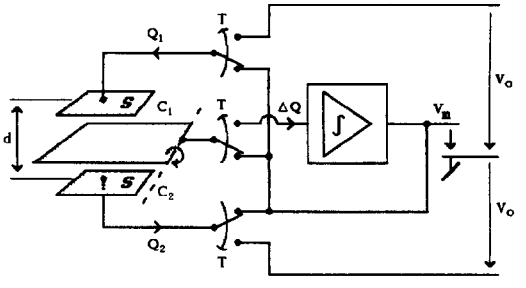

Fig 1 Block scheme

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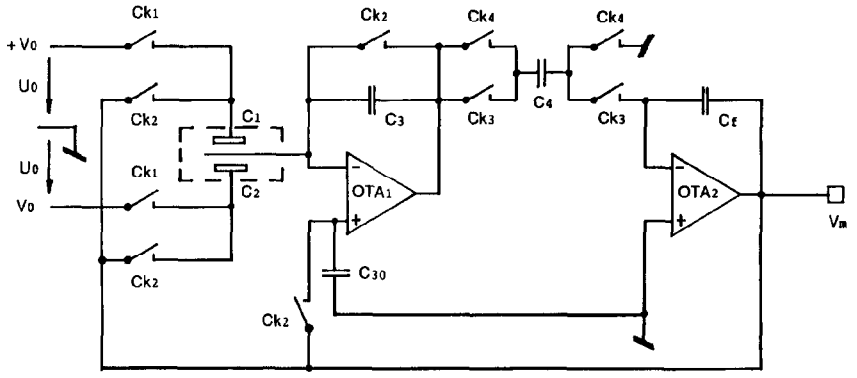

Fig 2 Self-balancing bridge

sampling stage and an integrator formed by OTA1 and OTA2 respectively (OTA operational transconductance amplifier) The switches used in these two stages are controlled by a clock sequence shown in Fig 3

The clock sequence can roughly be divided into a HOLD and a SAMPLE state During the HOLD state, the output voltage V_m remains constant and fixes the potential of the capacitors C_1, C_2 and C_3 which are all discharged through the switches controlled by clock Ck_2 In the following SAMPLE state the capacitors C_1 and C_2 are charged to the voltages $(V_o - V_m)$ and $(V_o + V_m)$ respectively The resulting net charge flow to the middle electrode, given by eqn (2), is integrated on capacitor C_3 and leads to an error voltage at the output of OTA1 This error voltage is sampled by capacitor C_4 and integrated on the filter capacitor C_f thereby defining the output voltage V_m of the next measurement cycle

The details of the timing diagram are chosen in such a way as to minimize the errors due to the offset voltage of OTA1 and the clock feedthrough

Dynamic Behavior

The charge integrated on capacitor C_f during the sampling sequence k is given by

$$C_f(V_m(k) - V_m(k-1)) = 4C_o \frac{C_4}{C_3}(V_o x(k) - V_m(k-1)) \quad (4)$$

where x is the normalized plate deflection defined by eqn (1) and $C_o = (1/C_1 + 1/C_2)^{-1}$ is the

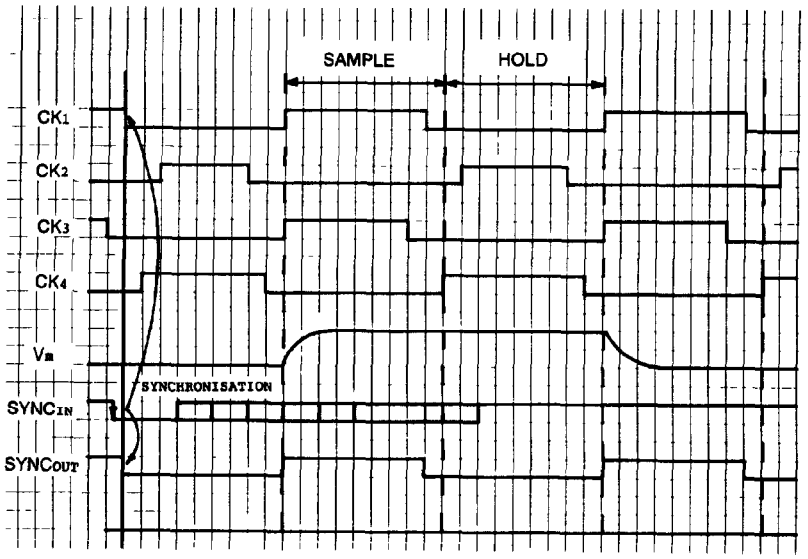

Fig 3 Clock sequence

total serial capacitance of the bridge The transfer function of the self-balanced capacitor bridge may be expressed using a z-transform description

$$F(z) = \frac{V_m(z)}{x(z)} = 4V_o \frac{C_o}{C_f}\frac{C_4}{C_3} \frac{z}{z - \left(1 - 4\dfrac{C_o}{C_f}\dfrac{C_4}{C_3}\right)} \quad (5)$$

and corresponds to a first-order low-pass filter The system is stable if the pole of its transfer function lays within the unity circle This condition determines the maximum value of the capacitance ratio

$$\frac{C_o}{C_f}\frac{C_4}{C_3} < \frac{1}{2} \quad (6)$$

The cut-off frequency f_c is given by the capacitance ratio and the sampling rate f_s

$$f_c = \frac{1}{2\pi} f_s \ln\left[\frac{z}{z - \left(1 - 4\dfrac{C_o}{C_f}\dfrac{C_4}{C_3}\right)}\right] \approx \frac{2}{\pi} f_s \frac{C_o}{C_f}\frac{C_4}{C_3} \quad (7)$$

Implementation

The self-balancing bridge has been implemented in an integrated circuit The IC contains the two-stage analog circuit, a sequencer generating the internal clock signals and a current reference used to bias the OTAs Capacitor C_f is an external component

An accelerometer self-test feature is based on a modified switching sequence yielding a net electrostatic force on the movable accelerometer plate It provides, upon request of a logical signal, a mechanical excitation at fixed frequency and amplitude during the measurement of the capacitors

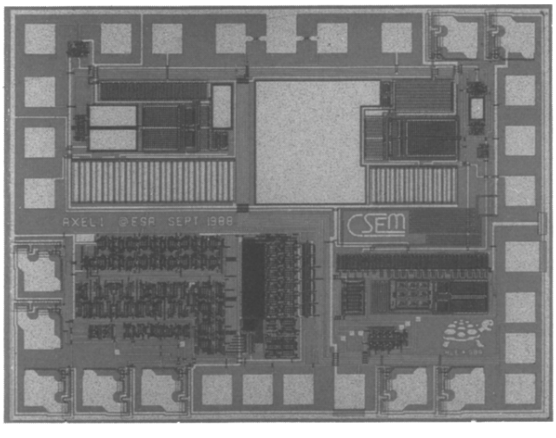

Fig 4 Chip photograph

TABLE 1 Chip characteristics

Chip size	1 8 mm × 2 3 mm
Supply voltage	± 2 5 V
Power consumption	12 mW
Output swing	± 2 0 V
Sampling rate	32 kHz
Bandwidth	1 Hz to 1 kHz
Output noise	− 110 dB V/√Hz

The chip is designed and realized in 3 μm SACMOS (self-aligned contact MOS) technology Its characteristics are summarized in Table 1 and a chip photograph is shown in Fig 4

Chip Performance

The evaluation of the circuit was done by electrical measurements and in combination with silicon microaccelerometers The circuit behaves as expected with respect to its quasi-static and dynamic response to differential capacitance changes The noise measured on a circuit with a 100 Hz bandwidth and with fixed capacitors of 22 pF replacing the acceleration sensor is shown in Fig 5 The resulting capacitance resolution corresponds to 0 04 fF for frequencies between 0 and 1 Hz

It has been found that the circuit does not degrade the excellent thermal behavior or the microaccelerometer chips [3] The capacitance resolution is sufficient to detect μg accelerations with acceleration sensors having a working range of $\pm 0\,1\,g$

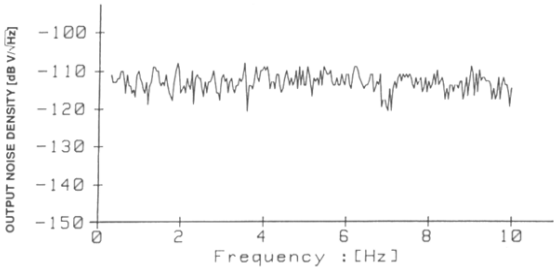

Fig 5 Output noise density

Discussion and Conclusions

An integrated circuit adapted to the measurement of the differential capacitor of an accelerometer has been developed It is based on a self-balancing bridge principle and generates an output signal which is independent of any specific circuit parameter The fabrication of the circuit is not critical nor is any trimming required This circuit proves that the electronic hardware needed for the

measurement of capacitive sensors can be highly miniaturized maintaining high performance with respect to resolution and stability

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