

Introduction to PCB design

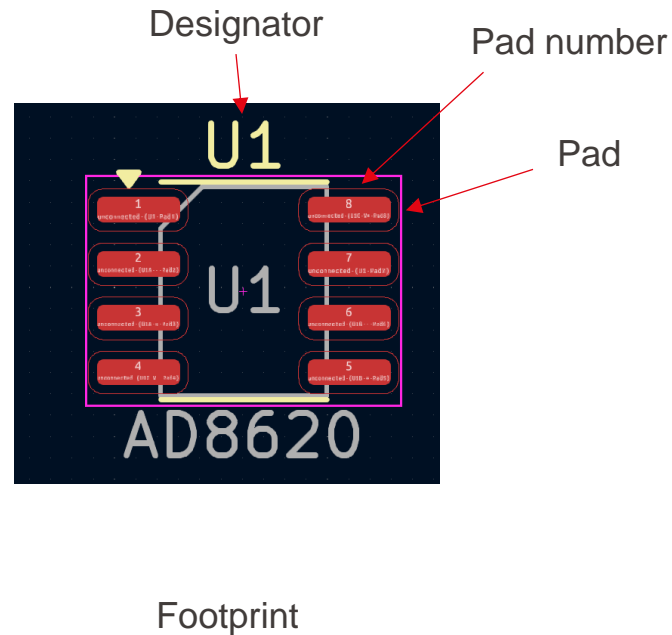
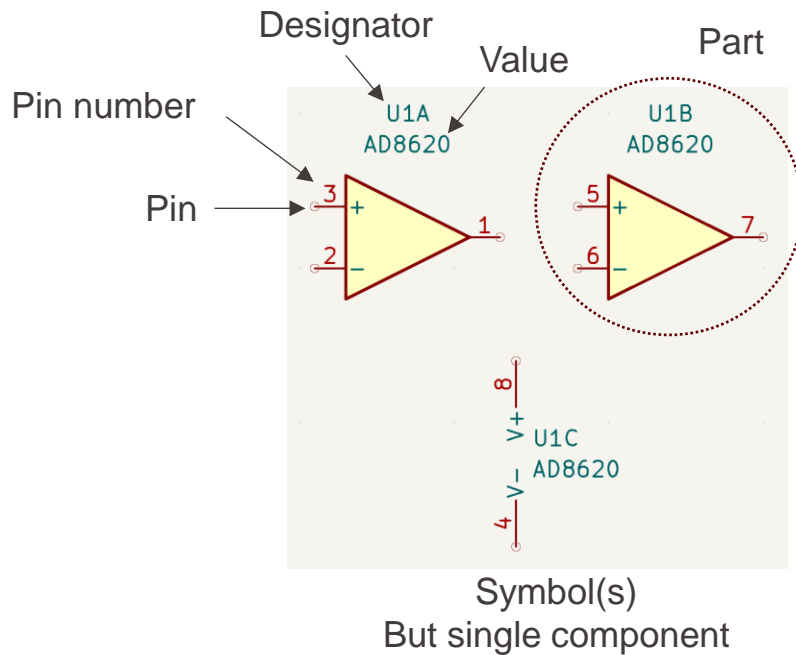
Claude Dahan
21st February 2025

- Electronic Design Automation (EDA), or ECAD
- Many choices with many capabilities:
 - Commonly used free software: KiCAD

Of importance to us:

- Schematic and Layout design capabilities
- Checks:
 - Electrical Rules Check (ERC): Does the schematic make sense?
 - Design Rules Check (DRC): Can the PCB be fabricated?
 - Layout Vs Schematic check (LVS): Does the layout match the schematic? (sometimes part of the DRC)

Symbols & Footprints

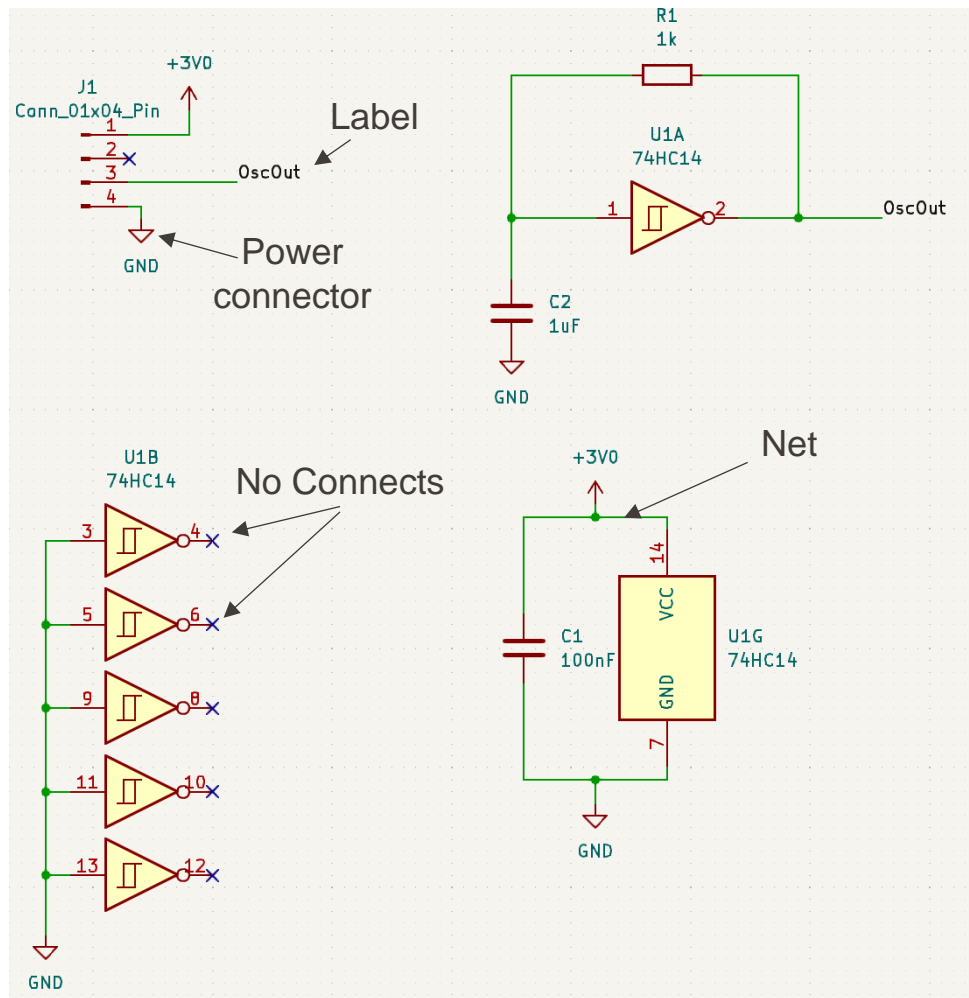


Pin and pad numbers should match with the component used
(refer to datasheet)

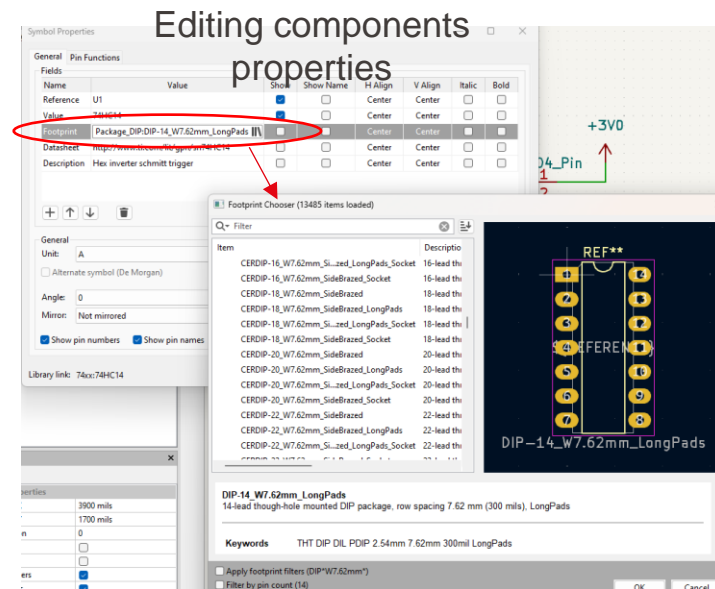
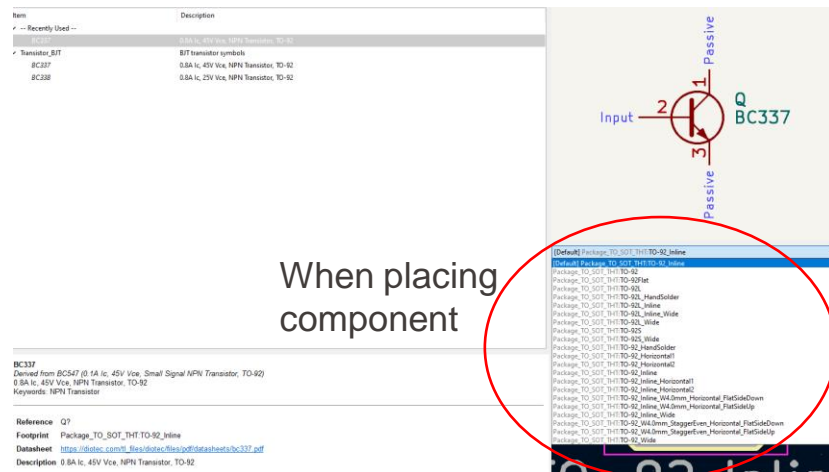
Schematic example: Basic clock

Tips & tricks:

- Use net labels to link nets without wires
(Possibility to have “global labels” to link between sheets)
- Use “No Connect” crosses when pins are unused
- Add decoupling capacitors to ICs
- Place unused parts on the schematic, tie inputs BUT NOT OUTPUTS (obviously)



- Make sure all footprints are already set in schematic
 - If footprint and/or symbol of your component does not exist, create it according to datasheet



Custom symbols and footprints

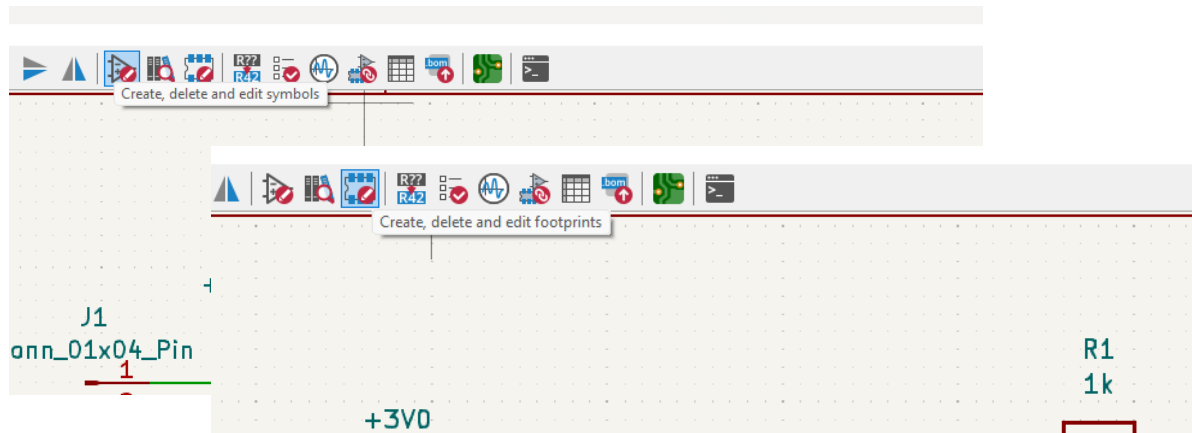
Default library should suffice in most cases, so only briefly shown during demo

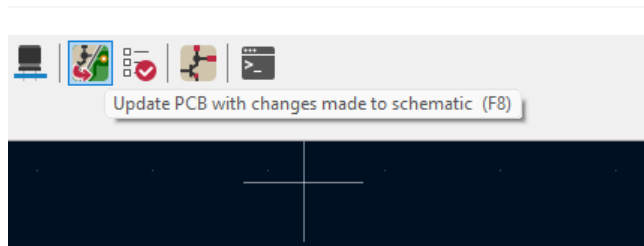
Steps quite self explanatory:

In create symbol window: File→New library
Select library
File→New component
Add pins, set designator, ...

Many resources online if need be, or ask us ☺

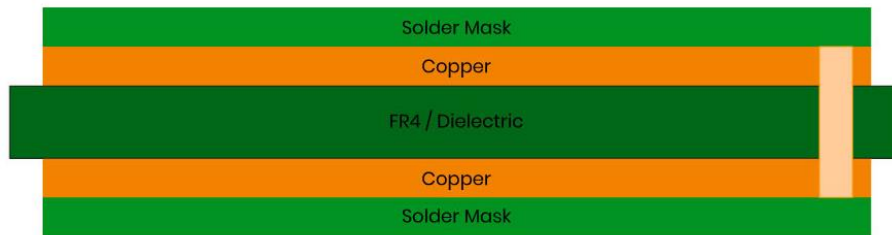
Take care to match pins and pads number order!





- Lists all the components/nets/... not matching between PCB and schematic
- All validated differences will be corrected on the PCB's side, adding components and connections alongside
- Note: Importing from schematic only checks that the component exists. If the footprint was changed in a library, you need to "update footprints from libraries"

2 LAYER RIGID PCB STACK-UP



TOTAL THICKNESS WITH MASK: 63.800 mils

LAYER DEFINITION

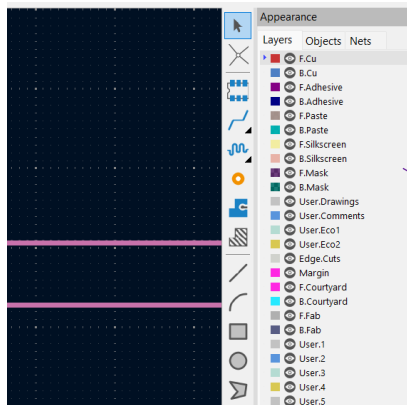
Mask

Layer 1

& silkscreens
(unavailable at ACI)

Layer 2

Mask



F. : Front side (more often called TOP)

B. : Back side (more often called BOTTOM)



Cu: Where there is copper (tracks, pads, ...)

Paste: For solder paste, usually equal to "mask"

Silkscreen: For annotations

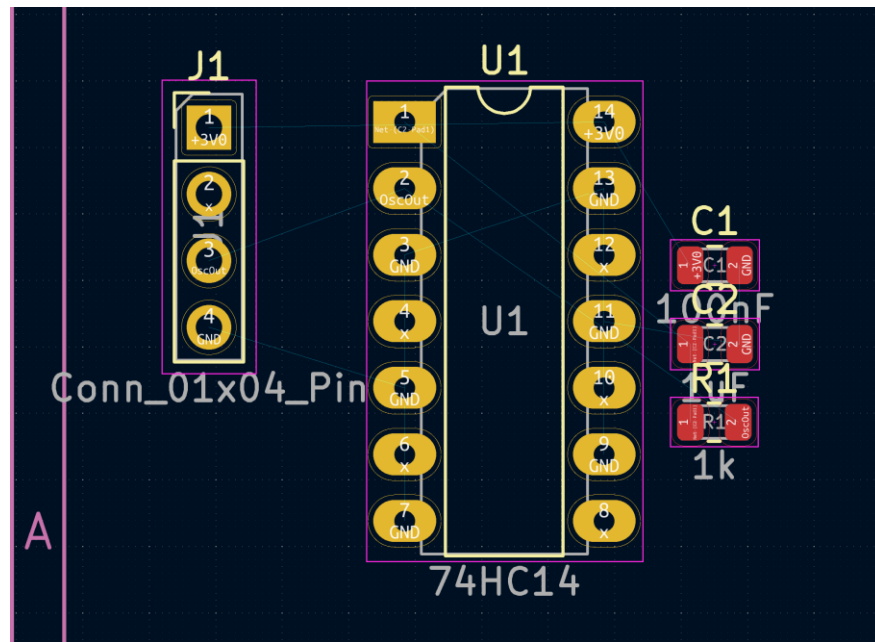
Mask: Where no solder mask should be placed

Edge cuts: Shape of the board

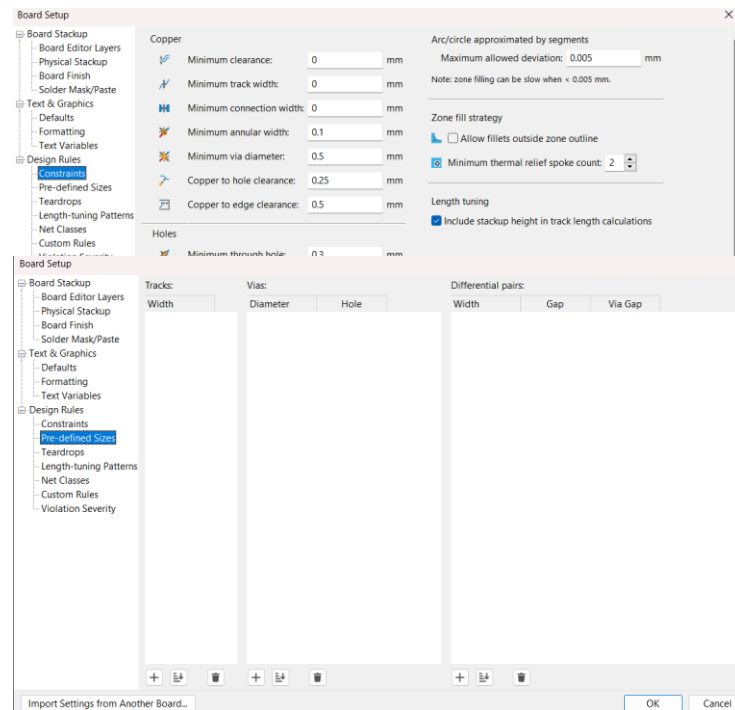
Fab: Fabrication schematic/annotations

...

- Once everything imported from schematics, it's time to plan the routing
- Keep the final application in mind:
 - Decoupling caps close to ICs' power pins
 - Mechanical constraints (location of connectors, holes, ...)
- Ratsnest: small lines showing the connections remaining



- Prepare rules corresponding to fabrication constraints
- **Good to do early on**



ACI gives set of rules.
(our PCB is made of FR4 0.8mm, 12um Cu)

Standard Dimensions (in mm)		
Description	PCB size max.	Panel size max.
Small	148 x 180	170 x 250
Medium	228 x 230	250 x 300
Large	228 x 310	250 x 380

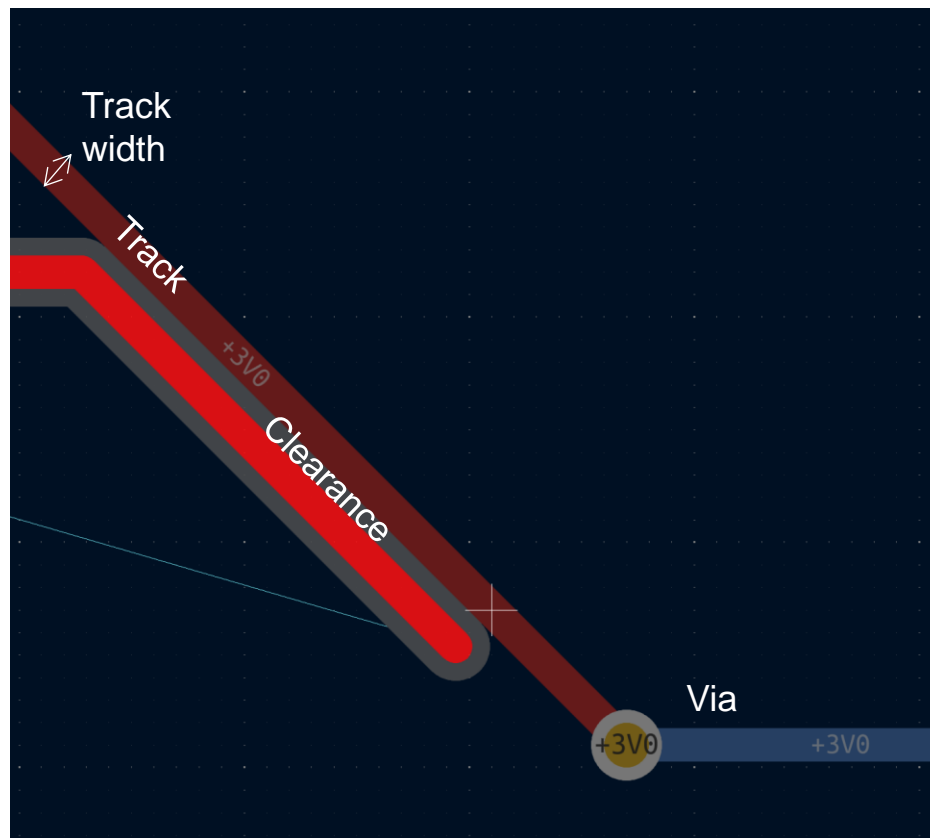
Hole Diameter (in mm)		
Material Thickness	Min. Hole Diameter	Max. Hole Diameter
	(c)	(c)
0.8	0.3	6.2

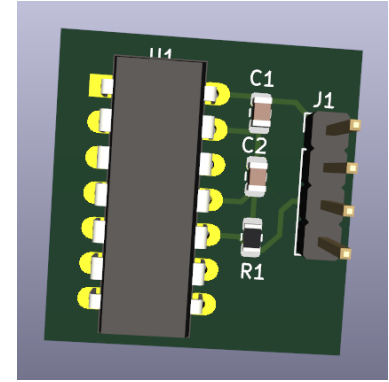
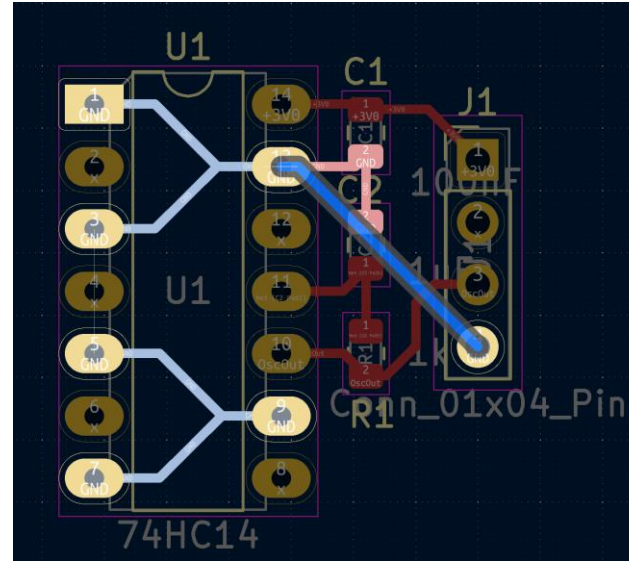
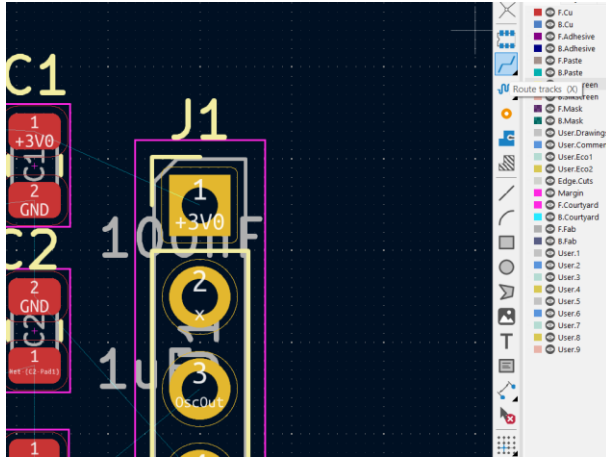
Available drills:

- From 0.25 up to 3.25 mm, by steps of 0.05
- From 3.30 up to 6.2 mm, by steps of 0.1
- Drill diameters above 6.2 mm must be placed in the Outline file, GERBER RS-274X format

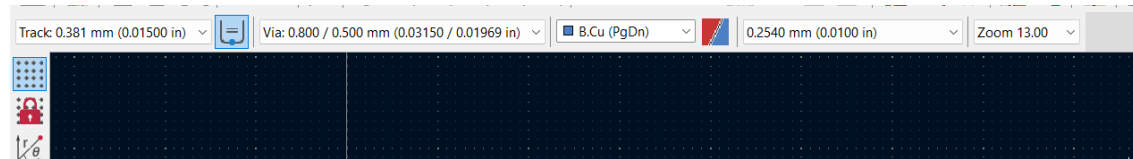
In brief, for our application:


- Width and clearance of minimum 250µm (10mil)
- Adapt width to current if high current application
- Via of 800µm, with hole of 500µm

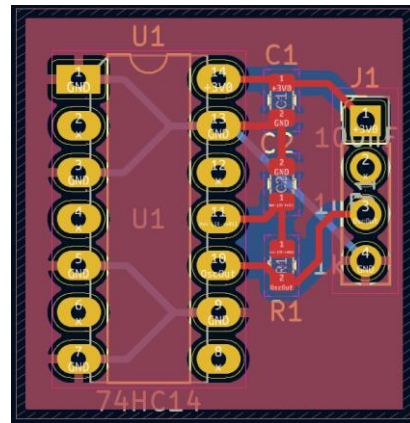
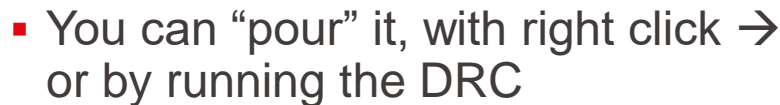




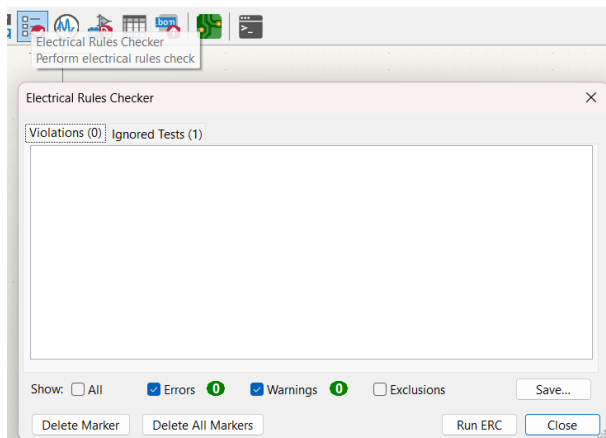
Use shortcuts:
Route (X), place vias (V), flip component
to other layer (F), ...



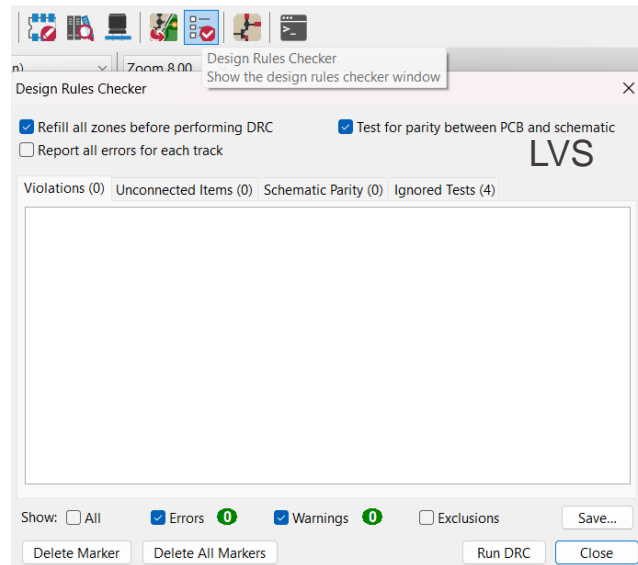
- Select a copper layer → 
- Add a zone following the PCB's edges, on TOP & BOTTOM, tied to GND

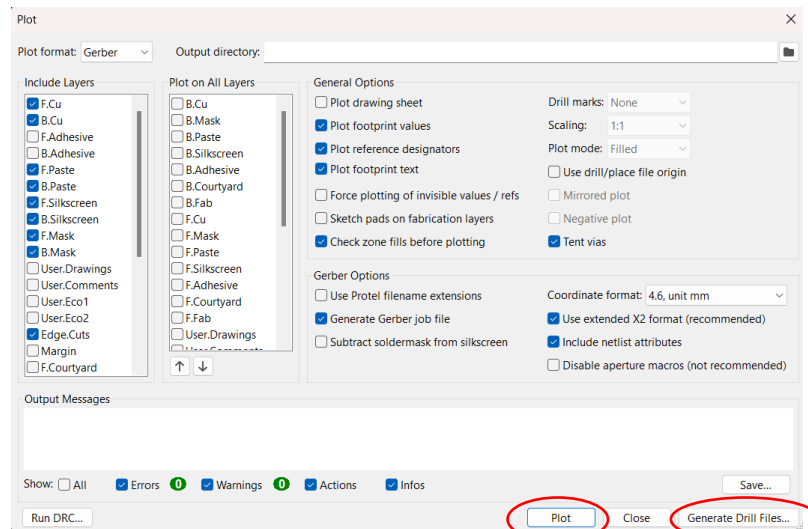
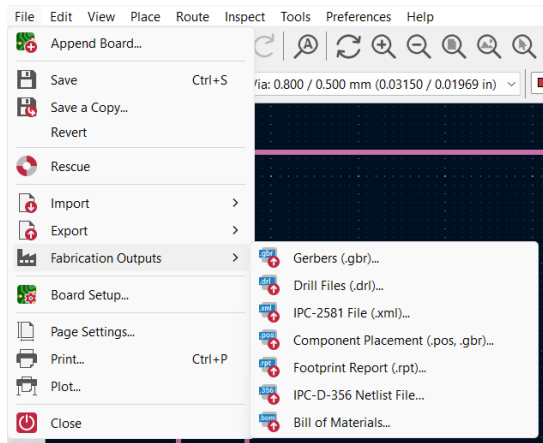


ERC



DRC





“Gerber files” are fabrication files containing each layer’s pattern
To make the PCB, both Gerber and Drill files are needed

“Include layers” → One file per layer, as needed for fabrication

“Plot on all layers” → Useful to export a PDF showing the final PCB and verify by hand

To provide: Gerbers of **Copper**, **Paste** and **Mask** layers (no silkscreen needed)
Drill Files (Excellon, other parameters should not matter as defined in the file itself)
PDF to scale of PCB layout