Nanofabrication of Multi-Gate Fully-Depleted Silicon-On-Insulator Nanowire Transistors for Electron Spin Qubits

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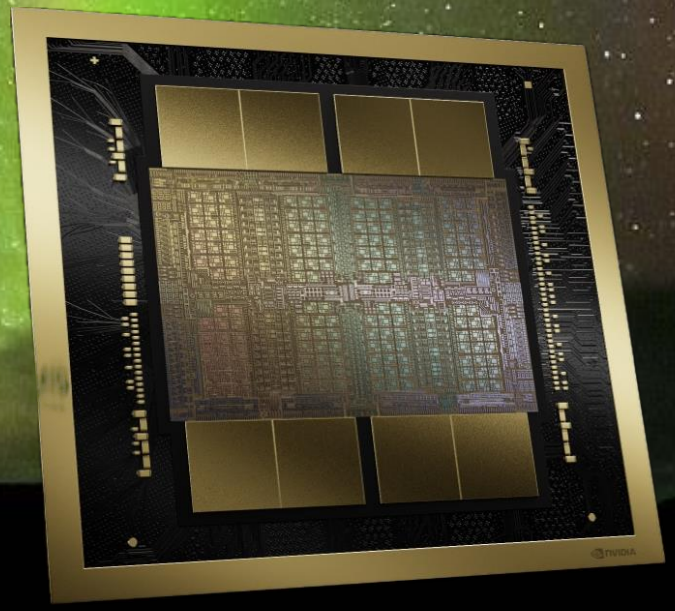
Outline

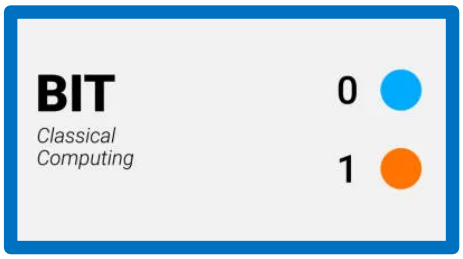
- Nanoscale processors and beyond
- Device functionality and structure
- Process flow
- Fabrication challenges of FDSOI nanowires vs bulk Si nanowires
- Growing of uniform gate oxides and contacts formation
- Patterning of nanogates: lift-off vs etching
- Insulation and encapsulation
- Conclusions

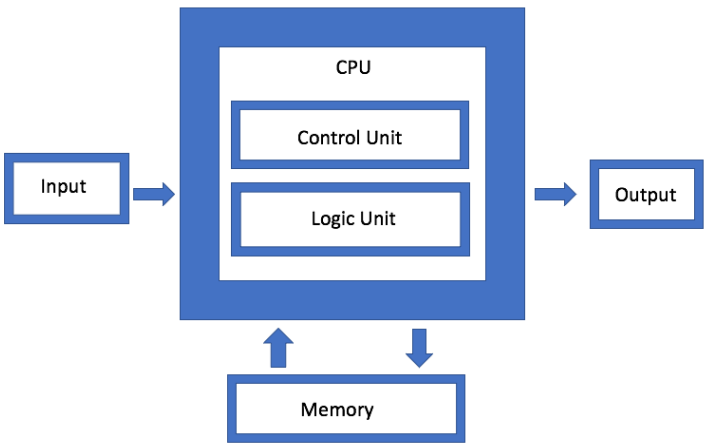
200B+ stars in the Milky Way

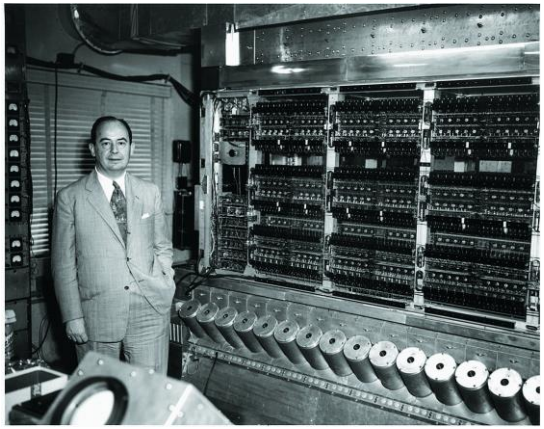
208B transistors in NVIDIA Blackwell, 576 GPUs, 10 TB/second chip-to-chip link



Von Neumann computing and beyond

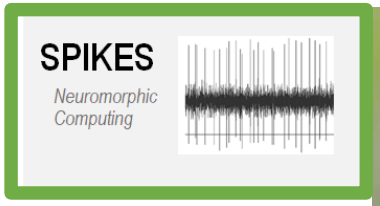


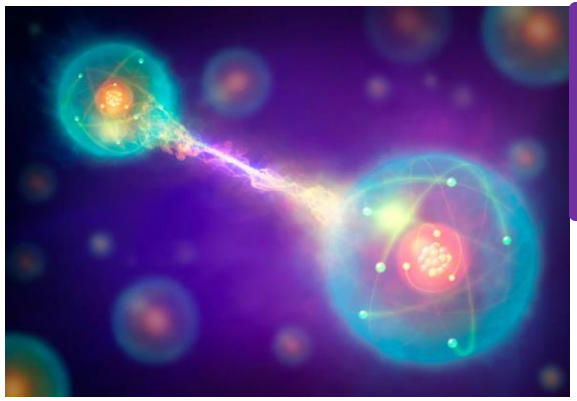




von Neumann in the 40's

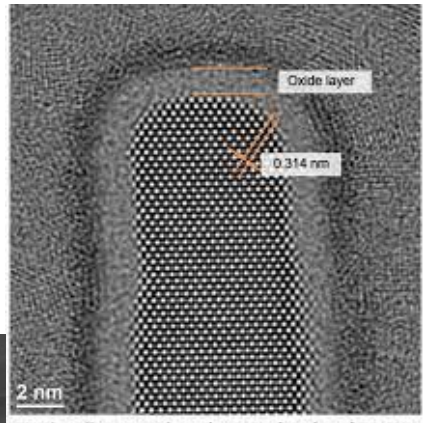
"The future of computing will not be based on ever-increasing processing power… it will rely on ***understanding and drawing inferences from massive collections of data****."*

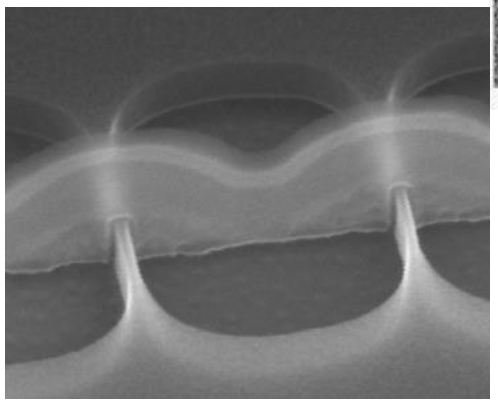


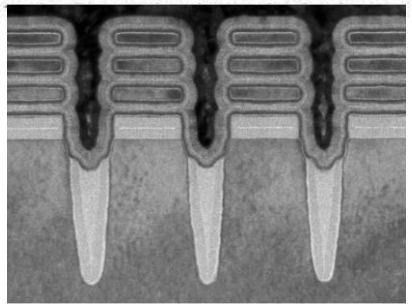


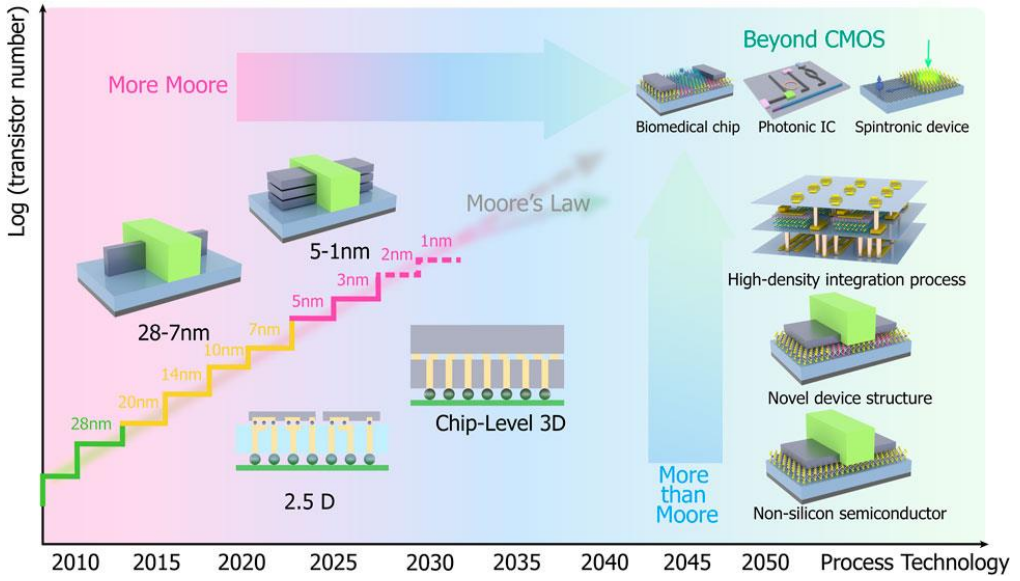
Moore's law and nano-CMOS

- From 100 micrometer down to 1 nanometer in 60+ years
- 100M to 1B transistors/mm^2
- Used by powerful von Neumann processors
- Largely dominant today

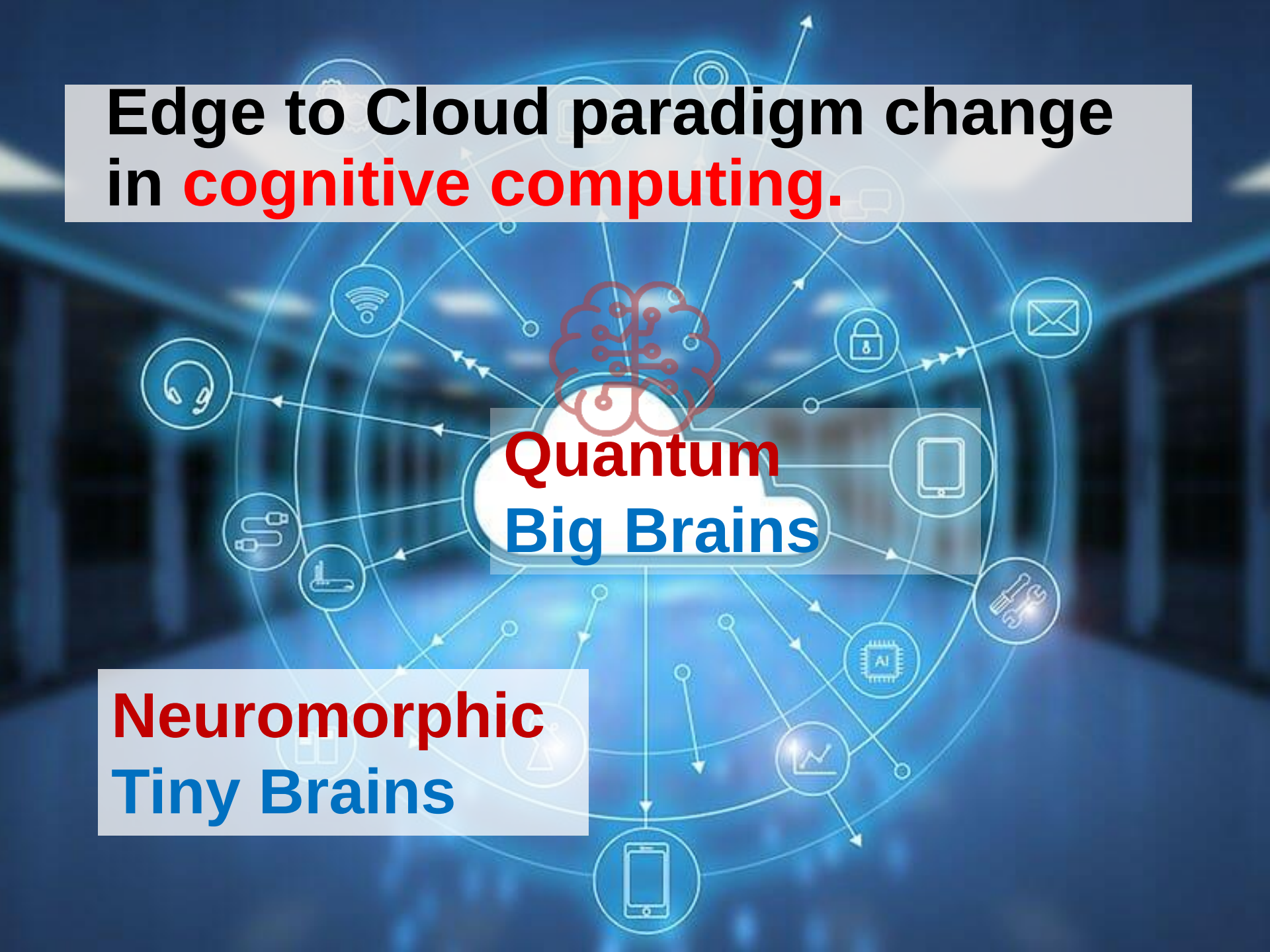








Edge to Cloud paradigm change in cognitive computing.

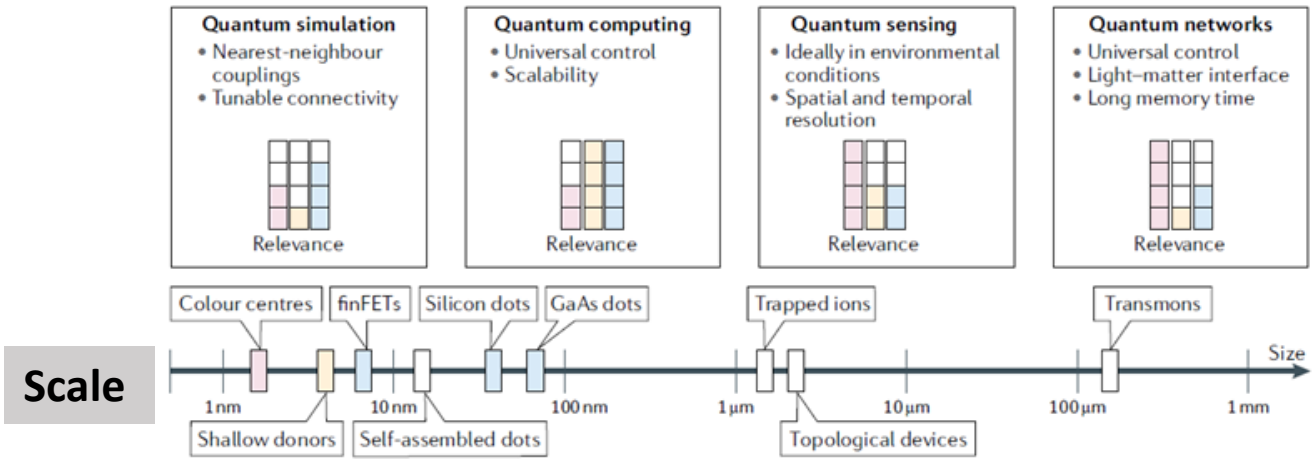


Semiconducting qubits for Quantum computing = why?

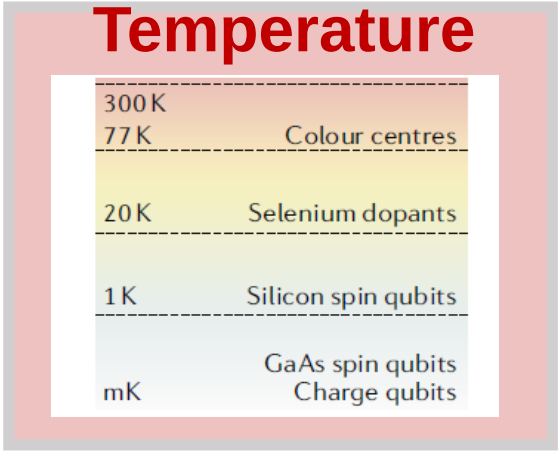
- **Qubits** = **spin** states of an atom or **electron/hole**, polarizations of a photon, energy levels of an ion, …
- **Superposition**
- **Entaglement**
- **Scaling =** N qubits – 2^N states
- **Probabilistic**

Qubit

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle,$$



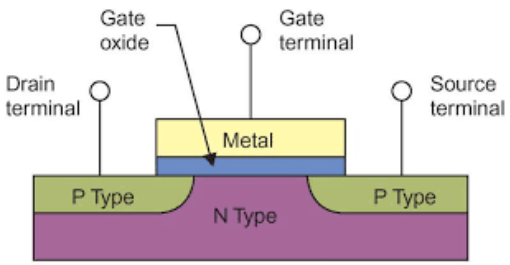
Scale

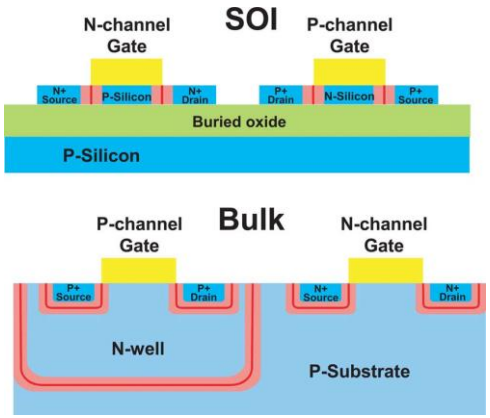


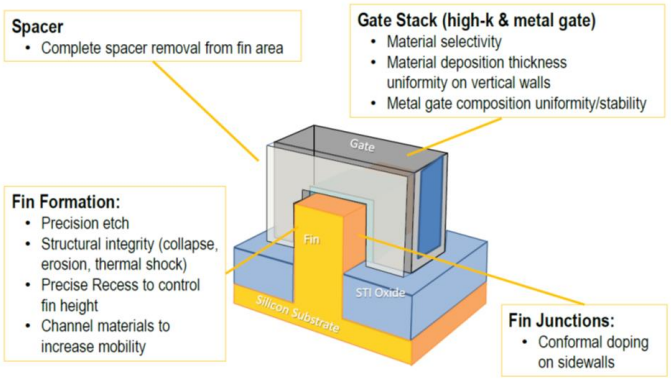
Semiconductor qubits need quantum dots and FET-like electrostatic gate control

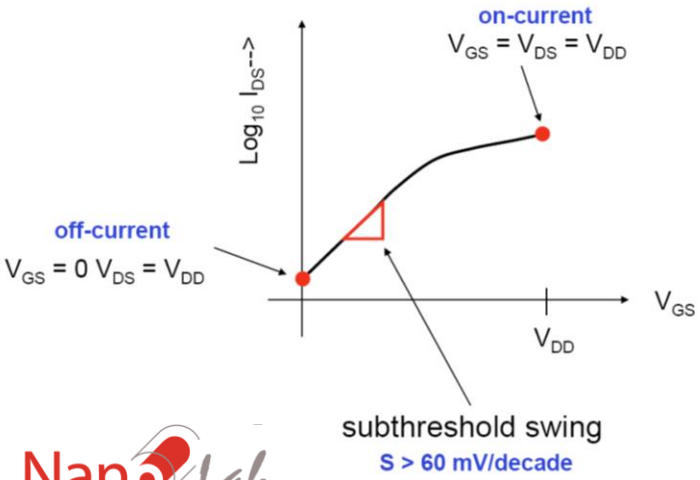
- What is a Field Effect Transistor?
- What is Fully Depleted Silicon On Insulator?
- What is a Quantum Dot (QD)?
- What is a Single Electron Transistor (SET)?

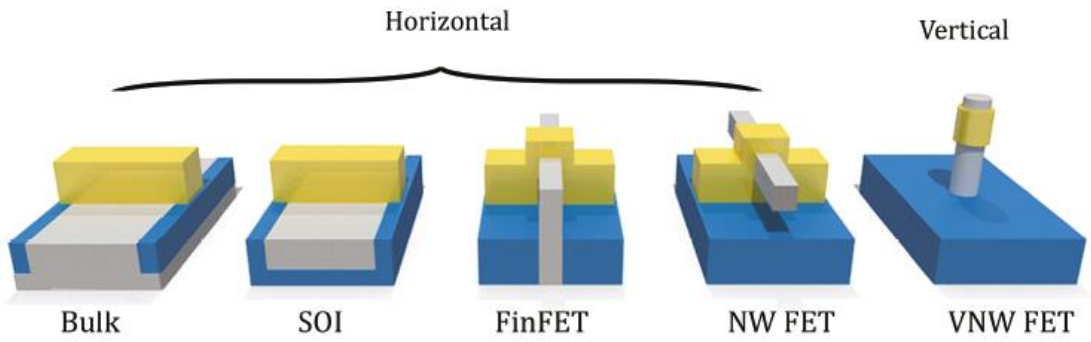
What is Metal Oxide Semiconductor Field Effect Transistor (MOSFET)?







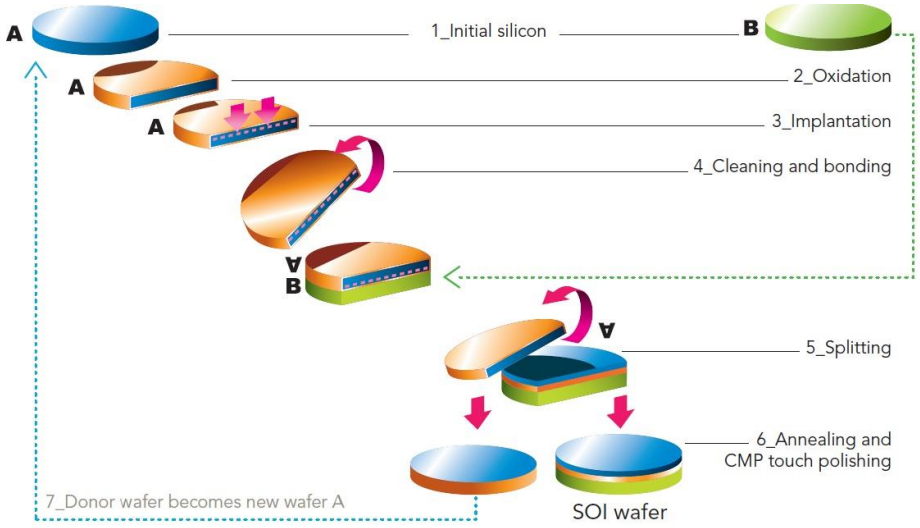




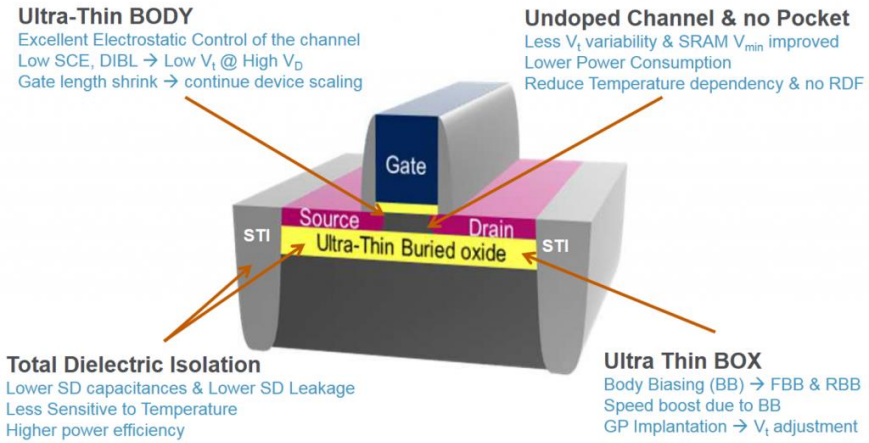
What is Fully Depleted Silicon On Insulator (FDSOI)?

SOI: a thin-film substrate alternative for advanced transistor technology.

FD SOI by Smartcut process



FD SOI MOSFET



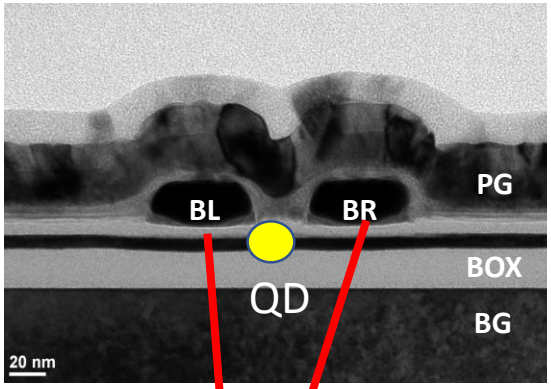
What is a Quantum Dot?

A quantum dot (QD) is a **semiconductor nanocrystal**

Nanomaterials have at least one dimension < 100 nm, for quantum dots it's all three dimensions → 0D material

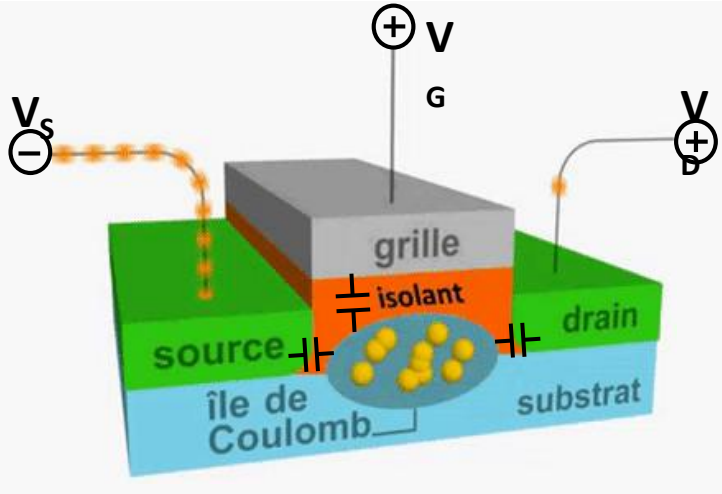
Quantum dots can be obtained by bottom-up or top-down approach

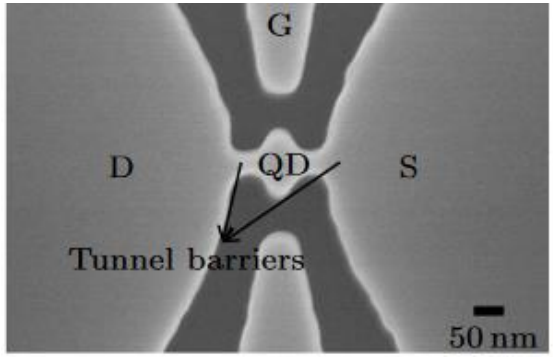
- Bottom-up → synthesis (ex. CdS), Nobel prize 2023
- Bottom-up → epitaxy
- Top-down → etching



Gates inducing potential barriers in the silicon (SOI) layer

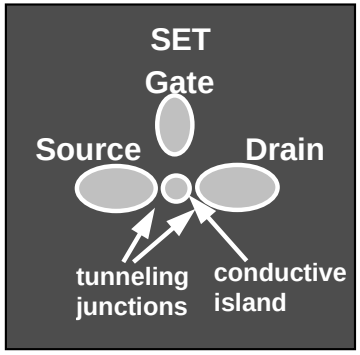
Our QDs are confined in **silicon** by potential barriers or etched structures

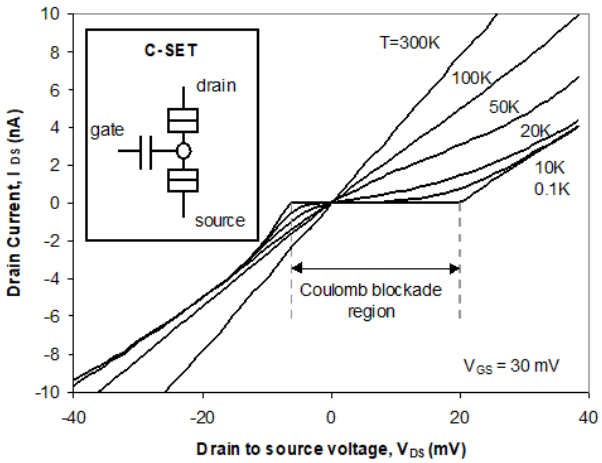


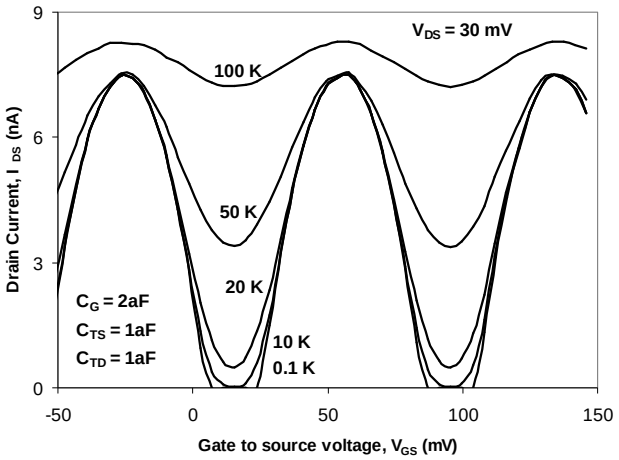


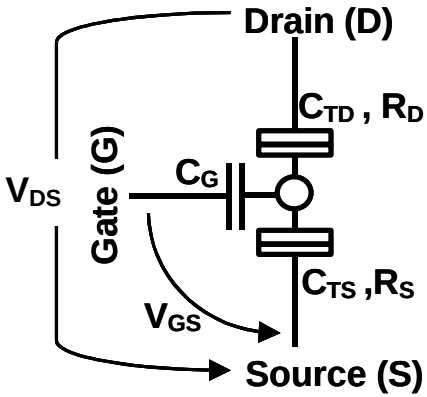
What is a Single Electron Transistor (SET)?

SET is a 3-terminal **electronic switch** using **Coulomb blockade**







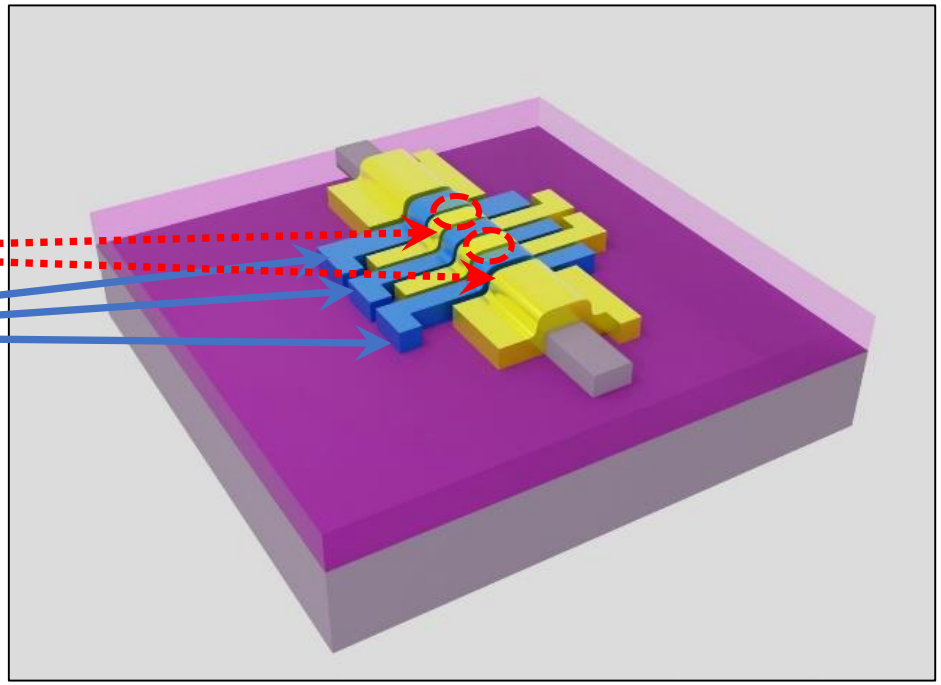


- electron conduction is one by one: by tunneling through a barrier
- drain & gate control Coulomb blockade (CB)
- needs opaque junctions: $R_T > R_Q$~26kW
- needs very small island (~1nm) for room temperature operation

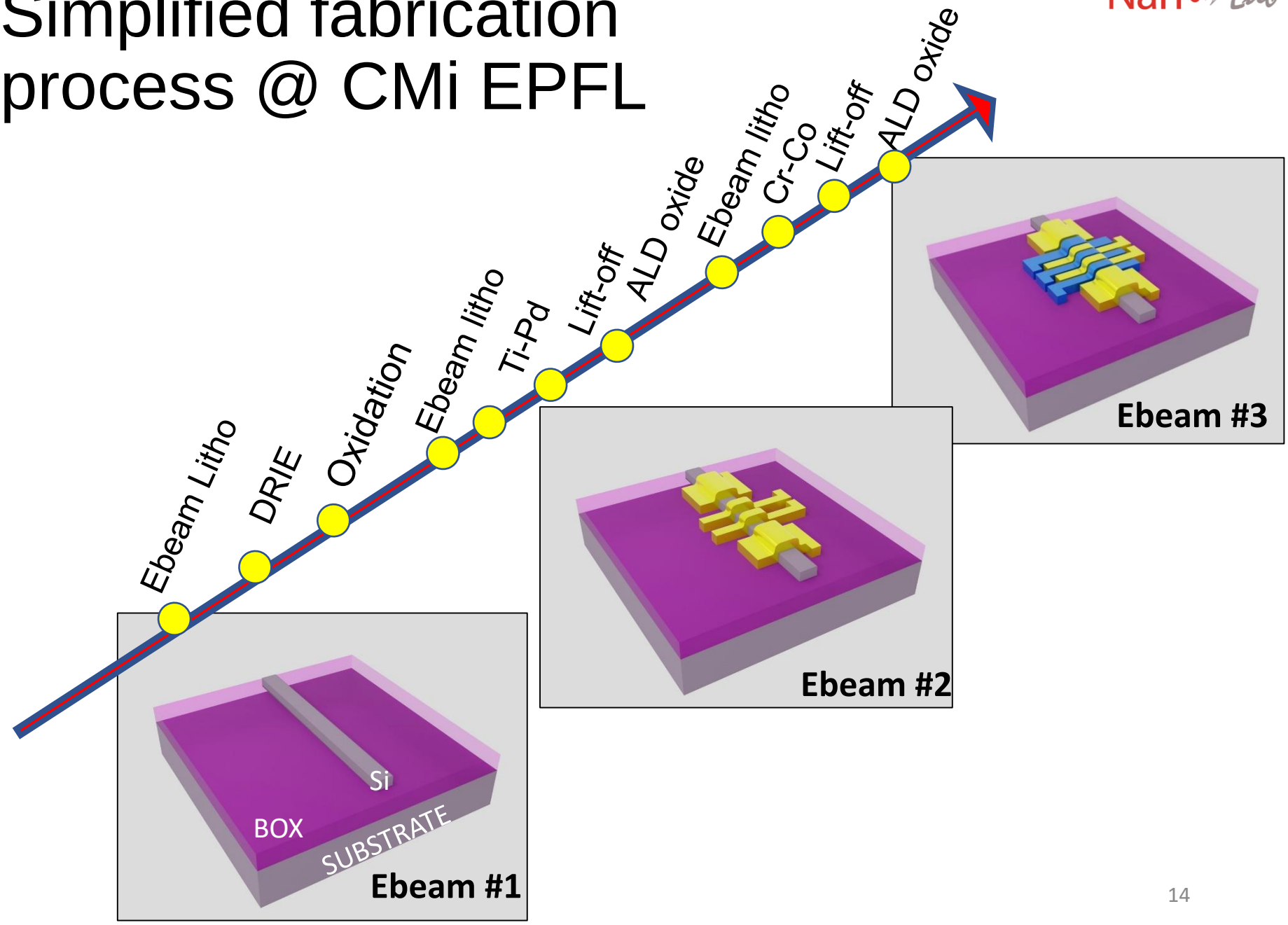
Scalable quantum dot silicon qubit

Electron spin qubit based on gated FD SOI quantum dots

- Silicon-On-Insulator
- Nanoscale QDs
- Ferromagnetic gates
- Tunable QD coupling

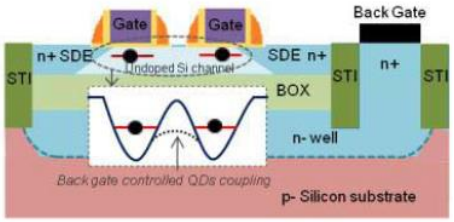


Simplified fabrication process @ CMi EPFL

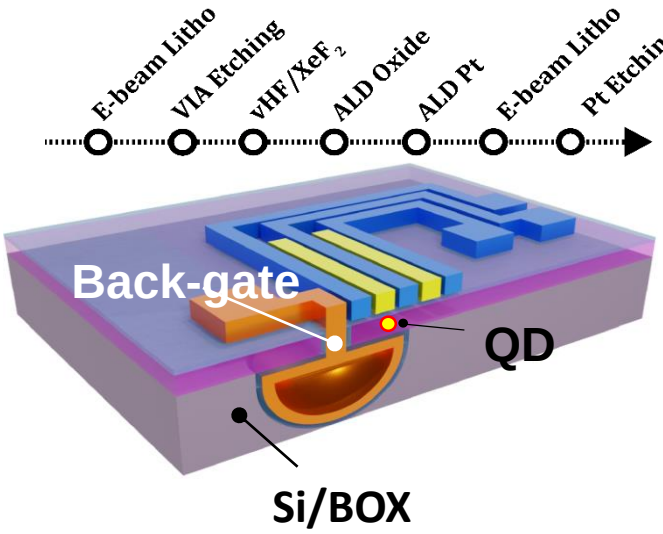


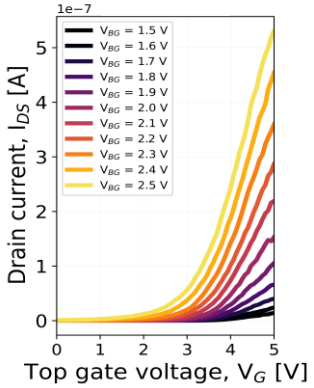
Additional feature: tunable double-gate quantum dots

Issue: back gating of qubits through n-well does not work properly at sub-100mK



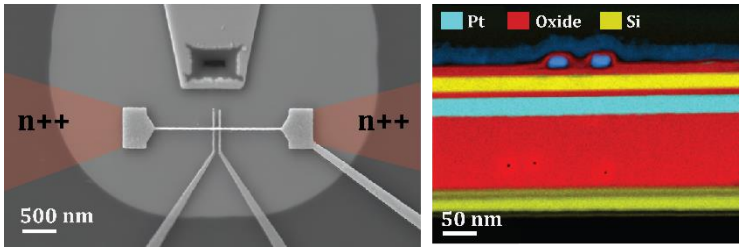
Solution: a metallic back-gate



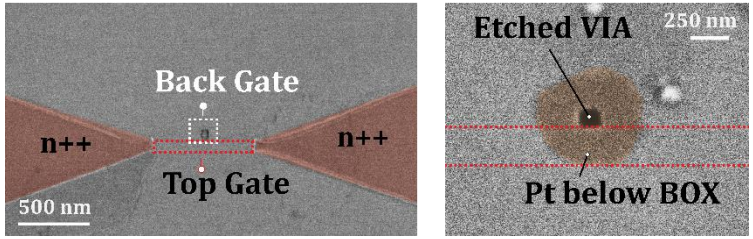


Silicon-On-Nothing

Nanomole - BOX Etching



Nanomole - Substrate Etching



Bersano, F., et al. *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*. IEEE, 2024.

Multi-Gate FDSOI Nanowire FETs

Simplified process flow

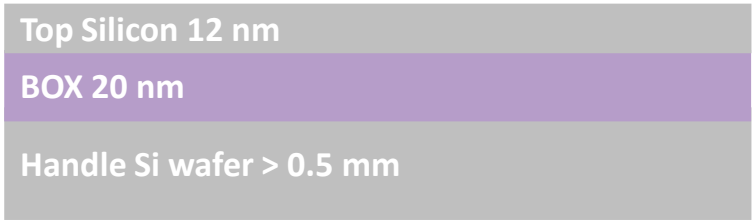
What	How	Why
1. Markers etching	e-beam lithography + dry etching	Layers alignment
2. Dopant implantation	Plasma immersion ion implantation	Doping of source and drain
3. Nanowire etching	e-beam litho + dry etching + HF etching	Lateral confinement
4. Gate oxide formation	Thermal oxidation or ALD/PECVD	Insulation for gating
5. Contacts: source and drain	e-beam litho + HF + evaporation + lift-off	Channel contacts
6. Contacts: first gate layer	e-beam litho + evaporation + lift-off	QD confinement
7. Interlayer oxide deposition	ALD or PECVD	Insulation between gates
8. Contacts: second gate layer	e-beam litho + evaporation + lift-off	QD and channel control
9. Passivation oxide deposition	ALD or PECVD	Protection
10. Post-metallization annealing	Forming gas thermal treatment	Charge traps reduction

Substrate: FDSOI vs bulk Si

SOI = Silicon On Insulator, FD = Fully Depleted (very thin top Si)

Why FDSOI?

- No channel doping is needed (= no **fixed charges** in the channel)
- Smaller depletion capacitance → reduced SS → lower gate bias required
- Better channel control → lower drain bias required
- Lower parasitic capacitance
- Lower leakage currents
- **Back-gating** is possible



BUT… there are fabrication challenges

Better power efficiency, less **heat dissipation** required.

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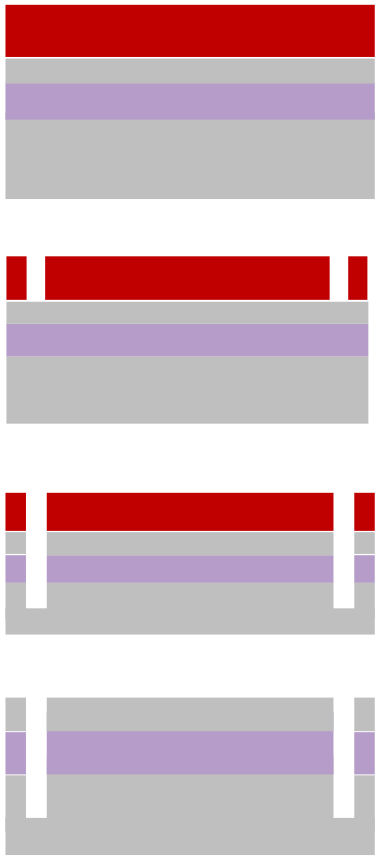
1. Markers Etching

- First layer, required to **<u>align</u>** the various lithography layers
- All the features in a device are positioned relative to the markers
  - The edges of the chip cannot be used, too rough and there are edge effects of the resist
- For the nanogates, a **<u>precision of ± 5 nm</u>** (!) is required
  - Three-steps alignment with different markers
- 20 µm wide and 2 µm deep markers are required for the e-beam
- In a FD-SOI?
  - The markers pass through the top Si and the BOX
  - The BOX is exposed in some of the subsequent steps
  - Some etching processes could affect the BOX and generate some roughness
  - A marker with rough edges will compromise the nanogates alignment



Importance of a good process flow and of the choice of all the materials and fabrication steps

Simplified Process Flow

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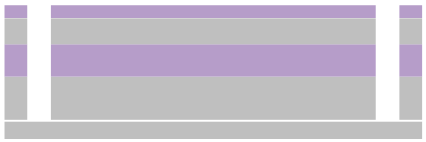
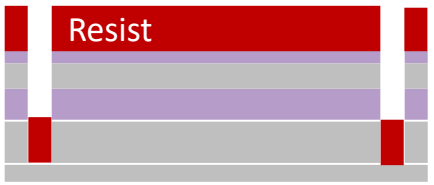
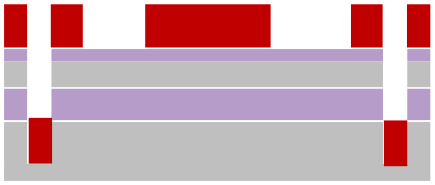
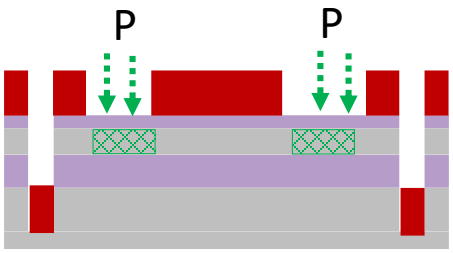
2. Dopant Implantation

- The fabrication step is outsourced (no equipment available in our cleanroom), but we have to ask for a specific implantation energy.
- An adequate doping level is important for the **ohmic** contacts.
- In bulk Si (for research purposes) → just use high enough energy.
- In FDSOI
  - Ideally, uniformly dope the top Si, stop at the BOX.
  - In practice, BOX gets damaged.
  - Often, some dopants are implanted below the BOX, a spurious channel can be formed in the substrate and leakage is observed.









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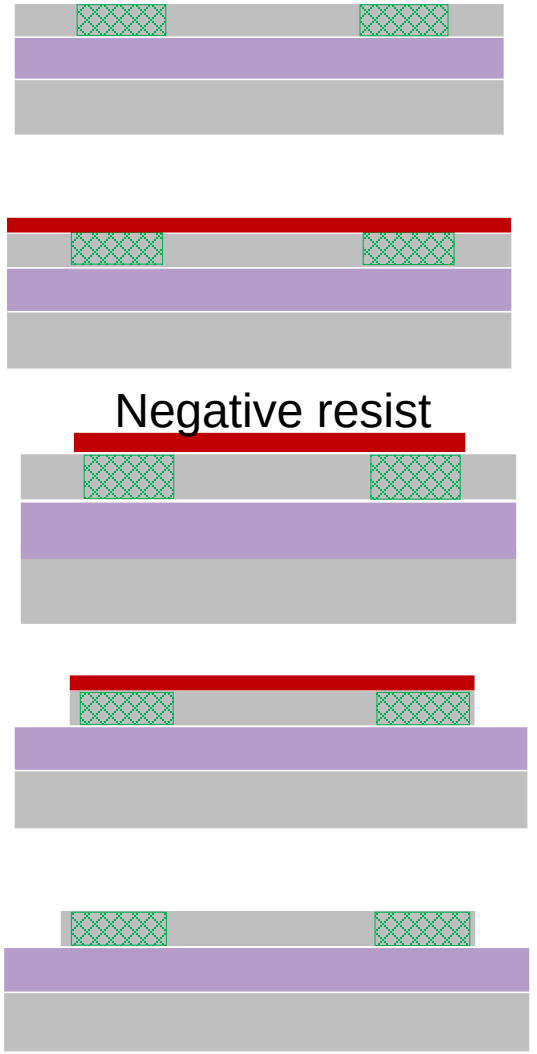
3. Nanowire etching

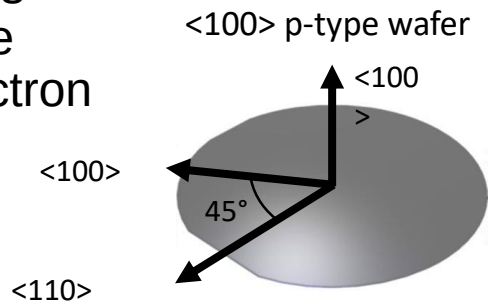
- The lateral dimension of the channel (30-60 nm) provide the **quantum confinement** required for the quantum dot (QD) formation
- A reliable and accurate process is required
- Sidewall roughness minimization is important for reduction of **device noise**

- Let's break down the process variables:
  - Nanowire direction
  - Resist choice
  - e-beam parameters
  - Etching choice
  - Resist removal

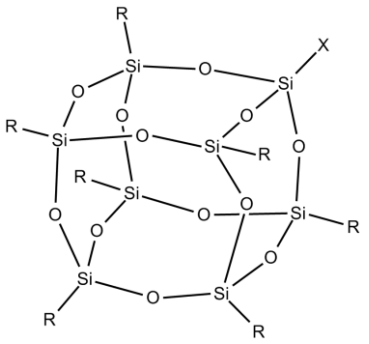


3. Nanowire Etching

- *Nanowire direction*
  - Orienting along the [100] direction ensures that the sidewalls are on the (100) plane, as for the top → uniform and well-characterized **thermal oxide growth**
  - BUT… at wafer scale, it means drawing diagonal lines with respect to the flat used for the alignment → more rough for how the e-beam lithography moves the electron beam
  - Possible solution → draw diagonal markers and dice chips with (100) sides

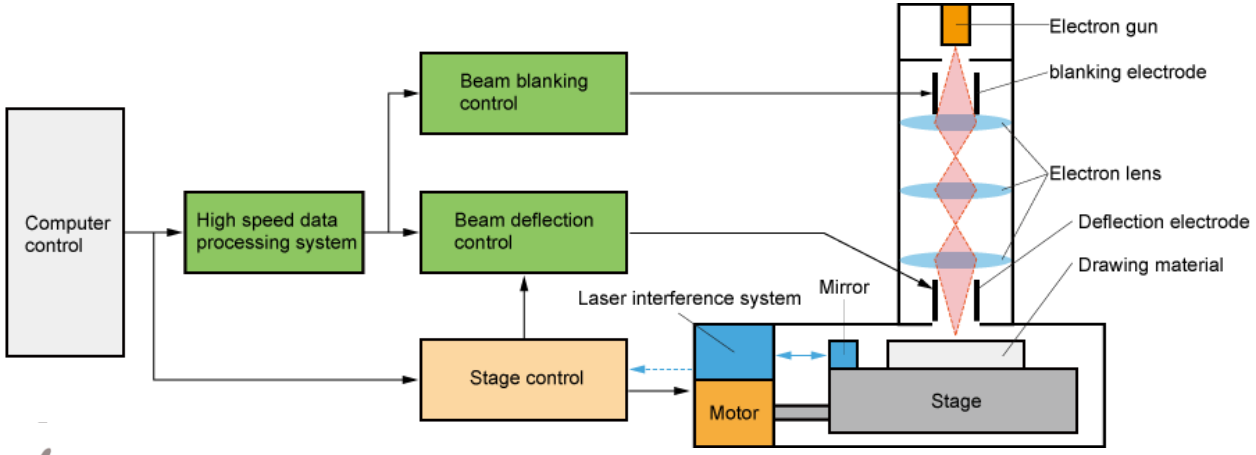


- *Resist choice*
  - To etch the nanowires, we want to preserve the resist only on them (<< 50 % of the area)
  - A **negative tone** resist is the best choice
  - To achieve the required dimensions, hydrogen silsesquioxane (HSQ) is the best choice



3. Nanowire Etching

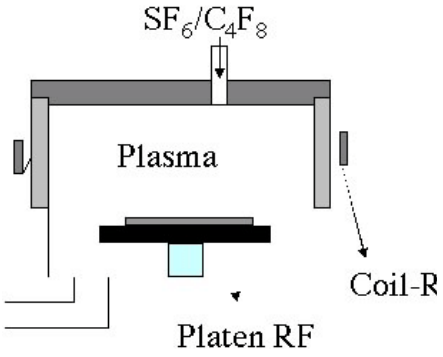
- *e-beam parameters*
  - By changing the beam current and the exposure time on each spot, the total charge per area (= dose μC/cm^2) is changed
  - A good **dose** allows to obtain the desired features in the correct dimension
  - If the dose is too small, the design will become blurry during the development and the resist may not act as a good mask during etching
  - If the dose is too high, it will be more difficult to remove the exposed resist after the etching

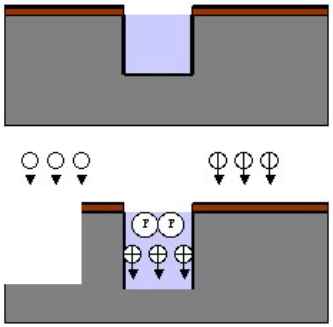


3. Nanowire Etching

Etching options

TMAH → sensitive to native oxide, not easy to calibrate and control
Ion beam etching → rough and very energetic
Anisotropic plasma (dry) etching → our choice, still needs **<u>calibration</u>**, it's very fast





Inductively Coupled Plasma etcher (ICP)

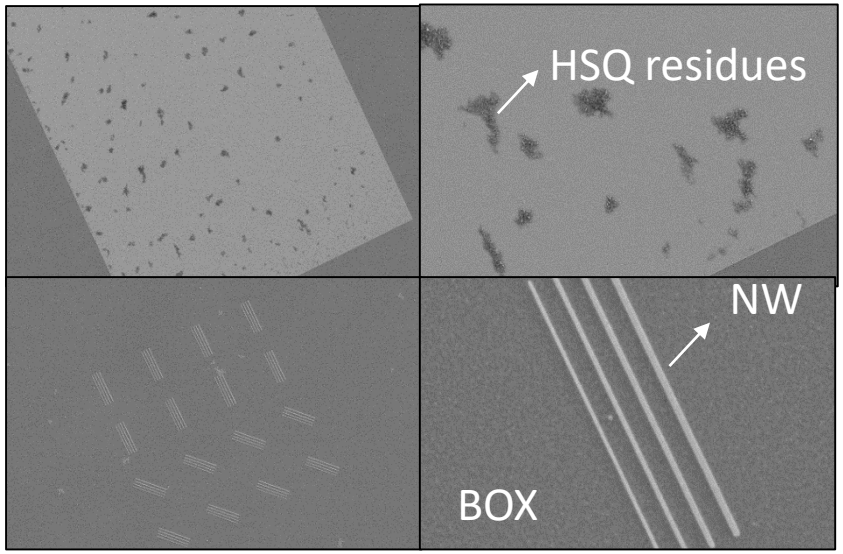
PlasmaPro 100 Cobra ICP

3. Nanowire etching

Resist removal

- Cross-linked HSQ is chemically similar to SiO_2, HF will remove it after the dry etching process
- BUT we work on FDSOI, the BOX is fully exposed after etching
- If the HF concentration is too high, or the wet etching too long, the BOX will be damaged or removed
- **A specific e-beam dose has been optimized, to allow obtaining the desired nanowires with the minimal dose possible (A lot of dose tests!)**
- In this way, the HSQ is only partially cross-linked and it's removed much easier that the BOX

What about stopping earlier the Si dry etching to leave a protection over the BOX? Too rough and fast, difficult to get a reproducible process.



Some SEM images of test nanowires and pads. Note the HSQ residues.

Simplified Process Flow

What	How	Why
1. Markers etching	e-beam lithography + dry etching	Layers alignment
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4. Gate oxide formation	Thermal oxidation or ALD/PECVD	Insulation for gating
5. Contacts: source and drain	e-beam litho + HF + evaporation + lift-off	Channel contacts
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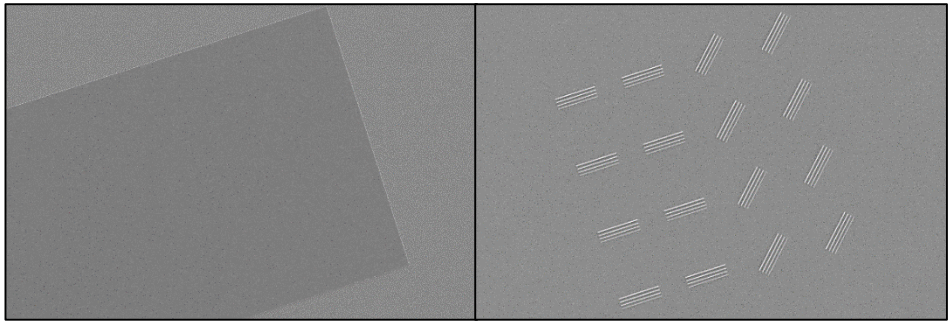
8. Contacts: second gate layer	e-beam litho + evaporation + lift-off	QD and channel control
9. Passivation oxide deposition	ALD or PECVD	Protection
10. Post-metallization annealing	Forming gas thermal treatment	Charge traps reduction

4. Gate oxide formation

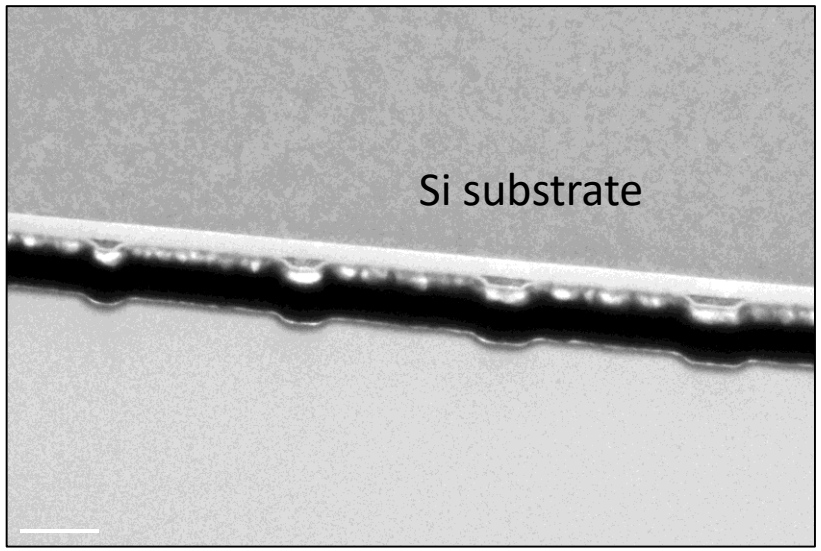
- Mandatory step for any gate stack
- To account for possible fabrication problems, we work on chip scale
- ALD is be the most flexible and convenient solution, but its oxides have generally a large charge trap density → source of **noise and decoherence** for the QD and qubits.
- Growth of **dry thermal oxide (SiO_2)** is the cleanest solution, BUT
  - The equipment is compatible with wafers → design of a dedicated chip holder
  - We cannot assume that the growth rate around a nanowire is the same as in a flat wafer → FIB lamella preparation, TEM characterization, and electrical testing.

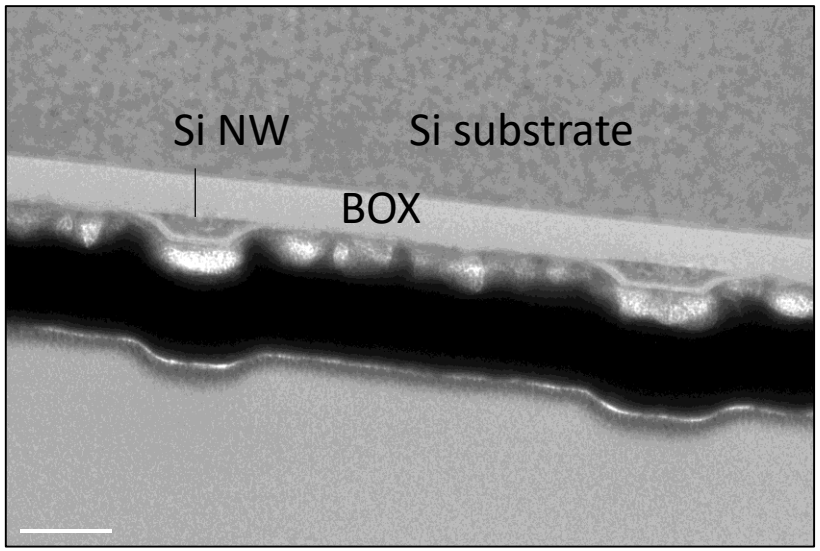


After the thermal oxidation, the HSQ residues disappear!

4. Gate oxide formation

Transmission Electron Microscopy (TEM) as a tool for inspection of cross sections: long (and expensive) procedure.





Example: cross sections of silicon nanowires with Pt on top to prevent Si amorphization during the lamella preparation.

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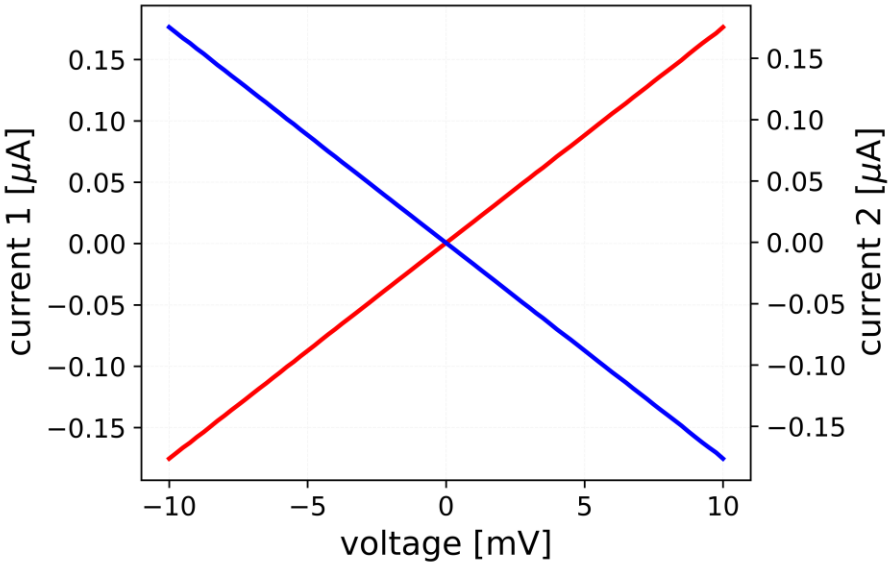
5. Contacts: Source and Drain

- Critical step to have ohmic contacts (= linear, compatible with low drain voltage)
- To have a ohmic contact we need to:
  - Choose a metal with an appropriate work function for band alignment
  - Highly dope the source and drain areas (our choice)
  - Generate some metal silicide by metal deposition and thermal treatment (only done by industry)



Example of ohmic contact: the contact between the metal and semiconductor is equivalent to a short circuit!

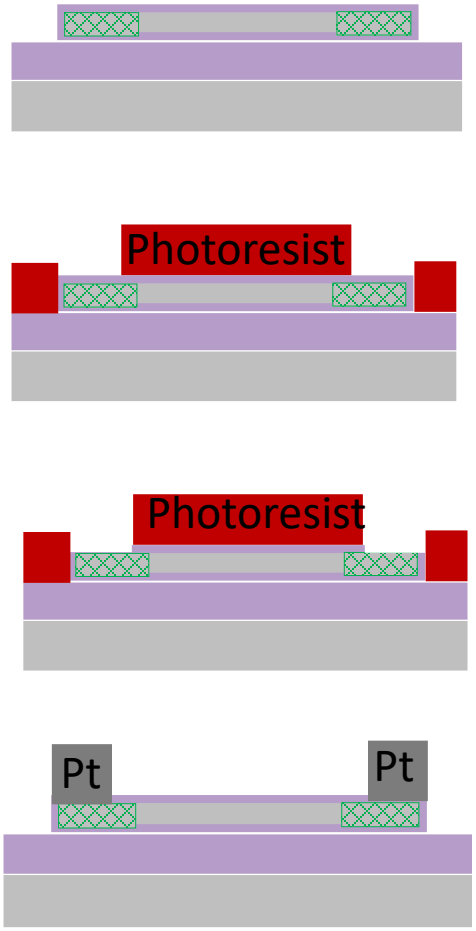
5. Contacts: Source and Drain

In FDSOI, the thin top Si provides a **high contact resistance**, how to solve?

- Larger source and drain areas → more chances of leakage (remember the dopant implantation?)
- Using both implantation and silicide → hard to optimize
- A high resistance contact can still be ohmic, there just has to be enough current at cryogenic temperature.

What can we control?

- The interface between Si and metal needs to be perfectly clean.
- HF etching of native oxide **minutes** before the metal (Ti/Pt) evaporation.



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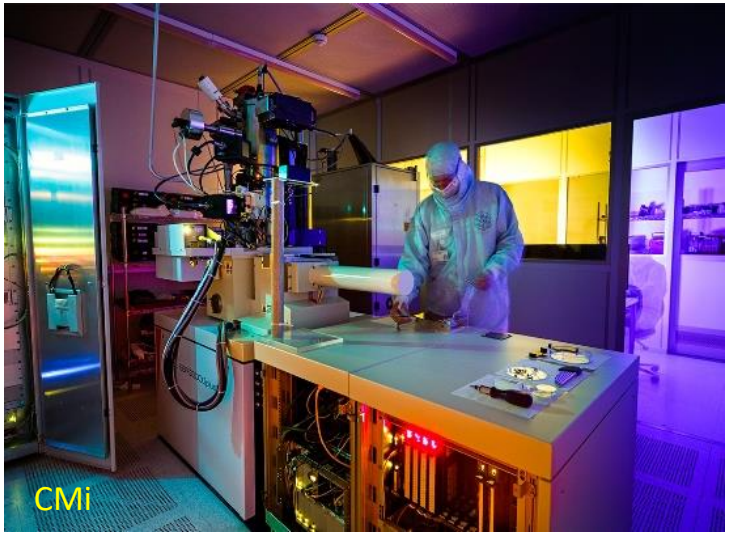
6. First Gate Layer

Goal: lift-off of 30 nm wide metallic lines spaced by 30 nm. The resolution needed is **<30 nm.** Expected alignment accuracy < 5 nm.

Only one solution (we are not Intel or TSMC): e-beam lithography with a POSITIVE tone resist. Which resists are available?

- **MMA/PMMA**: Positive tone. Polymer. Primarily used for lift-off, primary choice for wet etch, can be used for dry etch as well.
- **ZEP 520A:** Positive tone. Polymer. Primarily used for dry etch. Better resistance to dry etch than PMMA.
- **CSAR 62:** Positive tone. Polymer. Primarily used for dry etch. ZEP alternative.

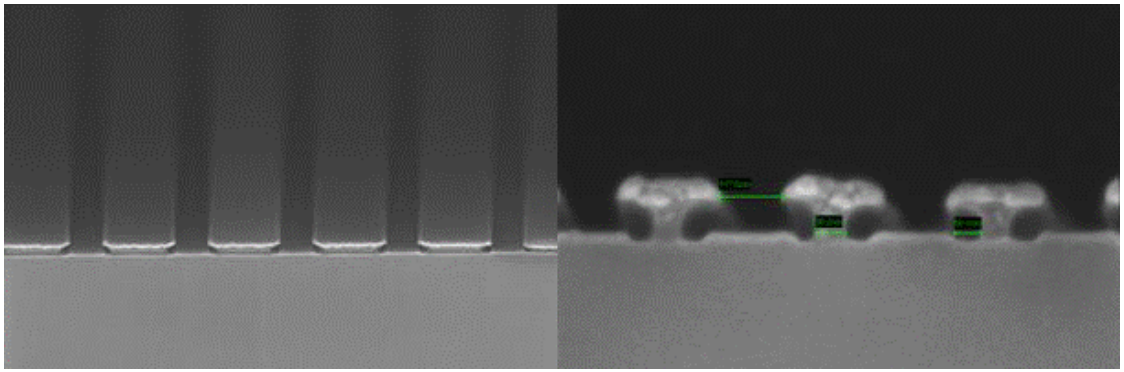


Ebeam system of EPFL

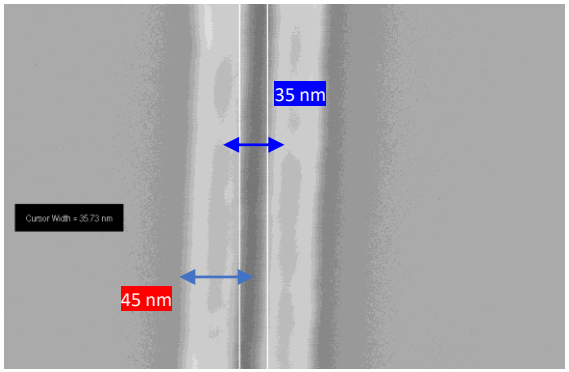
6. First Gate Layer

PMMA (poly methyl methacrylate) and MMA (methyl methacrylate) are positive e-beam resists consisting of long polymer chain of carbon atoms which comes in various molecular weights. The standard use for PMMA/PMMA and MMA/PMMA bilayers in EBL is for lift-off of metallic structures.

Do we need a *double layer* for a lift-off?
USUALLY yes, a double layer based on positive resists with different molecular weights would ease the lift-off of a metal. However, the undercut limits the final resolution, therefore we use a PMMA layer only.



Example of undercut in a MMA/PMMA bilayer.



Metallic wires patterned with PMMA only.

6. First Gate Layer

PMMA spin-coating

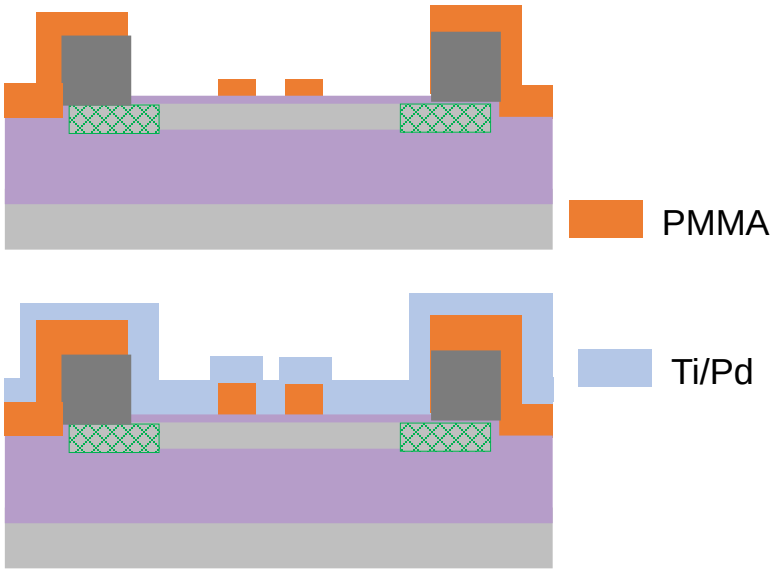
- Speed (rpm) chosen depening on the needed thickness

Ebeam exposure and development

- Dose and current tests
- Development in a “magic” chemical ☺

Ti/Pd evaporation

- The thickness should be high enough to climb the nanowire but small enough to enable a clean lift-off!

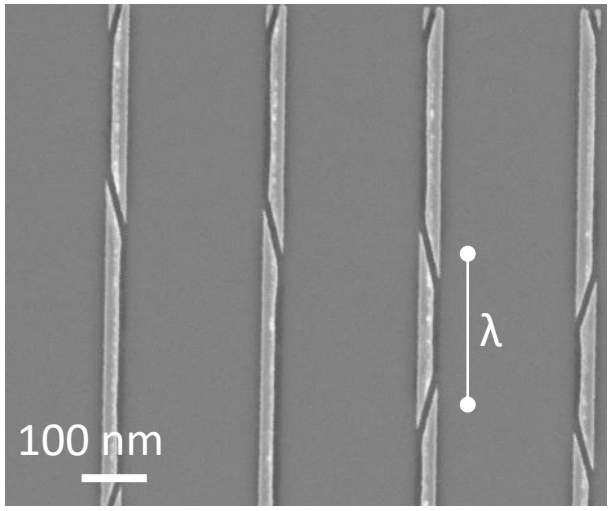


NOTE: typically a quick step of oxygen plasma is performed to clean the surface before metal evaporation.

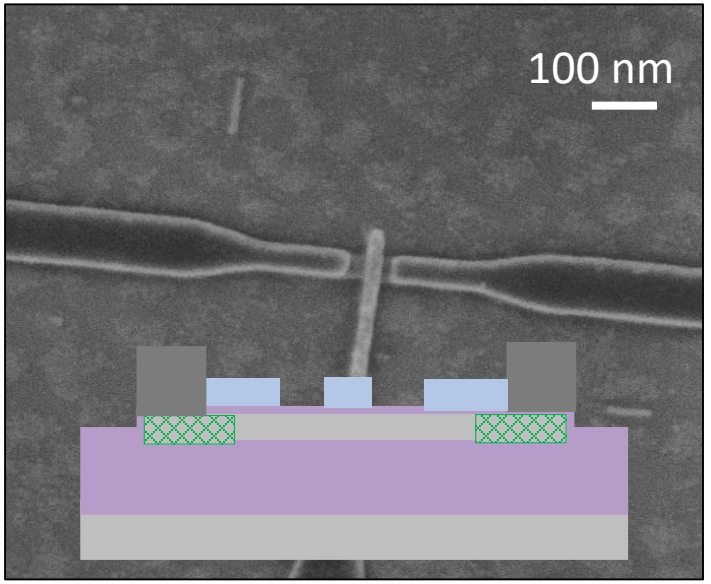
6. First Gate Layer

Lift-off

- in Acetone (organic solvent), used to dissolve polymers
- There are other commercial products stronger (and better) than acetone
- Should we use ultrasounds to “shake” the sample?? **NO!**



Metallic nanowires broken after sonication with ultrasounds.



SEM picture of a nanowire with the first layer of gates patterned and schematic of the cross section.

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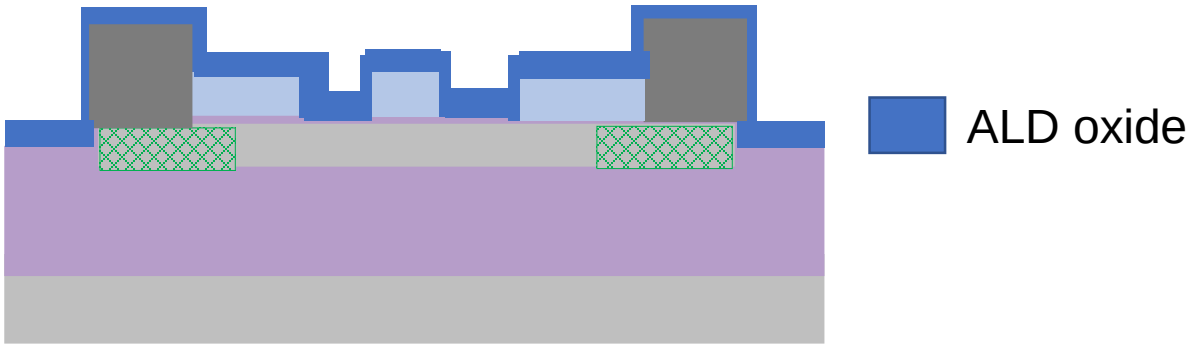
7. Interlayer Oxide

An interlayer oxide (insulator) is required to isolate the first metallization layer from the second, allowing independent field-effect control of the channel by the two sets of gates. This insulating layer ensures that each gate can apply its field without interference from the other.

Options:

- Atomic Layer Deposition (ALD) (very conformal)
  - **SiO_2** or Al_2O_3
- Plasma Enhanced Chemical Vapor Deposition (PECVD), for thicker layers.



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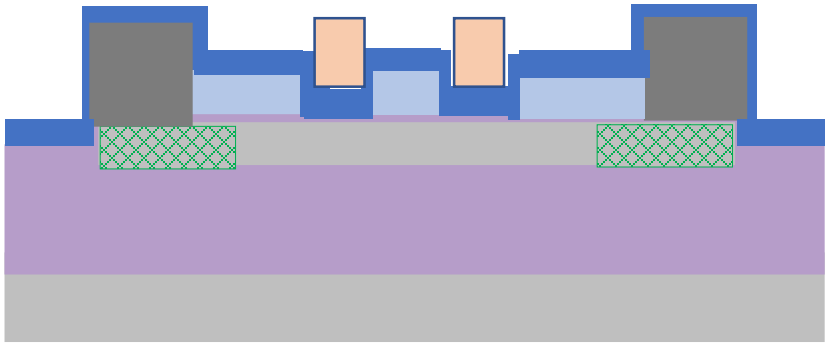
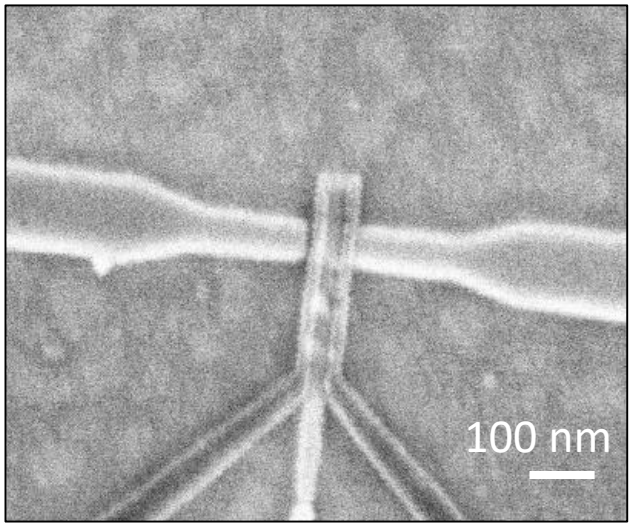
7. Second Gate Layer

We follow the same procedure of the first layer of gates:

- ❑ e-beam lithography
- ❑ Evaporation of metals
- ❑ Lift-off in Acetone



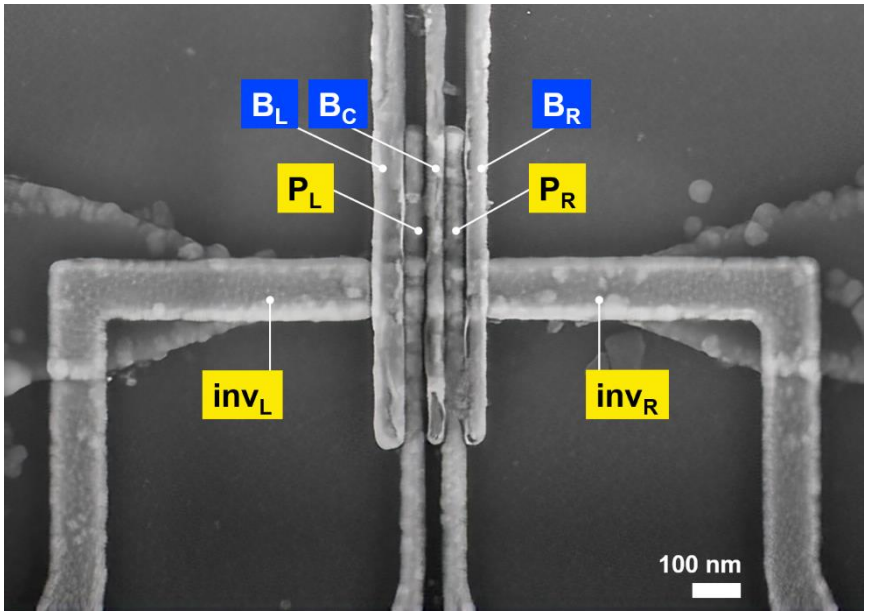
Ti/Pd: second metallization layer

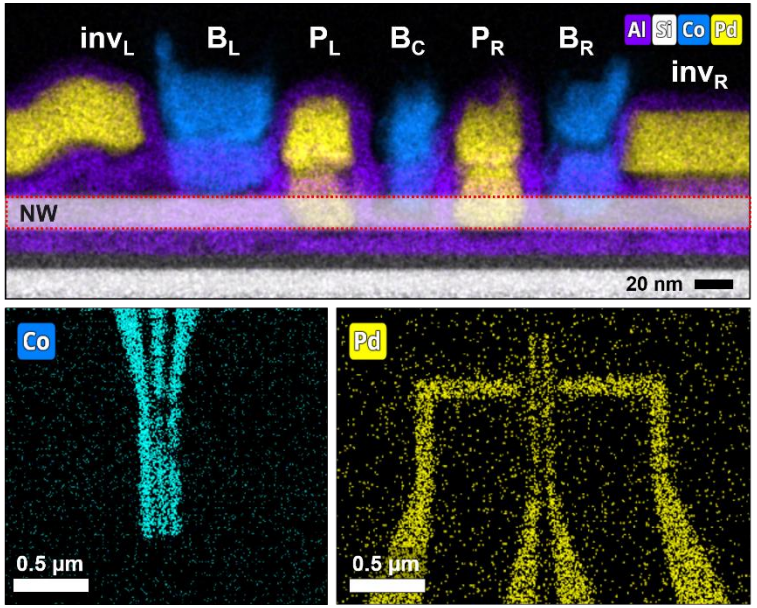


SEM picture of a single dot NW device after patterning the two layers of metal.

Spin Qubit Device

Bersano, Fabio, et al. "Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control." *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 2023.





In a practical spin qubit device, it's typical to require two quantum dots, as this configuration allows for the manipulation and coupling of individual electron spins to perform quantum operations. Additionally, a ferromagnetic component is integrated to provide the necessary magnetic field control for these electrons. This ferromagnetic element generates a localized or slanting magnetic field, which is essential for enabling electron dipole spin resonance (EDSR) and for achieving precise spin manipulation through electric fields.

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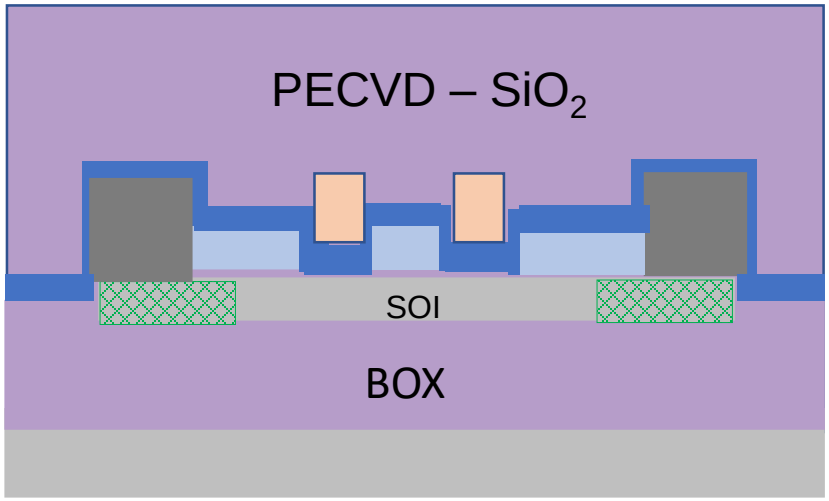
9-10. Encapsulation

Typically, the devices have to be encapsulated by a thick dielectric to be protected towards electrical discharge (EDS) and the external environment.

Options:

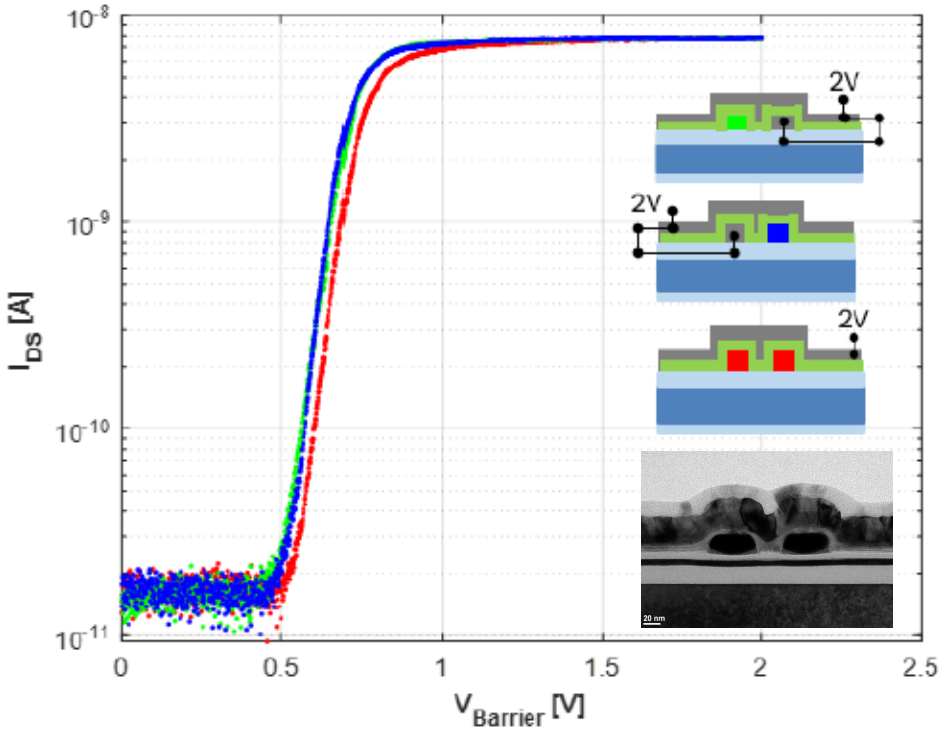
- ALD - conformal but slow, good for thin layers only
- PECVD – fast, good for thick oxide layers (SiO_2)



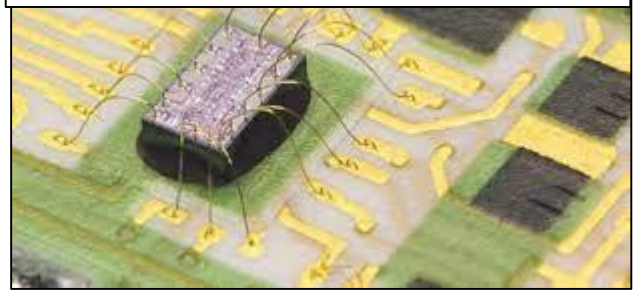
9-10. Encapsulation

An annealing in forming gas (95% N_2 5% H_2) is usually performed right before measurements to lower the density of charge traps that screen the electrical control of the gates.

What's next? Etching of vias, final metallization, and wire bonding.



Bonded device, ready for measurements.



Example of metallic nanogates transcharacteristics after the encapsulation step (i.e., field effect control over the SOI channel)

Conclusions

- The horizon of computing extends the current CMOS-based Data Centers with future **quantum computing in the Cloud**.
- **Semiconducting qubits** offer solutions for innovation and **scalability** to millions of qubits quantum computers. However, they involve complex processing, necessitating many successive steps and advanced metrology methods.
- **Operation at cryogenic temperatures** require particular selection of materials and technological solutions.
- At **CMi facilities @ EPFL**, our PhDs have the chance to explore beyond industrial standards, showcasing groundbreaking **quantum device concepts using nanotechnology processing**.

Interested in fabrication?

Nanolab

The Nanoelectronic Devices Laboratory (NanoLab) is working on research topics in advanced nanoelectronics, with special emphasis on the technology, design and modelling of nanoscale solid-state devices. The group explores new materials, novel fabrication techniques, and novel device concepts for future applications in energy efficient Edge Artificial Intelligence, Internet-of-Things and Quantum Computing.

Student Projects

Master Internship/Thesis Project Topics

Fall 2024/2025

If interested by the any of the topics below, please contact by email the co-supervisor with CC: to Adrian Ionescu