Course21

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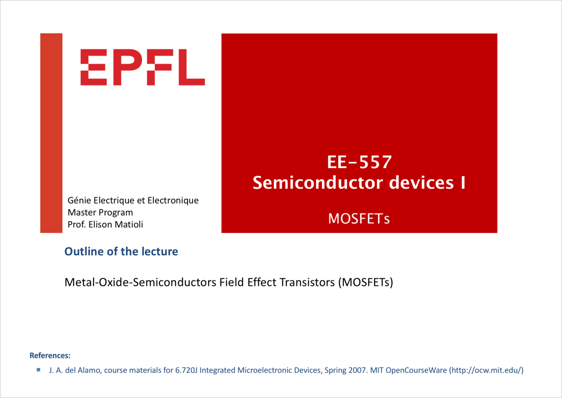
EE557
Course 21...



EE-557
Semiconductor devices I

MOSFETs

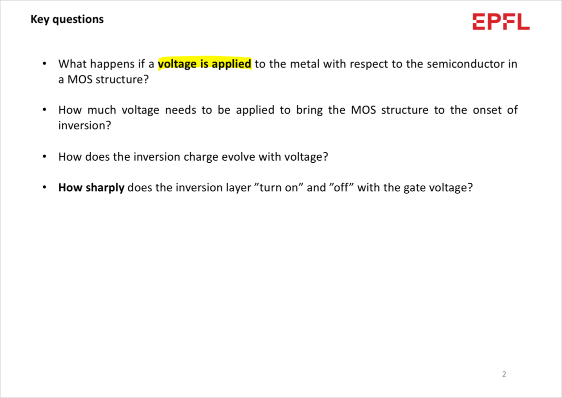
Génie Electrique et Electronique
Master Program
Prof. Elison Matioli

Outline of the lecture

Metal-Oxide-Semiconductors Field Effect Transistors (MOSFETs)

References:

- J. A. del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/)



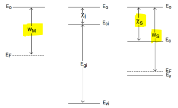
Key questions

- What happens if a **voltage is applied** to the metal with respect to the semiconductor in a MOS structure?
- How much voltage needs to be applied to bring the MOS structure to the onset of inversion?
- How does the inversion charge evolve with voltage?
- **How sharply** does the inversion layer ”turn on” and ”off” with the gate voltage?

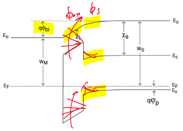
Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Depletion ($W_S > W_M$ in the case of a p-type semiconductor)



a) metal, insulator and semiconductor far apart

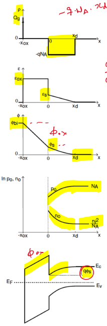


b) metal, insulator and semiconductor in intimate contact

$$q\phi_{bi} = W_S - W_M$$

$-q \cdot N_A \cdot x_d$ [C/cm²]

$Q_g = -Q_s$



C/cm²

$\frac{d\mathcal{E}}{dx} = \frac{\rho(x)}{\varepsilon}$

Integrated semiconductor charge:

$$Q_s \simeq -qN_Ax_d$$

Field at semiconductor surface:

$\varepsilon_{ox} E_{ox} = \varepsilon_s \cdot E_s$

$$\mathcal{E}_s \simeq \frac{qN_Ax_d}{\epsilon_s} = \frac{-Q_s}{\varepsilon_s}$$

Field in insulator:

$n = \frac{n_i^2}{N_A} \cdot \exp\left(\frac{+q\phi_s}{kT}\right)$

$$\mathcal{E}_{ox} \simeq \frac{qN_Ax_d}{\epsilon_{ox}}$$

$\int$ Surface potential:

$$\phi_s \simeq \frac{qN_Ax_d^2}{2\epsilon_s}$$

C/cm²

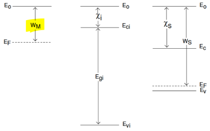
$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon}$$

$$E = \frac{Q_s}{\varepsilon_s}$$

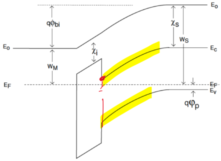
Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Inversion ($W_S >> W_M$ in the case of a p-type semiconductor)



a) metal, insulator and semiconductor far apart

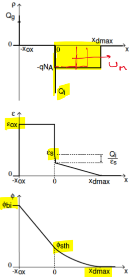


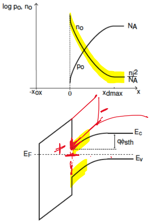
b) metal, insulator and semiconductor in intimate contact

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Inversion





$$Q_s = Q_d + Q_i$$

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Do **sheet-charge approximation**: inversion layer much thinner than any other vertical dimensions of the problem.

$$\phi_s = \frac{q N_A x_d^2}{2\varepsilon} \Rightarrow x_d = \sqrt{\frac{2\varepsilon\phi_s}{q N_A}}$$

Two consequences:

1. ϕ_s depends on Q_d but is independent of Q_i (ϕ does not change while crossing a sheet of charge):

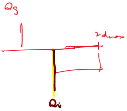
$$Q_d = -qN_Ax_d \simeq -\sqrt{2\epsilon_s qN_A\phi_s}$$

thus: $Q_{d,max} = -\sqrt{2 q \varepsilon_s \cdot N_A \cdot \phi_{sth}}$

2. ϕ_s in inversion rather insensitive to actual value of W_M:

$$\phi_s \simeq \phi_{sth}$$

ϕ_{sth} is *surface potential at threshold*



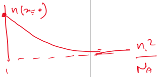
Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Rough estimate of ϕ_{sth}: value that brings surface right at edge of inversion, that is, $n_o(0) = N_A$:

$$n_o(x=0)|_{threshold} = \frac{n_i^2}{N_A}\exp\frac{q\phi_{sth}}{kT} = N_A$$

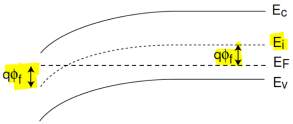
$$n_o(x=0) = \frac{n_i^2}{N_A} \exp \frac{q\phi_s}{kT}$$



Then:

$$\boxed{\phi_{sth} = 2\frac{kT}{q}\ln\frac{N_A}{n_i} \equiv 2\phi_f}$$

ϕ_s

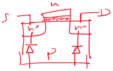


Threshold: when the semiconductor type changes at the surface from p-type to n-type

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Within the **sheet-charge approximation,** electrostatic problem is easy to solve:
In inversion, ϕ_s independent of W_M thus x_d independent of W_M:



$$x_d \simeq x_{dmax} = \sqrt{\frac{2\epsilon_s\phi_{sth}}{qN_A}}$$

$V_{th} > 0$

$V_G = 0 \longrightarrow$ off

Total depletion region charge:

$$Q_d \simeq Q_{dmax} = -qN_Ax_{dmax} = -\sqrt{2\epsilon_s qN_A\phi_{sth}}$$

$$\phi_{bi} = \phi_s + \underbrace{\phi_{ox}}_{\frac{-Q_s}{C_{ox}}}$$

From fundamental electrostatics relation in inversion:

$$\phi_{bi} = \phi_s - \frac{Q_s}{C_{ox}} = \phi_{sth} - \frac{Q_i + Q_{dmax}}{C_{ox}}$$

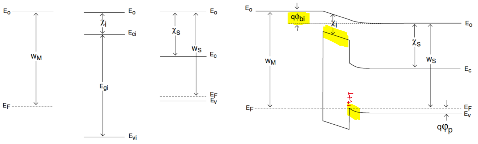
Derive expression for Q_i in inversion:

$$Q_i = -C_{ox}(\phi_{bi} - \phi_{sth}) - Q_{dmax}$$

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Accumulation ($W_S < W_M$)



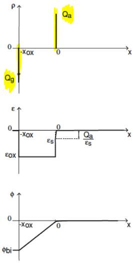
a) metal, insulator and semiconductor far apart

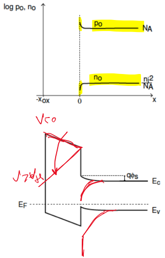
b) metal, insulator and semiconductor in intimate contact

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Accumulation





$$\cancel{Q_s} = Q_a$$

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Sheet-charge approximation again:

$$\phi_s \simeq 0$$

Use fundamental electrostatics equation again:

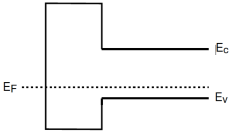
$$Q_a \simeq -C_{ox}\phi_{bi}$$

Metal-Oxide-Semiconductor Structure

Ideal MOS structure under zero bias

Flat-band

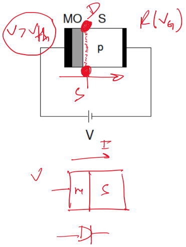
If $\phi_{bi}=0$: $Q_s=0$, $E_s=0$, $E_{ox}=0$, $\phi_s=0$ ⇒ **Perfect charge neutrality everywhere**.

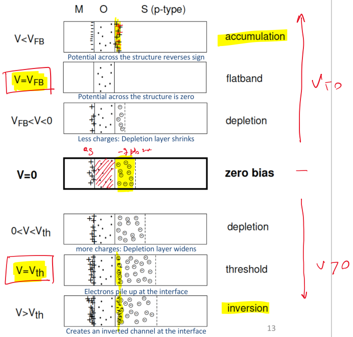


Metal-Oxide-Semiconductor Structure

Ideal MOS structure under bias

Apply voltage V to metal with respect to semiconductor:





$V<V_{FB}$	Potential across the structure reverses sign	accumulation
$V=V_{FB}$	Potential across the structure is zero	flatband
$V_{FB}<V<0$	Less charges: Depletion layer shrinks	depletion
$V=0$		**zero bias**
$0<V<V_{th}$	more charges: Depletion layer widens	depletion
$V=V_{th}$	Electrons pile up at the interface	threshold
$V>V_{th}$	Creates an inverted channel at the interface	inversion

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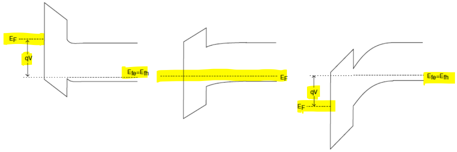
Ideal MOS structure under bias



a) accumulation (V<0)

b) zero bias (depletion)

c) inversion (V>0)

MOS structure can **swing all the way from accumulation to inversion**.

Semiconductor remains in quasi-equilibrium (no carrier flow, no carrier injection)

$$E_{fe} = E_{fh} = E_F$$

Electrostatics identical to zero bias but potential difference across structure changed:

$$\boxed{\phi_{bi} \longrightarrow \phi_{bi} + V}$$

$\phi_{bi} \longrightarrow \phi_{bi} + V$

Ideal MOS structure under bias

Total potential build-up across structure:

$\phi_{bi} = \phi_s + \phi_{ox}$

$$[1] \quad \phi_{bi} + V = \phi_s - \frac{Q_s}{C_{ox}}$$

Several important results:

Flat-band voltage: $\phi_s = 0,\ Q_s = 0$: $\boxed{V_{FB} = -\phi_{bi}}$

Threshold voltage for inversion: $Q_i = 0,\ Q_d = Q_{dmax},\ \phi_s = \phi_{sth}$:

$$[1] \longrightarrow \quad V_{th} = \underbrace{-\phi_{bi}}_{V_{FB}} + \phi_{sth} - \frac{Q_{dmax}}{C_{ox}} = V_{FB} + \phi_{sth} + \underbrace{\gamma\sqrt{\phi_{sth}}}_{\frac{\sqrt{q N_A 2\varepsilon_s}}{C_{ox}}\sqrt{\phi_{sth}}}$$

$\gamma = \frac{\sqrt{q N_A 2 \varepsilon_s}}{C_{ox}}$

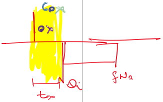
$Q_d = q N_A x_d$

$= \sqrt{2 \varepsilon_s q N_A \phi_{sth}}$

Ideal MOS structure under bias

$$V_{th} = -\phi_{bi} + \phi_{sth} - \frac{Q_{dmax}}{C_{ox}} = V_{FB} + \phi_{sth} + \gamma\sqrt{\phi_{sth}}$$

$Q = CV$

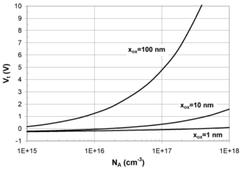


In inversion (V > V$_{th}$): $\boxed{Q_i = -C_{ox}(V - V_{th}) \quad \text{for } V \geq V_{th}}$

Once reached inversion, the **inversion charge increases linearly with the applied voltage in excess of V$_{th}$.**

$Q_i = -C_{ox}(V - V_{th})$

V$_t$ plays key role in MOSFET operation.



Key dependencies:

$N_A \uparrow \rightarrow V_t \uparrow$

$x_{ox} \uparrow \rightarrow V_t \uparrow$

Exercise

Consider an MOS structure made out of a W gate (WM = 4.54 eV), a 4.5 nm SiO2 insulator, and a p-type doped Si substrate with Na = 6 x 10^{17} cm-3.

1.Estimate the electric field in the oxide and the surface potential at zero bias.

$\phi_s (V=0)$

2. Now let's use of a poly-Si gate (W_M= 4.04 eV). Calculate Qs and its extent into the semiconductor for V = -0.5 V.

3. Compute V_T and Qi for V = 2 V

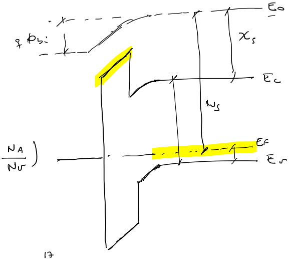
MOS :

W gate : $W_m = 4.54\ eV$

SiO_2 : $t_{ox} = 4.5\ nm$

$N_A = 6 \times 10^{17}\ cm^{-3}$

$$W_s = \underline{\chi_s} + \underline{E_g} - \underbrace{(E_F - E_v)}_{KT \ln\left(\frac{N_A}{N_v}\right)}$$



$$= 4.04 + 1.12 + 0.026 \ln\left(\frac{6 \times 10^{17}}{3.1 \times 10^{19}}\right) = 5.06\ eV$$

$W_m < W_s \Rightarrow$ Depletion

$$\cdot\ \phi_{bi} = \frac{1}{q}(W_s - W_m) = 5.06 - 4.54 = 0.52\ V$$

$$\cdot\ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}\ F/cm}{4.5 \times 10^{-7}\ cm} = 7.7 \times 10^{-7}\ F/cm^2$$

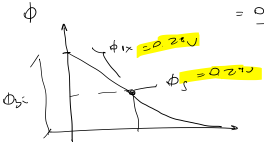
$$\cdot\ \gamma = \frac{\sqrt{2 \cdot \varepsilon_s \cdot q\, N_A}}{C_{ox}} = \frac{\sqrt{2 \cdot 1.04 \times 10^{-12}\ F/cm \times 1.6 \times 10^{-19}\ C \times 6 \times 10^{17}\ cm^{-3}}}{7.7 \times 10^{-7}\ F/cm^2} = 0.58\ V^{1/2}$$

$$x_d = \frac{\varepsilon_s}{C_{ox}}\left(\sqrt{1 + \frac{4\phi_{bi}}{\gamma^2}} - 1\right) = 23\ nm$$

$$E_{ox} = \frac{q N_A \cdot x_d}{\varepsilon_{ox}} = \frac{1.6 \times 10^{-19} \cdot 6 \times 10^{17} \cdot 23 \times 10^{-7}}{3.45 \times 10^{-13}\ F/cm} = 6.4 \times 10^{5}\ V/cm$$

$$\Rightarrow \phi_{ox} = E_{ox} \cdot t_{ox}$$

$$\phi_s = \frac{q \cdot N_A \cdot x_d^2}{2 \varepsilon_s} = \underline{0.24V}$$



$= \underline{0.28V}$

MOS structure under bias

Dynamics of the MOS structure

- MOS structure looks and behaves like capacitor
- C-V characteristics summarize complex behavior of MOS
- **C-V characteristics**: powerful diagnostic tool of wide applicability

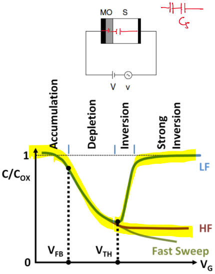
Three key issues to study:

- impact of bias voltage
- impact of frequency of small-signal
- Dynamic behavior under fast changing conditions

MOS structure under bias

Dynamics of the MOS structure

Qualitative discussion first: C_{ox}



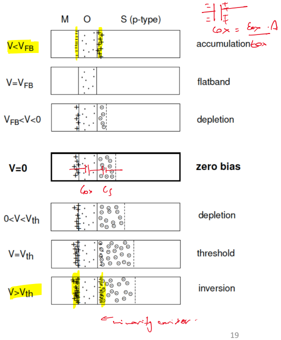


Image from: http://en.citizendium.org/wiki/MOS_capacitor

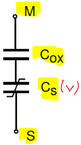
MOS structure under bias

Dynamics of the MOS structure

General definition of capacitance:

$$C = \frac{dQ_g}{dV} = -\frac{dQ_s}{dV}$$

After some algebra:



$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s}}$$

where C_s is defined as:

$$C_s = -\frac{dQ_s}{d\phi_s}$$

Note: $C_s > 0$.

Qs is defined as the charge in the depletion region:

$Q_s \simeq -qN_A x_d$ where $x_d \simeq \frac{\epsilon_s}{C_{ox}}(\sqrt{1+\frac{4\phi_{bi}}{\gamma^2}}-1)$ $\gamma = \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_A}$

MOS structure under bias

Quasi-static C-V characteristics

If frequency of AC voltage signal is low enough:
quasi-static conditions: use Poisson-Boltzmann formulation:

Accumulation

$$\boxed{C_s \simeq \frac{q}{2kT}C_{ox}(V_{FB}-V)}$$

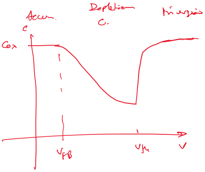
For **|V| sufficiently larger than $|V_{FB}|$**, **C_s becomes large**, and independent of V :

$$\boxed{C \simeq C_{ox}}$$

MOS structure under bias

Quasi-static C-V characteristics

Depletion



Semiconductor capacitance $\boxed{C_s \simeq \frac{C_{ox}}{\sqrt{1+4\frac{V-V_{FB}}{\gamma^2}}-1}}$

Total capacitance $\boxed{C \simeq \frac{C_{ox}}{\sqrt{1+4\frac{V-V_{FB}}{\gamma^2}}}}$

Square-root dependence on V.

MOS structure under bias

Quasi-static C-V characteristics

Q = C. V

Inversion

$$C_s \simeq \frac{q}{2kT} C_{ox} (V - V_{th})$$

$Q_i = C_{ox}(V - V_{th})$

For V sufficiently larger than V_{th}, C_s is large and:

$$\boxed{C \simeq C_{ox}}$$

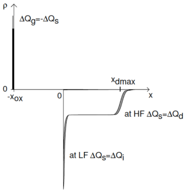
Independent of V

MOS structure under bias

Quasi-static C-V characteristics

For **high-frequency AC signals**, inversion layer can't keep up with the frequency: since it is formed by minority carriers. So the time constants are in the order of **µs-ms**

C-V characteristics modified in inversion.
Evolution of ΔQ in inversion for LF and HF:


ρ
$\Delta Q_g = -\Delta Q_S$
0
$-x_{ox}$
0
x_{dmax}
x
at HF $\Delta Q_S = \Delta Q_d$
at LF $\Delta Q_S = \Delta Q_i$

At low-frequency:

$$\Delta Q_s \simeq \Delta Q_i$$

At high-frequency:

$$\Delta Q_s \simeq \Delta Q_d$$

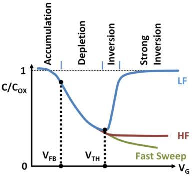
Since $x_d \sim x_{dmax}$,

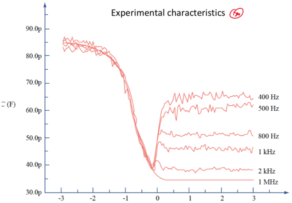
$$C_{s,HF} \simeq C_{s,dep}(V_{th}) \simeq \frac{\gamma C_{ox}}{2\sqrt{2\phi_f}} \equiv C_{sth}$$

MOS structure under bias

Quasi-static C-V characteristics

C-V characteristics:





Key conclusions

In inversion, $\phi_s \sim \phi_{sth}$, roughly independent of metal.

In accumulation, $\phi_s \sim 0$, roughly independent of metal.

At Si/SiO_2 interface, semiconductor can **swing all the way from accumulation to inversion** by the application of a voltage.

To first order, surface potential in inversion and accumulation does not change with V.

Flatband voltage: voltage that produces flatband:

$$V_{FB} = -\phi_{bi}$$

Threshold voltage: voltage beyond which an inversion layer of electrons is formed:

$$V_{th} = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_f}$$

Beyond threshold, absolute inversion **charge increases linearly with voltage**:

$$Q_i = -C_{ox}(V - V_{th})$$

Key conclusions

In **sub-threshold regime**, inversion charge drops exponentially with V below threshold:

$$Q_e \propto \exp\frac{q\phi_s}{kT} \propto \exp\frac{q(V - V_{th})}{nkT}$$

Inverse sub-threshold slope:

$$S = n\frac{kT}{q}\ln 10 \geq 60\ mV/dec \ \text{ at 300 K}$$

Typical inverse sub-threshold slope of well designed MOSFETs at300K: S ~80−100 mV/dec.

MOS capacitance: series of oxide capacitance and semiconductor capacitance:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s}$$

For low-frequency excitation: $C(acc) \simeq C(inv) \simeq C_{ox}$