EE-523 ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN TP-2025

PRACTICAL EXERCISE SESSION No. 1

Note: For students connecting virtually, the details of the Zoom Meeting for this TP session are given below

Topic: Advanced Analog IC Design Zoom Meeting

Time: Feb 28, 2025 02:00 PM Amsterdam, Berlin, Rome, Stockholm, Vienna

Join Zoom Meeting:

https://epfl.zoom.us/j/66887254608?pwd=MBLOAjyTb7PaR02tNUeDaHDb1q5WID.1

Meeting ID: 668 8725 4608

Passcode: 191600

Objectives of this Practical Exercise Session

1. Connect to the helvetios cluster, run Cadence Virtuoso, and familiarize the Process Design Kit (PDK) – UMC 180nm.

2. Simulate a differential pair with the given set of specifications, and analyze the following:

    a. DC operating point using the DC Analysis
    b. Frequency Response using the AC Analysis
    c. Visual sinusoid check using the Transient Analysis

    For this part, you will be provided with the circuit diagram and transistor sizes. The goal is to familiarize the Cadence Virtuoso tool and different analyses (DC, AC, and Transient), and **not to arrive** at the sizing on your own. The sizing will be covered during a later lecture/TP session.

TIP OF THE DAY: Save your work frequently

Accessing the Helvetios Cluster

Connecting to a VM

We use Ubuntu virtual machines (VM) to connect to the servers that host the EDA tools. You can use a computer room or use your own computer to access a VM.

Working in computer rooms

The computer rooms **BC 07-08** (that is where we will be for the TP sessions), CO 260, and MXF 014 are equipped with Dell thin clients providing access to virtual machines (VM). Each thin client has a display, a keyboard, a mouse, and a small Wyse network box located on the rear side of the display. You can use any seat in the room and **login with your GASPAR account**. Do not store personal files in the Ubuntu VM.

To use a Dell thin client:

1. If required, turn the display on.
2. If the client is down, start it by pressing the start button (on the left side of the Wyse box). Wait until you get the start button blue-lighted.
3. At the appearance of the login window, **enter your GASPAR username and password.**
4. After a successful login, you see a list of available virtual machines on the left of the screen. Select the Linux virtual machine **STI-EDA-LABS-RTX**.

Working with your own computer

The **STI-EDA-LABS-RTX** virtual machine can be used from a personal computer as follows (note that if you work from home, it is recommended not to use the EPFL VPN):

Using a web browser: Login to **vdi.epfl.ch** using your GASPAR credentials.

1. Once the Ubuntu desktop is displayed (it may take some time), change the keyboard layout from French to US if required.
2. Open a terminal window (Ctrl-Alt-T or right-click in the desktop area and select Open in Terminal).
3. From the VM terminal window, connect to the helvetios cluster with your GASPAR credentials.

```
>> ssh -X GASPARusername@helvetios.hpc.epfl.ch
```

Please note that >> denotes the Ubuntu terminal prompt, and you should not type it.

Do not forget the -X (capital X) option, otherwise, the display won't be redirected properly to the local screen.

Now, we need to setup the EDA environment for our lab. For this, run the following script from your home folder (you are already here).

```
>> /work/fvlsi/run_edadk
```

You need to run this setup script every time you connect to the helvetios server.

Do not confuse the terminal windows running locally on the Ubuntu VM and the terminal running on the remote Linux server. EDA tools are *not* available on the Ubuntu VM.

When you are done working, quit running tools, log out from the helvetios server (type *exit* in the terminal), and then disconnect from the Ubuntu VM. There are several ways to quit the Ubuntu VM:

- In the top **Options** menu, select **Disconnect** and **Log Off** (selecting Disconnect only disconnects the VM, but keeps the session active).
- In the top right menu, select your name and then select **Log Out**.

Running Cadence Virtuoso

Setting up the workspace

Once you are connected to the helvetios server and have run the edadk setup script, run the following commands in your terminal:

```
>>cd
>>gtar -xvf /education/classes/2024-2025/EE523/EE523_2025.tar.gz
```

This will create a directory named EE523_2025 which contains subdirectories for various tools. **We will always work in the subdirectory for Cadence Virtuoso (CDS_VISO).**

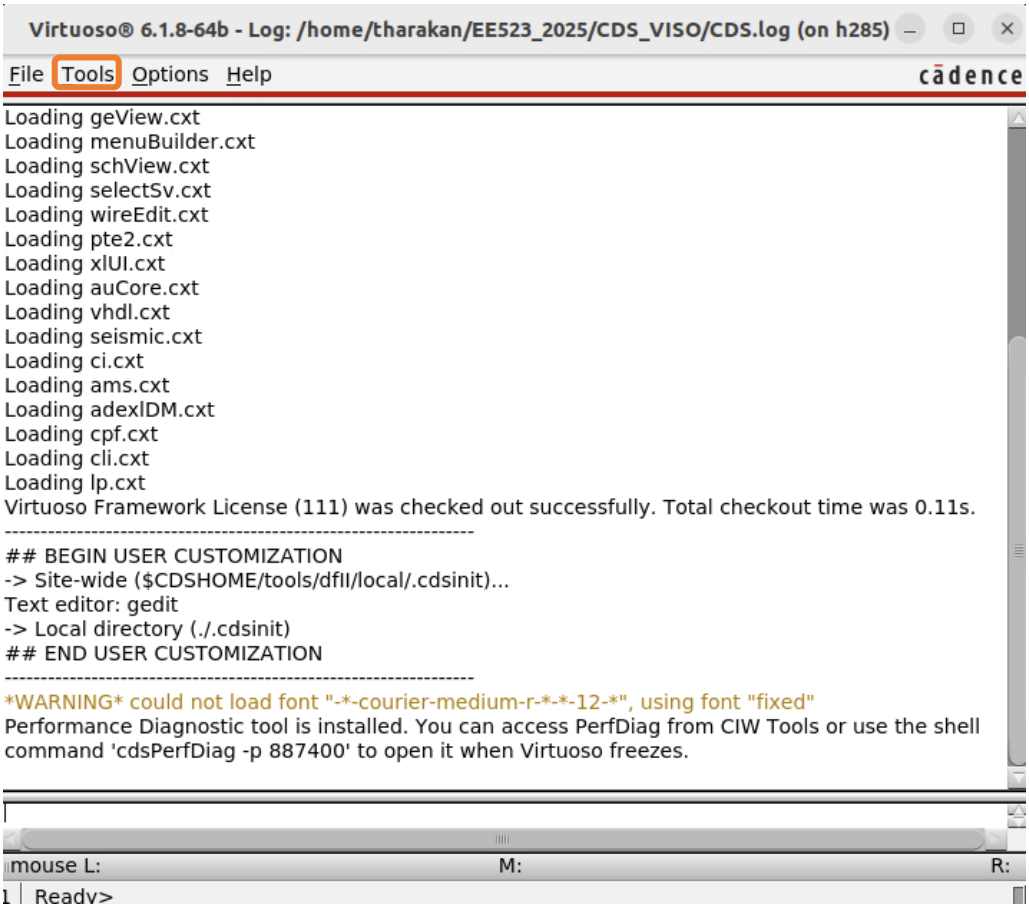
<u>You will have to do this only once.</u> You will use this workspace for all exercise sessions.

Starting Cadence Virtuoso

Go to your EE523_2025/CDS_VISO directory and run the virtuoso command followed by an ampersand.

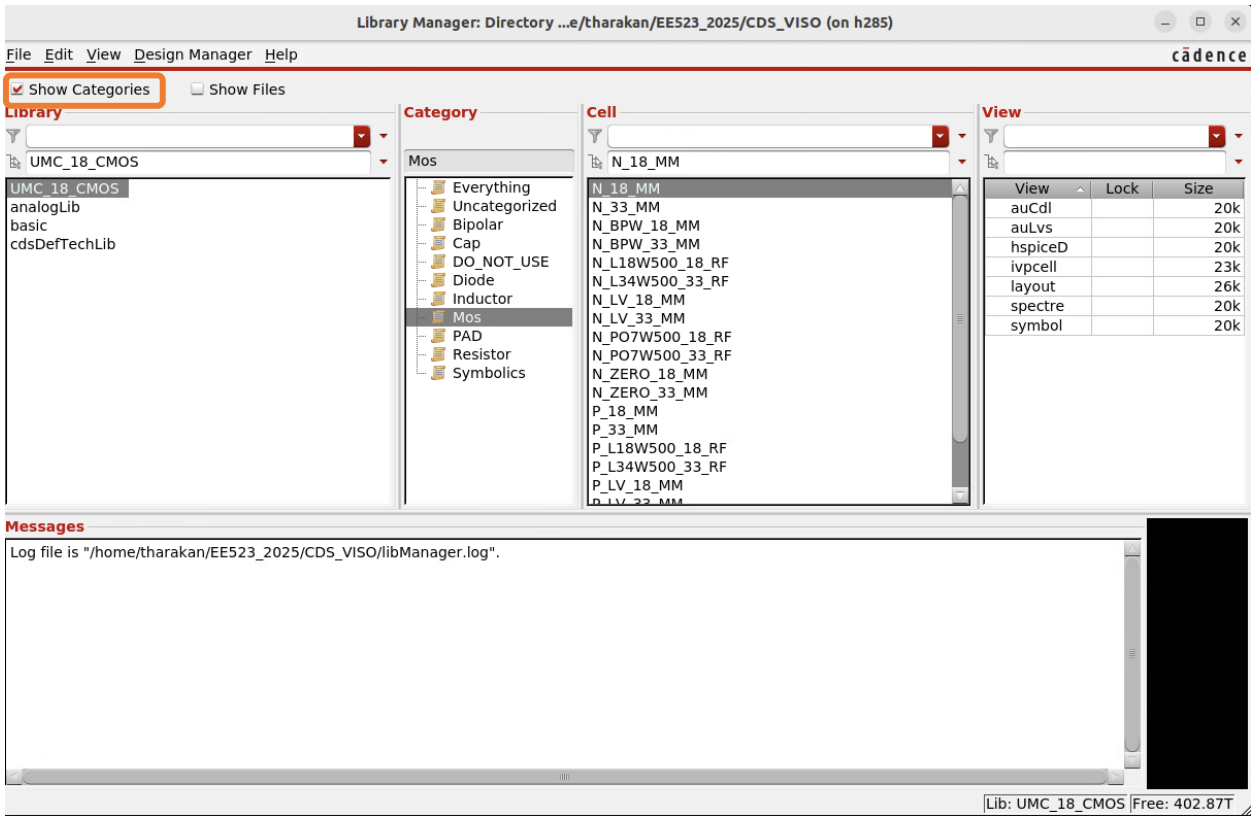
```
>> cd
>> cd EE523_2025/CDS_VISO
>> virtuoso &
```

You will see the main command window open. This window is called CIW – Command Interpreter Window. This is where you can access various tools and settings within the Virtuoso Suite, and where you can exit Virtuoso.



The Library Manager

In the CIW window, click **Tools>Library Manager**. The library manager is where you will find all the technology libraries and where you will create your own custom-design libraries.

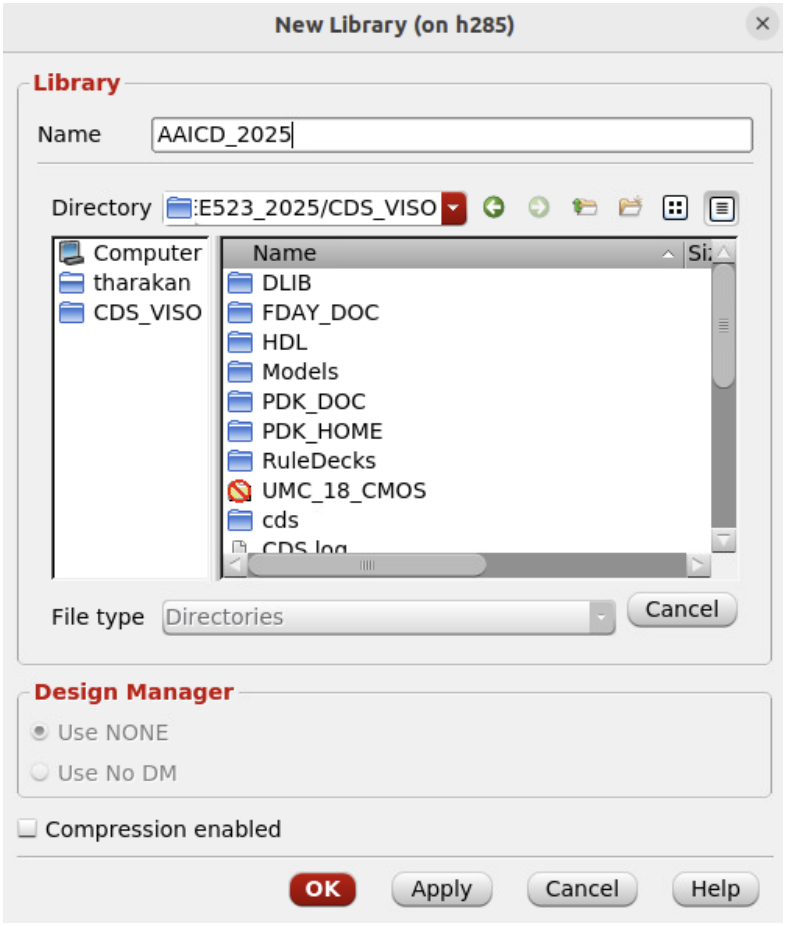


In your library manager, click on the **"Show categories"** button at the top of the window. Find the **"UMC_18_CMOS"** library and observe its contents. You will see circuit elements such as transistors (Mos and Bipolar), capacitors (Cap), resistors (Resistor), and so on. These are created and characterized by the foundry (UMC), so they are ready to be simulated and manufactured.

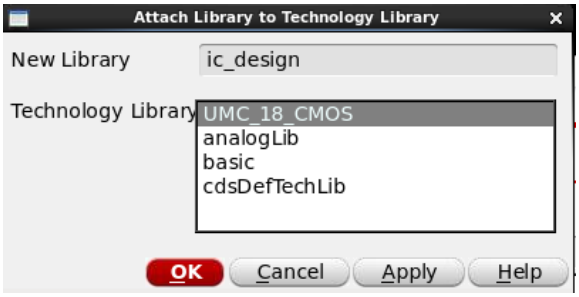
Find the **"analogLib"** library and observe its contents. You will see generic passive components and dependent/independent sources. These are created by Cadence to help your simulations. These cannot be manufactured.

You need a dedicated library to store your own work. This library will have a collection of custom circuit blocks called cell views. Click **File>New>Library**. Give a meaningful name to your library. We suggest "AAICD_2025". Click OK.

Do not forget to choose the "Attach to an existing technology library option" and select UMC_18_CMOS!


New Library (on h285)
Library
Name
AAICD_2025
Directory
:E523_2025/CDS_VISO
Computer
tharakan
CDS_VISO
Name
DLIB
FDAY_DOC
HDL
Models
PDK_DOC
PDK_HOME
RuleDecks
UMC_18_CMOS
cds
File type
Directories
Cancel
Design Manager
Use NONE
Use No DM
Compression enabled
OK
Apply
Cancel
Help

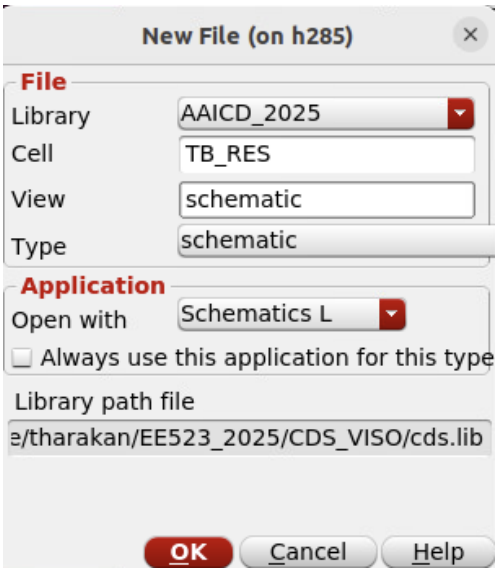

Technology File for New Library
Technology File for library "ic_design"
You can
Compile an ASCII technology file
Reference existing technology libraries
Attach to an existing technology library
Do not need process information
OK
Cancel
Help


Attach Library to Technology Library
New Library
ic_design
Technology Library
UMC_18_CMOS
analogLib
basic
cdsDefTechLib
OK
Cancel
Apply
Help

1. Warm-up example: a resistive voltage divider test bench

Creating a schematic

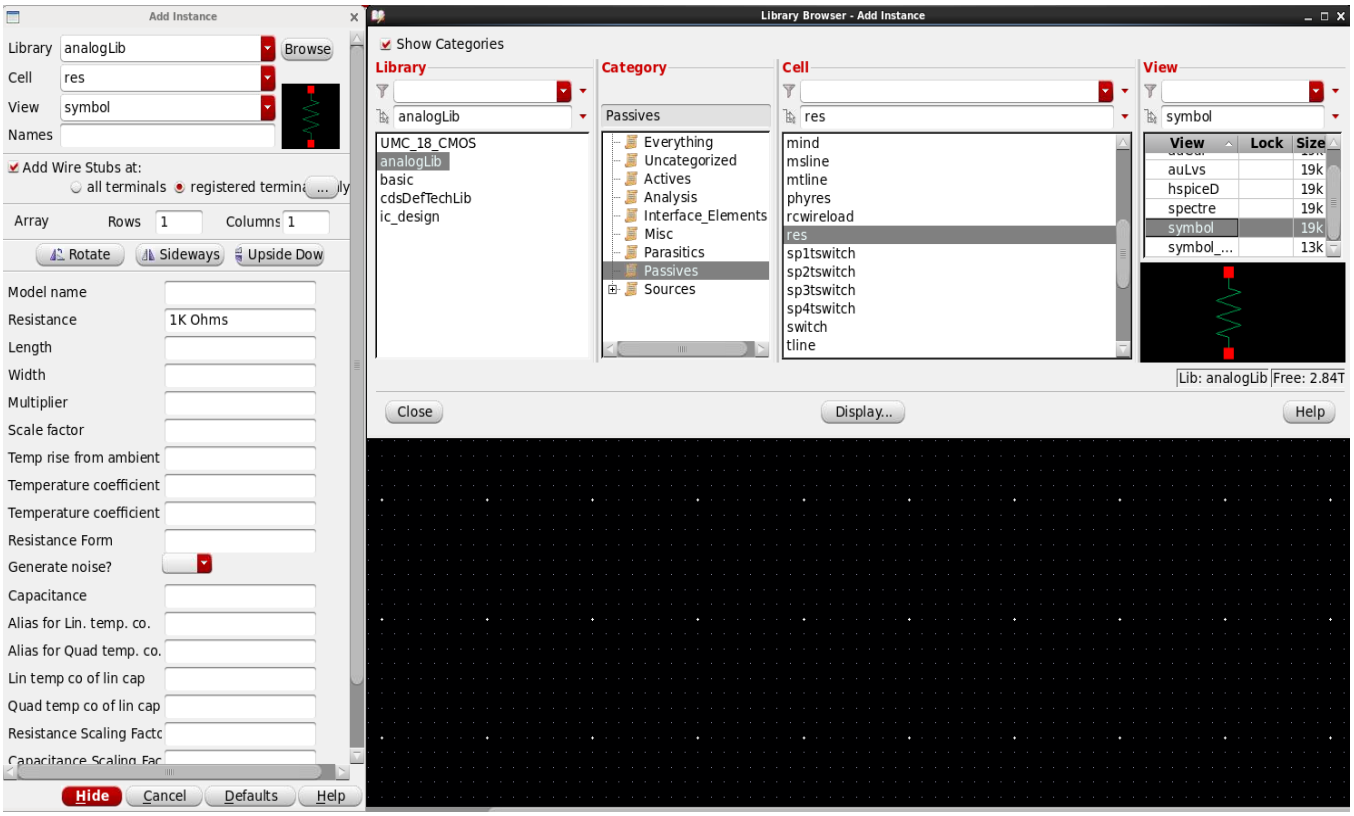
In your library manager, select your new library and click **File>New>Cellview**. Select **“schematic”** as the type of your cellview. Name your schematic as “TB_RES”. Click OK.



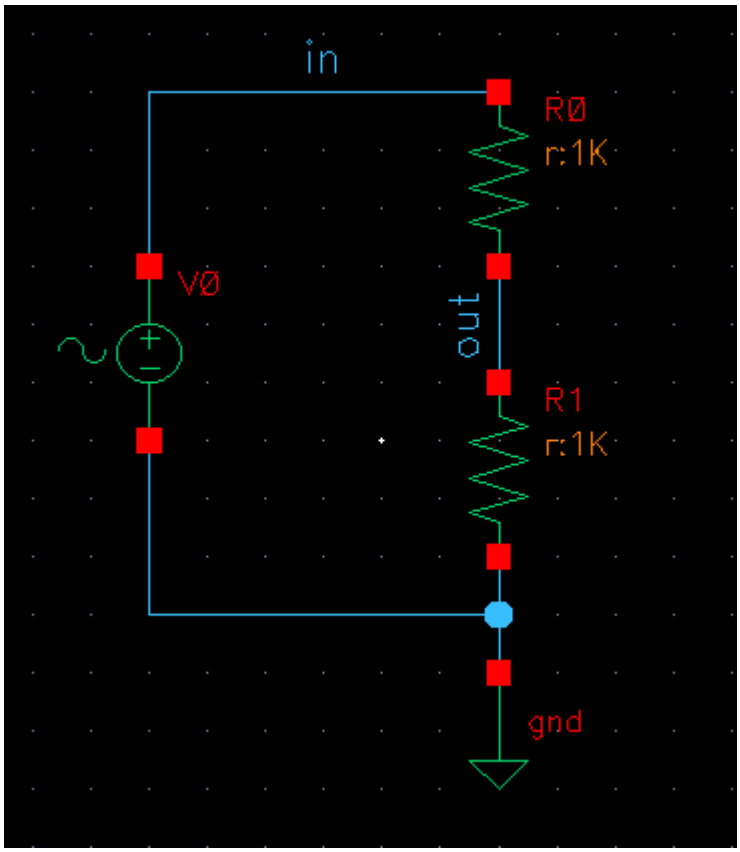
You will see an empty black canvas. Go to **Options>Editor** and change the “**Add instance browser type”** setting to **“library”**, then click OK.

- Return to your canvas and press the key “**i**” on your keyboard, which will open the **“Add Instance”** dialogue.

Click browse, select the library analogLib, and select “res”.



Place the resistor on your canvas. Then browse to analogLib and place the independent voltage sources and grounds (vsin and gnd) as shown in the schematic below. (Note: “**u**” key is for undo)



We use wires and wire labels to create connections between component pins.

- Press “**w**” on your window to bring the wiring tool. Connect all components as shown in the schematic.

The default name for each wire is “netXX”, which is not descriptive at all. It is good practice to give meaningful names to your wires.

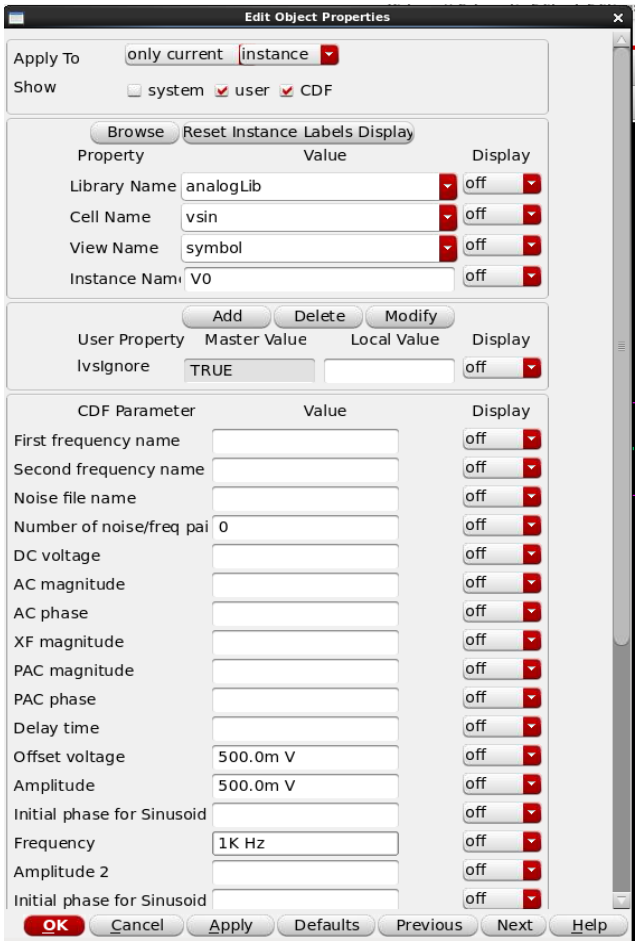
- Press “**l (this is lowercase L)**” on your keyboard to bring the wire label dialogue. Name the “in” and “out” as shown in the figure. All ground nets connected to a gnd instance are named **globally as “gnd!” by default**, so you don’t need to put a label on them.
- Once you made all the connections and labeling, select the voltage source (vsin) and press “**q**” which will bring the **“Properties”** dialogue.

Set the values so that the applied waveform has 0.5V mean, 0.5V amplitude, and 1 kHz frequency.

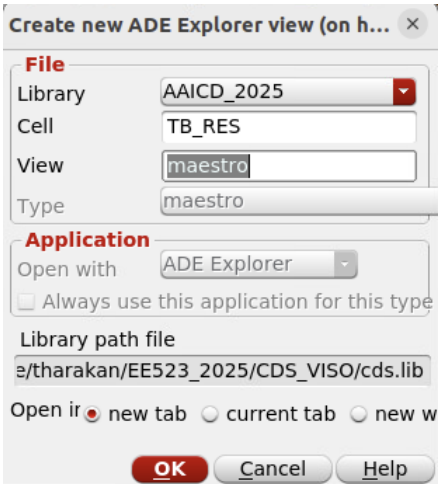
We are now ready to simulate this schematic.

- Press “**Shift+x**” to check and save your schematic. This will check the schematic for any floating wires, open terminals etc. Note that the undo history is lost after you save.

- If there are any warnings or errors, you can view them by pressing “**g**”.

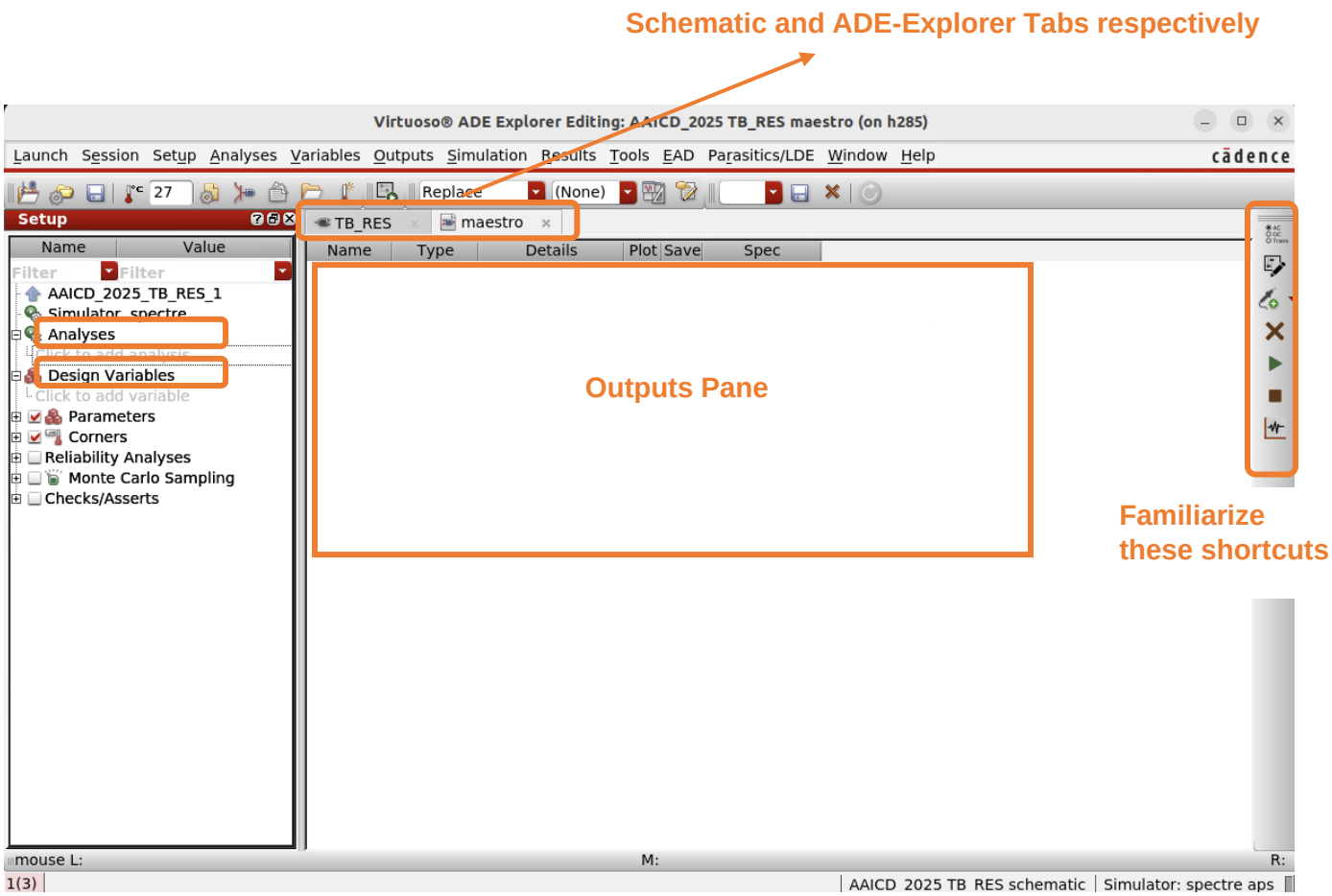


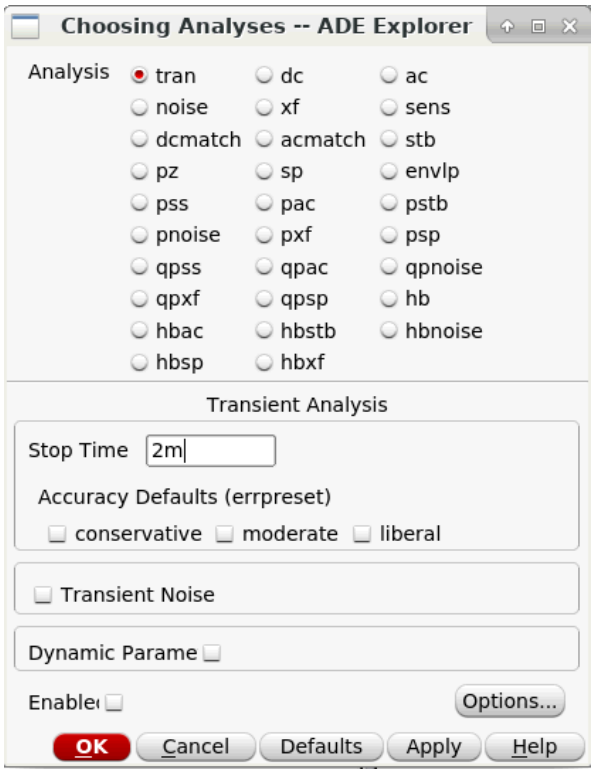
Transient simulation



On your schematic window, click **Launch>ADE Explorer**. In the next prompt, select **Create New View**. Keep the View as **maestro**, select **Open in new tab**, and press OK.

ADE stands for “Analog Design Environment”. One could also use ADE-L, ADE-XL, but of late, Cadence is asking its users to migrate to ADE Explorer/ADE Assembler (the support for ADE-L and ADE-XL might end in the near future!). For our simulations, ADE Explorer is sufficient. ADE Assembler can be used when running multiple tests on a design.

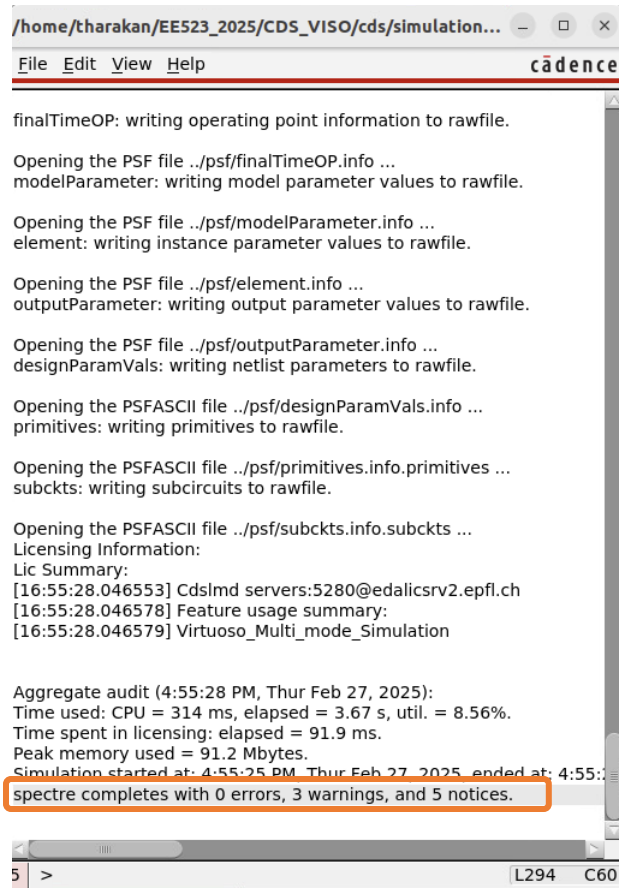




In the above window, familiarize the **Analyses**, **Design Variables**, and **Outputs Pane**.

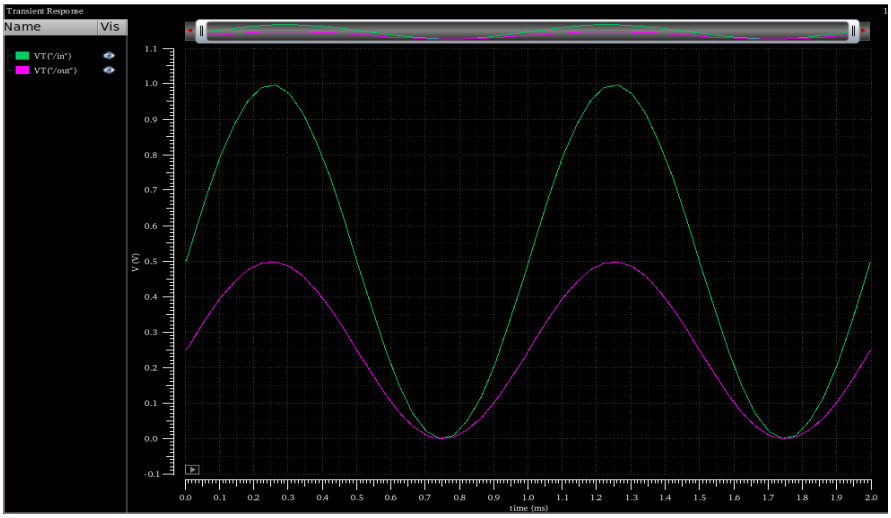
Now to start off our simulations, we first need to add an Analysis type. For this click on **Click to Add Analysis**. It should draw up a window like the one shown below. Here, you will see many analyses types, but for this exercise, we will only perform **"tran"** (transient) analysis. Set a stop time that will allow you to see two periods of the sine waveform. Click **OK**.

Now, click on the **green run play button (** **)** in the shortcuts to run the simulation. Once you run the simulation, an output log (spectre.out) will pop up on your screen. Once the simulation is over, check the bottom of the output log to ensure that there are no errors. Warnings and notices are okay, but feel free to review them.



Displaying transient results

Click **Results>Direct Plot>Transient Signal**. Click on “in” and “out” nets in your schematic. Hit **“Esc”**. This will show the selected net voltages varying over time. When running in ADE-Explorer for the first time, you may have to undock your Viva waveform window (follow the instructions on the prompt).

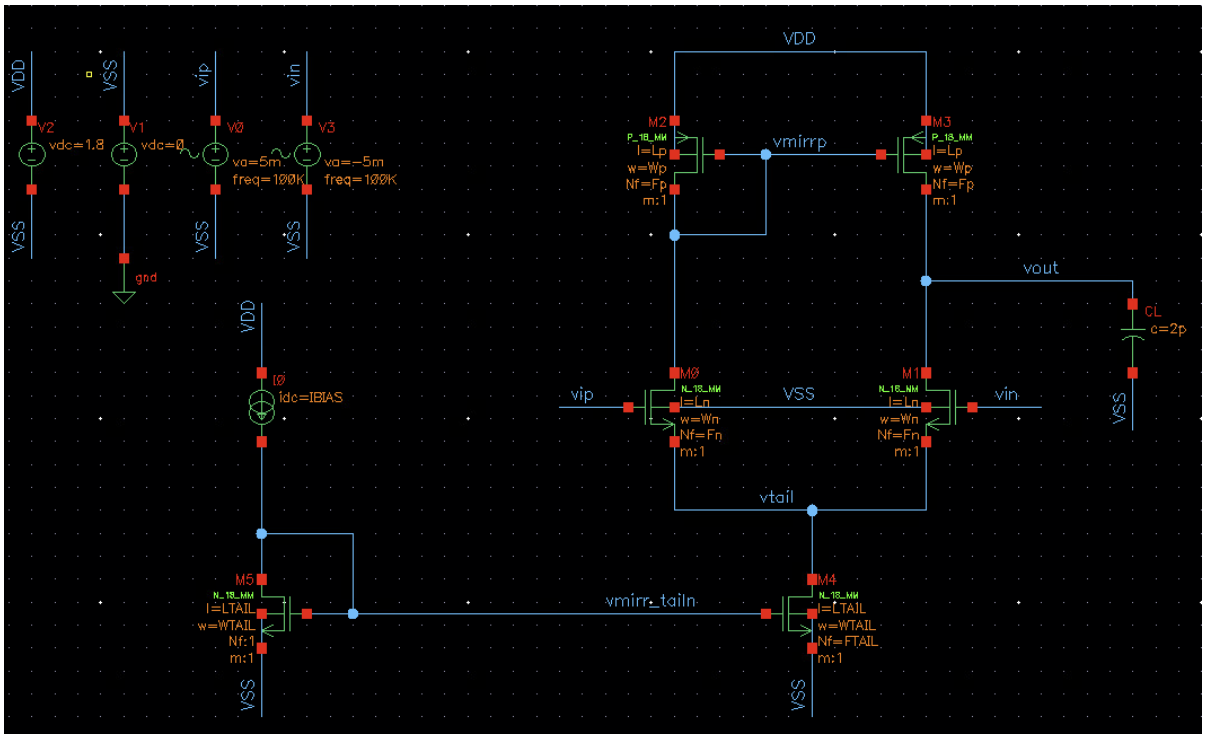


2. Simulating a Five-Pack Operational Transconductance Amplifier

Design Specifications

Differential Input to Single-Ended Output Amplifier (often called the Five-Pack OTA [1])

- DC Gain (A_V) > 30dB = 32V/V
- Unity Gain Bandwidth (UGB) > 20MHz
- Output Load Capacitance (C_L)= 2pF
- $V_{OUT, DC} \approx 1V$
- $V_{IN, DC} = 1V$
- $V_{TAIL, DC} \approx 0.4V$



For the circuit, we know that the voltage gain $A_V = g_{mn}.(r_{on}||r_{op})$

To simplify the above gain expression, we make a reasonable assumption, $r_{on} = r_{op} = r_o$

Therefore, after rounding up to a multiple of 10,

$$g_{mn}.r_o > 70 \quad \text{.... (1)}$$

Unity Gain Bandwidth (UGB, for a linear first order system) = Gain * Bandwidth = g_{mn}/C_L

$$g_{mn} > 2\pi.UGB.C_L$$

$$g_{mn} > 251.2\mu S \quad \text{.... (2)}$$

[1] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Second Edition, Chapter 5.3

From the output DC voltage, we note that,

$$V_{OUT,DC} = V_{DD} - V_{DS3}$$

We note that for the above circuit $V_{DS3} \approx V_{DS2} = V_{GS2}$

$$V_{GS2} = 0.8V \quad \dots (3)$$

From the input DC voltage, we note that,

$$V_{IN,DC} = V_{TAIL,DC} + V_{GS0}$$

$$V_{GS0} = 0.6V \quad \dots (4)$$

Work out the sizes for each transistor, and the tail current by writing out the square-law equations or if you are familiar with any of the design methodologies like g_m/I_D or Inversion Coefficient (IC), please feel free to use them.

For hand calculations, $\mu_n C_{ox}$ = 278µA/V², $V_{TH,N}$ = 0.4V, $\mu_p C_{ox}$ = 61µA/V², $|V_{TH,P}|$ = 0.54V

For your convenience and in the interest of time, these parameters (approximate values) are provided below:

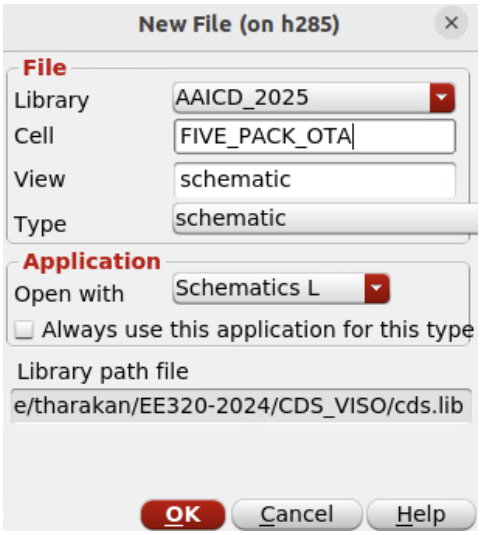
I_{TAIL}	L_{TAIL}	W_{TAIL}	F_{TAIL}	L_n	W_n	F_n	L_p	W_p	F_p
40µ	720n	1µ	3	720n	1µ	6	540n	1µ	2

Here I_X denotes the current, L_X the channel length, W_X the width, and F_X the number of fingers.

Now we will familiarize the following analyses:

a. DC operating point using the DC Analysis
b. Frequency Response using the AC Analysis
c. Visual sinusoid check using the Transient Analysis

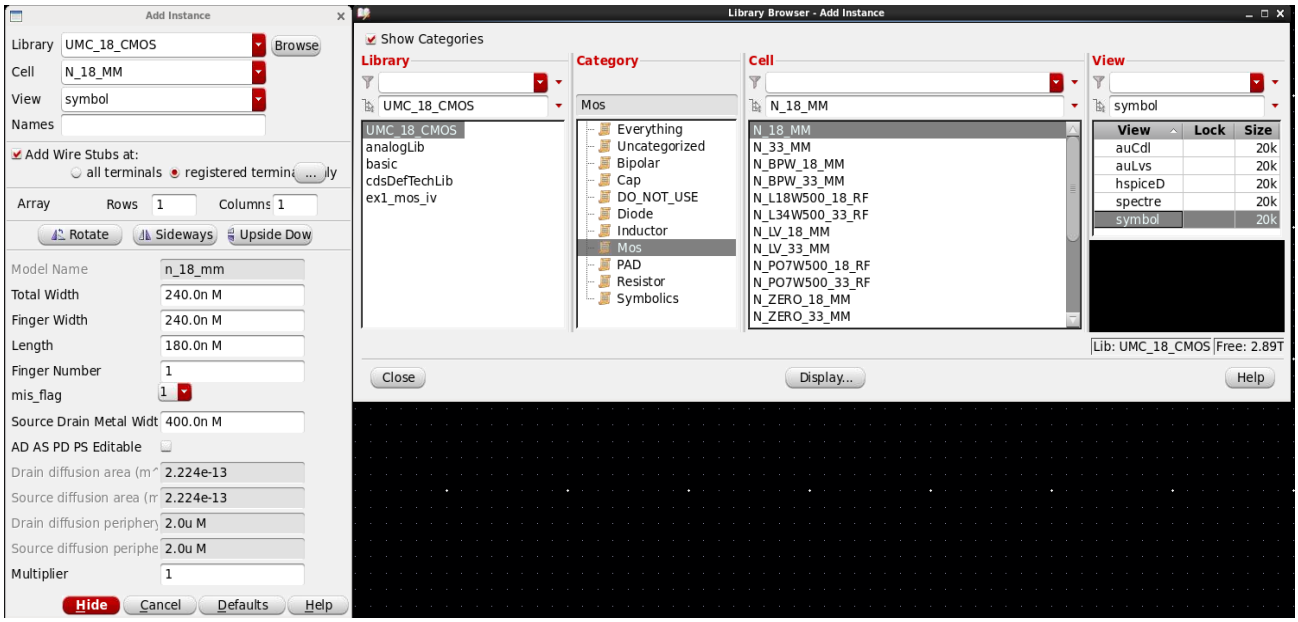
Creating the schematic



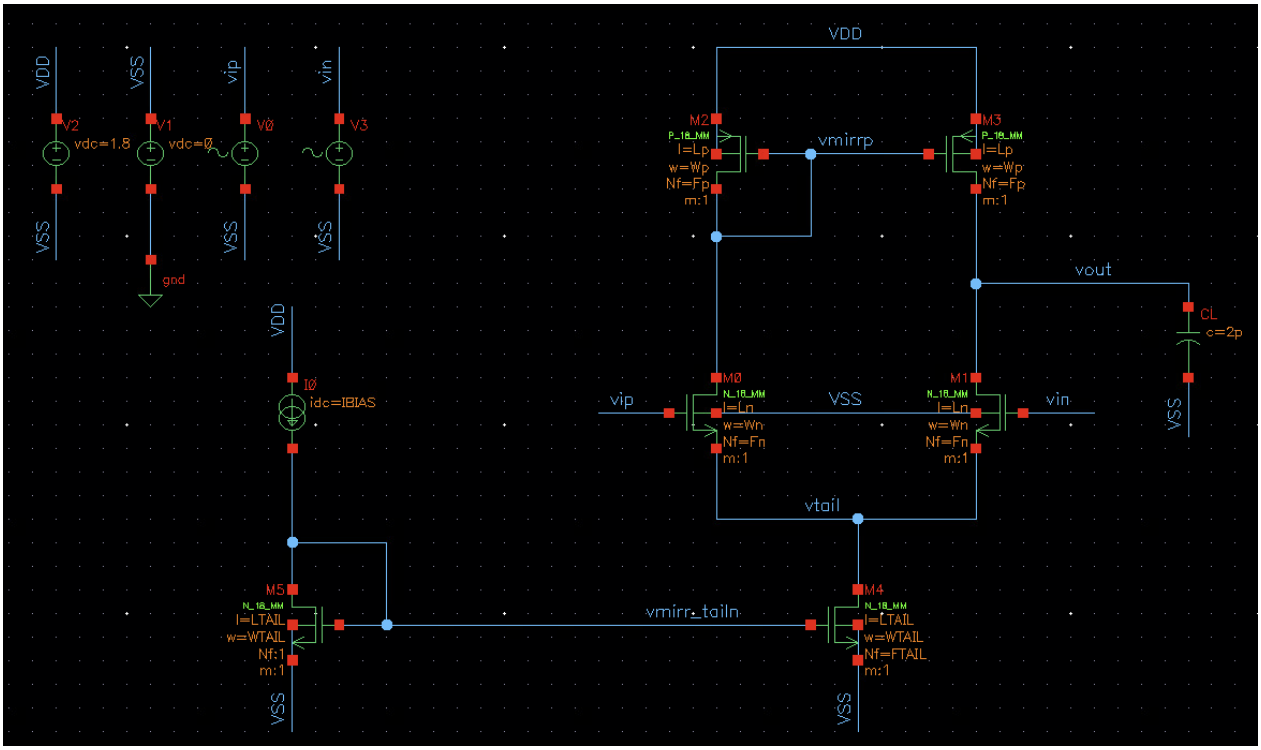
In your library manager, select your new library and click **File>New>Cellview**. Select **"schematic"** as the type of your cellview. Give a meaningful name to your schematic. We suggest "FIVE_PACK_OTA". Click OK.

- Press the key “**i**” on your keyboard, which will open the **“Add Instance”** dialogue.

Click browse, select the library UMC_18_CMOS and select **“N_18_MM”.** (You will notice different flavors of transistors. For our transistor “N_18_MM”, “N” denotes NMOS. “18” denotes that the transistor can withstand a maximum of 1.8 V on its terminals. “MM” means that the transistor is to be used in low frequency (mixed mode digital and analog circuits). “RF” transistors are characterized for high frequencies.)

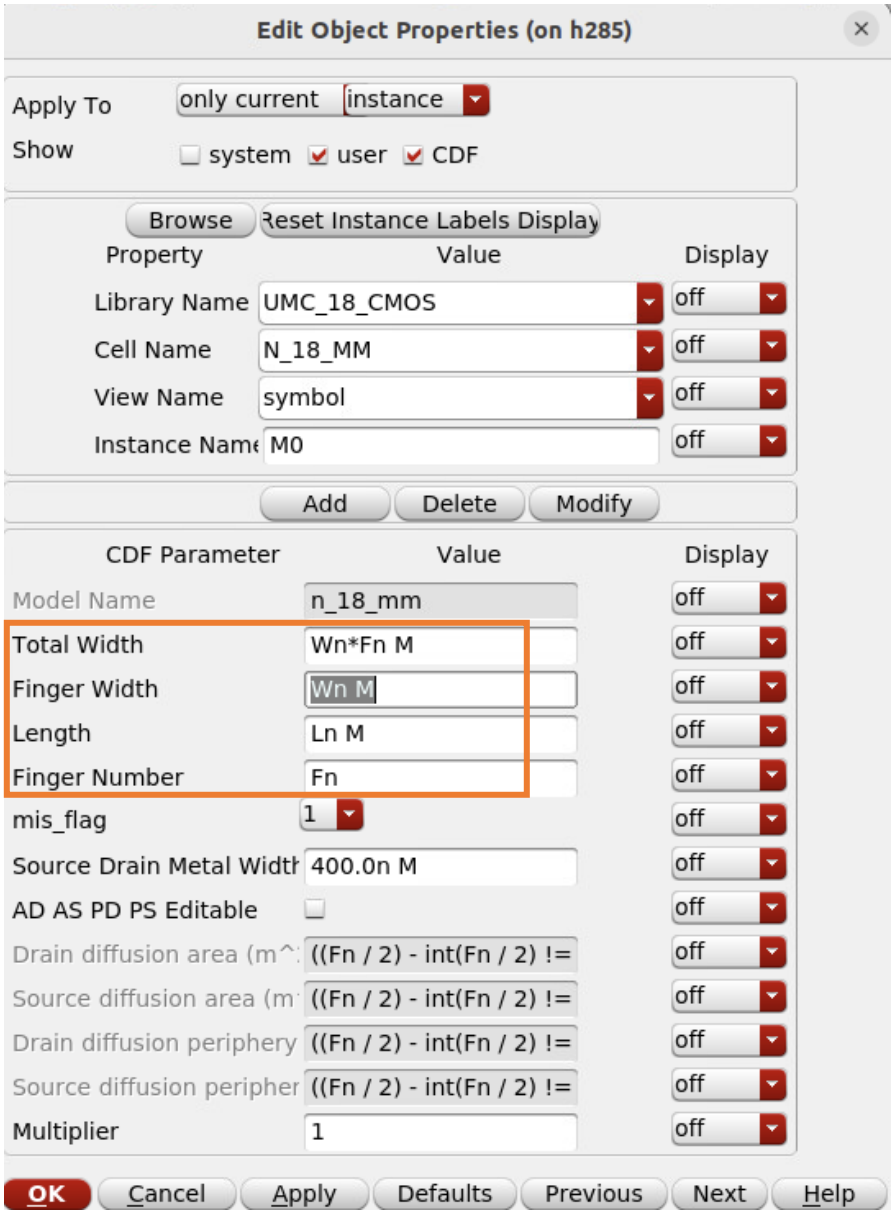


Place the transistor on your canvas. Similarly, use “P_18_MM” for the PMOS transistors. Then browse to analogLib and place the independent voltage sources and grounds (vdc, vsin, and gnd) as shown in the schematic below. Again, press l (it is lowercase L) to create labels for wires as in the snippet below.



- Once you made all the connections and labeling, select a transistor and press “**q**” which will bring the **“Properties”** dialogue.

You can change the instance name if required to match the schematic shown above. Here you can see the parameters that you can control as the designer, which are mainly **“Finger Width”**, **“Length”, and ”Finger Number”.** You can enter real numbers like 2µ or 180n, or you can set them as custom parameters like **“Wn”**, **“Ln”, “Fn”, etc**. These parameters can be changed in simulation without having to go back to the schematic each time during an iteration.



For the vip and vin sine wave sources (vsin from analogLib), setup the form as shown below. On the left is the source for vip and on the right is the source for vin (Notice the sign for AC magnitude and Amplitude).

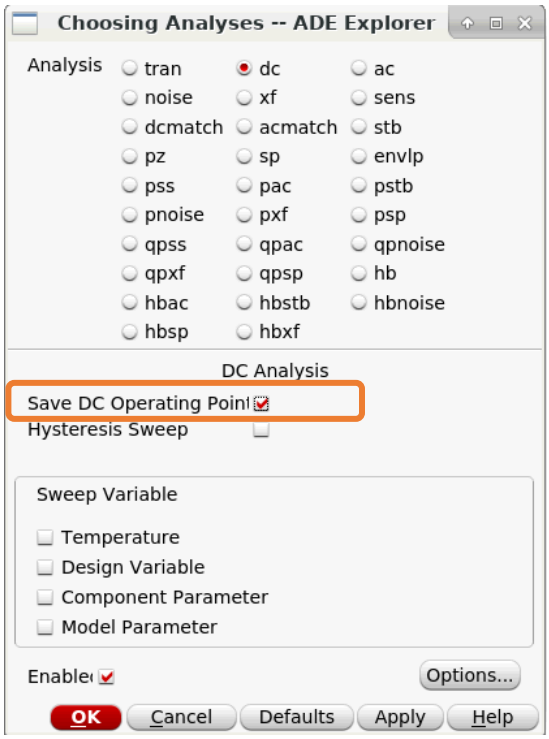
We are now ready to simulate this schematic.

- Press "**Shift+x**" to check and save your schematic.

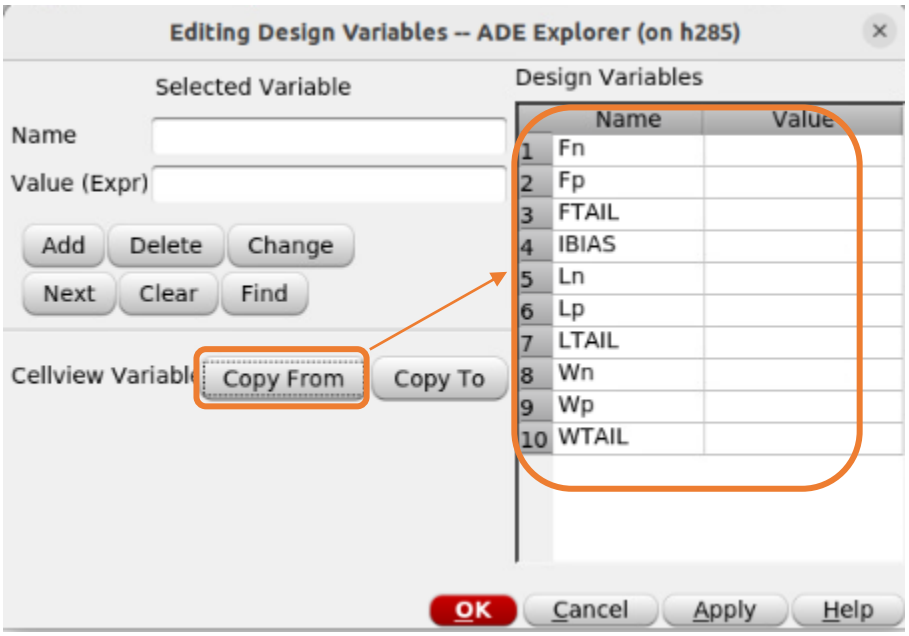
a. DC Operating Point using the DC Analysis

On your schematic window, click **Launch>ADE Explorer**. In the next prompt, select **Create New View**. Keep the View as **maestro**, select **Open in new tab**, and press OK.

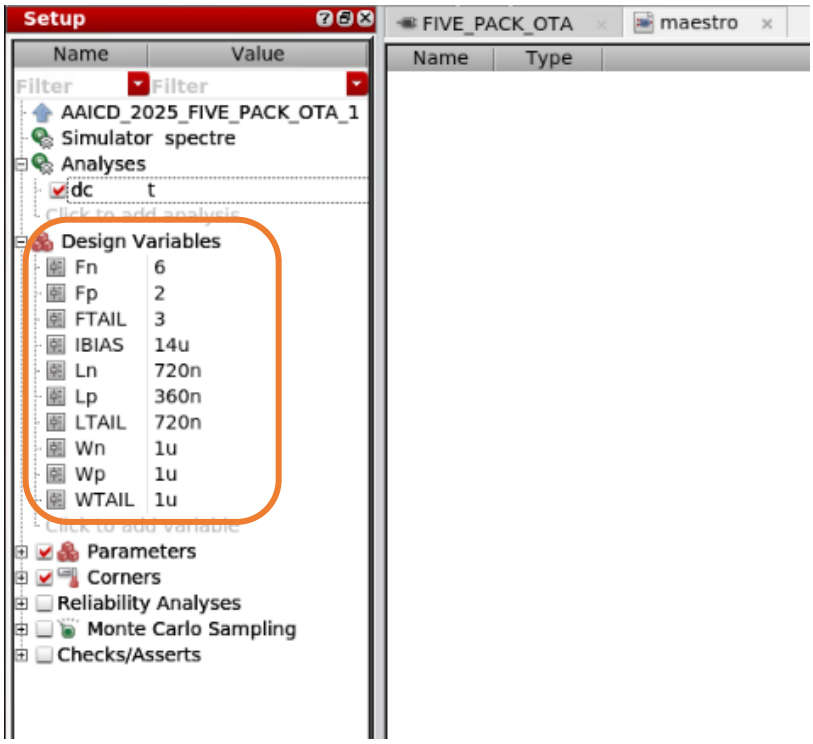
Click on “**Click to add analysis”** and fill the form as shown below. **Don’t forget to check the “Save DC Operating Point” box!**



Below the Design Variables, click on **Click to add variable**. Select **“Copy from Cellview”**.



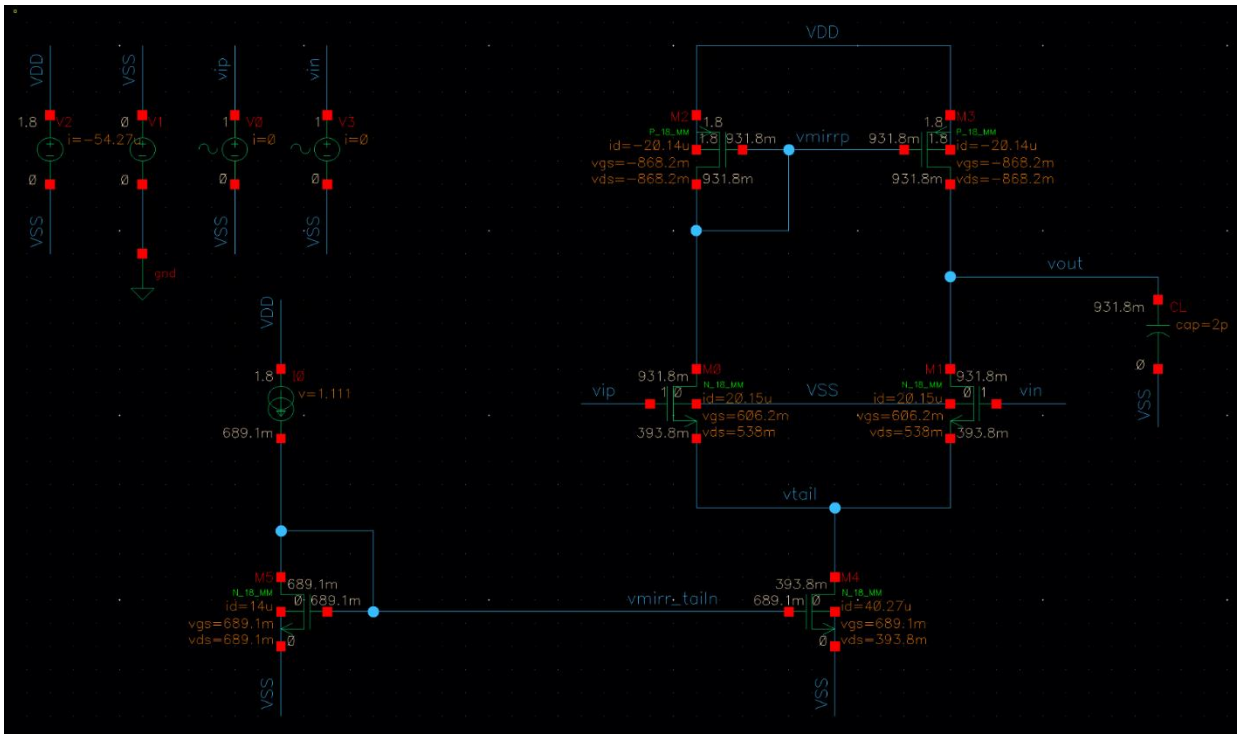
This will load the component parameters you defined earlier in the schematic. Set the values for your variables as shown below (also mentioned in the table earlier).



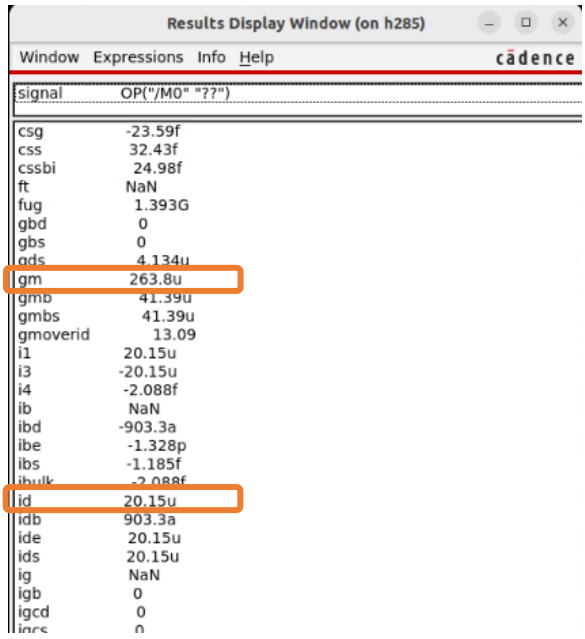
Click on the **green play button (** **)** to run the simulation.

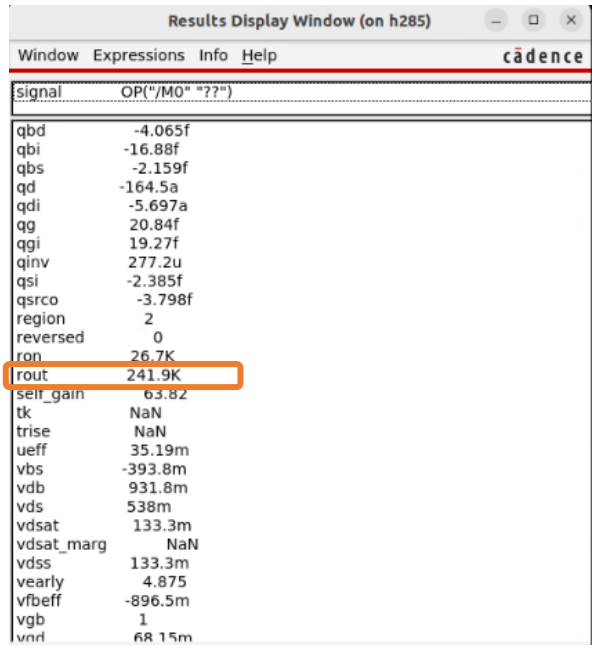
Analyzing DC results

Click **Results>Annotate>DC node voltages**. This will annotate DC node voltages on your schematic. Check the voltage and currents. Make sure they look reasonably accurate.



Click **Results>Print>DC Operating point**, then click on the transistor M0. In this list, you will find the small signal parameters that are derived from the transistor model and the bias point. Check for the different parameters that we designed for, namely, r_o, g_m, etc. We note that the small signal parameters are reasonably close to the desired design value.





Verify the DC operating point for all the other transistors in the design.

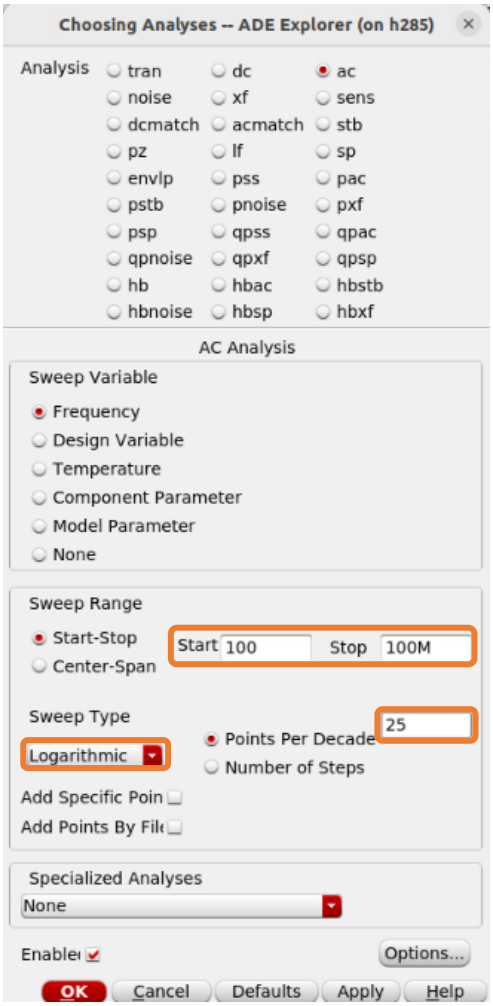
b. Frequency Response using the AC Analysis

In order to verify the Unity Gain Bandwidth (UGB) specification, we run the AC analysis. The AC analysis will let us plot the frequency response of the amplifier.

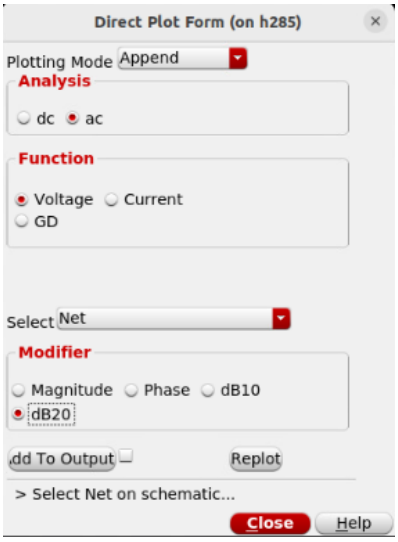
A few notes about AC analysis:

- To apply an AC input, we set the AC magnitude of the source (vdc or vsin) to a non-zero value. Remember, we set the AC magnitude to 500m and -500m for vip and vin sources respectively.
- The AC analysis is a small signal analysis.

To run the AC analysis, under the “Analyses” pane, click on “Click to add analysis”. Choose ac and setup the form as shown below.

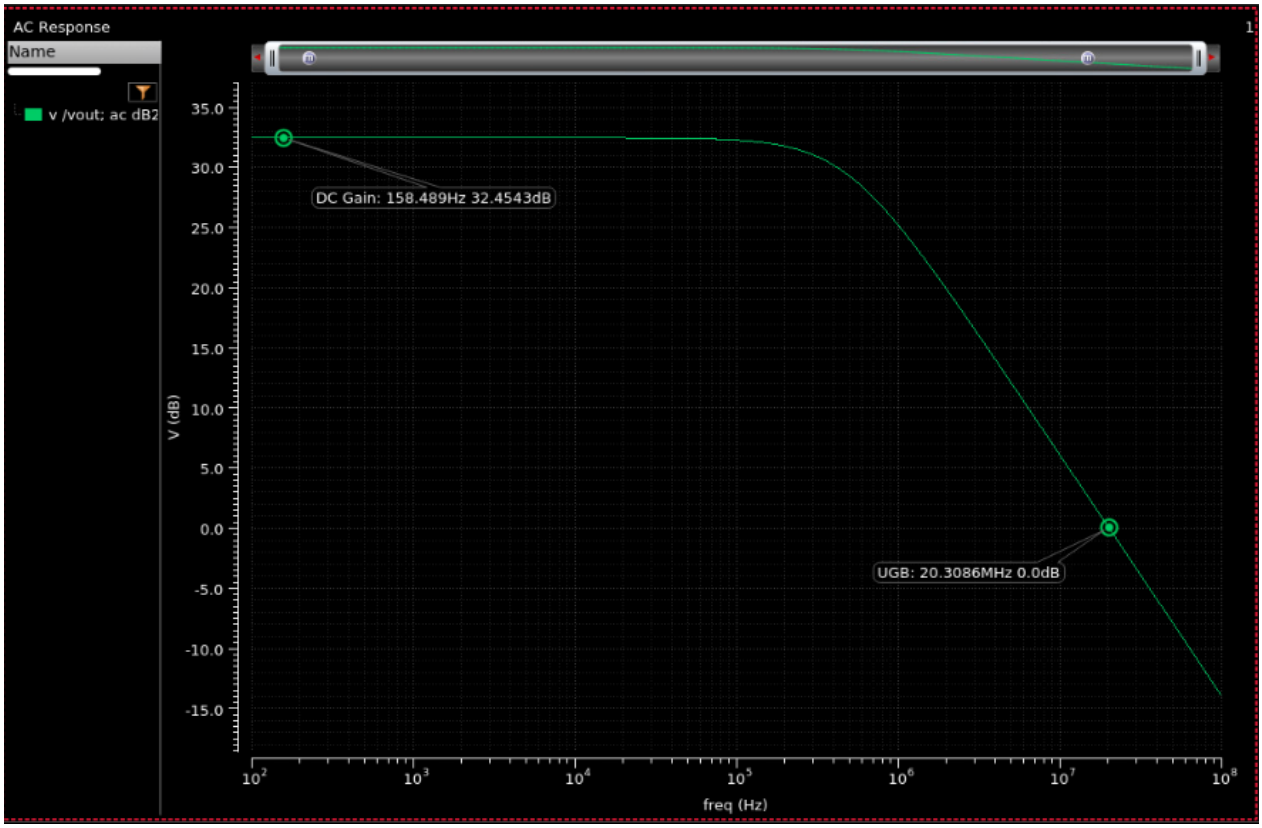


Click OK and launch the simulation by clicking on the green button.



To view the simulation results, in the maestro window, go to **Results>Direct Plot>Main Form.** Now, fill out the form as shown on the left and then click on the output net "vout" in schematic. Press Esc.

The AC magnitude response plot should now come up on your screen.



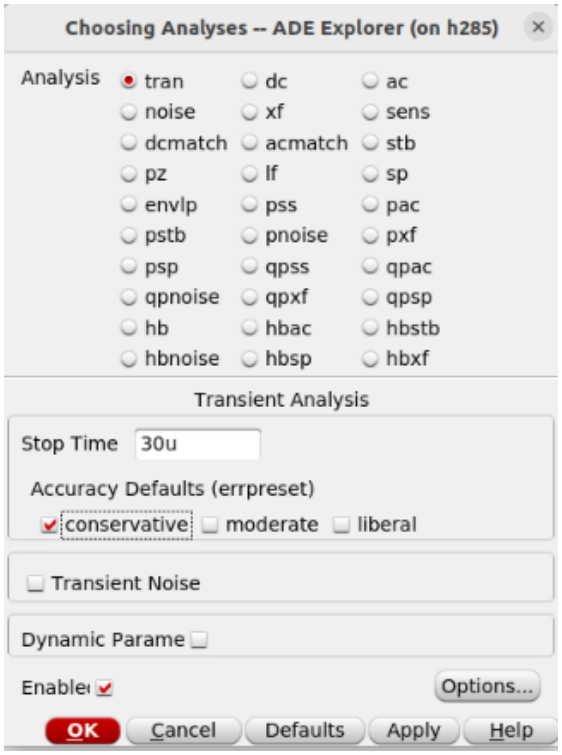
In the AC response, we aim to verify two specifications:

- The DC gain which we designed for ($\approx 20\log_{10}(35) = 31$dB)
- The Unity Gain Bandwidth ($\approx$ 20MHz)

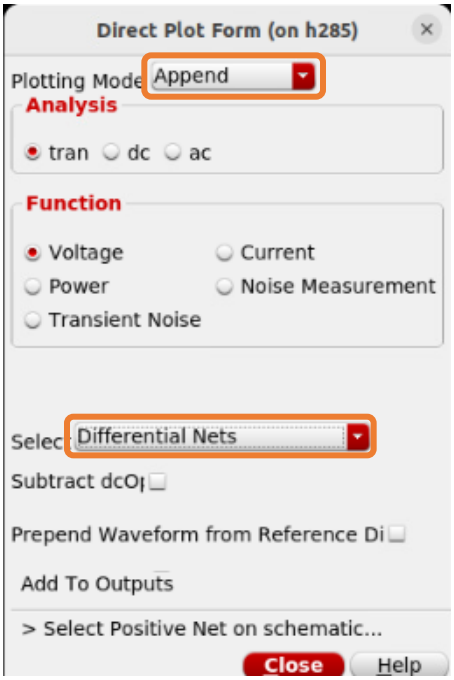
From the plot, we notice a close agreement between the design and simulated values.

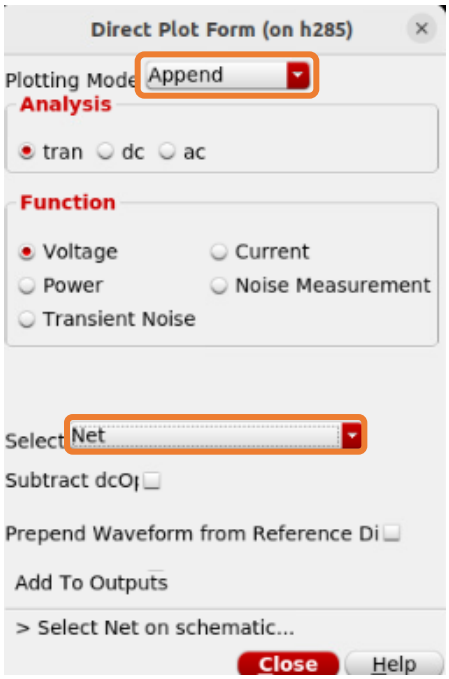
c. Visual sinusoid check using the Transient Analysis

In the maestro window, add a new analysis by clicking on "**Click to Add Analysis"**. Fill the transient simulation form as shown below and run the simulation.



To plot the waveforms, select **Results>Direct Plot>Main Form**

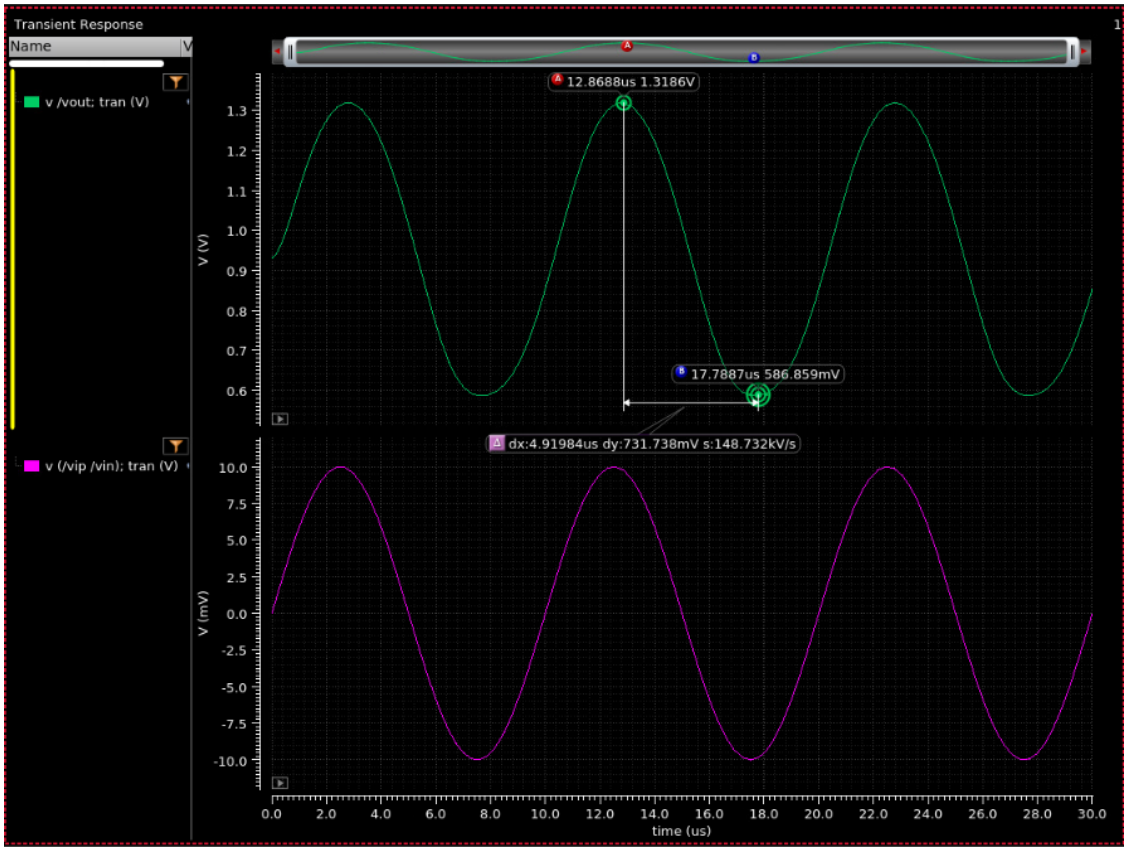




In the above snippet, the Direct Plot Form on the left shows how to plot Differential Nets. This is useful when you want to plot the differential input “vip – vin”. After selecting the “Differential Nets” option click on “vip” and “vin” nets in the schematic. This should bring up the waveform for vip-vin.

To plot, single-ended signals, use the “Net” option as shown in the Direct Plot Form on the right. After selecting the “Net” option click on the “vout” net in the schematic.

To make sure that both “vip-vin” and “vout” appear on the same window, make sure that the “Append” option is selected as the “Plotting Mode” in the form above.



From the plot, we see that the differential input = 20mVpp, and the single-ended output is 732mVpp. This corresponds to a gain of 36.6V/V ($20\log_{10}(36.6)$ = 31.2dB). This matches well with the gain in the AC response.

Apply a 20MHz sine wave as input to the amplifier. What do you expect the gain to be? Is it close to 1? Why?