## TP-1 Appendix

Here, we describe the $g_m/I_D$ methodology used to size the transistors for TP1. While one can attempt to solve the square law and arrive at the transistor sizes, it would require multiple iterations to arrive at the desired specifications – as the square law is an approximation and actual transistors are often modeled by more than 100 parameters. The $g_m/I_D$ methodology or any other methodology for that matter, tries to reduce the number of these iterations.

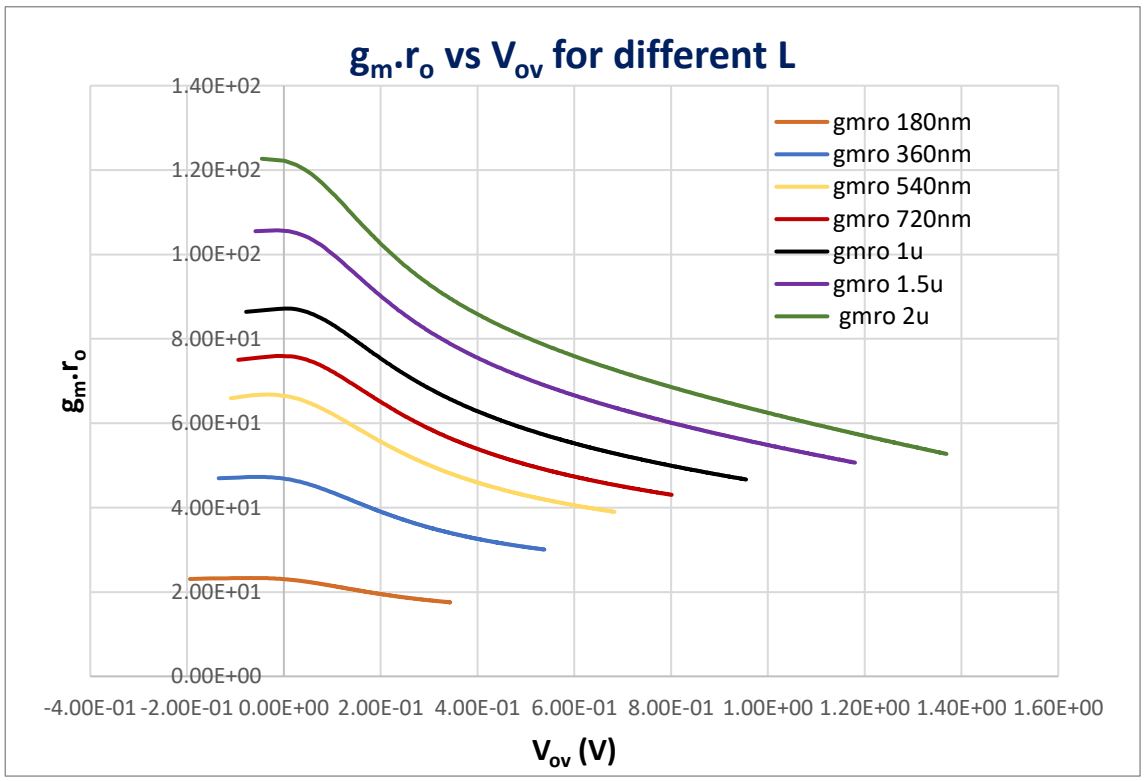
You can find the excel sheet ("CHAR_DATA_NMOS_ALL_L.xlsx" and "CHAR_DATA_PMOS_ALL_L.xlsx") used to construct these plots, on Moodle.

From this sizing exercise, we want to determine the parameters in the following table. For a more detailed description, please refer to the TP-1 problem statement for the Five-Pack OTA (Pages 11 and 12 of the TP-1 document).

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| ? | ? | ? | ? | ? | ? | ? |

### Sizing the NMOS Input Pair

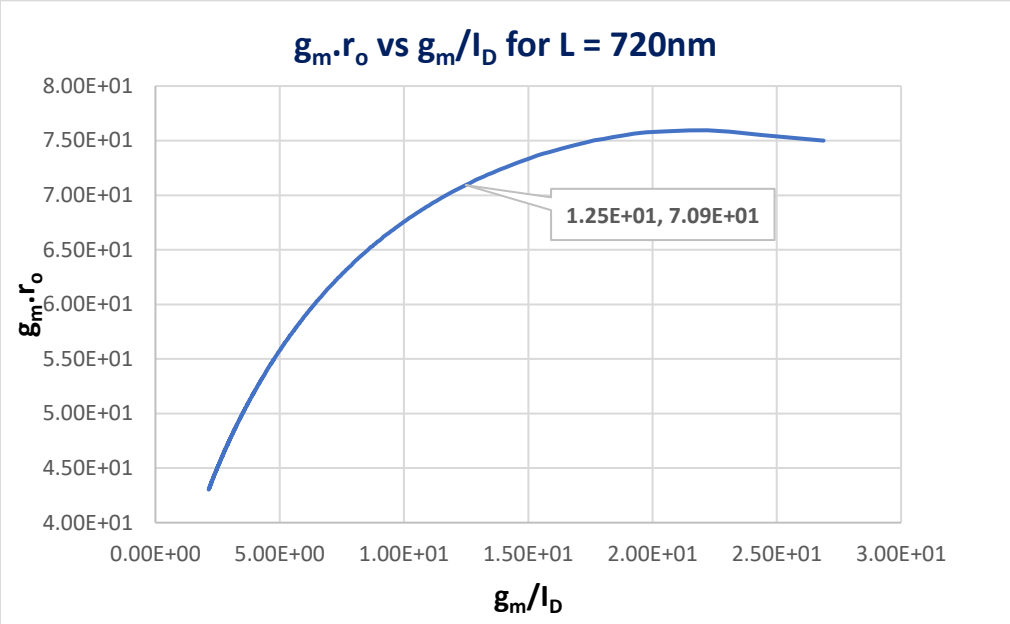
The Excel spreadsheet provided to you lists the different small signal parameters like $g_m$, $g_m.r_o$, $g_m/I_D$, $I_D/W$, $g_m/C_{gg}$, etc. for different values of overdrive voltage. There are seven sheets, each corresponding to a different value of L starting from $L_{min}$ = 180nm to L = 2um.



To identify the minimum length needed to meet the gain requirement in (1), we plot the $g_m.r_o$ as a function of $V_{ov}$ for different values of L. From the plot, we notice that for L < 720nm, the gain specification cannot be satisfied. So, the minimum length required to meet the gain specification = 720nm. In our excitement, let us quickly fill the table 😆

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| ? | 720nm | ? | ? | ? | ? | ? |

Let us now try and determine the current that satisfies the $g_m$ requirement in (2). For this we can plot $g_m.r_o$ vs $g_m/I_D$ for L = 720nm as $g_m.r_o$ and $g_m$ are known and $I_D$ is the only unknown.



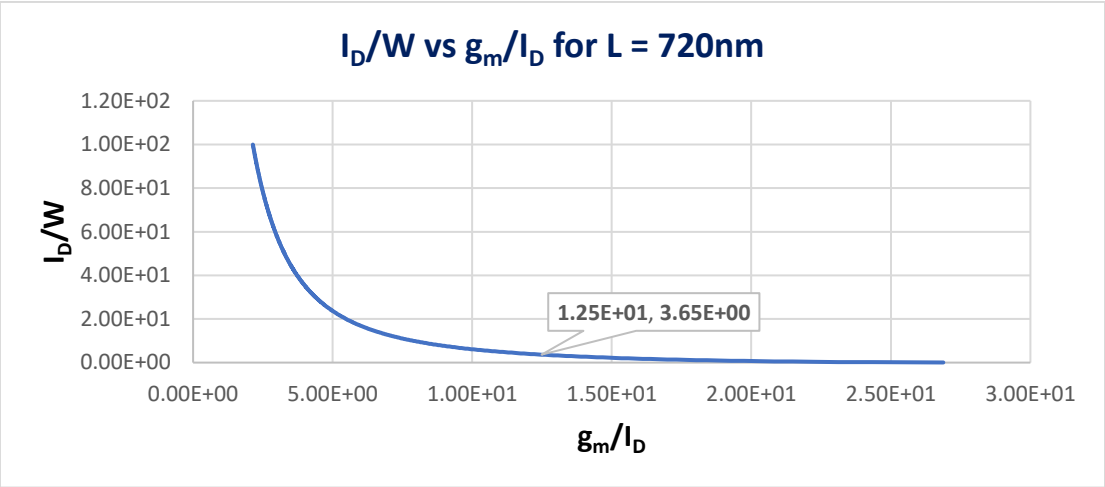

The plot suggests that for a $g_m.r_o$ = 70.9, we have a $g_m/I_D$ = 12.5. This implies,

$$I_D = \frac{g_m}{12.5} = 20\mu A \text{ and } I_{TAIL} = 2I_D = 40\mu A$$

Again, with reinvigorated enthusiasm, let us fill our nice little table. Two down. Five to go🚀

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| $40\mu A$ | 720nm | ? | ? | ? | ? | ? |

Let us now determine the width $W_n$. For this, one could plot $I_D/W$ vs $g_m/I_D$ for $L_n$ = 720nm as $g_m$ and $I_D$ are known, and W is the only unknown.




As can be seen from the plot, the value of $I_D/W$ corresponding to $g_m/I_D = 12.5$ is 3.65. Therefore, $W_n = 20/3.65 = 5.5\mu m \approx 6\mu m$. Yes, yes, we get what to do now. Fill the table!

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| $40\mu A$ | 720nm | $6\mu m$ | ? | ? | ? | ? |

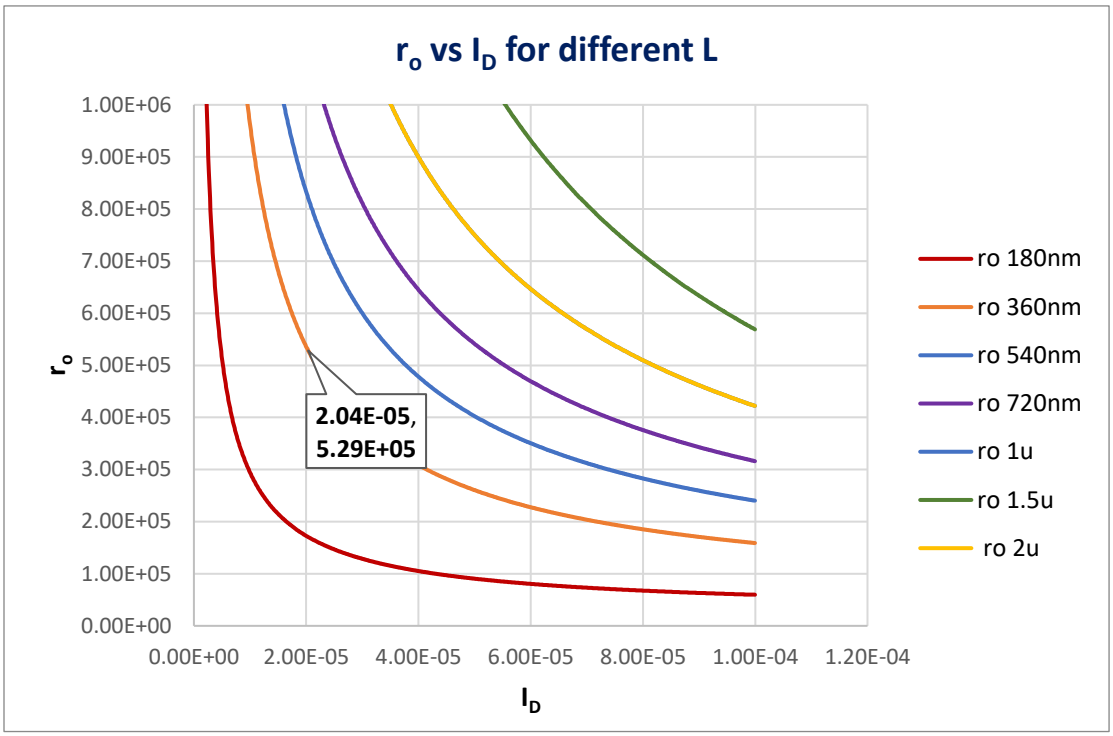

Also check the Overdrive voltage ($V_{OV}$) and $V_{DSAT}$ to make sure that the transistor will be in saturation.

### Sizing the PMOS Transistor

For the PMOS transistor, we note that the requirements are the output impedance and the $V_{GS}$ values.

- The output impedance should be larger than $r_o = A_V/g_{mn} = 279K\Omega$ for a current $I_D = 20\mu A$.
- The overdrive voltage, $V_{OV} = V_{GS}-V_{TH} = 0.8 – 0.54 = 0.26V$. We note that this is an approximate value as we do not know the exact $V_{TH}$

First, we identify the required length by plotting $r_{op}$ as a function of $I_D$ for different values of the length L.




From the above plot, we see that L = 360nm satisfies the required output resistance specification.

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| 40$\mu A$ | 720nm | 6$\mu m$ | 360nm | ? | ? | ? |

To determine the width W, we can look at the ID/W corresponding to an overdrive voltage of -0.26V as shown below. $I_D$/W = 6.55. Therefore, W = 20/6.55 = 3µm.

| L 360nm | Vov 360nm | gm 360nm | ID 360nm | gm/ID 360nm | gmro 360nm | ID/W 360nm | gm/W 360nm | gm/Cgg 360nm | 1/(ID.ro) 360nm | VDSAT 360nm | W 360nm | ro 360nm | Cgg 360nm | gds 360nm |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.60E-07 | -2.60E-01 | 4.28E-05 | 6.55E-06 | 6.54E+00 | 5.94E+01 | 6.55E+00 | 4.28E+01 | 1.64E+10 | 1.10E-01 | -2.76E-01 | 1.00E-06 | 1.39E+06 | 2.62E-15 | 7.21E-07 |

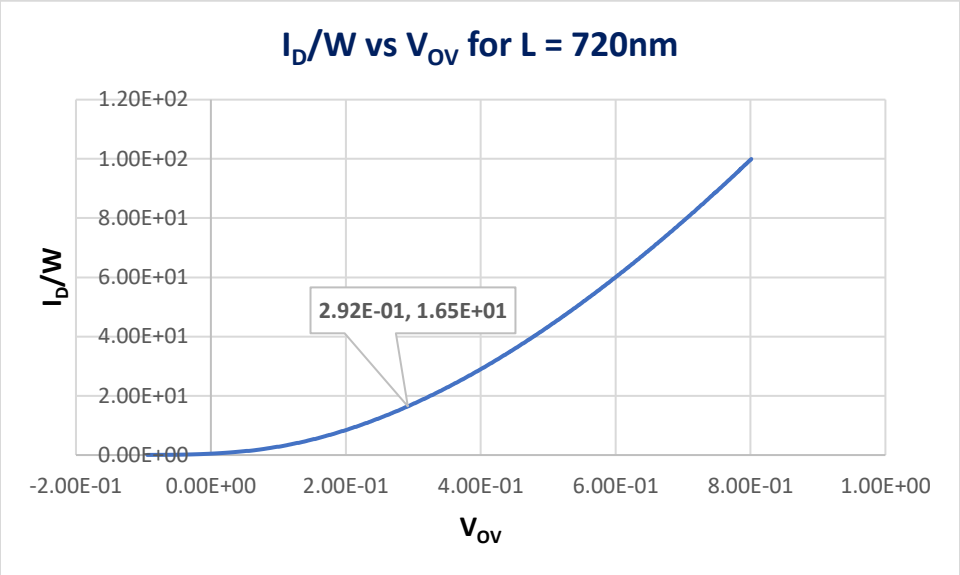
Did you notice something? No?

We simulated with Wp = 2µm in TP-1😆

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| 40$\mu A$ | 720nm | 6$\mu m$ | 360nm | 3$\mu m$ | ? | ? |

**Sizing the Current Mirror Transistors**

The choice of length is decided by the accuracy of the current mirroring required. At this point in time, we can consider L = 4*$L_{min}$ as a safe value to start off with. To determine W, one can look at $V_{OV}$ as a function of $I_D$/W. Typically, for current mirrors, we would like to limit the $V_{OV}$ to less than 300mV.




From the above plot, $I_D$/W = 16.5. This corresponds to a W = 40/16.5 = 2.4$\mu m$

| $I_{TAIL}$ | $L_n$ | $W_n$ | $L_p$ | $W_p$ | $L_{TAIL}$ | $W_{TAIL}$ |
|---|---|---|---|---|---|---|
| 40$\mu A$ | 720nm | 6$\mu m$ | 540nm | 3$\mu m$ | 720nm | 3$\mu m$ |