**EE-523 ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN TP-2025**

**PRACTICAL EXERCISE SESSION No. 6**

**Note:** For students connecting virtually, the details of the Zoom Meeting for this TP session are given below

**Topic**: Advanced Analog IC Design Zoom Meeting

**Time**: May 30th, 2025 01:00 PM Amsterdam, Berlin, Rome, Stockholm, Vienna

**Join Zoom Meeting:**
https://epfl.zoom.us/j/67484830091?pwd=o67Tzl6JepsuXaW4BowdwuPM7wRunY.1

**Meeting ID:** 674 8483 0091

**Passcode:** 979194

**Objectives of this Practical Exercise Session**

1. Layout of a five transistor OTA

    a) Introduction to CMOS layout
    b) Practice the layout of the OTA
    c) Perform DRC (Design Rule Check) and LVS (Layout Versus Schematic)

2. Parasitic Extraction and Post-layout simulation

    a) Perform PEX (Parasitic EXtraction)
    b) Perform post-layout simulation with the extracted netlist

## 1. Layout of a five transistor OTA

### Introduction

The end of the design process is to create the layout, which consists of a set of drawings, one for each layer needed in the manufacturing process. It is important for an analog IC designer to understand the basic device physics and layout editing with commercial tool (i.e. Cadence Virtuoso).

In this tutorial, we will use the differential pair (similar design as TP1) as an example. To facilitate the subsequent layout verification and post-layout simulation, create a new schematic without any ideal components from analogLib (e.g. vdc and vsin), or any parameters (e.g. Ln and Lp), as shown in Fig. 1. Also create a symbol for later use in the testbench.

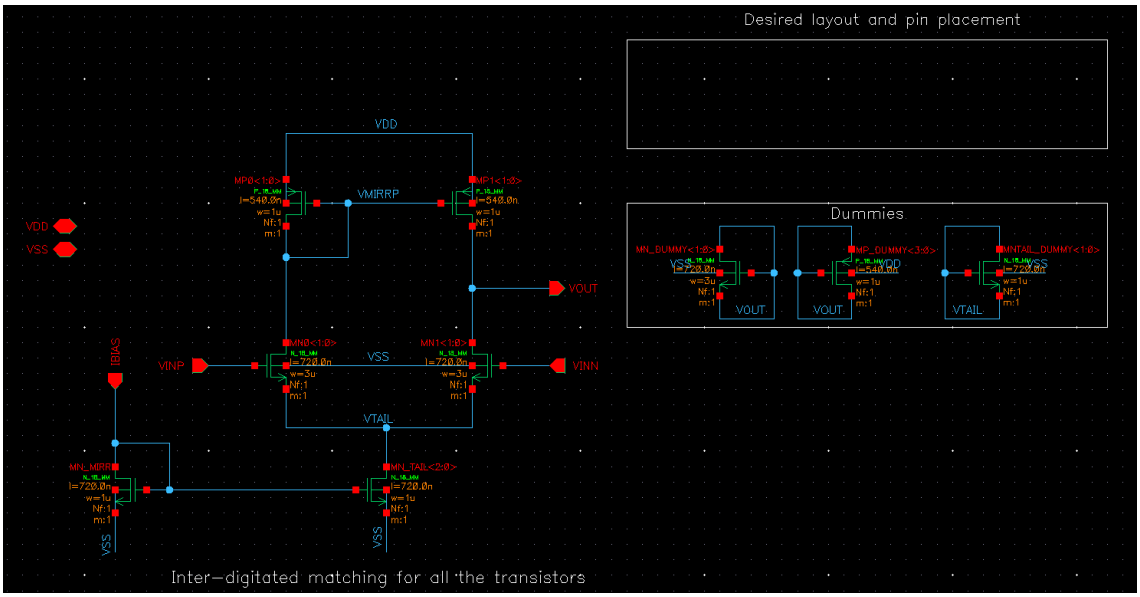



Fig. 1 Schematic of the differential pair circuit

### Preparing your schematic for layout

In our usual circuit simulations, we assume that the transistors in the differential pair are well-matched, that is, MN0 and MN1 are well-matched, MP0 and MP1 are well-matched. However, there could be mismatch between these devices – random or systematic. Random mismatch could be because of variation of doping concentration (Poisson process), oxide thickness variation, or other factors. We can get an idea of the random mismatch by performing the Monte-Carlo simulations.

Systematic mismatch usually results from any asymmetry or imbalance in the layout of your transistors and can be “almost” always be avoided. Systematic mismatch may result from well proximity effects, asymmetrical routing, Shallow Trench Isolation stress, etc.

In layout, our main goal is to mitigate the systematic mismatch. Due to the limitations in the fabrication process, there will be some linear variation in the process parameters across the die area. What are some of the sources of these variations?

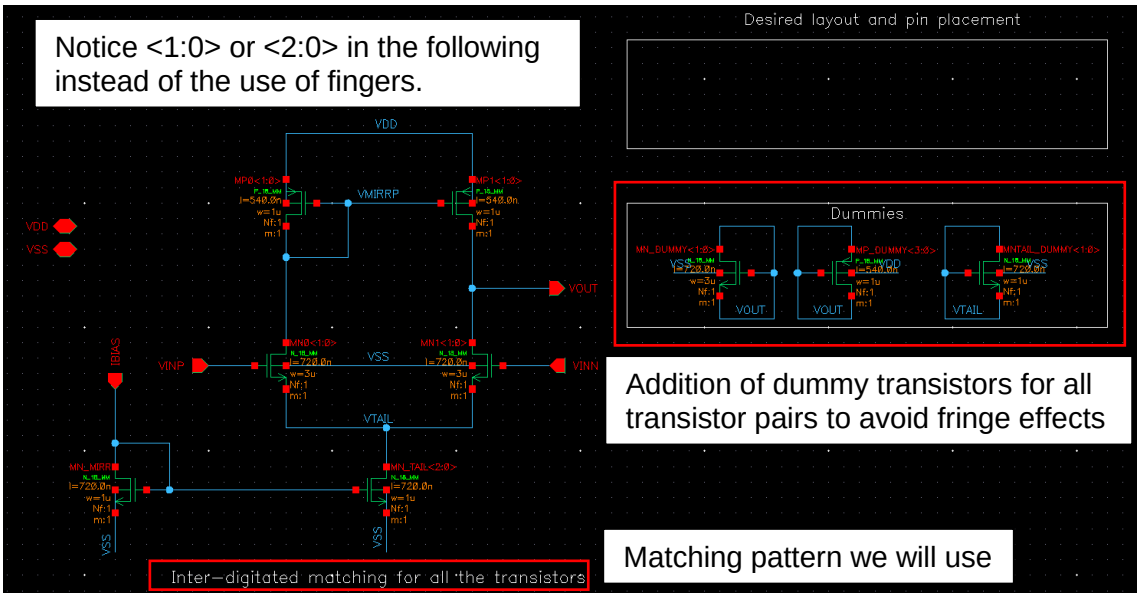
- Temperature Gradients: During furnace processes (like oxidation or annealing), slight differences in heat distribution across the wafer can lead to linear variations in oxide thickness, dopant diffusion, and threshold voltage.
- Gas Flow Non-uniformity**:** During deposition or etching, gases might not distribute perfectly uniformly in the reactor, leading to material thickness gradients.

**Why linear?**

While variations could be arbitrary, linear gradients are common because many process non-uniformities (like heat, gas flow, pressure) vary gradually and directionally. For instance:

- In a deposition chamber, if gas enters from one side and exits the other, material thickness may vary linearly across the flow direction**.**
- Thermal processes often result in center-to-edge gradients, which approximate linear segments “locally”.

In our case, we will assume that there is a linear gradient in both the X and Y direction of our chip. So, we need to ensure that the center of the transistors we want to match are at the same point. The schematic in TP-1 is not very amenable to matching as the center of the transistors lie at different points (as we use fingers instead of multiple transistor units). For the time-being, we will modify the schematic as shown below and later come back and see why it makes sense.



**Read up on inter-digitated vs common-centroid matching. What are their pros and cons?**

To start layout drawing, in the schematic view, ***click Launch (in the top left corner) → Layout XL → "OK" in the Startup Option → "OK" in the New File***. This will bring the layout editing window as shown in Fig. 2. ***Click "Create" to add instance, wire, via, path, label, and so on.*** Some useful shortcuts are listed in Table 1 for your reference. There are multiple layers listed on the right side of left side of the window. Simply tick the corresponding layer to control its visibility (V) and stretchability (S). After layout, we will use the Assura for DRC and LVS. **Ask the nearby TA when you are confused with the software 😊.**

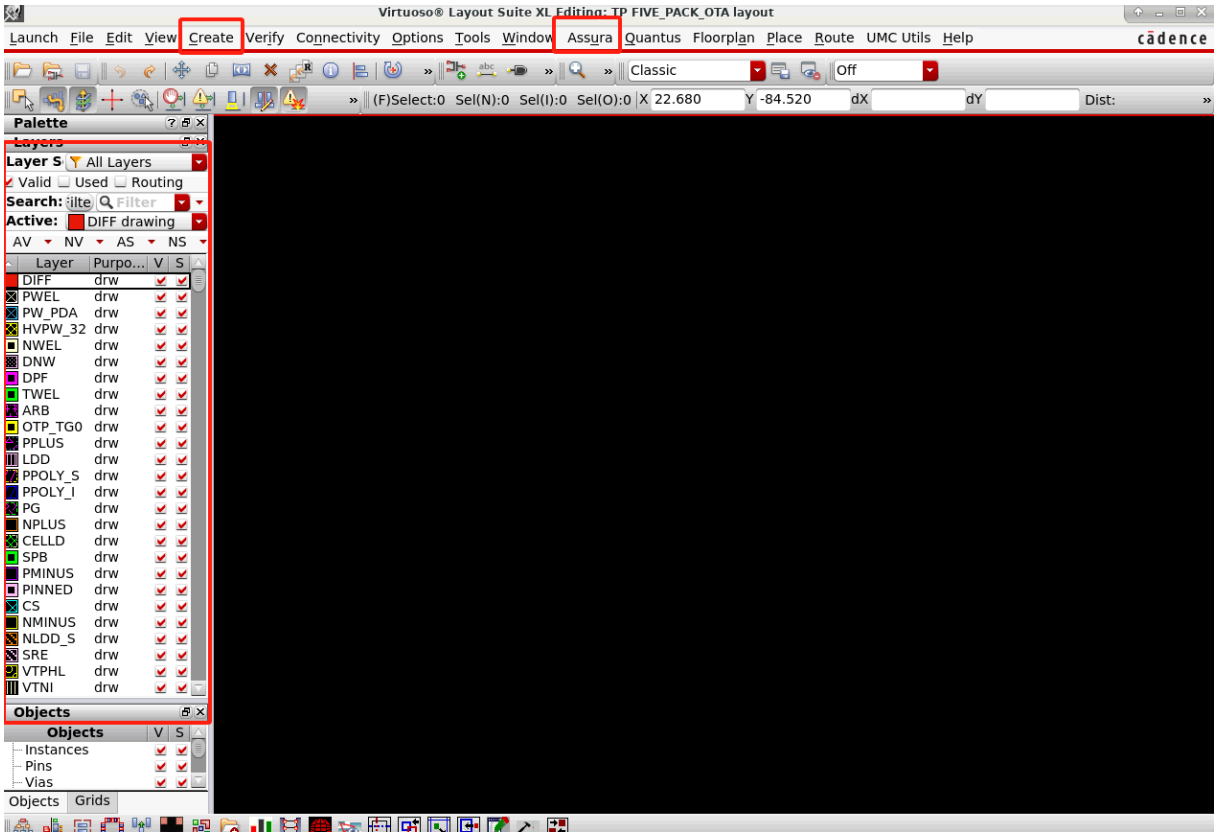



Fig. 2 Layout editing window in Cadence Virtuoso

Table I. Shortcuts of layout editing

| Shortcut | Menu Point | Description |
|---|---|---|
| **i** | Create > Instance | Instantiate another design/device in the current design |
| **r** | Create > Rectangle | Create a rectangle for drawing any layer in layout |
| **p** | Create > Path | Draw path with pre-defined width between two points |
| **o** | Create > Contact | Add contacts/vias between multiple layers from the technology library |

| | | |
|---|---|---|
| **l** | Create > Label | Create labels to indicate the terminals in the layout |
| **q** | Create > Properties | View and edit properties of the geometry in the layout |
| **c** | Edit > Copy | Copy any shape, instances in the layout |
| **m** | Edit > Move | Move any shape, instances in the layout |
| **s** | Edit > Stretch | Stretch any shape one side at a time |
| **u** | Edit > Undo | Undo actions one at a time |
| **F3** | N/A | Show additional properties for the selected command |
| **f** | Window > Fit All | Fit the entire layout into the layout window |
| **k** | Window > Create Ruler | Create a ruler to measure the distance between two points |
| **z** | Window > Zoom > In | Zoom in inside the layout window |
| **e** | Options > Display | To change the layout window display settings |

**A transistor is the basic component of layouts. Create the "P_18_MM" and "N_18_MM" instance in the layout. *Right click on the instance → click "Descend Edit"*, and you will be able to move the layer of the transistor one by one. Review the basic device structure with the layout.**

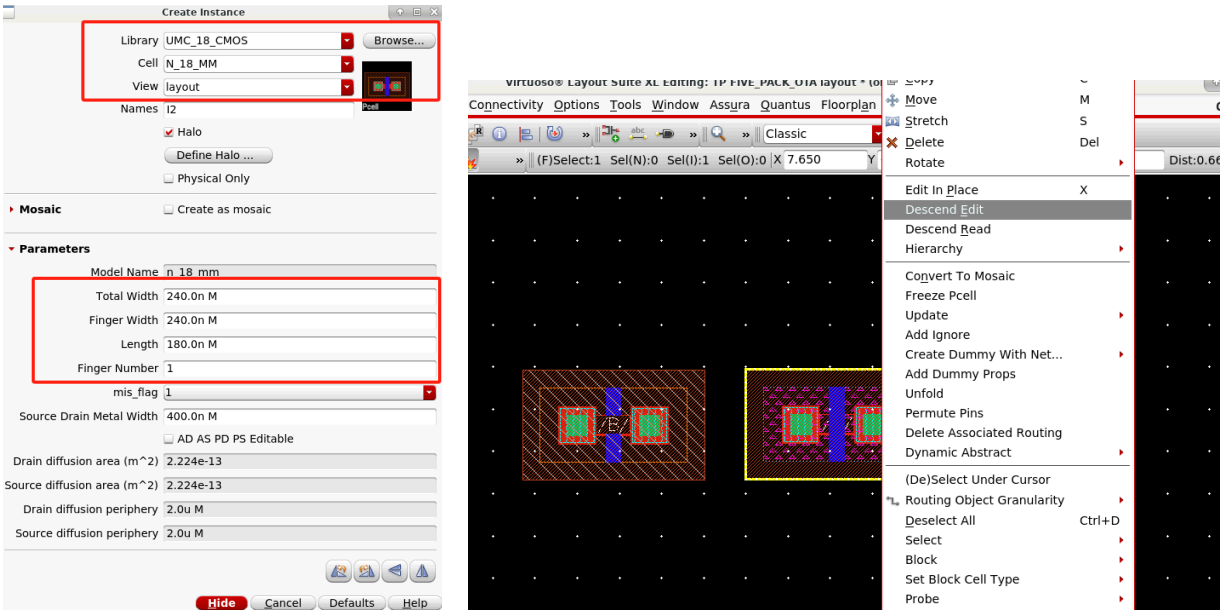



Fig. 3 Creation of transistor instances and "Descend Edit"

## Layout Practice of a Differential Pair

We will now layout the differential pair shown in Fig. 1. Note that any asymmetries in the differential circuits will introduce offsets and limit the minimum differential signals that can be detected. One should be very careful to maintain the symmetry of devices of interest and their surrounding environment during layout editing.

**Read Chapter 19.1-19.2 (especially 19.2) of Razavi, "Design of Analog CMOS Integrated Circuits". How would you plan the placement and routing of your layout?**

Here an example layout is provided in Fig. 4, which will be discussed further during the TP. For more detailed instructions regarding instantiating the MOSFETs, routing nets, adding contacts and labels, please refer to the Appendix.

**Layout Verification (DRC & LVS)**

There are several checks once the layout is done. DRC is performed to guarantee proper fabrication of transistors and interconnects, while LVS is to make sure the layout matches the schematic in terms of device dimensions and connections.

For DRC: ***click Assura → Run DRC → Configure the window as shown in Fig. 5a***.

For LVS: ***click Assura → Run LVS → Configure the window as shown in Fig. 5b.***

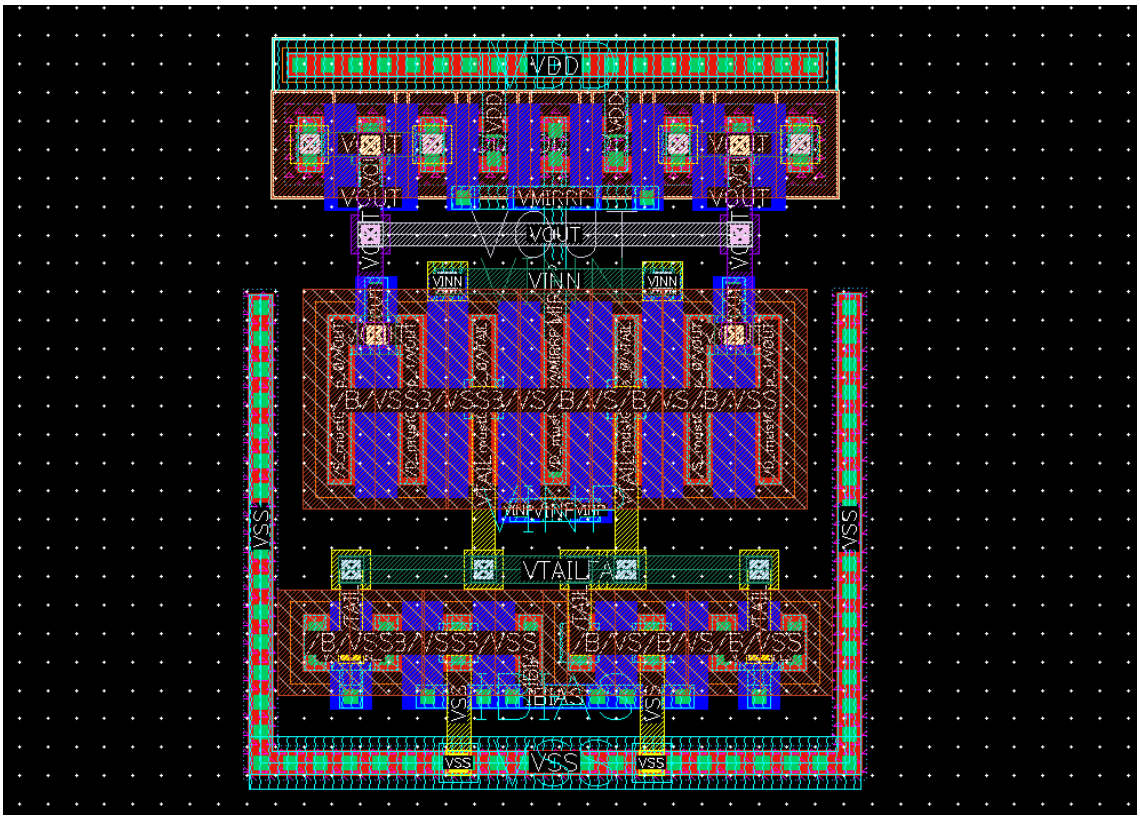
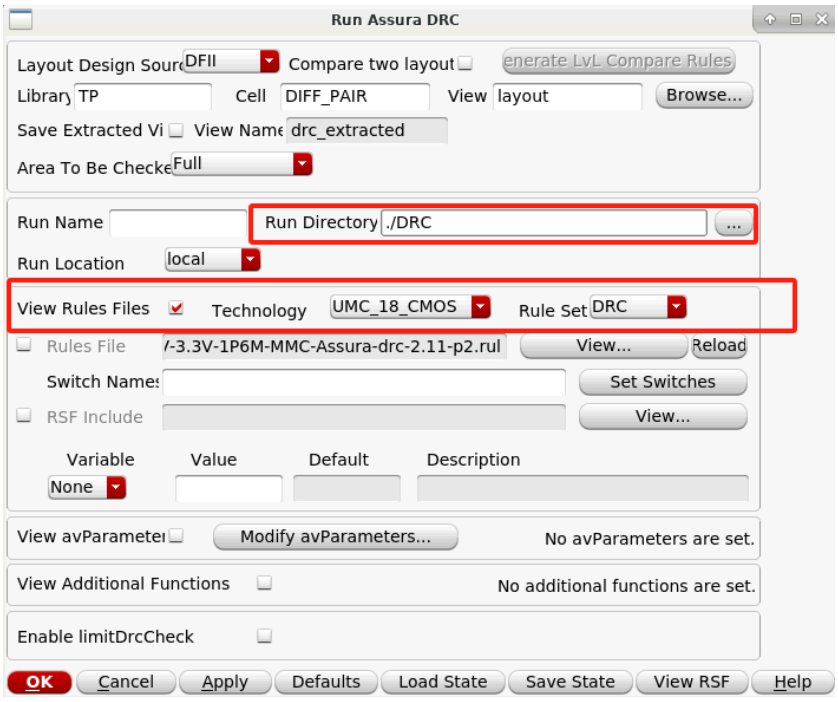
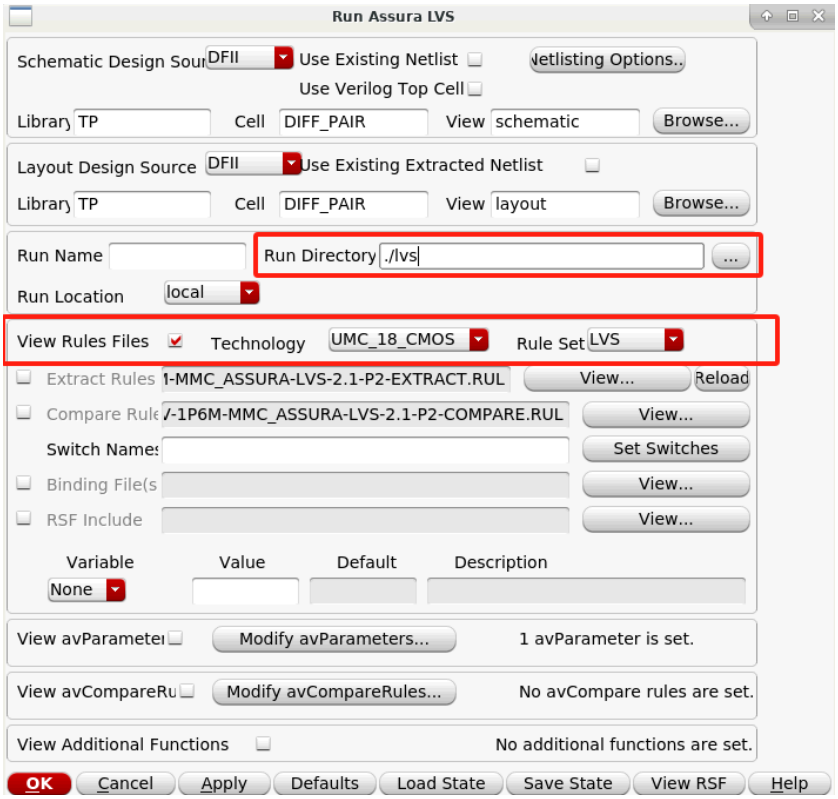



Fig. 4 Layout of the differential pair circuit




(a)




(b)

Fig. 5 (a) DRC and (b) LVS setup window in Assura

## 2. Post-layout Simulation

### Parasitic Extraction

After being laid out physically, we need to simulate how the circuit will actually behave in silicon, accounting for non-idealities introduced during the layout process. To extract the netlist after layout, we should perform PEX (Parasitic EXtraction).

We need to copy the rule file from /dkits folder and adapt the rule to PEX. To do so, first copy the following folder containing the rule file to your own directory.

/dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/Calibre/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_CALIBRE-LVS-2.1-P8

```
EDARHEL7[chuang@jst370 CDS_VISO]$ cp -r /dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/Calibre/G-DF-MIXED_MODE_RFCMOS1
8-1.8V_3.3V-1P6M-MMC_CALIBRE-LVS-2.1-P8 ./
```

Go to the copied folder, open the .txt rule file, and go to lines 496 and 497. Enable the PEX option and point to the .tec file as shown below, which is located at:

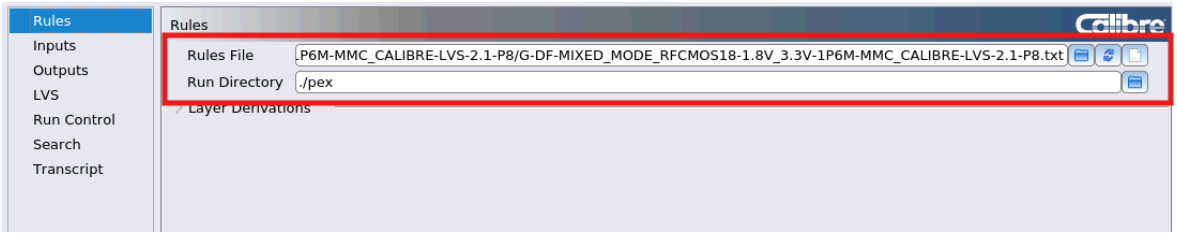
/dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/XRC/G-DF-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL20.6K_XRC-LPE-1.3_P1.tec

```
496  #DEFINE PEXRUN              // TO RUN HSPICE with XRC, Please turn on it.                    //
497  INCLUDE "/dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/XRC/G-DF-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL20.6K_XRC
    -LPE-1.3_P1/G-DF-MIXED_MODE_RFCMOS18-1P6M-MMC_TOP_METAL20.6K_XRC-LPE-1.3_P1.tec"       // To RUN RC, Please inc
    lude the tech file                          //
```

We are ready to run PEX. Here, we use Calibre for PEX. To embed Calibre in the Virtuoso window, open the edadk.conf in your CDS_VISO folder and add the following command lines. You might need to restart the Virtuoso to use Calibre.

```
cds mgc_clbre 2020.1
mgc_clbre 2020.1
```

Once Calibre is ready in your layout window. Click “Calibre” → configure the window as shown in Fig. 6 → Run PEX



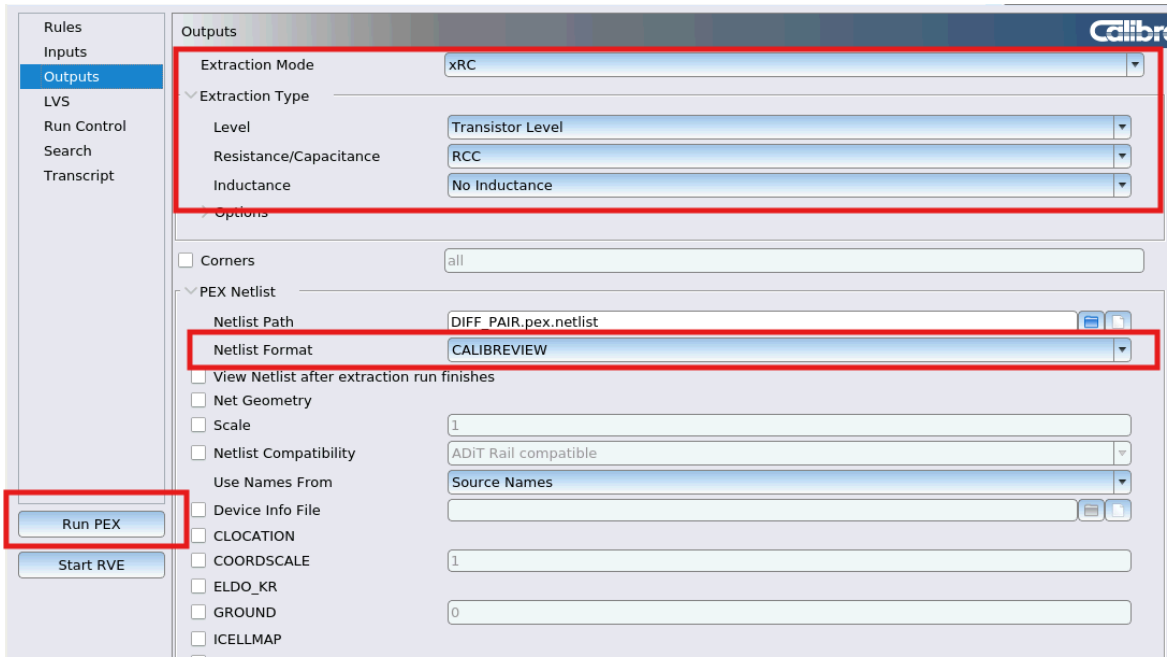
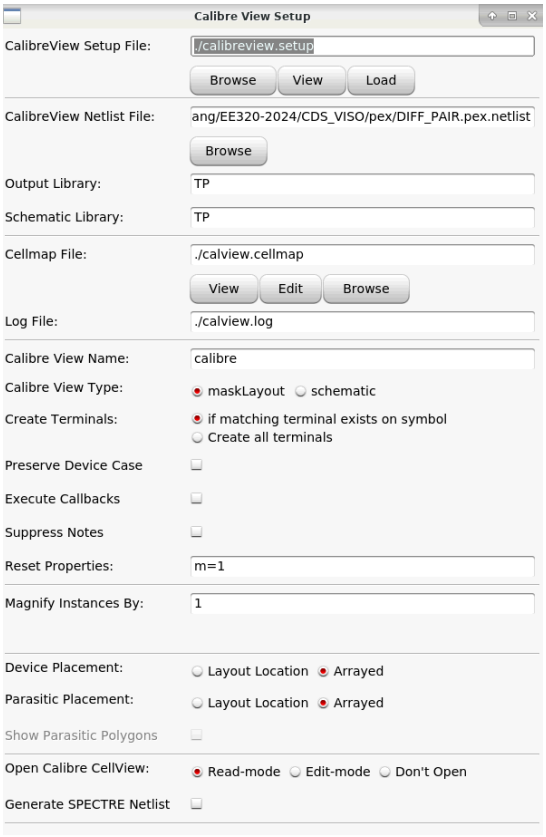



Fig. 6 Calibre PEX configuration window (use the rule file you've modified)

When the PEX run finishes, a window comes out and you will be able to see the Calibre view.



**Post-layout Simulation**

Create a testbench using the symbol of the differential pair circuit. Further create a testbench and connect all the necessary inputs, power and ground supply, and loading (refer to TP1), as shown in Fig. 6.

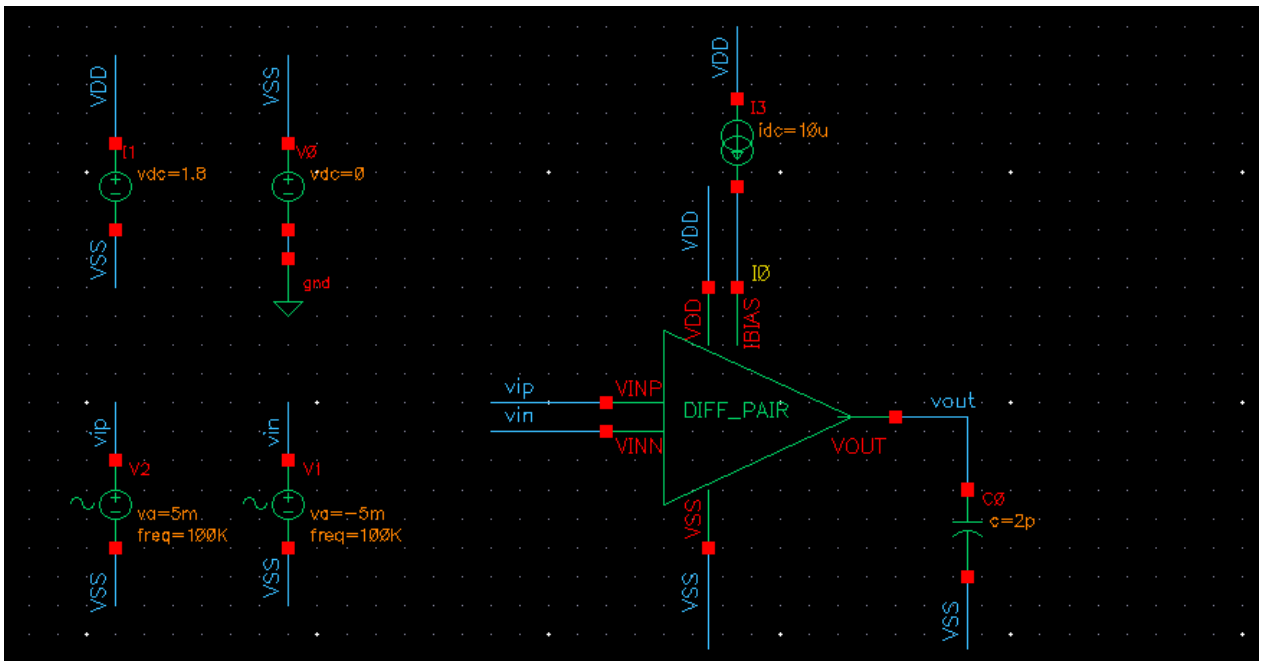



Fig. 6 Testbench of the differential pair

To enable post-layout simulation, in the maestro window, ***click "Setup → Environment", type "calibre" at the beginning of "Switch View List", then click "OK",*** as shown in Fig. 7. Now you will be able to perform post-layout simulation using the Calibre view (extracted netlist).

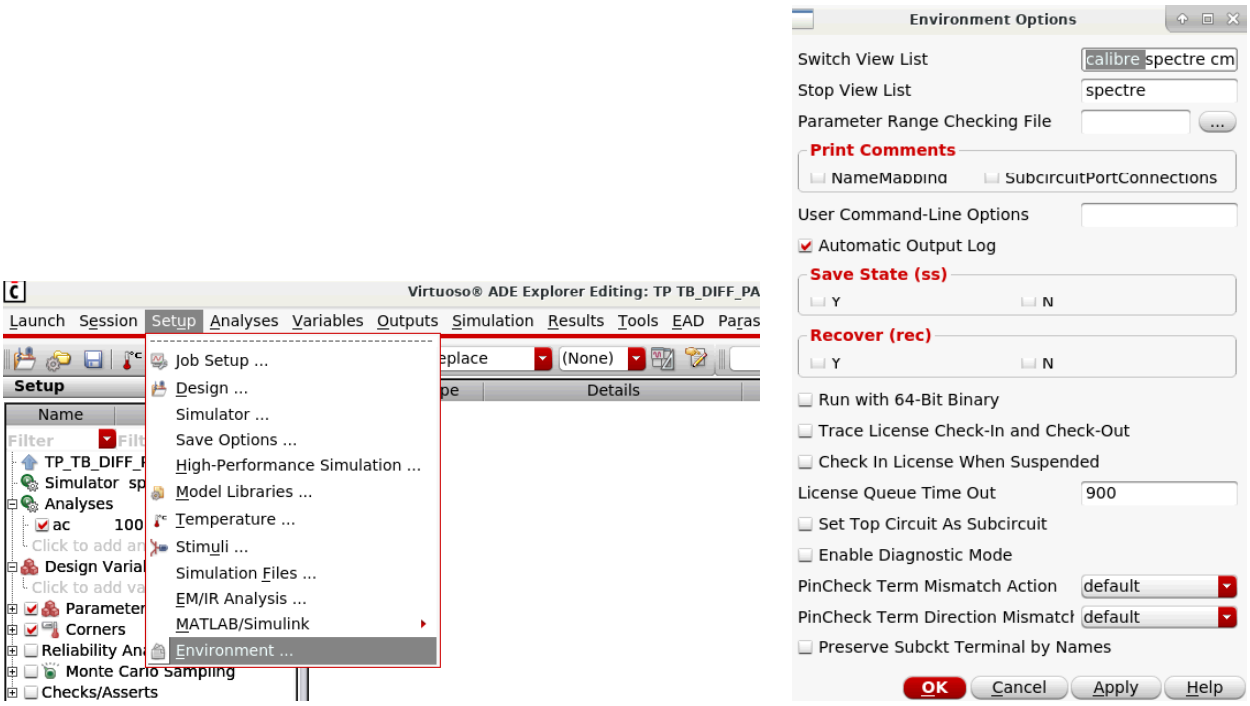



Fig. 7: Post-layout simulation setup

**Perform AC simulation (pre-layout and post-layout) for the AC response (DC gain, UGB). Do the simulation results match well? Try to explain any differences observed.**

## 3. File Sharing for the Course Project

**This section is intended for students who work with others in the course project. If you work on your own, feel free to skip this part.**

In order to share files with your partner (such as schematic and layout), the server management team created a folder: /work/fvlsi/classes/EE-523/ (this folder is accessible when you exit the edadk mode or before run_edadk). Now create and name a folder that only belongs to your group, as shown in Fig. 8. Note that unfortunately, since everyone can access contents in this folder, **we highly suggest you NOT putting any important materials in this folder (atleast not for long, transfer and delete)**. For example, instead of transferring the circuit design from student A to student B, transfer the testbench from student B to student A. Those who access and copy other groups' contents will face penalties and lose marks when grading!

```
[chuang@jed ~]$ cd /work/fvlsi/classes/EE-523/
[chuang@jed EE-523]$ mkdir example
[chuang@jed EE-523]$ chown -R :users.edadk example
[chuang@jed EE-523]$ chmod -R 770 example
[chuang@jed EE-523]$ ls
example  tp6
```

Fig. 8: Create a folder to share files with your partners

Lastly, thank you all for your hard work during the semester. Wishing you a great course project and final exam! 😊