EE-523 ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN TP-2025

PRACTICAL EXERCISE SESSION No. 3

Note: For students connecting virtually, the details of the Zoom Meeting for this TP session are given below

Topic: Advanced Analog IC Design Zoom Meeting

Time: April 4th, 2025 01:00 PM Amsterdam, Berlin, Rome, Stockholm, Vienna

Join Zoom Meeting:

https://epfl.zoom.us/j/66887254608?pwd=MBLOAjyTb7PaR02tNUeDaHDb1q5WID.1

Meeting ID: 668 8725 4608

Passcode: 191600

Objectives of this Practical Exercise Session

1. Design and simulate a fully differential amplifier with common mode feedback (CMFB):

   a) Following the design procedures, design a fully differential amplifier with CMFB that meets the given set of specifications
   b) Perform DC Analysis for DC operating point
   c) Perform AC Analysis for frequency response

2. Improve the gain by adding the "gain-boosting" technique to the fully differential amplifier:

   a) Following the design procedures, add the gain-boosting technique to the fully differential amplifier
   b) Perform DC Analysis for DC operating point
   c) Perform AC Analysis for frequency response
   d) Perform noise simulation for the amplifier
   e) Perform CMRR simulation for the amplifier
   f) Perform PSRR simulation for the amplifier

1. Design and Simulate a Fully Differential Amplifier

Design Specification

- DC Gain (A_V) > 65 dB ≈ 1800 V/V
- Unity Gain Bandwidth > 20MHz
- Output Load Capacitance (C_L) = 2pF
- $V_{OUT, DC}$ ≈ 1.15 V
- $V_{IN, DC}$ = 0.9 V
- V_{DD} = 1.8 V
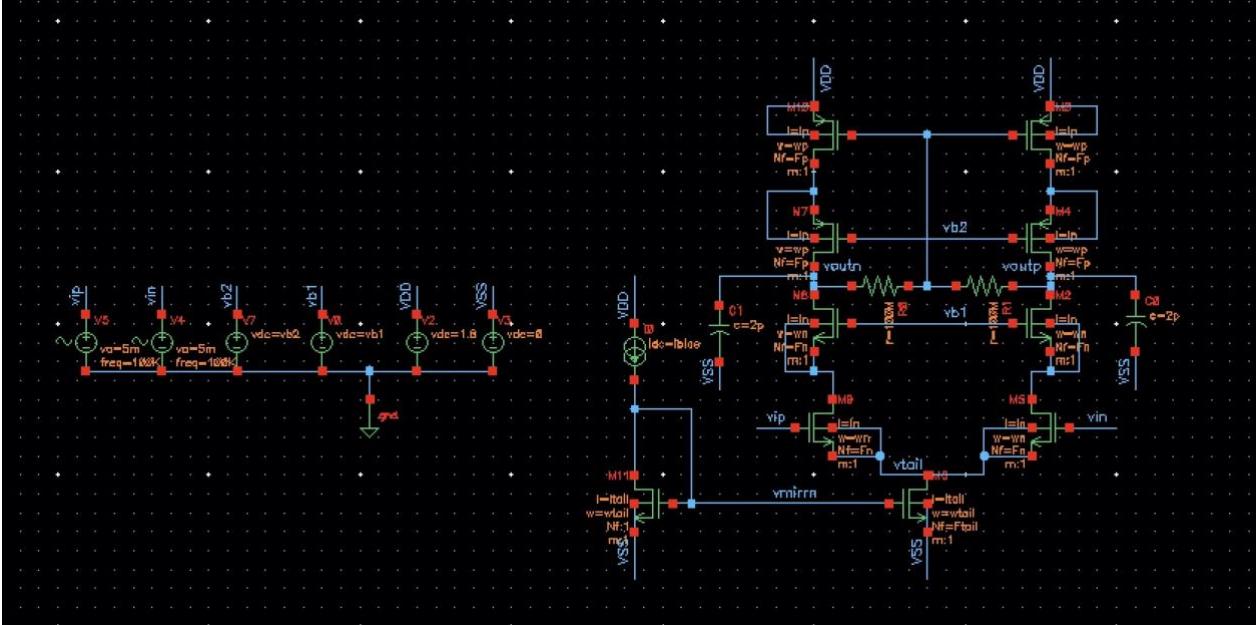
Fig. 1: Schematic of the Fully Differential Amplifier

The circuit schematic is shown in Fig. 1. The design of the fully differential amplifier is very similar to the operational transconductance amplifier (OTA) discussed in TP2. The transistor sizing is the same as that of the cascode OTA presented in TP2. You can refer to TP2 for the sizing methodology.

To make the amplifier fully differential, instead of using a diode-connected current mirror node, a common-mode feedback (CMFB) circuit is applied to bias the load current mirror. The resistor used in the CMFB circuit is an ideal resistor from the 'analogLib' library, with the component name 'res'. As could be seen from the TP 2, the output impedance of the amplifier is close to 8MΩ. Here the resistor for the common mode feedback is set to 100MΩ to reduce the degradation of the output impedance.

I_{BIAS}	L_{TAIL}	W_{TAIL}	F_{TAIL}	L_n	W_n	F_n	L_p	W_p	F_p	V_{b2}
19 μA	720 nm	1 μm	2	720 nm	1 μm	7	360 nm	1 μm	12	0.8

Building the Schematic

The way of building the schematic is the same as the FIVE_PACK_OTA example demonstrated in TP1. Here are a few points to help you quickly create the schematic shown in Fig. 1.

- Create new cellview in the library manager and select "Schematic".
- Choose "N_18_MM" and "P_18_MM" in the UMC_18_CMOS library for transistors.
- Choose "vsin" in the analogLib library for vip/vin input sources. The DC voltage should be 900 mV.
- Press "i" to add instances.
- Press "q" to bring the "Properties" dialogue.
- Press "w" for wiring connection of all components.
- Press "l" (the lowercase L) to label the nets.
- Press "Shift+x" to check and save your schematic.

DC Operating Point using DC Analysis

The way of creating the simulation window is the same as the FIVE_PACK_OTA example demonstrated in TP1. Here are a few points to help you start the simulation.

- On your schematic window, click **Launch>ADE Explorer**. Select **Create New View**. Keep the View as **maestro**, select **Open in new tab**, and press OK.
- Click on "**Click to add analysis**". Choose dc analysis, and don't forget to check the **"Save DC Operating Point"** box.
- Below the Design Variables, click on Click to add variable. Select **"Copy from Cellview"**. Then fill in the variables derived from the hand calculation above.
- Click on the **green play button (▶)** to run the simulation.

After running the simulation, click **Results>Annotate>DC node voltages / DC operating points**. This will annotate DC node voltages / DC operating points on your schematic. Check the voltage and currents. Make sure they are close to the desired values. You can also click **Results>Print>DC Operating point** to check the small-signal variables of each transistor.
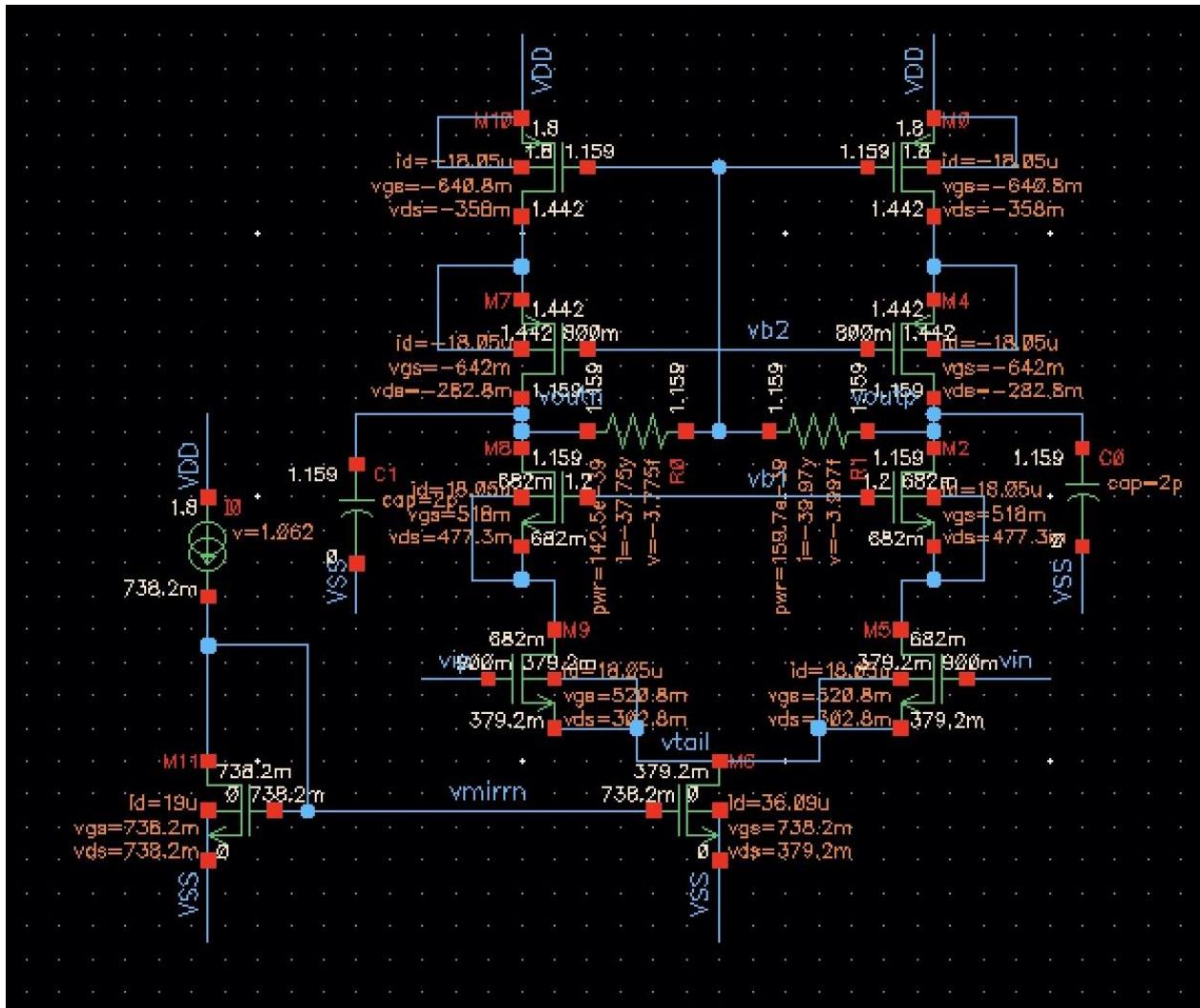
Fig. 2: Annotation of DC node voltages / DC operating points

Frequency Response using AC Analysis
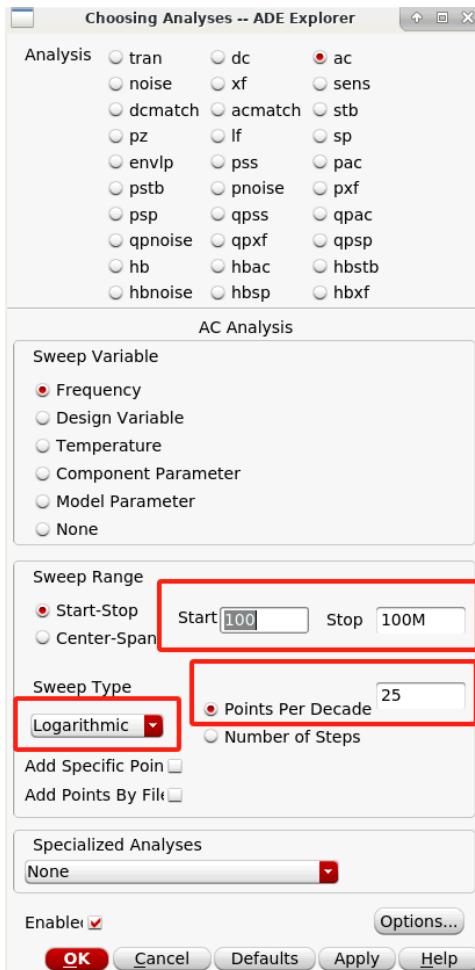
Fig. 3: AC Analysis setup

*Tip: To view the simulation results, as introduced in TP1, click **Results>Direct Plot>Main Form** and select vout in your schematic. You can also use **Results>Direct Plot>Main Form**, the select bar should be set as differential net and the modifier should be set to 20dB, as shown in Fig. 5. After this setup you could click on the voutp and voutn to plot the differential output.*
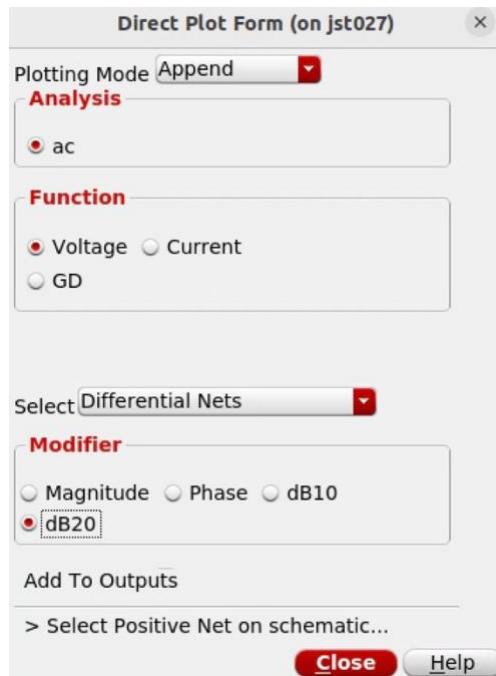
Fig. 4: Direct Plot Form setup
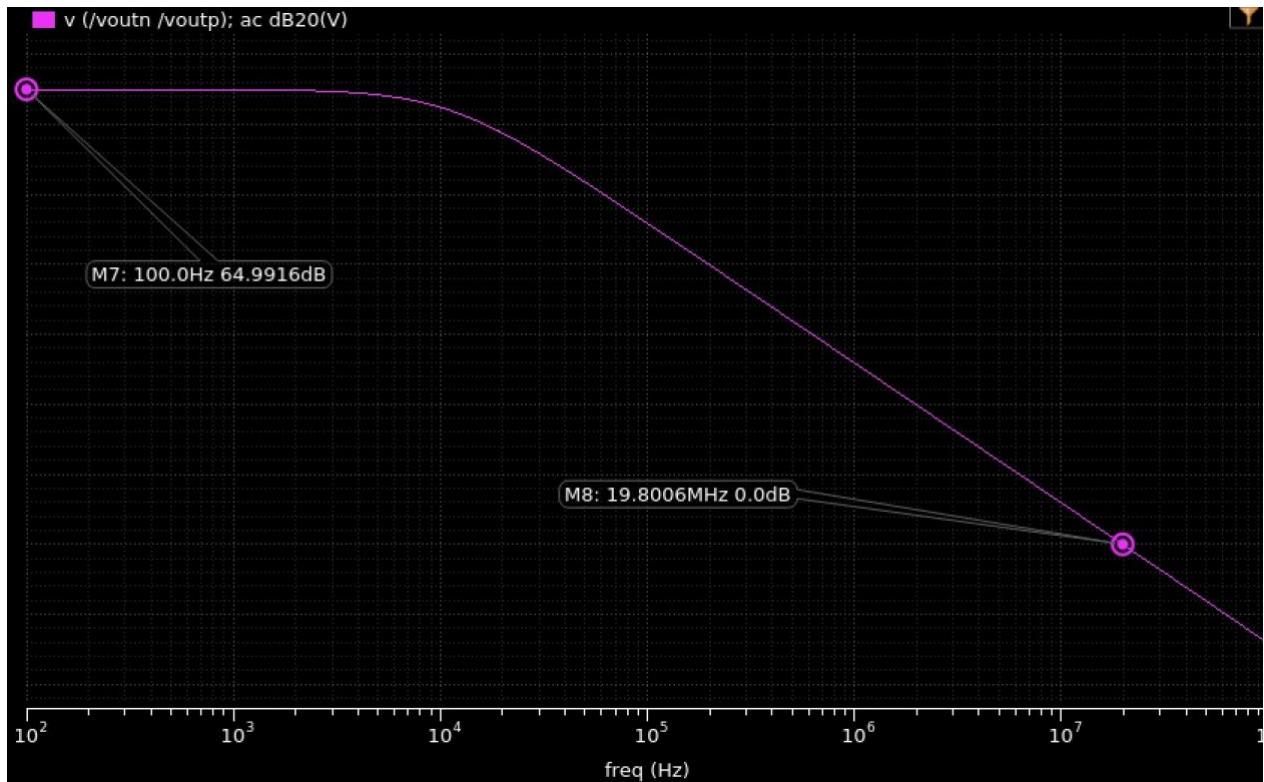
Fig. 5: Frequency response of the differential output

2. Design and Simulate a Differential Amplifier with Gain-Boosting Technique

Design Specifications

- DC Gain (A_V) > 70 dB ≈ 3160 V/V
- Output Load Capacitance (C_L) = 2pF
- V_{DD} = 1.8 V
- $V_{IN, DC}$ = 1.0 V
- Output Swing > 1.2 V
- 3-dB Bandwidth > 9kHz

The gain-boosting technique is used to increase the effective transconductance (G_m) of the transistor. In this case, we apply the technique to the cascode transistor of the input pair. The transconductance of the cascode transistor is increased by a factor of A_A, where A_A is the gain of the auxiliary amplifier. We can reuse our previous Fully-Differential amplifier design for this purpose. The drain terminals of the input pair are connected to the input of another differential amplifier, which is the same amplifier design used in the previous section of this TP. The output of this amplifier is then connected to the gate of the cascode transistor.
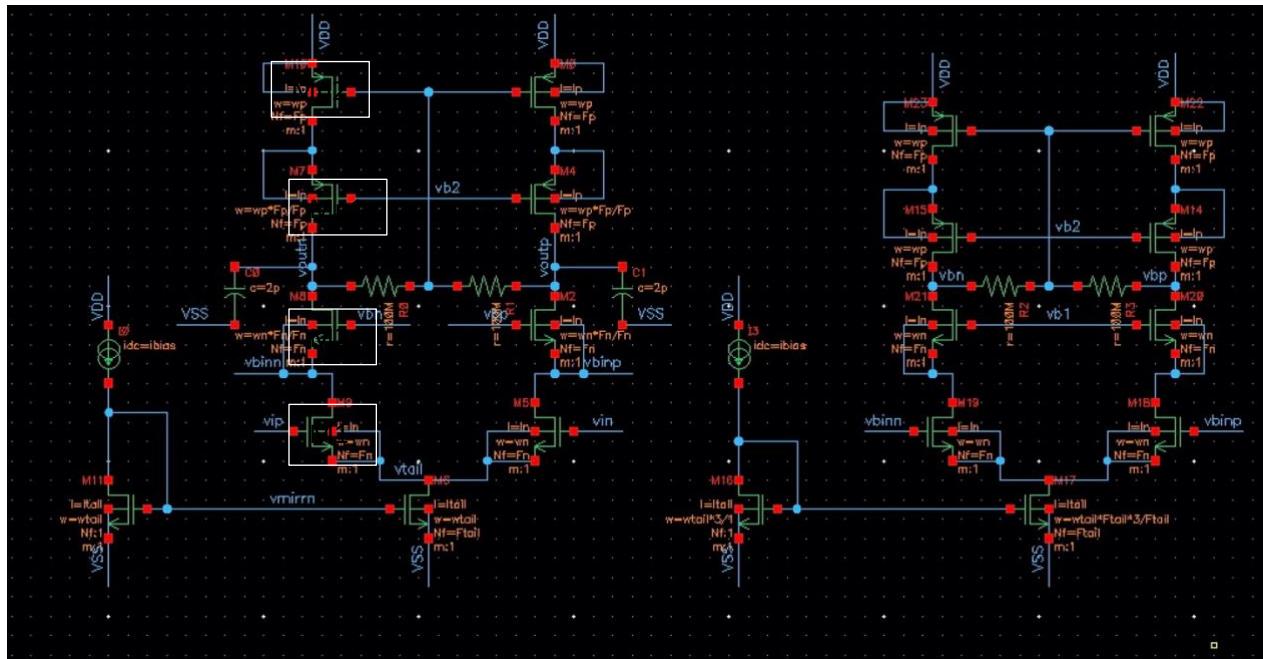
Fig. 6: Schematic of the Fully Differential Amplifier with Gain-Boosting

Referring to Lecture 2, if we go through the mathematical derivation, the effective transconductance of the cascode transistor increases to $g_{m2}(1+A_A)$, while the effective output impedance of the input pair increases to $g_{m2} \cdot r_{o1} \cdot r_{o2} \cdot (A_A+1)$. The total output impedance is given by $(r_{o1} \cdot r_{o2} \cdot (A_A+1) \cdot g_{m2}) \| (r_{op1} \cdot r_{op2} \cdot g_{mp})$. Based on the simulation of the differential amplifier from the previous part of this TP, A is approximately 1800. Assuming $r_{op1} \cdot r_{op2} \cdot g_{mp}$ is close to $r_{o1} \cdot r_{o2} \cdot g_{m2}$, the total output impedance should increase approximately by a factor of 2 when only the NMOS

cascode is gain-boosted. Here the gain does not increase significantly, because of the limitation of pmos current mirror output impedance, same technique could be applied for the cascode transistor of pmos current mirror if you want to further increase the gain.

With the same transconductance for the input transistor, the gain of the differential amplifier is expected to double (approximately a 6 dB increase). It is important to note that the input common-mode voltage of the auxiliary amplifier assisting the gain-boosting technique is around 700 mV, compared to 900 mV in the previous design. To accommodate this change in the input common-mode voltage, the tail current source of the auxiliary amplifier has a width-to-length (W/L) ratio three times larger, which reduces the overdrive voltage. This allows the common-mode input voltage to shift to 700 mV while maintaining a similar gate-source voltage (V_{GS}) for the input transistors.

DC Operating Point using DC Analysis

Repeat the DC Analysis steps. Run the DC simulation and annotate the DC operating point.
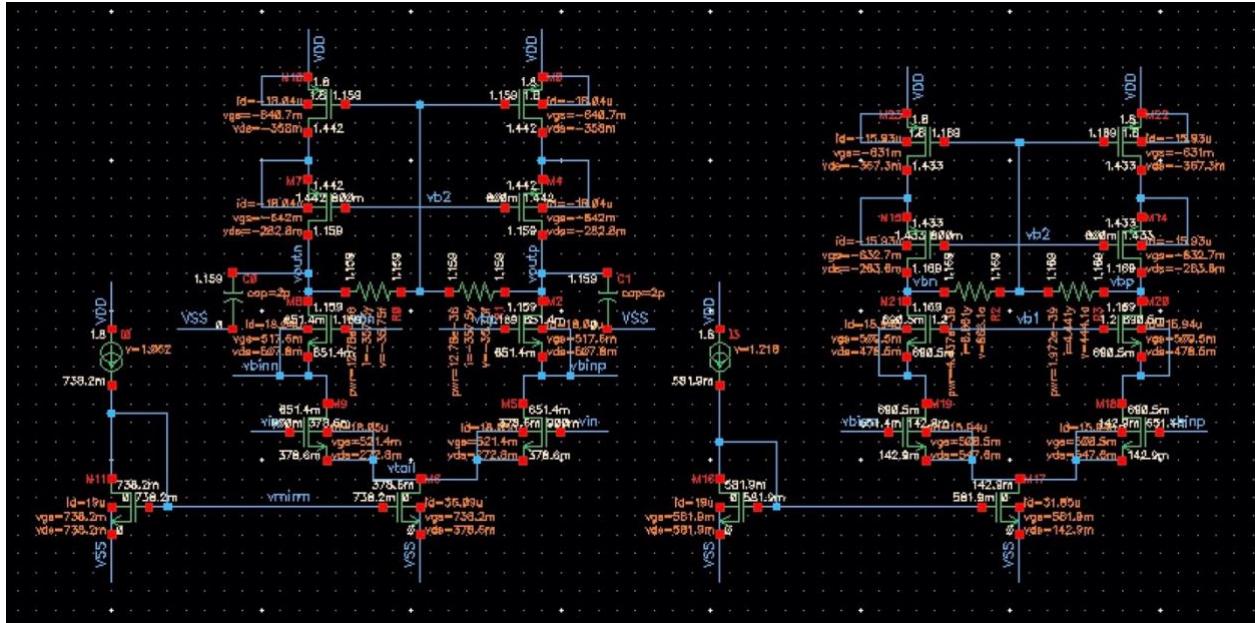
Fig. 7: DC Analysis of Gain-Boosting Differential Amplifier

Design a simpler Gain-Boosting Auxiliary amplifier without the cascode transistors and re-do the simulations

Frequency Response using AC Analysis

Repeat the AC Analysis steps. Run the simulation and plot the frequency response. Verify the DC gain and the Unity Gain Bandwidth.
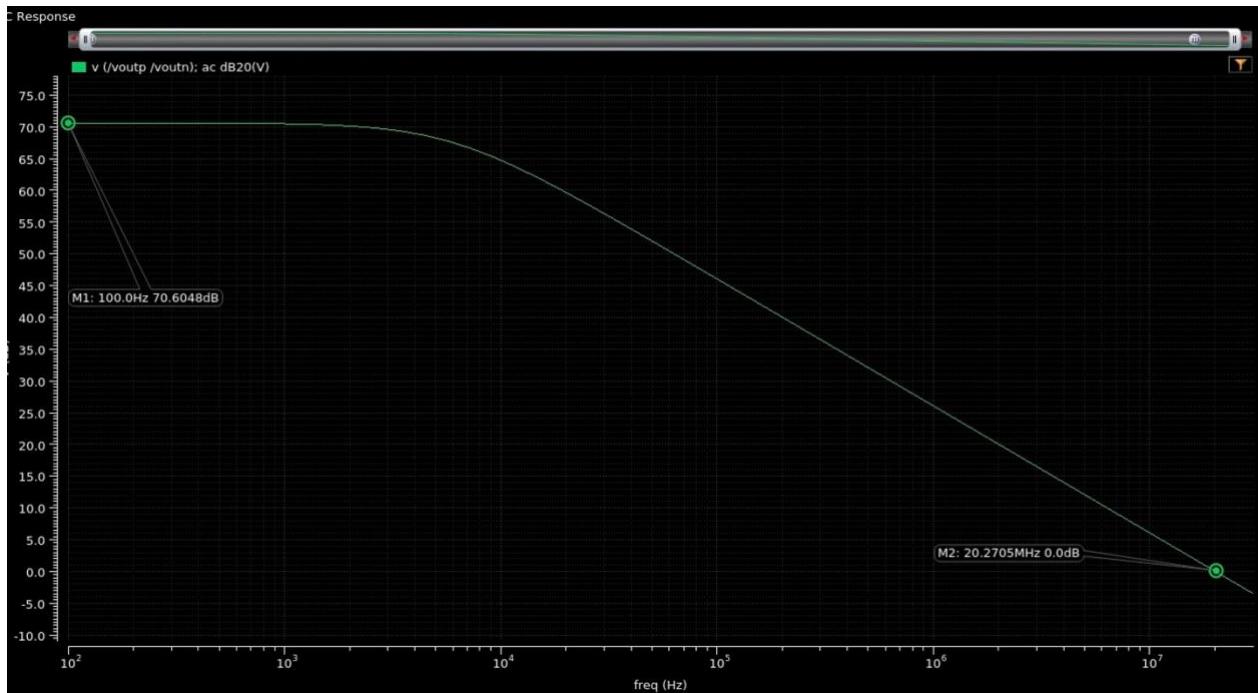

Fig. 8: AC Analysis of the Fully Differential Amplifier with Gain-Boosting

Noise Simulation using Noise Analysis

In the maestro window, you could add the noise analysis with the following setup to simulate the noise spectral density of the amplifier.
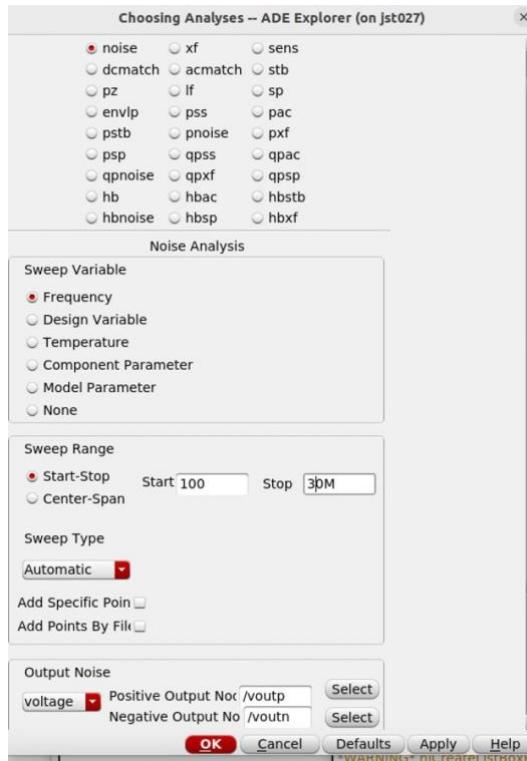
After running the simulation, you could plot the noise spectral density by *clicking* **Results>Direct Plot>Main Form** and setting up the Direct Plot Form as shown below*. Click Plot.*
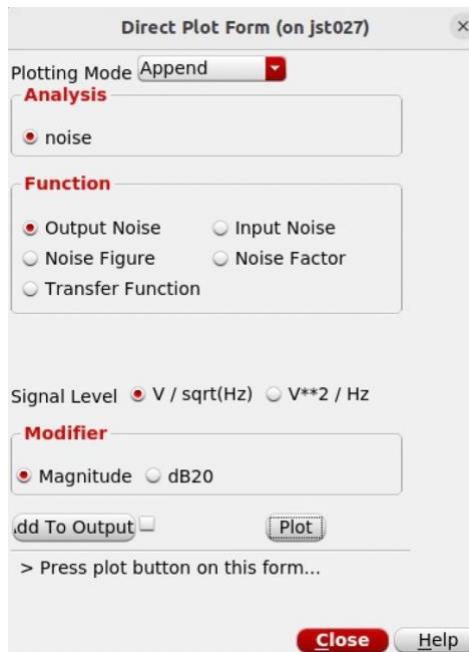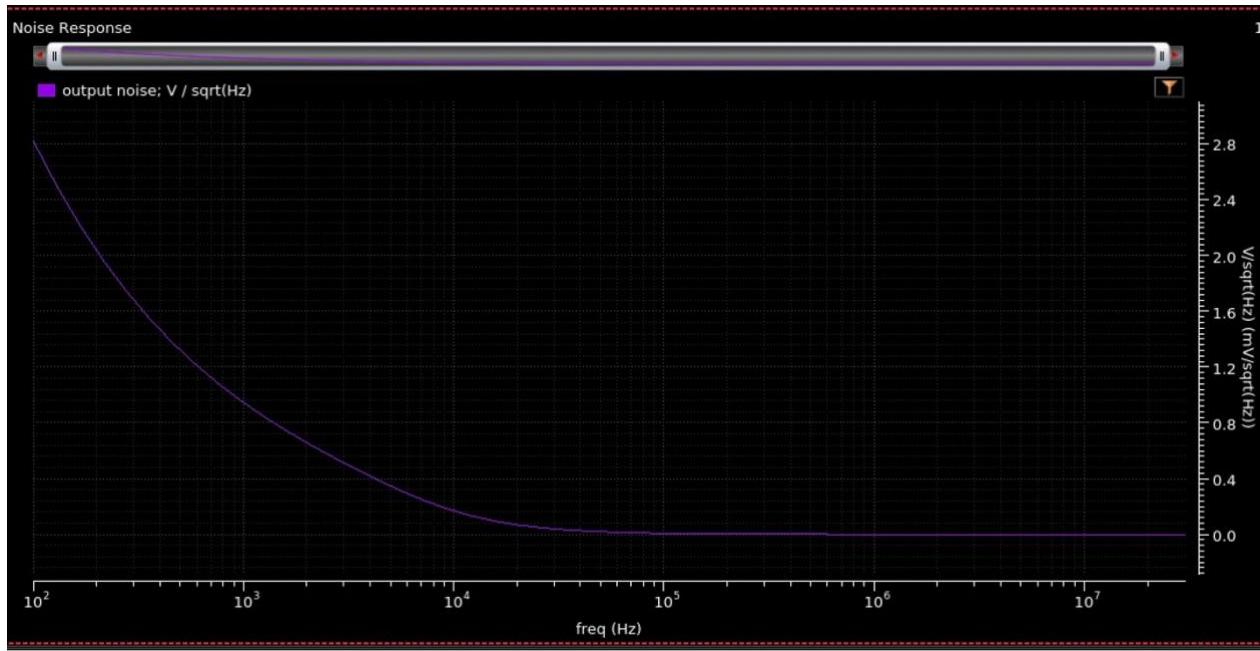
Fig. 9: Noise Simulation of the Fully Differential Amplifier with Gain Boosting

Common Mode Rejection Ratio (CMRR) Simulation

For the CMRR simulation, we assume +/- 1% mismatch for the input transistors of the amplifier. The mismatch could be added by changing the width of the input as shown in the figure below.
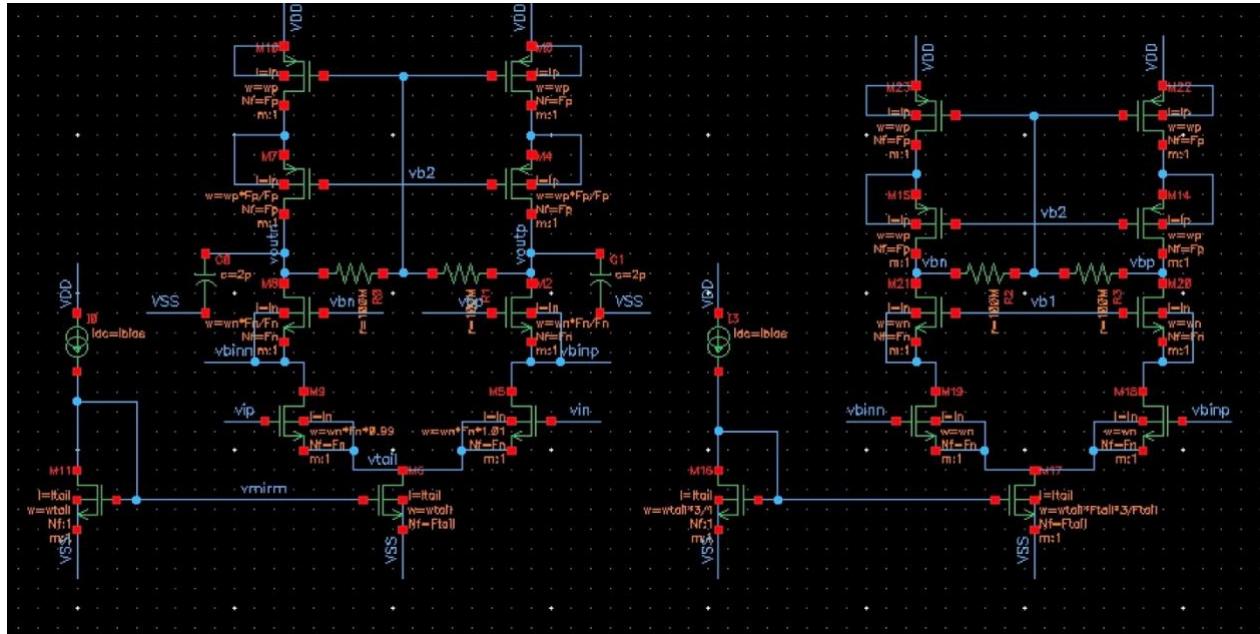
Fig. 10: Schematic of the differential amplifier with 1% mismatch in input transistors

To simulate the CMRR of the amplifier, only the common mode input should be applied to the input transistors. By measuring the output gain, we could get the CMRR. You could set the ac magnitude to 1 for both of the inputs and run the ac analysis using the same way as measuring the gain of differential amplifier. The CMRR result could be viewed by measuring the ac magnitude of the differential output (same way as measuring the gain of the amplifier). The CMRR could be calculated by $20\log_{10}(A_{DM}/A_{CM})$, which is around 103dB.
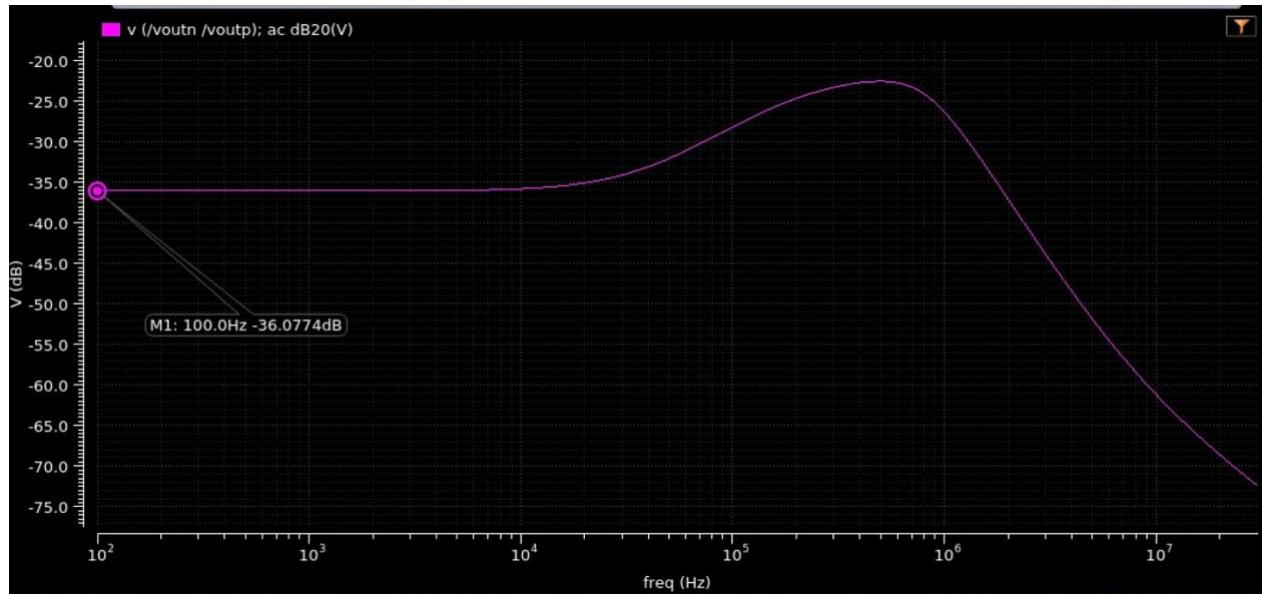

Fig. 11: Common - Mode Gain Plot

Power Supply Rejection Ratio (PSRR) Simulation

The PSRR is defined by the voltage change in power supply divided by the voltage change in the output.

$$PSRR = 20\log_{10}(A_{DM} * \frac{\Delta VDD}{\Delta Vout})$$

To simulate the PSRR of the amplifier, you need to deactivate all the inputs and applied the ac magnitude to the supply voltage (VDD). Set the ac magnitude of the inputs to 0 and the ac magnitude of the VDD to 1. Run the ac analysis using the same as measuring the gain of differential amplifier. The $20\log10(\frac{\Delta Vout}{\Delta VDD})$ result could be viewed by measuring the ac magnitude of the differential output (same way as measuring the gain of the amplifier). The PSRR of the amplifier is around 68.5dB.
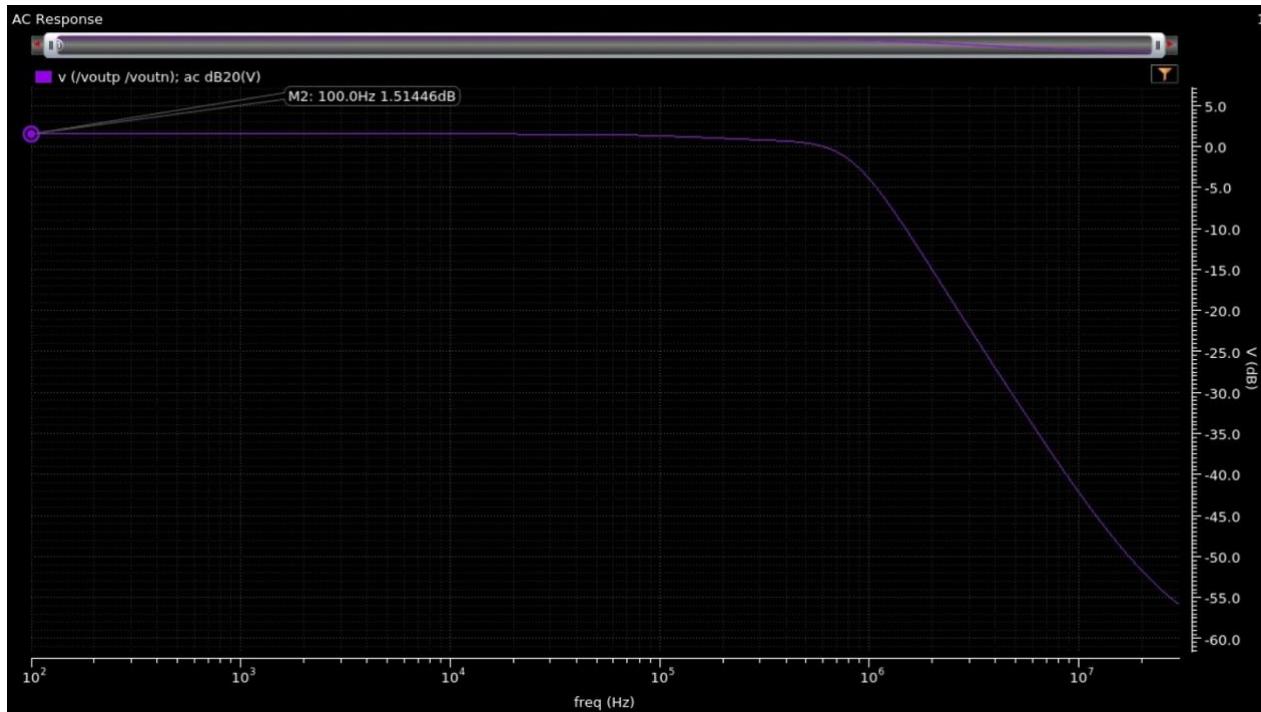
Fig. 12: Plot of $20\log10(\frac{\Delta Vout}{\Delta VDD})$