EE-523 ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN TP-2025

PRACTICAL EXERCISE SESSION No. 2

Note: For students connecting virtually, the details of the Zoom Meeting for this TP session are given below

Topic: Advanced Analog IC Design Zoom Meeting

Time: March 14, 2025 01:00 PM Amsterdam, Berlin, Rome, Stockholm, Vienna

Join Zoom Meeting:

https://epfl.zoom.us/j/66887254608?pwd=MBLOAjyTb7PaR02tNUeDaHDb1q5WID.1

Meeting ID: 668 8725 4608

Passcode: 191600

Objectives of this Practical Exercise Session

1. Design and simulate a cascode op amp:
    a) Following the design procedures, design a cascode op amp that meets the given set of specifications.
    b) Perform DC Analysis for DC operating point.
    c) Perform AC Analysis for frequency response.
    d) Perform Transient Analysis with the unity-gain buffer configuration.

2. Design and simulate a two-stage op amp:
    a) Following the design procedures, design a two-stage op amp that meets the given set of specifications.
    b) Perform DC Analysis for DC operating point.
    c) Perform AC Analysis for frequency response.
    d) Perform Transient Analysis for output swing observation

TIP OF THE DAY: Save your work frequently

1. Design and Simulate a Cascode op amp

Design Specification

- DC Gain (A_V) > 65 dB ≈ 1800 V/V
- Unity Gain Bandwidth (UGB) > 20MHz
- Output Load Capacitance (C_L) = 2pF
- $V_{OUT, DC}$ ≈ 1.15 V
- $V_{IN, DC}$ = 0.9 V
- V_{DD} = 1.8 V

Hand Calculation

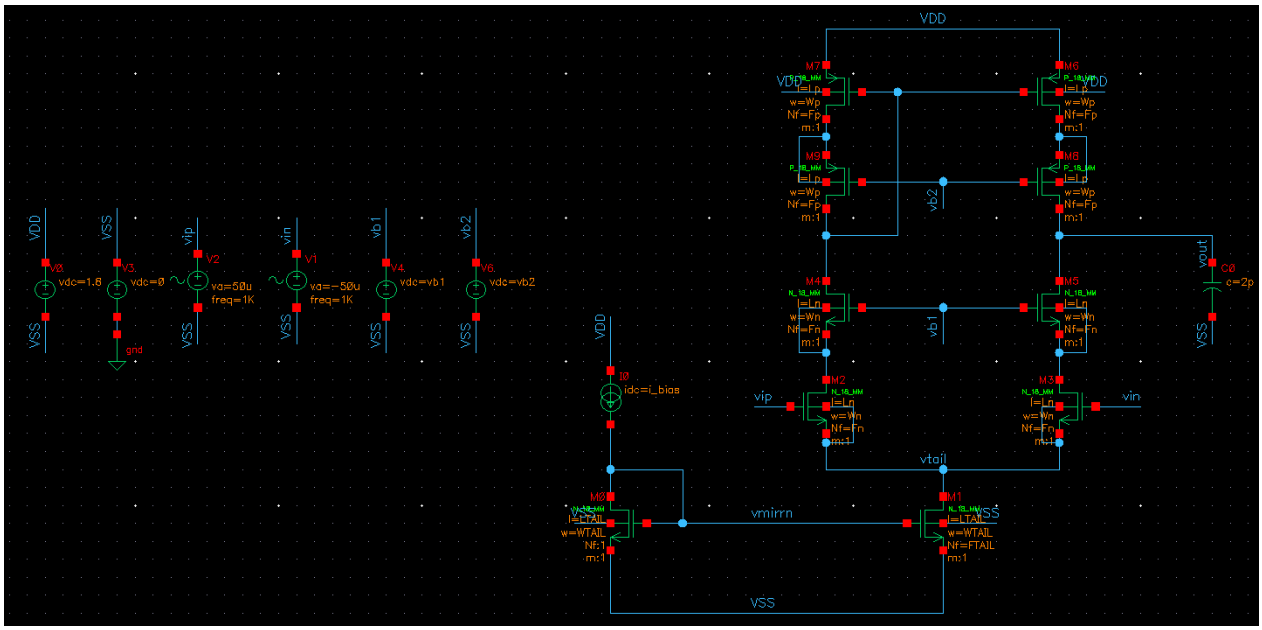


Fig. 1. Schematic of the Cascode op amp

The circuit schematic is shown in Fig. 1. For simplicity, please connect the body terminals of transistors to their source terminals. We also suggest to group M0-M1, M2-M5, as well as M6-M9. Transistors in the same group have the same Finger Width, Length, and Finger Number (Note that the current mirror M0 and M1 have Finger Number of 1 and FTAIL, respectively), as shown in Fig. 1

Work out the sizes for each transistor, and the biasing current/voltages by writing out the square-law equations or if you are familiar with any of the design methodologies like gm/ID or Inversion Coefficient (IC), please feel free to use them.

For hand calculations, $\mu_n C_{ox}$ = 278 μA/V², $V_{TH, N}$ = 0.4 V, μpCox = 61 μA/V², $|V_{TH, P}|$ = 0.54V.

Overall, we have the following parameters to achieve the required specifications. Here I_X denotes the current, L_X the channel length, W_X the width, F_X the number of fingers, V_{b1} and V_{b2} the biasing voltages.

I_{BIAS}	L_{TAIL}	W_{TAIL}	F_{TAIL}	L_n	W_n	F_n	L_p	W_p	F_p	V_{b1}	V_{b2}

We use g_m/I_D methodology to determine the sizing of transistors. Based on the specifications, we have:

$$UGB = \frac{g_{mn}}{2\pi C_L} > 20\ MHz \rightarrow g_{mn} > 251.2\ \mu S \quad (1)$$

$$A_v = g_{mn}(g_{mn}r_{oN}^2 // g_{mp}r_{oP}^2) \approx \frac{1}{2}g_{mn}^2 r_{oN}^2 > 1800 \rightarrow g_{mn}r_{oN} > 60 \text{ (assume } g_{mn}r_{oN}^2 \approx g_{mp}r_{oP}^2) \quad (2)$$

$$V_{ov6} = V_{OUT,DC} - V_{DD} - V_{TH,P} = 1.15 - 1.80 - (-0.54) = -0.11\ V \quad (3)$$

The first step is to choose the length of transistor. We plot the $g_{mn}r_{oN}$ as a function of V_{ov} for different values of L_n, as shown in Fig. 2. Considering some margins (65~75 for $g_{mn}r_{oN}$) and moderate inversion operations (**g_m/I_D in the range of 12-16, and V_{ov} ~ 0.1 V for the amplifying transistors in this technology**), L_n = 720 nm was chosen for our initial trial.

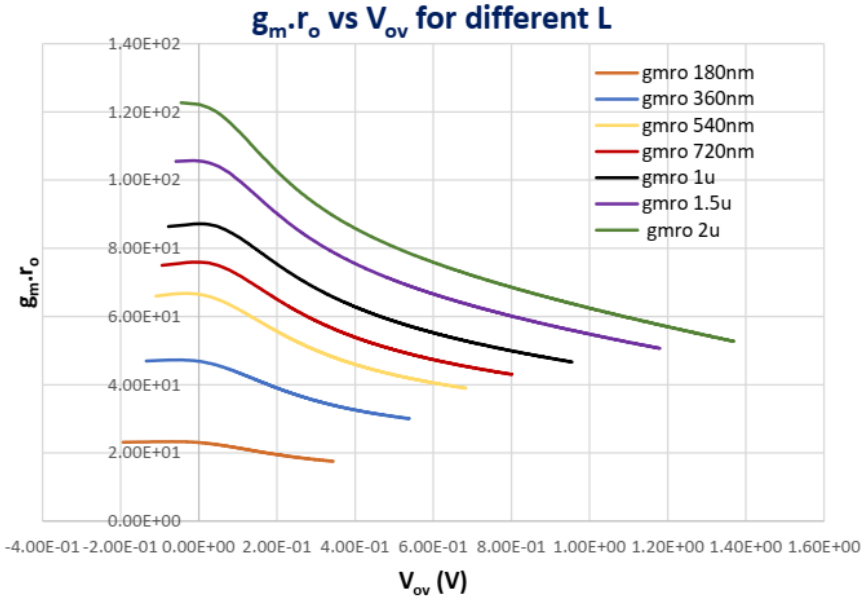


Fig. 2. $g_{mN}r_{oN}$ as a function of V_{ov} under different L_n

In the Excel sheet of **L_n = 720 nm**, we identify the following point, where $g_m r_o$ = 72.2, g_m/I_D = 13.7, and V_{OV} ≈ 0.1 V. That seems a nice point to start with.

1	L 720nm	Vov 720nm	gm 720nm	ID 720nm	gm/ID 720nm	gmro 720nm	ID/W 720nm	gm/W 720nm	gm/Cgg 720n	1/(ID.ro) 720nm	VDSAT 720nm	W 720nm	ro 720nm	Cgg 720nm	gds 720nm
30	7.20E-07	1.01E-01	3.91E-05	2.85E-06	1.37E+01	7.22E+01	2.85E+00	3.91E+01	7.73E+09	1.90E-01	1.22E-01	1.00E-06	1.85E+06	5.06E-15	5.41E-07

Let's further calculate the required I_D and tail current I_{TAIL}. According to the identified g_m/I_D and (1), we have: I_D > 251.2/13.7 = 18.3 μA (rounding up to 19 μA), I_{TAIL} = 2 * I_D = 38 μA. How about the width? Since I_D/W = 2.85, the total width of NMOS is derived as 19/2.85 = 6.7 μm (**W_n = 1μm, F_n = 7**).

Now we move to the sizing of PMOS transistors. **L_p = 360 nm** is chosen because it generally provides higher $g_m r_o$ (up to 100+). According to (3), we identify the following point in the Excel sheet of L_p = 360 nm, where V_{OV} ≈ -0.11 V, g_m/I_D = 12.7. Since I_D/W = 1.55, the total width of PMOS is derived as 19/1.55 = 12.3 μm (**W_p = 1μm, F_p = 12**).

1	L 360nm	Vov 360nm	gm 360nm	ID 360nm	gm/ID 360nm	gmro 360nm	ID/W 360nm	gm/W 360nm	gm/Cgg 360nm	1/(ID.ro) 360nm	VDSAT 360nm	W 360nm	ro 360nm	Cgg 360nm	gds 360nm
17	3.60E-07	-1.05E-01	1.97E-05	1.55E-06	1.27E+01	9.82E+01	1.55E+00	1.97E+01	7.73E+09	1.29E-01	-1.46E-01	1.00E-06	4.99E+06	2.54E-15	2.00E-07

As for the current mirror transistors M0-M1, the length could be the same as L_n, while we choose W_{TAIL} based on the V_{ov}. Typically, for current mirror, the g_m/I_D does not need to be high for reduced noise, which limits V_{OV} to be a bit less than 300 mV. We identify the following point, where $V_{ov} \approx 0.29$ V and $g_m/I_D = 6.1$. $I_{TAIL}/W = 16.5$. Therefore, the total width of the tail transistor is derived as 38/16.5 = 2.3 μm **(W_{TAIL} = 1μm, F_{TAIL} = 2)**, and **$I_{BIAS} = I_{TAIL}/F_{TAIL}$ = 19 μA.**

	L 720nm	Vov 720nm	gm 720nm	ID 720nm	gm/ID 720nm	gmro 720nm	ID/W 720nm	gm/W 720nm	gm/Cgg 720n	1/(ID.ro) 720nm	VDSAT 720nm	W 720nm	ro 720nm	Cgg 720nm	gds 720nm
166	7.20E-07	2.92E-01	1.00E-04	1.65E-05	6.09E+00	5.92E+01	1.65E+01	1.00E+02	1.95E+10	1.03E-01	2.58E-01	1.00E-06	5.91E+05	5.13E-15	1.69E-06

There are allowable ranges for the biasing voltage V_{b1} and V_{b2}. In this case, $V_{OV1} + V_{OV3} + V_{OV5} + V_{THN} < V_{b1} < V_{OUT,DC} + V_{THN}$ → 0.9 V < V_{b1} < 1.55 V, and $V_{OUT,DC} - |V_{THP}| < V_{b2} < V_{DD} - |V_{OV6}| - |V_{OV8}| - |V_{THP}|$ → 0.61V < V_{b2} < 1.04 V. We may set V_{b1} = 1.2 V and V_{b2} = 0.8 V for our first trial. With DC analysis, we can revisit the biasing voltages to ensure similar V_{DS} across the cascode transistors, which helps maximize the gain.

I_{BIAS}	L_{TAIL}	W_{TAIL}	F_{TAIL}	L_n	W_n	F_n	L_p	W_p	F_p	V_{b1}	V_{b2}
19 μA	720 nm	1 μm	2	720 nm	1 μm	7	360 nm	1 μm	12	1.2	0.8

Building the Schematic

The way of building the schematic is the same as the FIVE_PACK_OTA example demonstrated in TP1. Here are a few points to help you quickly create the schematic shown in Fig. 1.

- Create new cellview in the library manager and select “Schematic”.
- Choose “N_18_MM” and “P_18_MM” in the UMC_18_CMOS library for transistors.
- Choose “vsin” in the analogLib library for vip/vin input sources. The DC voltage should be 900 mV.
- Press “i” to add instances.
- Press “q” to bring the “Properties” dialogue.
- Press “w” for wiring connection of all components.
- Press “l” (the lowercase L) to label the nets.
- Press “Shift+x” to check and save your schematic.

DC Operating Point using DC Analysis

The way of creating the simulation window is the same as the FIVE_PACK_OTA example demonstrated in TP1. Here are a few points to help you start the simulation.

- On your schematic window, click **Launch>ADE Explorer**. Select **Create New View**. Keep the View as **maestro**, select **Open in new tab**, and press OK.
- Click on “**Click to add analysis”**. Choose dc analysis, and don’t forget to check the **“Save DC Operating Point”** box.

- Below the Design Variables, click on Click to add variable. Select **"Copy from Cellview"**. Then fill in the variables derived from the hand calculation above.
- Click on the **green play button (** **)** to run the simulation.

After running the simulation, click **Results>Annotate>DC node voltages / DC operating points**. This will annotate DC node voltages / DC operating points on your schematic. Check the voltage and currents. Make sure they are close to the desired values. You can also click **Results>Print>DC Operating point** to check the small-signal variables of each transistor.

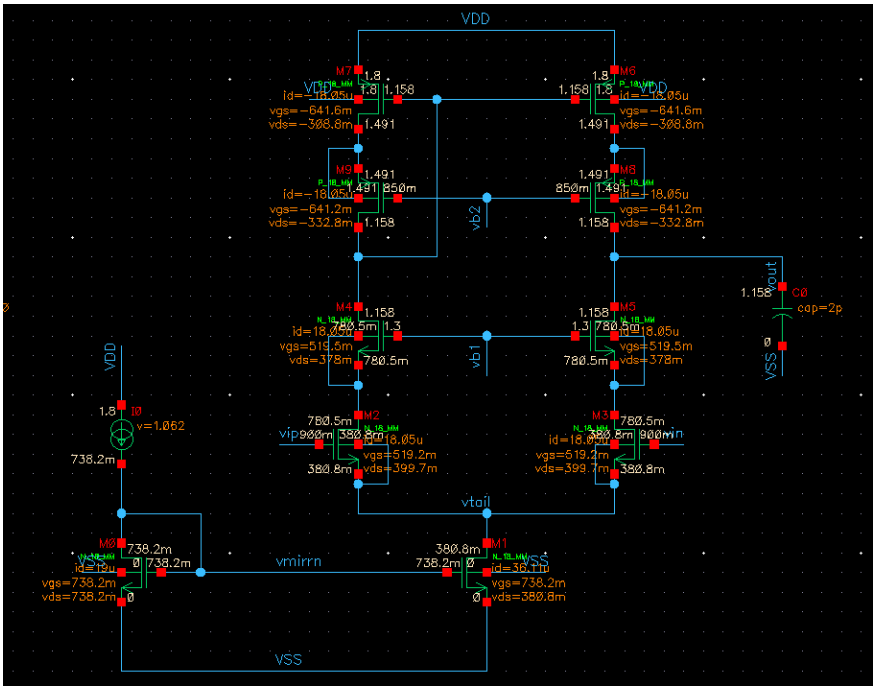
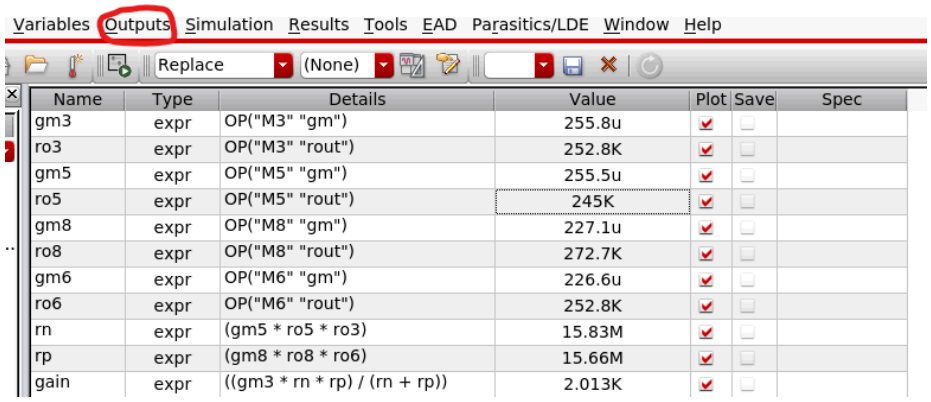


Fig. 3. Annotation of DC node voltages / DC operating points

Verify the DC operating point for all the transistors in the design.

Tip: *Here, we introduce a new way of saving the small signal variables by clicking* ***Outputs>Add>Expression****. Type the expressions listed in Fig. 4 so that you can quickly verify the small-signal variables (such as g_m and r_o) and DC gain after each simulation run.*



Name	Type	Details	Value	Plot	Save	Spec
gm3	expr	OP("M3" "gm")	255.8u	☑	☐	
ro3	expr	OP("M3" "rout")	252.8K	☑	☐	
gm5	expr	OP("M5" "gm")	255.5u	☑	☐	
ro5	expr	OP("M5" "rout")	245K	☑	☐	
gm8	expr	OP("M8" "gm")	227.1u	☑	☐	
ro8	expr	OP("M8" "rout")	272.7K	☑	☐	
gm6	expr	OP("M6" "gm")	226.6u	☑	☐	
ro6	expr	OP("M6" "rout")	252.8K	☑	☐	
rn	expr	(gm5 * ro5 * ro3)	15.83M	☑	☐	
rp	expr	(gm8 * ro8 * ro6)	15.66M	☑	☐	
gain	expr	((gm3 * rn * rp) / (rn + rp))	2.013K	☑	☐	

Fig. 4. Expressions of small-signal variables and DC-gain calculation

Frequency Response using AC Analysis

In order to verify the Unity Gain Bandwidth (UGB) specification, we perform the AC analysis. Similar to TP1, we click on **"Click to add analysis"**, choose ac, and setup the form as shown in Fig. 5.

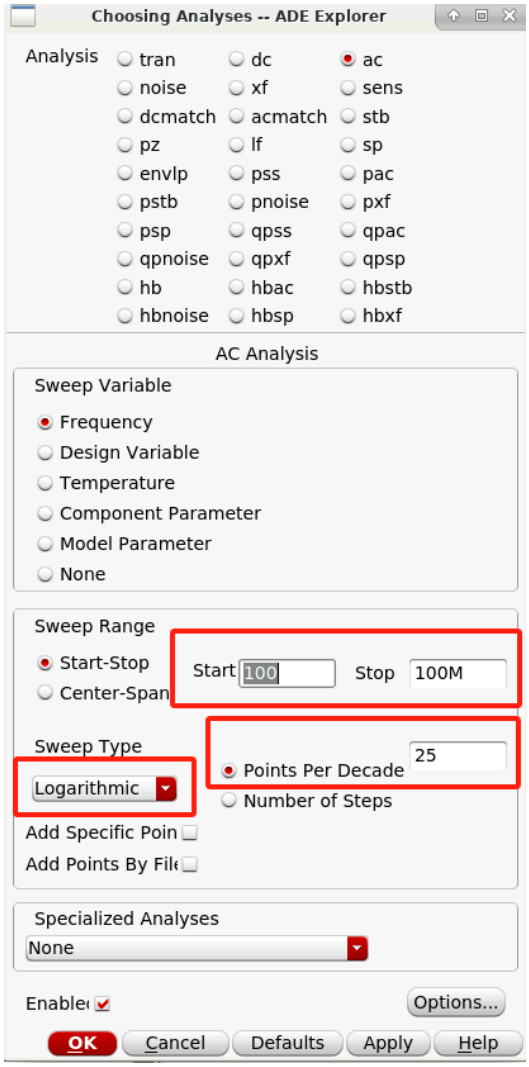
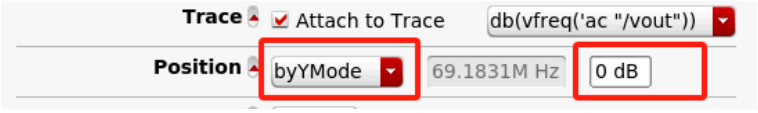


Fig. 5. AC Analysis setup

Tip: *To view the simulation results, as introduced in TP1, click* ***Results>Direct Plot>Main Form*** *and select vout in your schematic. You can also use* ***Outputs>Add>Expression*** *and type the expression as follows, which will plot the AC magnitude (in dB) frequency response after each simulation run, as shown in Fig. 6.*

Tip: *To create the marker as shown in Fig. 6, press "m", and move the marker to where you want. To identify the UGB point, double click the marker, choose "by YMode" and type "0 dB" in the "Position", so that the frequency point with 0 dB magnitude (UGB) is identified.*



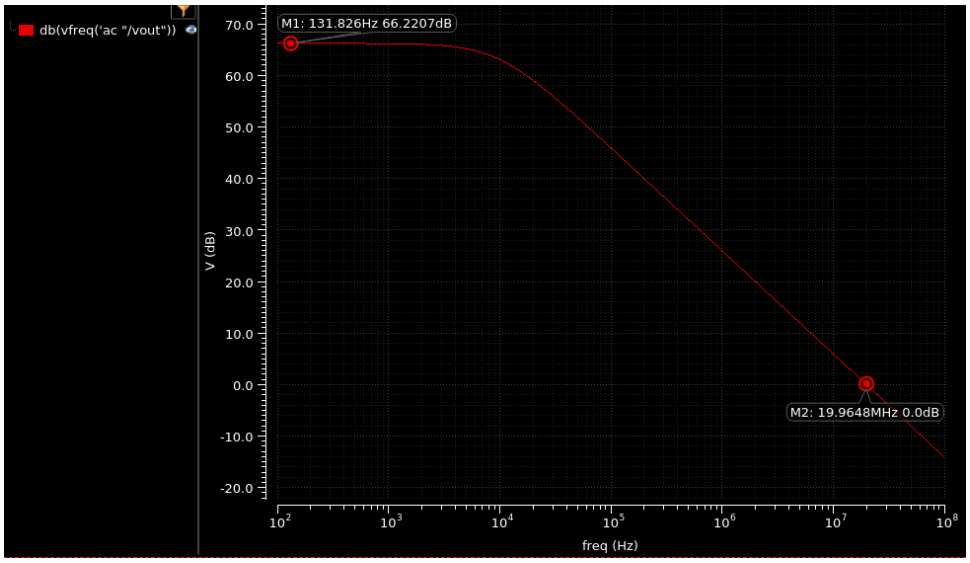


Fig. 6. Frequency response of vout AC magnitude

Verify if the DC gain and UGB meet design specifications in the design. Little deviations from the required specifications are acceptable, as long as you understand how to fix it 😊

Unity-gain buffer configuration with Transient Analysis

A high-gain op amp is commonly used as a unity-gain buffer. To do that, please short the vout and vin terminals, as shown in Fig. 7. However, as mentioned in Lecture-2-Slide page-6, it is difficult to use a cascode op amp as a unity-gain buffer due to the limited output swing. In our case, $(V_{b1} - V_{TH,N}) < V_{OUT} < (V_{b1} - V_{OV5})$, $V_{b1} = 1.3$ V, thereby 0.9 V < V_{OUT} < 1.2 V

To visually check it, we will perform a Transient Analysis. Click on **"Click to Add Analysis"** and fill in the transient simulation form as shown in Fig. 7. Also modify the swing of vip to a bit out of the boundary. For example, change the DC voltage as 1.1 V and Amplitude as 0.3 V, so that we get 0.8 ~ 1.4 V of vip.

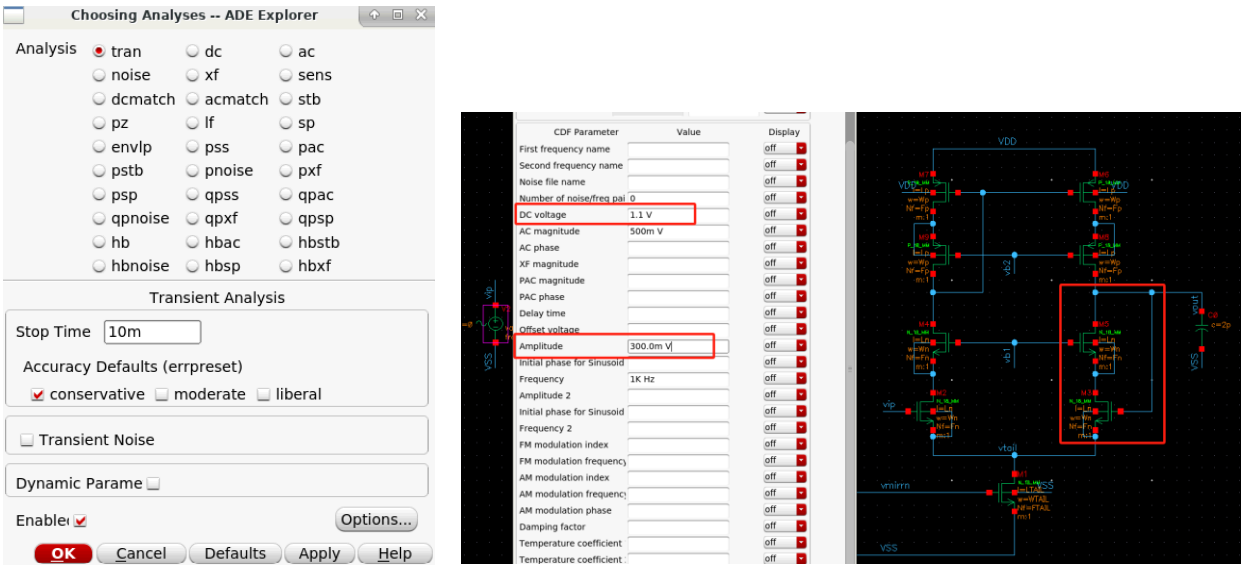


Fig. 7. Transient Analysis setup and unity-gain buffer configuration

To plot the waveforms, select **Results>Direct Plot>Main Form**, and select **"Differential Nets"** and **"Net"** for plotting (vip-vin) and vout, respectively. Again, you can also click **Outputs>Add>Signal** to bring out the waveforms after each simulation run.

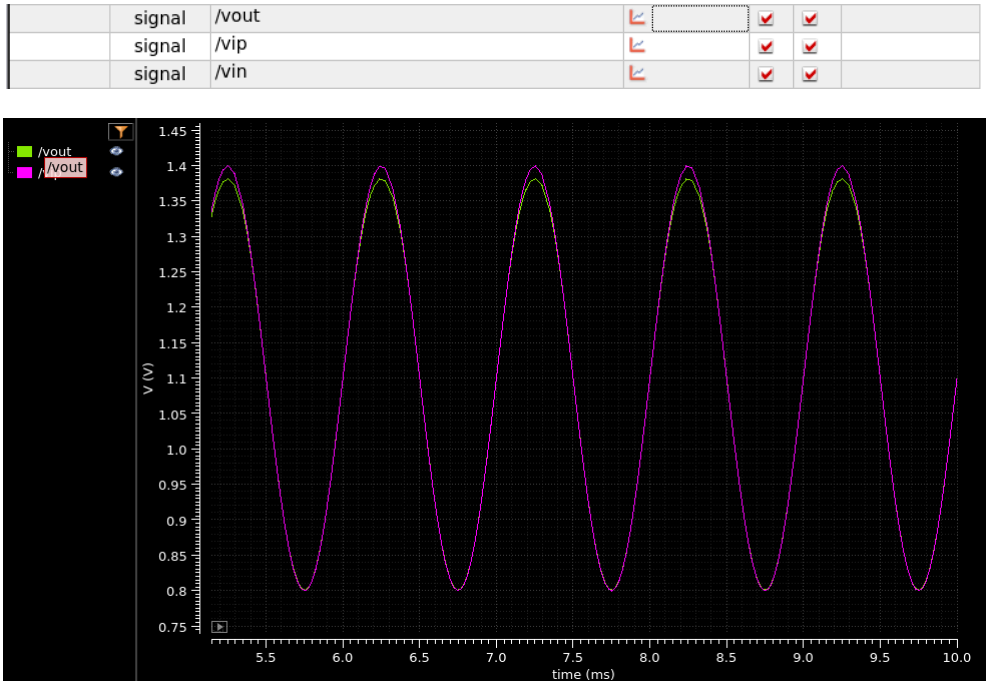


Fig. 8. Transient waveforms as a unity-gain buffer

It is not quite obvious to check if vout closely follows vip from the transient waveforms. You can perform DC simulation at $V_{IN,DC}$ = 0.8 V, 1.1 V, and 1.4 V, respectively, and check if the cascode transistors are all in the saturation region. An example is shown in Fig. 9.

	expr	OP("M3" "region")	1	☑	☐
	expr	OP("M5" "region")	2	☑	☐
	expr	OP("M6" "region")	2	☑	☐
	expr	OP("M8" "region")	1	☑	☐

Fig. 9. M3 and M8 are in linear region when $V_{IN,DC}$ = 1.4 V (0: Cut-off region, 1: Linear region, 2: Saturation region).

2. Design and Simulate a Two-Stage op amp

Design Specifications

- DC Gain (A_V) > 61 dB ≈ 1200 V/V
- Output Load Capacitance (C_L) = 2pF
- V_{DD} = 1.8 V
- $V_{IN,\,DC}$ = 1.0 V
- Output Swing > 1.2 V
- Unity Gain Bandwidth (UGB) > 20MHz

Hand Calculation

The circuit schematic is shown in Fig. 10. For stability considerations, we put an additional compensation capacitance (C_c) of 2 pF, which leads to UGB = g_{mn3} / (2*π*C_c). Besides, it is suggested that g_{mp6} / C_L ≈ 3 *

g_{mn3} / C_c (also for stability). Since the topics of stability and frequency compensation are not covered in the lectures, feel free to check Chapter 10.2-10.3, 10.5 of *Razavi, "Design of Analog CMOS Integrated Circuits"* if you are interested. It is fine to simply use the conclusions above in this TP. 😄

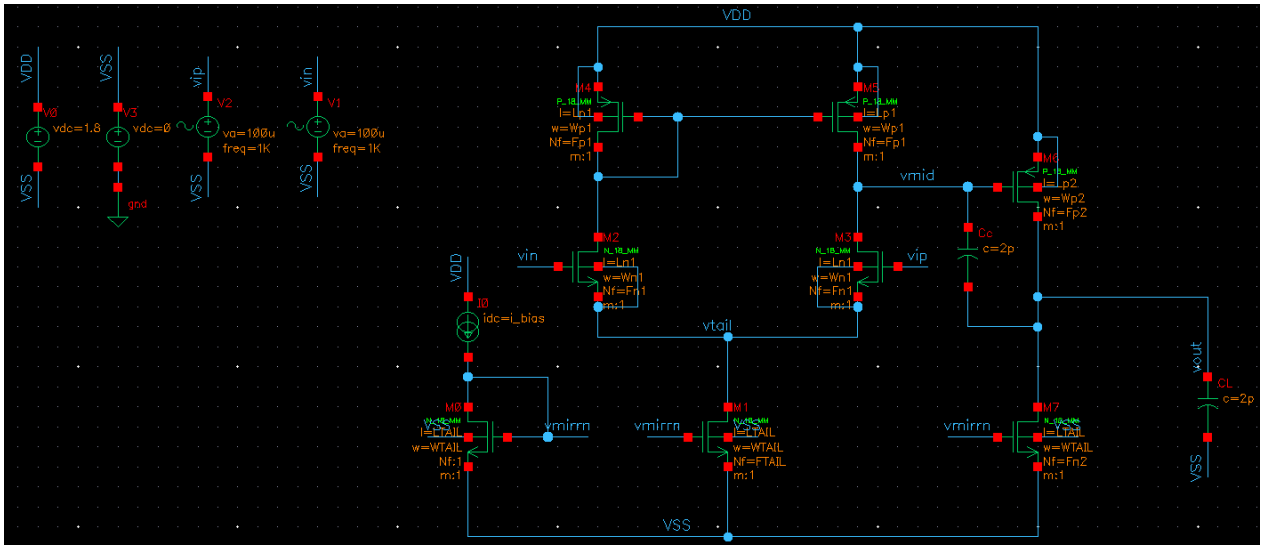


Fig. 10. Schematic of the two-stage op amp

For simplicity, we will directly re-use the FIVE_PACK_OTA of TP1 as the first stage, with the circuit parameters and specifications listed below. Firstly, the FIVE_PACK_OTA provides >40 V/V DC gain, leaving ~30 V/V DC gain for the second stage. Secondly, to achieve the output swing requirements, we allocate an overdrive voltage of ~0.3 V to M6 and M7 each, and luckily, $|V_{OV6}| = |V_{MID,DC} - V_{DD} - V_{TH,P}| = 0.26\ V < 0.3\ V$.

I_{BIAS}	L_{TAIL}	W_{TAIL}	F_{TAIL}	L_{n1}	W_{n1}	F_{n1}	L_{p1}	W_{p1}	F_{p1}
14 μA	720 nm	1 μm	3	720 nm	1 μm	6	360 nm	1 μm	3

Design specifications of FIVE_PACK_OTA:

- $V_{IN,\,DC}$ = 0.9 V
- $V_{OUT,\,DC}$ = 1.0 V
- DC gain ≈ 45
- Load C_L = 2 pF
- UGB = 20 MHz

Work out the sizes for the second stage by writing out the square-law equations or if you are familiar with any of the design methodologies like gm/ID or Inversion Coefficient (IC), please feel free to use them.

For hand calculations, $\mu_n C_{ox}$ = 278 μA/V², $V_{TH,\,N}$ = 0.4 V, μpCox = 61 μA/V², $|V_{TH,\,P}|$ = 0.54V.

Here we briefly demonstrate again how to use the g_m/I_D methodology to facilitate the sizing.

As mentioned before, $g_{mp6}/C_L \approx 3 * g_{mn3}/C_c$, thereby $g_{mp6} \approx 3 \times g_{mn3} = 3 \times 251.2\ \mu S = 753.6\ \mu S$.

According to V_{ov6} = -0.26 V, we identify the following point in the Excel sheet of L_p = 360 nm, where $g_m r_o$ = 59.4, which should be sufficient to provide ~30 V/V DC gain.

	L 360nm	Vov 360nm	gm 360nm	ID 360nm	gm/ID 360nm	gmro 360nm	ID/W 360nm	gm/W 360nm	gm/Cgg 360nm	1/(ID.ro) 360nm	VDSAT 360nm	W 360nm	ro 360nm	Cgg 360nm	gds 360nm
67	3.60E-07	-2.60E-01	4.28E-05	6.55E-06	6.54E+00	5.94E+01	6.55E+00	4.28E+01	1.64E+10	1.10E-01	-2.76E-01	1.00E-06	1.39E+06	2.62E-15	7.21E-07

$g_m/I_D = 6.54 \rightarrow I_{D6} = 115\ \mu A$.

$I_D/W = 6.55 \rightarrow$ Total width of M6 = 17.6 μm (W_{p2} = 1 μm, F_{p2} = 18).

$F_{n2} = I_{D6}/I_{BIAS} = 8$.

L_{p2}	W_{p2}	F_{p2}	F_{n2}
360 nm	1 μm	18	8

DC Operating Point using DC Analysis

Repeat the DC Analysis steps of casecode op amp. Run the simulation. Annotate the DC node voltages / DC operating points and check if they match the desired values. You can also use **Outputs>Add>Expression** to save small-signal variables and calculate the DC gain and the output swing.

gm3	expr	OP("M3" "gm")	259.3u	✓	
ro3	expr	OP("M3" "rout")	292.5K	✓	
ro5	expr	OP("M5" "rout")	455.5K	✓	
gm6	expr	OP("M6" "gm")	758.2u	✓	
ro6	expr	OP("M6" "rout")	61.66K	✓	
ro7	expr	OP("M7" "rout")	100.9K	✓	
ro0	expr	OP("M0" "rout")	653.1K	✓	
gain_1st	expr	((gm3 * ro3 * ro5) / (r...	46.19	✓	
gain_2nd	expr	((gm6 * ro6 * ro7) / (r...	29.02	✓	
gain	expr	(gain_1st * gain_2nd)	1.34K	✓	
vdsat7	expr	OP("M7" "vdsat")	243.3m	✓	
vdsat6	expr	OP("M6" "vdsat")	-278.3m	✓	
vout_swing	expr	((1.8 - vdsat7) + vdsa...	1.278	✓	

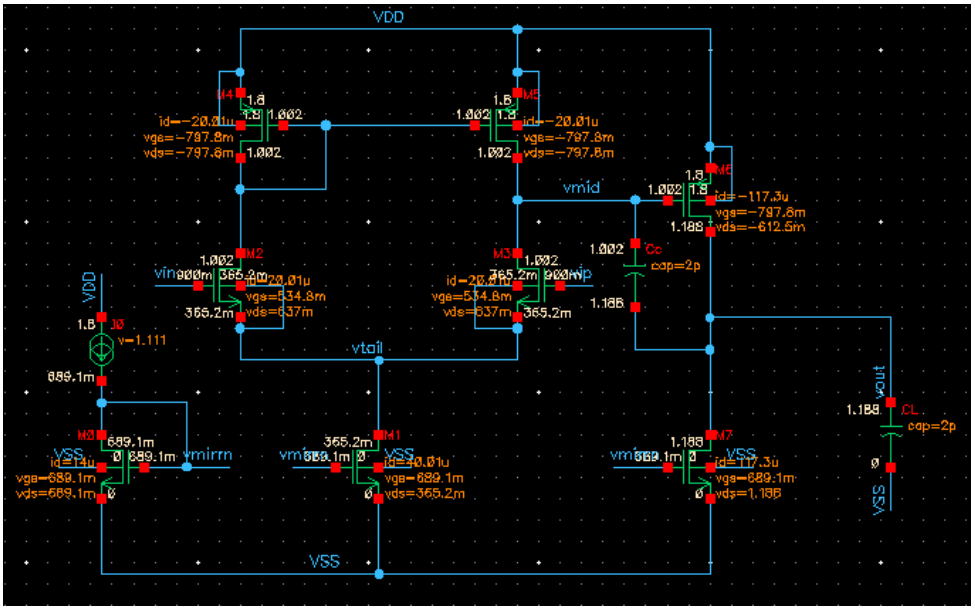


Fig. 11. DC Analysis of two-stage op amp

Frequency Response using AC Analysis

Repeat the AC Analysis steps. Run the simulation. Plot the frequency response of AC magnitude. Verify the DC gain and UGB.

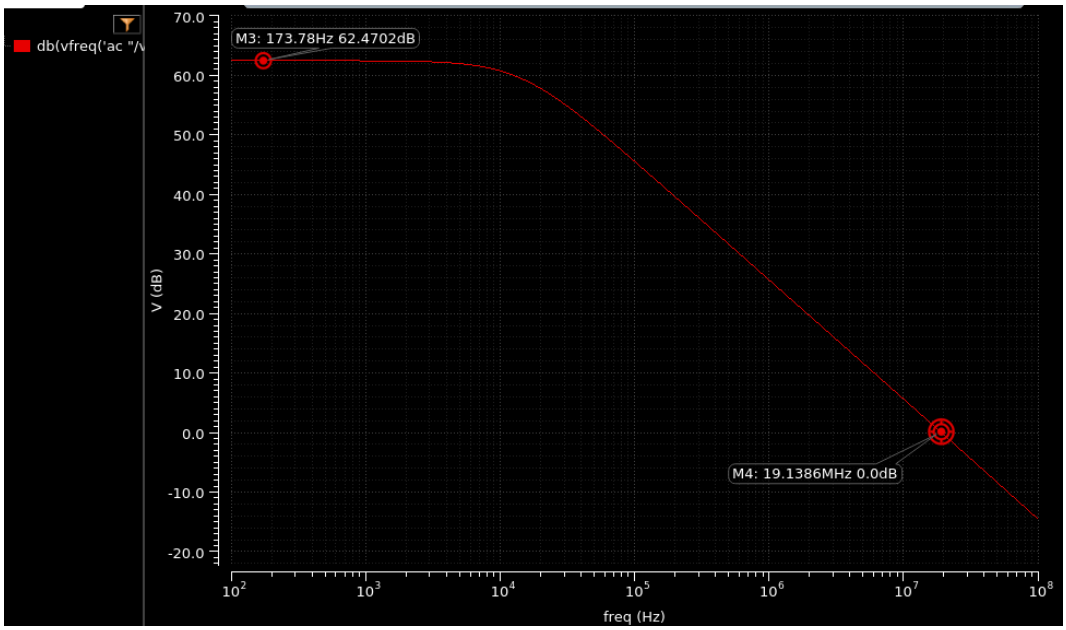


Fig. 12. AC Analysis of two-stage op amp (To improve UGB, you can reduce C_c a bit)

Output Swing Check using Transient Analysis

Verify if the output swing is greater than 1.2 V by performing Transient Analysis. How will you set the input DC voltage and Amplitude?