



# Advanced analog integrated circuit design (EE-523)

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## 2025 IEEE International Solid-State Circuits Conference (ISSCC)

### PAPER SESSIONS

1	Plenary - Invited Papers.....	16
2	Processors.....	18
3	Amplifiers and Analog Front-Ends.....	20
4	Analog Techniques.....	21
5	Front-End Circuits for High-Performance Transceivers.....	22
6	Imagers and Displays.....	24
7	Ultra-High-Speed Wireline.....	26
	<b>Demonstration Session 1.....</b>	<b>28</b>

### PAPER SESSIONS

8	Digital Techniques for System Adaptation, Power Management and Clocking.....	30
9	Ubiquitous Power Delivery.....	32
10	Transceiver Chipsets for Communications and Radar.....	34
11	RF and mm-Wave Wireless Receivers.....	35
12	Innovations from Outside the (ISSCC's) Box.....	36
13	Cool Computation Circuits.....	37
14	Compute-in-Memory.....	38
15	Neural Interfaces and Edge Intelligence for Medical Devices.....	40
16	Invited Industry.....	42
17	Hardware Security.....	43
18	Noise-Shaping and SAR-Based ADCs.....	44
19	Frequency Synthesizers and Series-Resonance VCOs.....	46
20	Sensors and Actuators for Health & Autonomy.....	48
21	Compute and USB Power.....	50
22	Memory Interface.....	52



## 2025 IEEE International Solid-State Circuits Conference (ISSCC)

### PAPER SESSIONS

23	AI-Accelerators.....	56
24	High-Frequency ADCs.....	58
25	High-Concepts at High Frequencies.....	60
26	Wireless Transmitters and Front-Ends.....	61
27	Sensor Interfaces.....	62
28	Capacitive Sensor Readout.....	63
29	SRAM.....	64
30	Nonvolatile Memory and DRAM.....	65
31	Energy Harvesting and IoT Transfer.....	66
32	Isolated Power and Gate Drivers.....	67
33	Components for Beyond 100GHz.....	68
34	Digital PLLs and Waveform Shaping.....	69
35	Implantable and Wearable Biomedical Devices.....	70
36	Ultra-High-Density D2D and High-Performance Optical Transceivers.....	72
37	Design-Technology Optimization and Digital Accelerators.....	74



## TUTORIALS

**8:30 AM**

- T1:** Low-Noise Current Sensing
- T2:** Fundamentals of DRAM I/O: Standards and Circuits
- T3:** Fundamentals of Cryo-CMOS Circuits and Systems for Quantum Computing

**10:30 AM**

- T4:** Fundamental Circuits for Nanopower and Energy-Harvesting Applications
- T5:** Fundamentals of RF System Analysis for IC Designers
- T6:** Front-End Circuit Design for High-Speed Optical Transceivers

**1:30 PM**

- T7:** High-Speed Analog-to-Digital Converters
- T8:** Intelligent Neural Interfaces: Fundamentals and Future Directions

**3:30 PM**

- T9:** Generative AI on Edge Devices: Models, Hardware and Systems
- T10:** mm-Wave Oscillator Design

## T8: Intelligent Neural Interfaces: Fundamentals and Future Directions

**Mahsa Shoaran**

*EPFL, Geneva, Switzerland*

In the past decade, there has been growing interest in developing AI-enabled neural interfaces for various neurological disorders and emerging brain-machine interface (BMI) applications. The focus has shifted from raw signal acquisition and data compression for off-body processing to intelligent systems featuring on-site signal processing, neural biomarker extraction, and AI. In this tutorial, I discuss the key characteristics, design trade-offs, and recent advances in CMOS-based systems-on-chip (SoCs) for diverse categories of intelligent neural prostheses. These categories include real-time symptom tracking and closed-loop stimulation, intelligent BMI systems for movement and communication recovery following paralysis, and beyond.

**Mahsa Shoaran** is currently a Tenure-Track Assistant Professor in Electrical and Micro Engineering and Neuro-X at EPFL and Director of the Integrated Neurotechnologies Laboratory. From 2017 to 2019, she was an Assistant Professor of ECE at Cornell University, following her Postdoctoral work in EE and MedE at Caltech (2015 to 2017). She received her PhD from EPFL in 2015 and her B.Sc. and M.Sc. degrees from Sharif University of Technology (2008, 2010). Dr. Shoaran is a recipient of the ERC Starting Grant (2021) and the Google AI Faculty Research Award in Machine Learning and Data Mining (2019). Her team received the IEEE SSCS-Brain Best Paper Award in 2022 for its work on NeuralTree. She was named a Rising Star in EECS at MIT in 2015. Her research focuses on low-power IC design for neural interfaces, machine-learning hardware, and neuromodulation therapies for neurological and psychiatric disorders. Dr. Shoaran serves or has served on the Technical Program Committee of the IEEE ISSCC and CICC, as an Associate Editor for IEEE TBioCAS, and on the ISSCC SRP committee.



# Today's schedule

- **This is a new course!**
- **We want to understand:**
  - Your prior knowledge in CMOS design
  - Your prior experience with actual IC design in Cadence Virtuoso
- **Today's schedule:**
  - Fill out a simple questionnaire
  - A short quiz (not for grading!)
- **Next week (Feb 28):**
  - The first lecture [\(1:15-2pm\) in INJ218](#)
  - The first TP session [\(2:15pm-4pm\) in BC07-08](#)
- **Important:** Complete the [EDA assignment for TP1](#) **by Feb 26<sup>th</sup>**

# ISSCC: The Art of Chip Design!



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