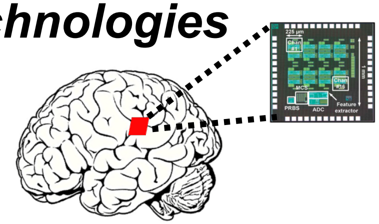
Integrated Neurotechnologies Laboratory

EPFL



Advanced analog integrated circuit design (EE-523), Lecture 6

Prof. Mahsa Shoaran

Institutes of Electrical and Micro Engineering and Neuro-X, School of Engineering, EPFL

Recap: Nonlinearity

- Two types of nonidealities: **nonlinearity and mismatch**

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$$

$$\begin{aligned} y(t) &= \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 \cos^3 \omega t + \cdots \\ &= \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2}[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3 \cos \omega t + \cos(3\omega t)] + \cdots \end{aligned}$$

$$\boxed{\mathrm{THD} = \frac{(\alpha_2 A^2/2)^2 + (\alpha_3 A^3/4)^2}{(\alpha_1 A + 3\alpha_3 A^3/4)^2}}$$

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- Two types of nonidealities: **nonlinearity and mismatch**

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$$

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$$= \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2}[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3 \cos \omega t + \cos(3\omega t)] + \cdots$$

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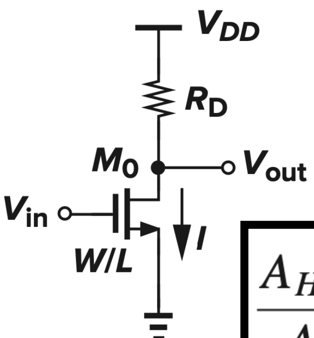
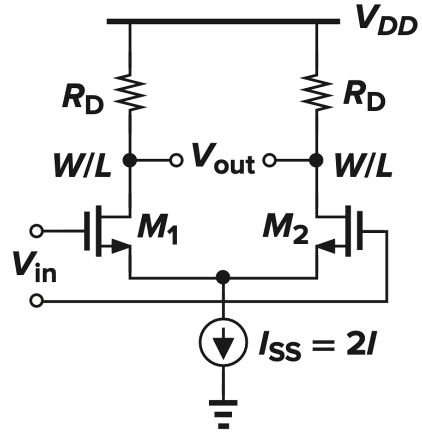


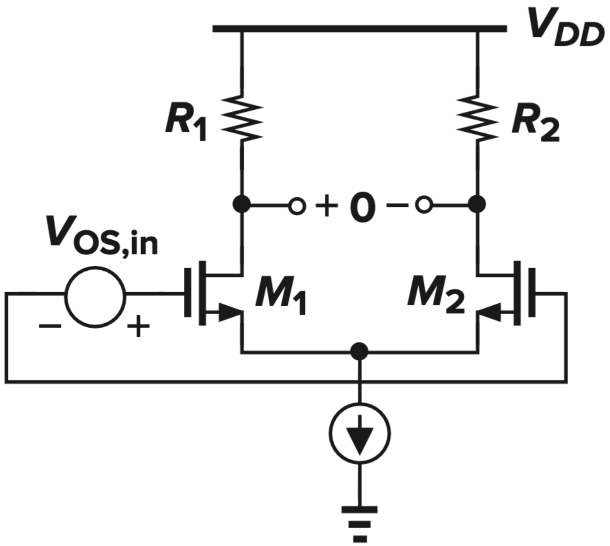
$$\frac{A_{HD2}}{A_F} = \frac{V_m}{4(V_{GS} - V_{TH})}$$



$$\frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2}$$

Recap: Mismatch

- Mismatch typically leads to 3 important effects: **dc offsets, even-order distortion, and lower common-mode rejection.**



$$V_{TH1} = V_{TH}, V_{TH2} = V_{TH} + \Delta V_{TH}$$

$$(W/L)_1 = W/L, (W/L)_2 = W/L + \Delta(W/L)$$

$$R_1 = R_D, R_2 = R_D + \Delta R$$

$$V_{OS,in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH}$$

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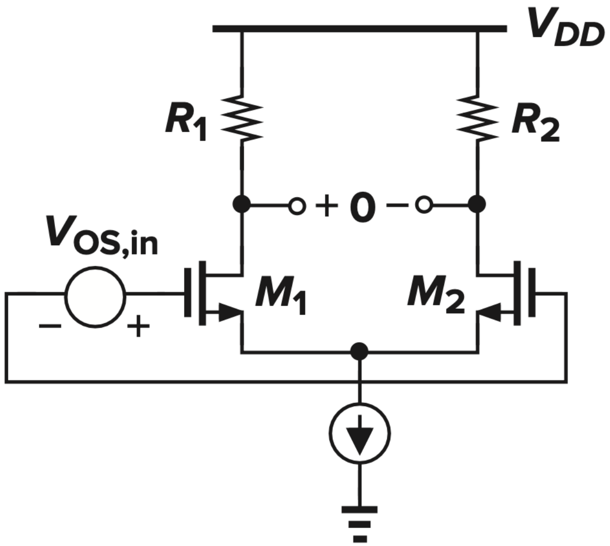

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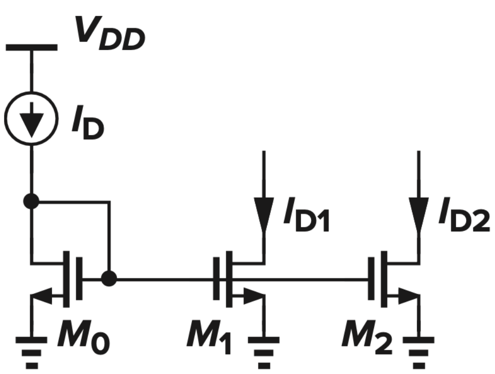


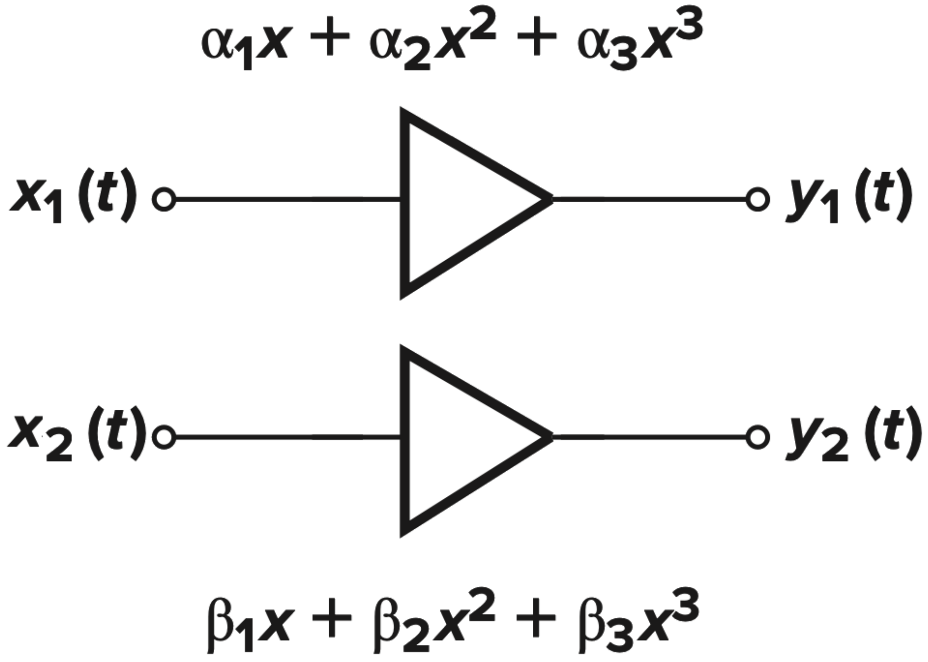
$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{W/L} - 2\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}$$

Even-Order Distortion

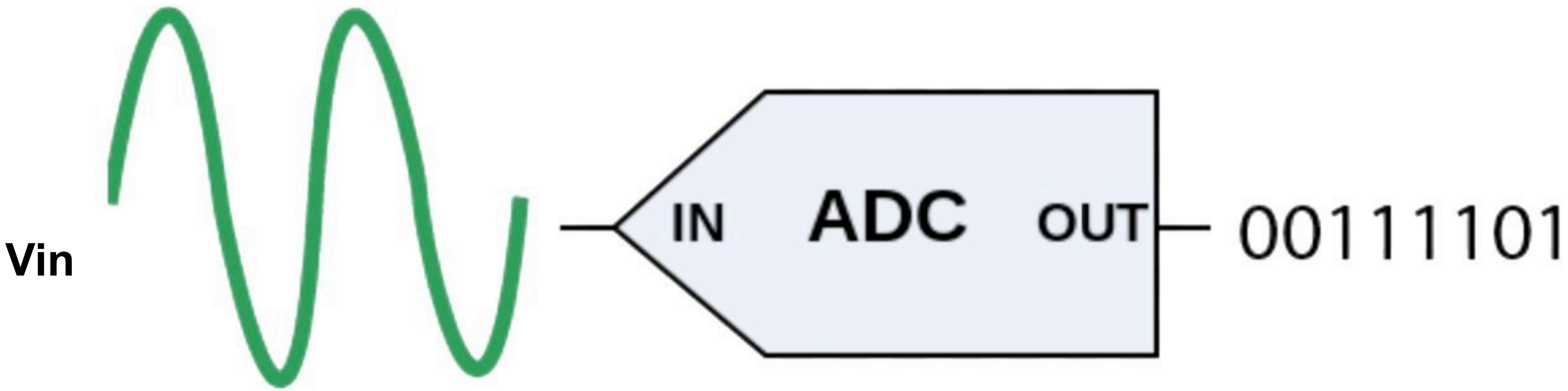
$$y_1 \approx \alpha_1 x_1 + \alpha_2 x_1^2 + \alpha_3 x_1^3 \text{ and } y_2 \approx \beta_1 x_2 + \beta_2 x_2^2 + \beta_3 x_2^3$$

$$y_1 - y_2 = (\alpha_1 x_1 - \beta_1 x_2) + \left(\alpha_2 x_1^2 - \beta_2 x_2^2\right) + \left(\alpha_3 x_1^3 - \beta_3 x_2^3\right)$$

$$y_1 - y_2 = (\alpha_1 + \beta_1)x_1 + (\alpha_2 - \beta_2)x_1^2 + (\alpha_3 + \beta_3)x_1^3$$



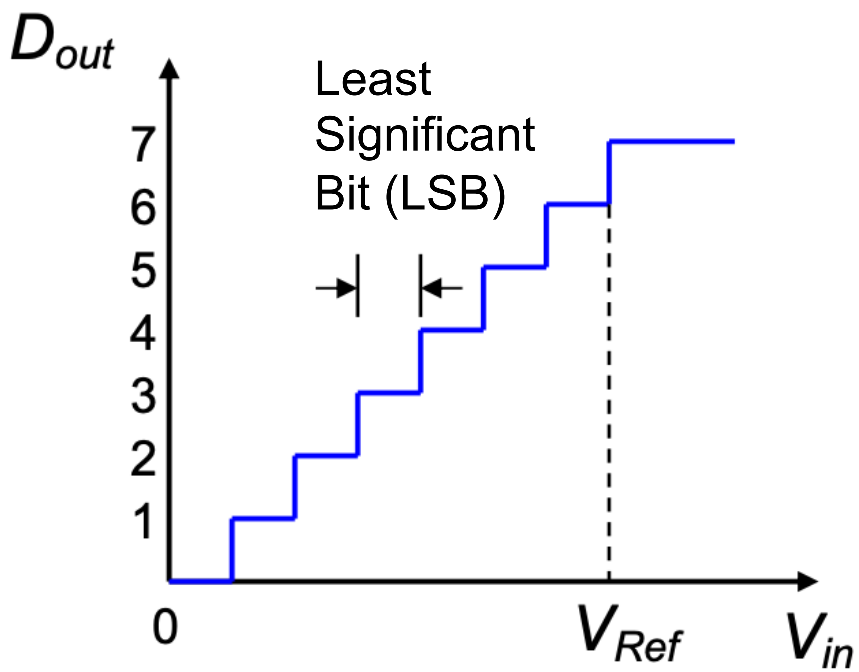
Analog-to-digital Converter (ADC): Introduction



An ADC generates N bit binary representation of Vin

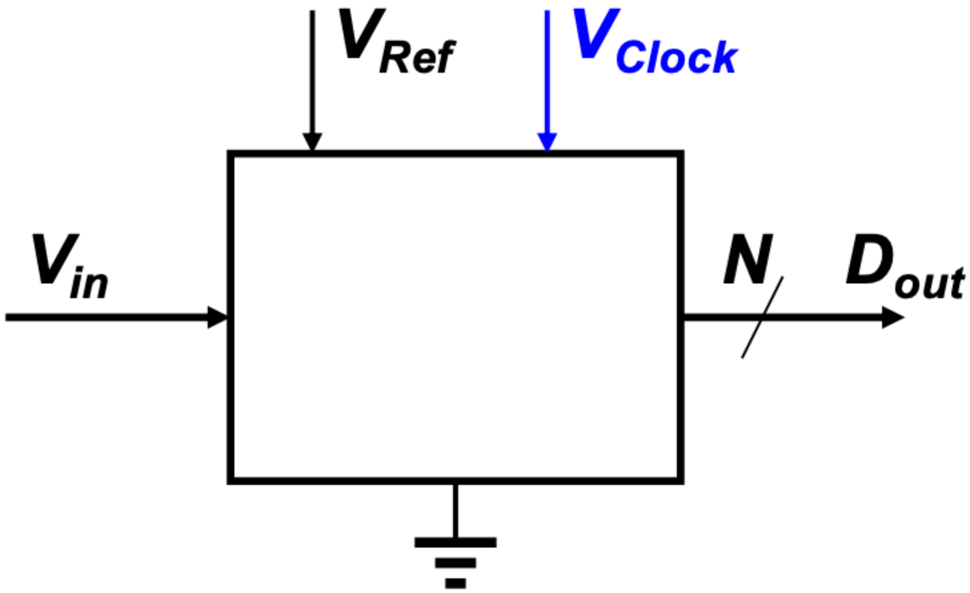
- In most cases, a reference voltage is supplied to the ADC (for example a bandgap reference)
- The analog input, Vin, is “quantized” in the voltage range

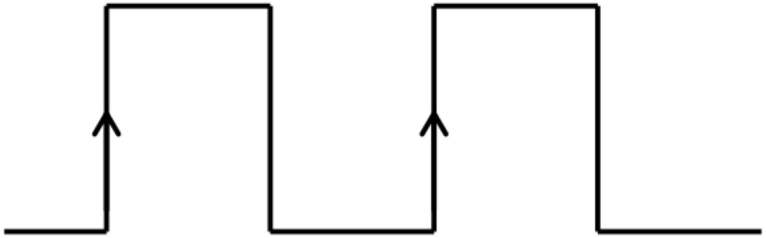
ADC Introduction: LSB



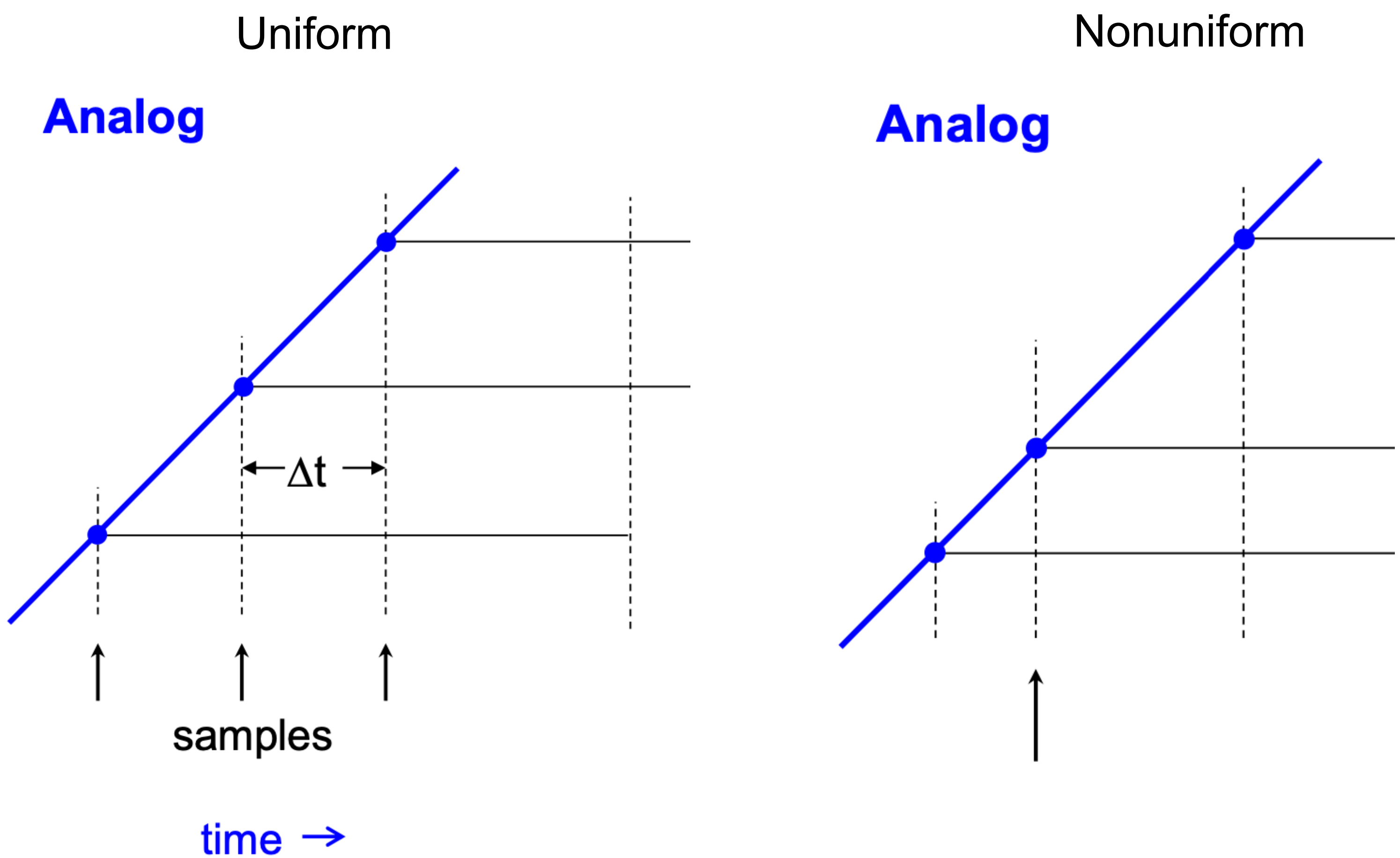
- The voltage change associated with an LSB change in the digital output

ADC Introduction: Clock





Uniform and Nonuniform Sampling

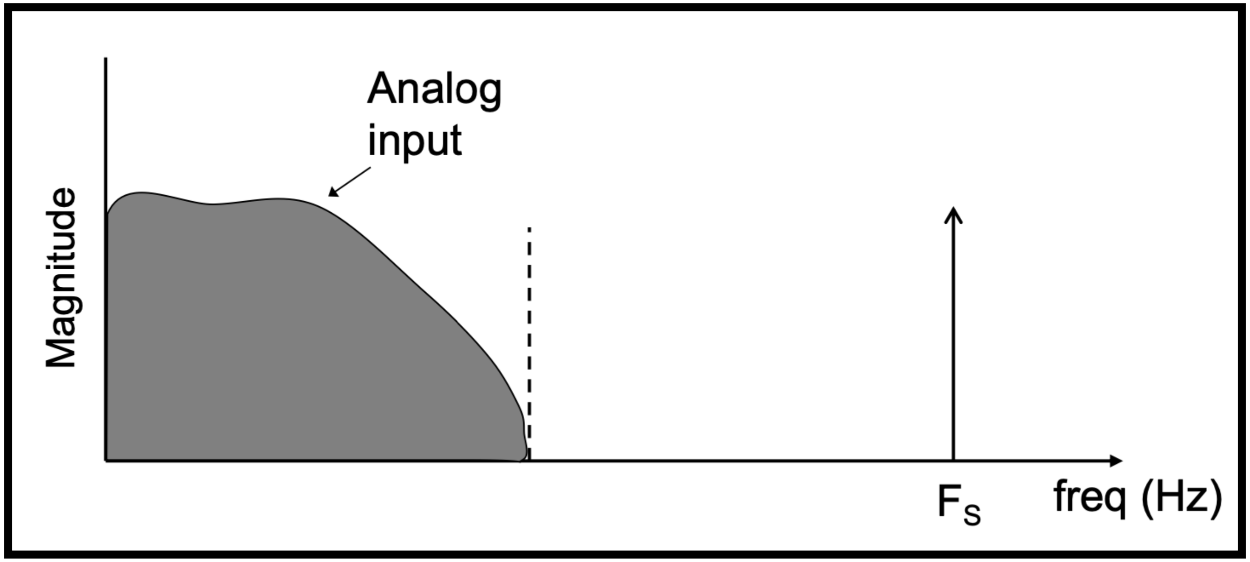


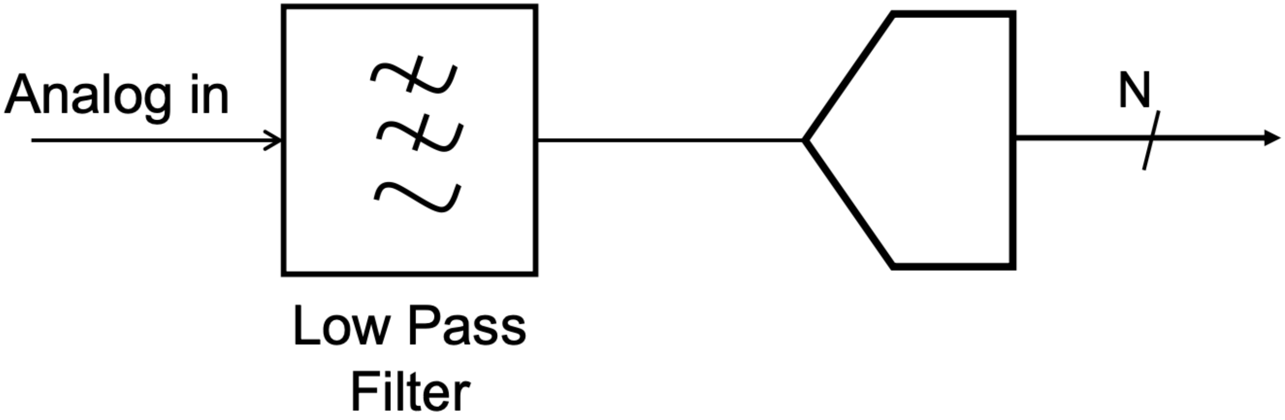
Various Types of Data Converters

Data Converters

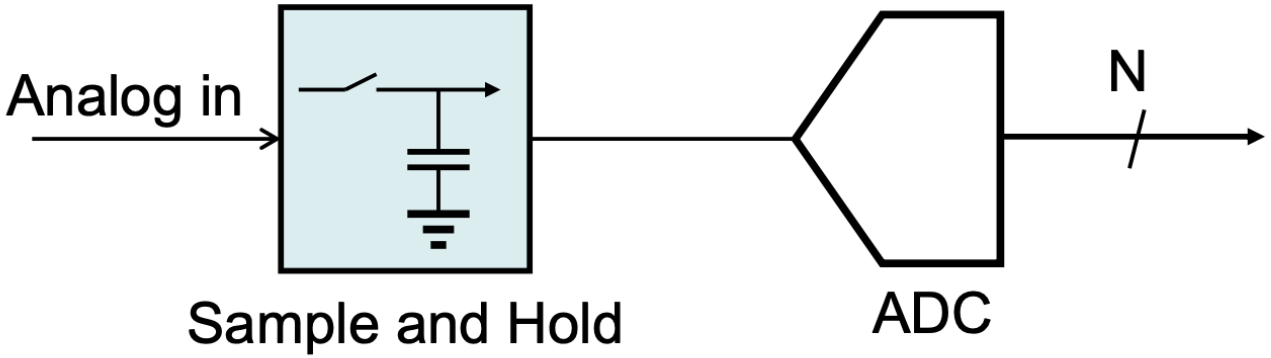
- **Nyquist Rate**
  - ADC
    - Flash
    - Folding
    - Pipeline
    - Successive Approximation
    - Dual Slope
    - ⇩ HDD, Wireless IF/baseband, Wireline comms. DSL, cable modem, Video, Sensors
  - DAC
    - Current steer
    - Resistor string
    - Charge redistribution
    - ⇩ Video, Comms
- **Oversampled (ΣΔ)**
  - ADC
    - ΣΔ
    - NS SAR
    - ⇩ Audio, Seismic, Wireless baseband, Sensors
  - DAC
    - ΣΔ
    - ⇩ Audio, Wireless

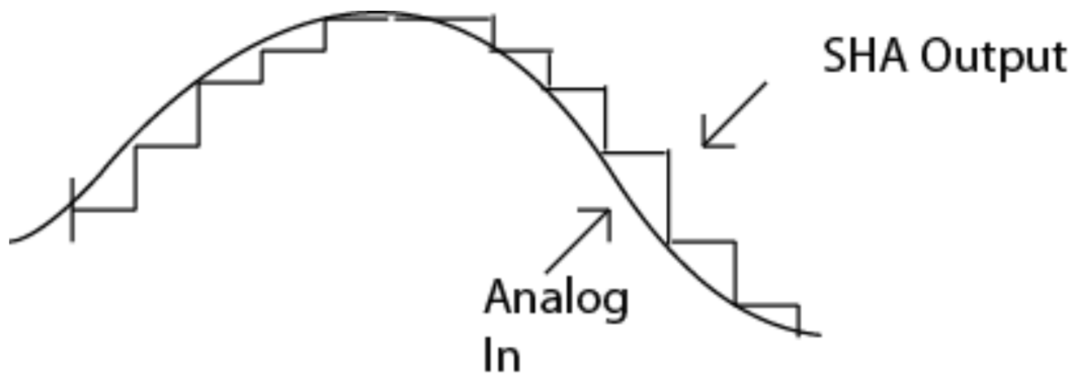
Nyquist rate sampling, aliasing



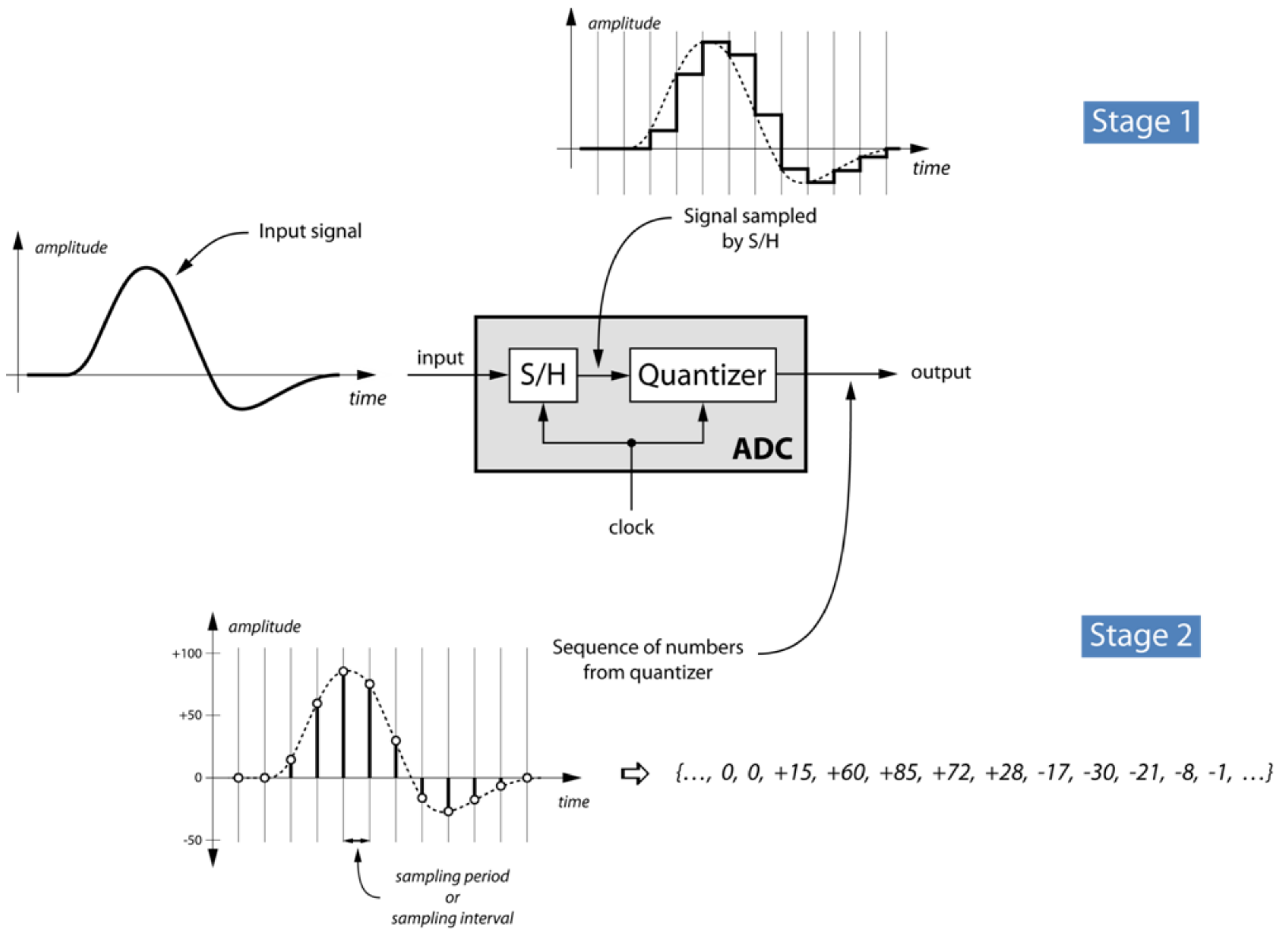


Sample and Hold





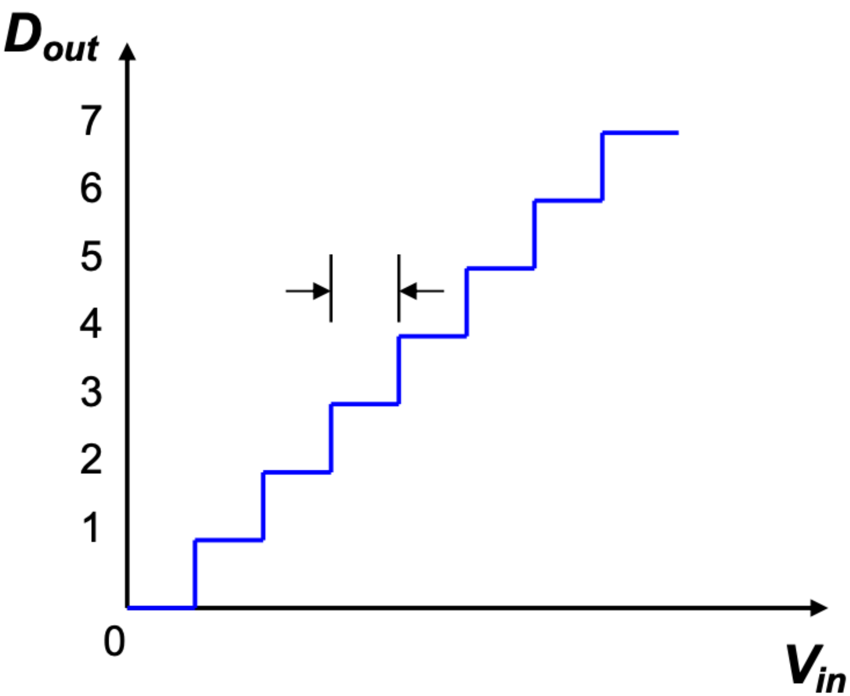
Sample and Hold

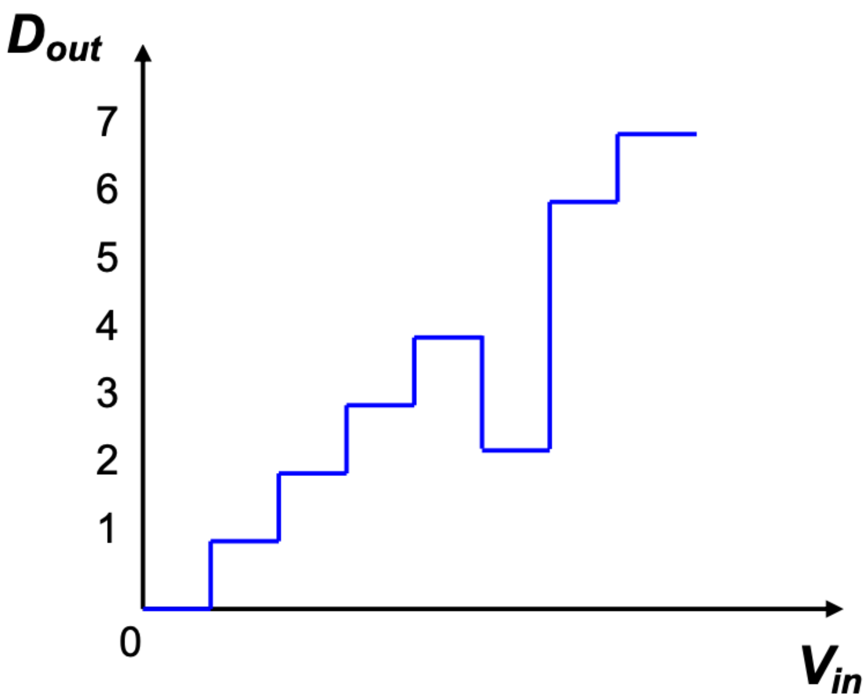


DC Characteristics – Monotonicity

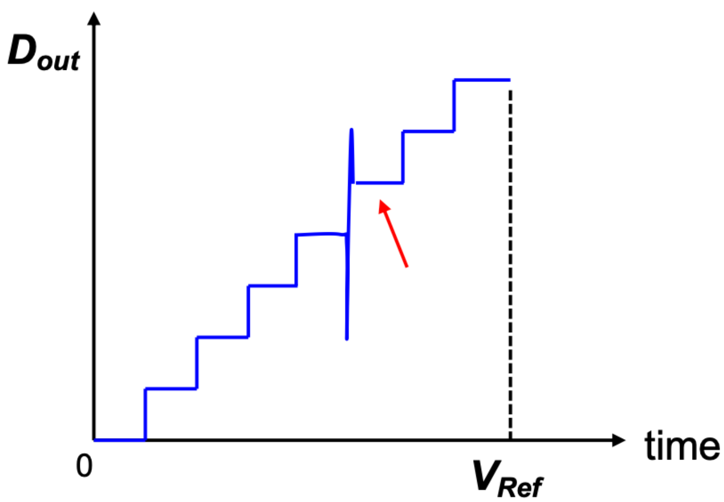
- Monotonicity is usually required in ADCs
- Output code should increase with increasing input voltage

Monotonic

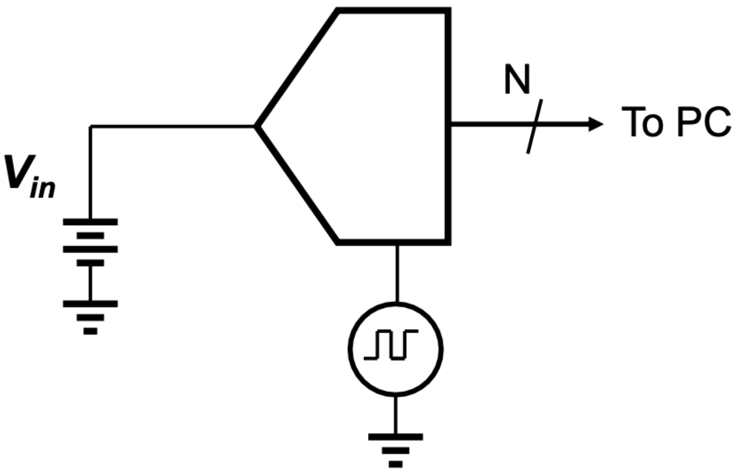




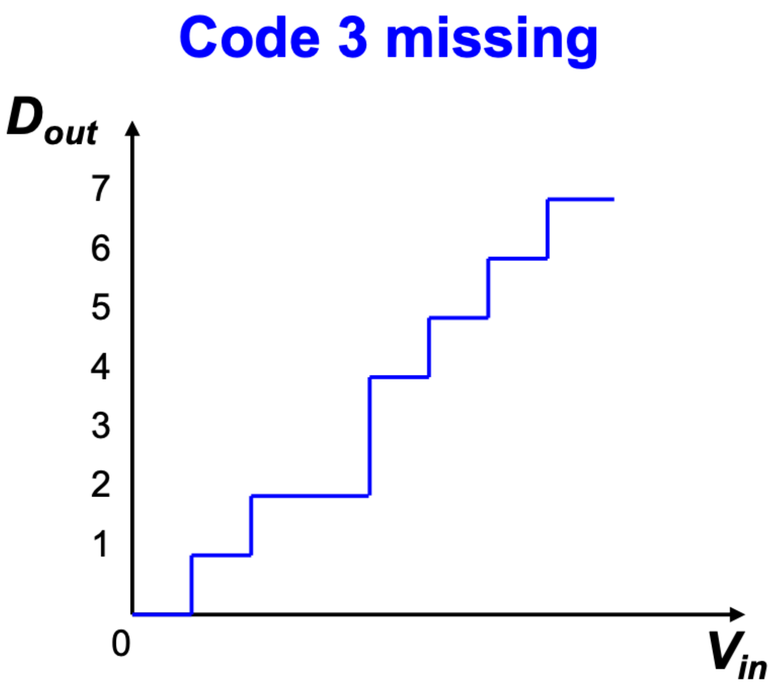
DC Test Setup

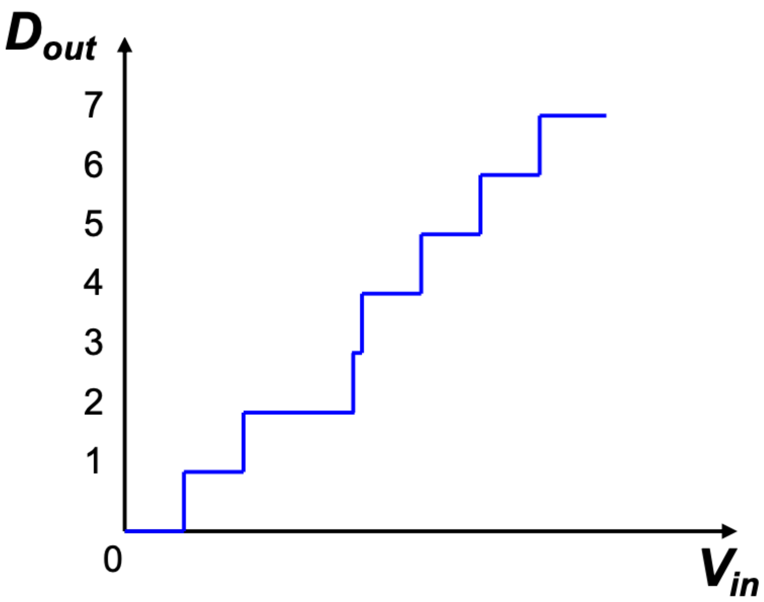


Test Setup

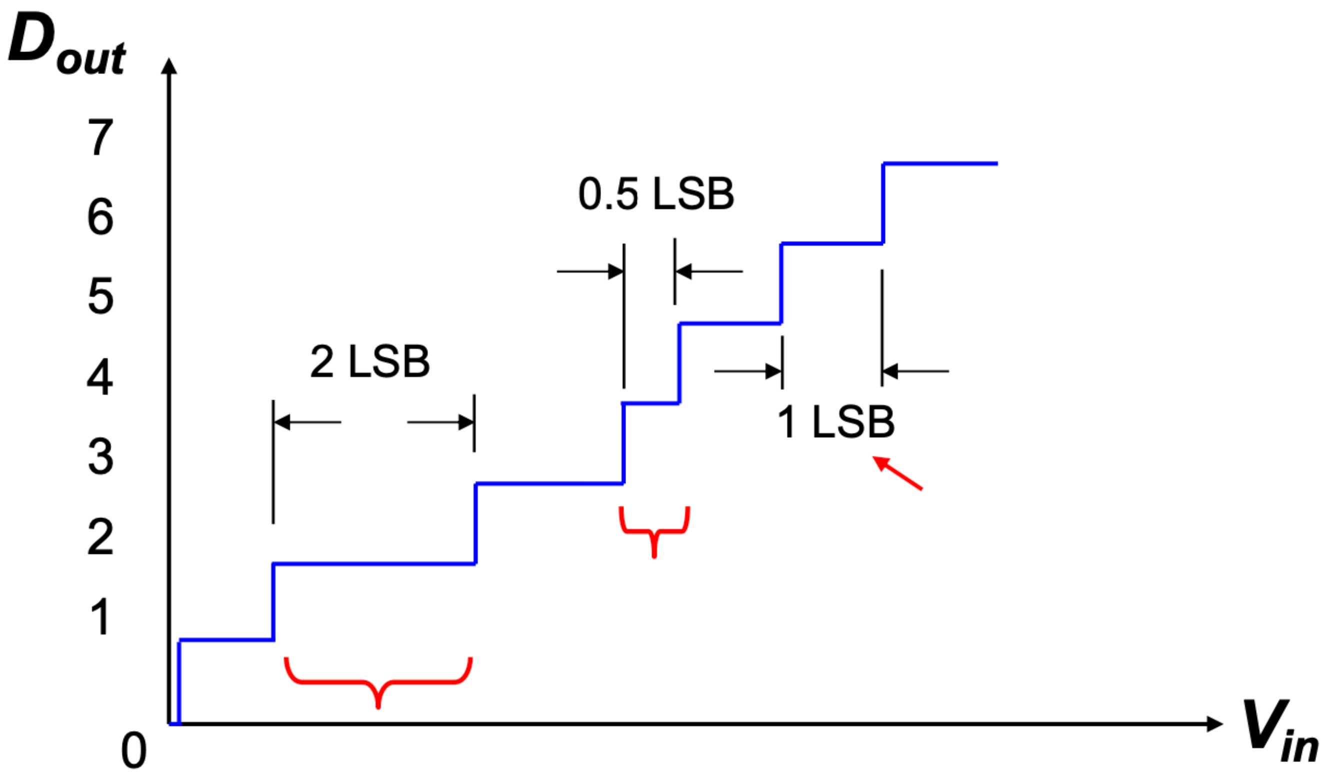


Missing Codes



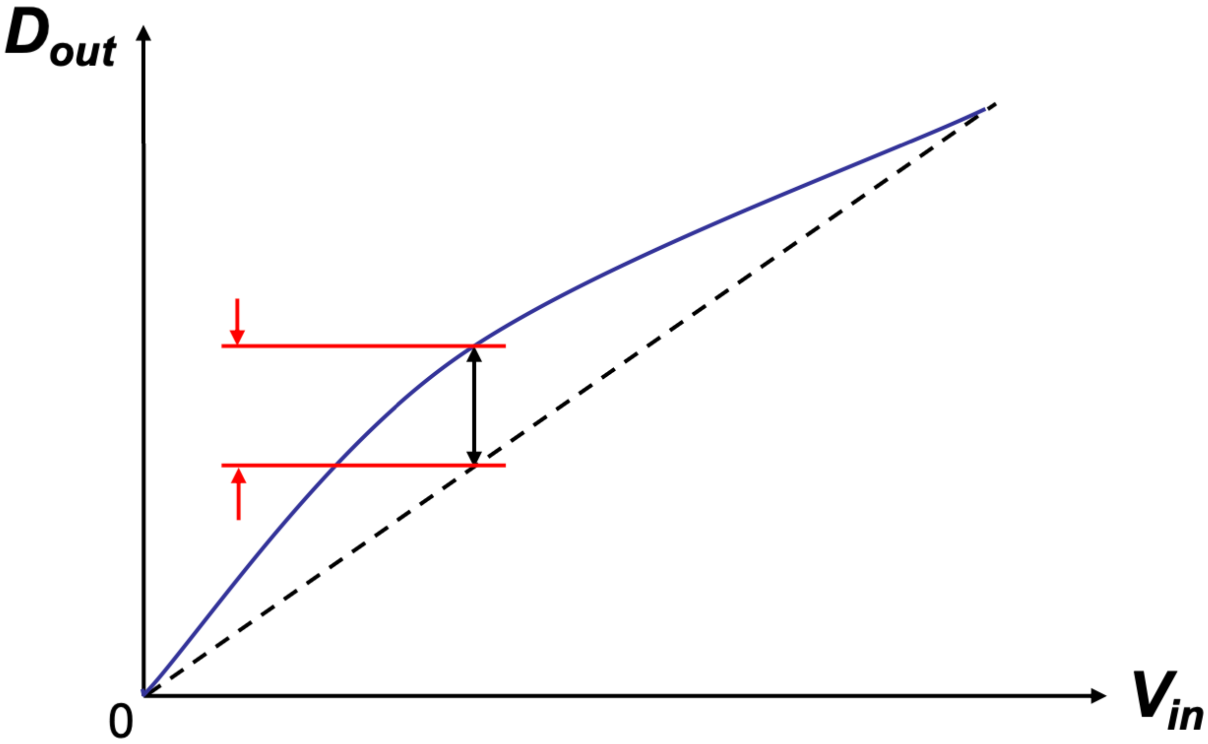


Differential Non-Linearity (DNL)



DNL = Actual width (in LSB) – Ideal width (i.e. 1 LSB)

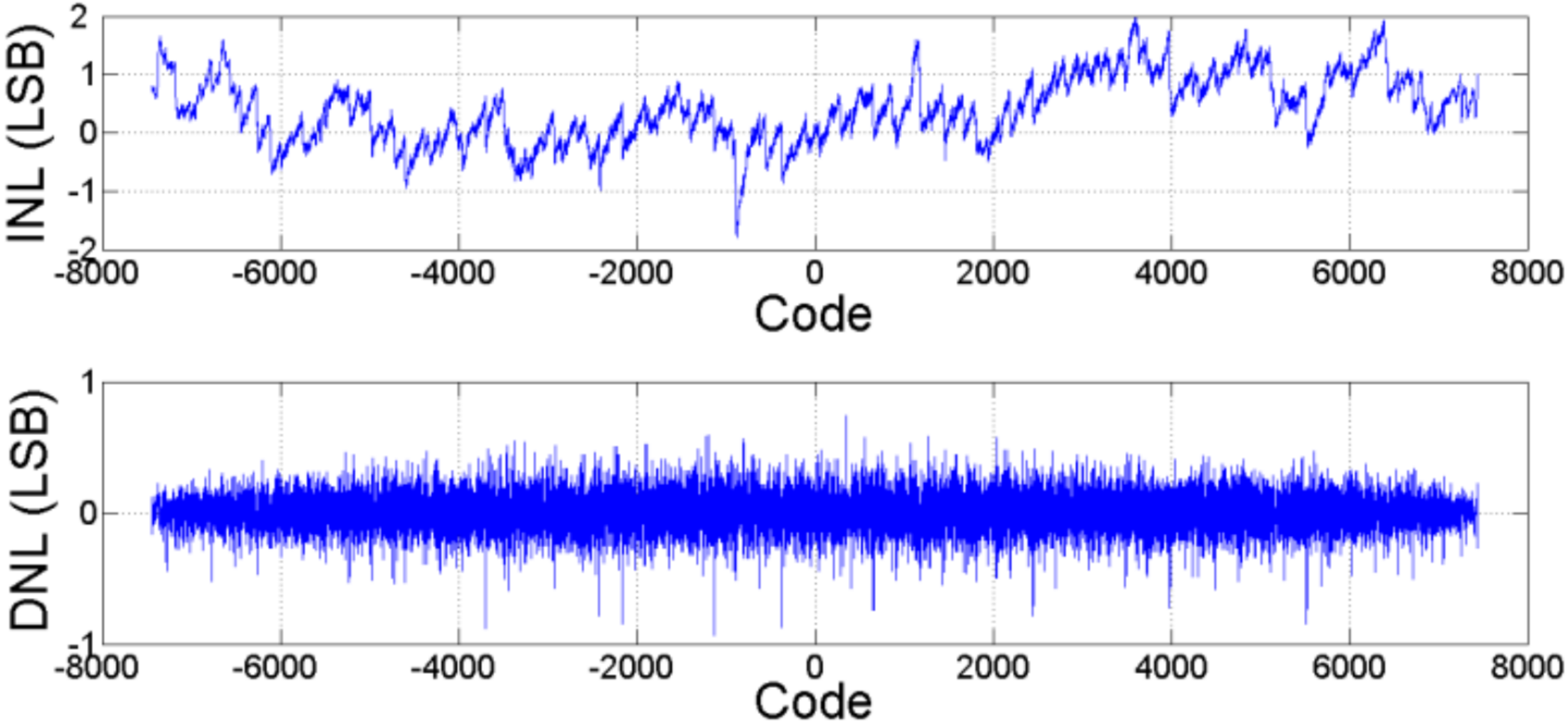
Integral Non-Linearity (INL)



- Just like DNL, INL can be specified at each code
- INL is often derived form DNL information

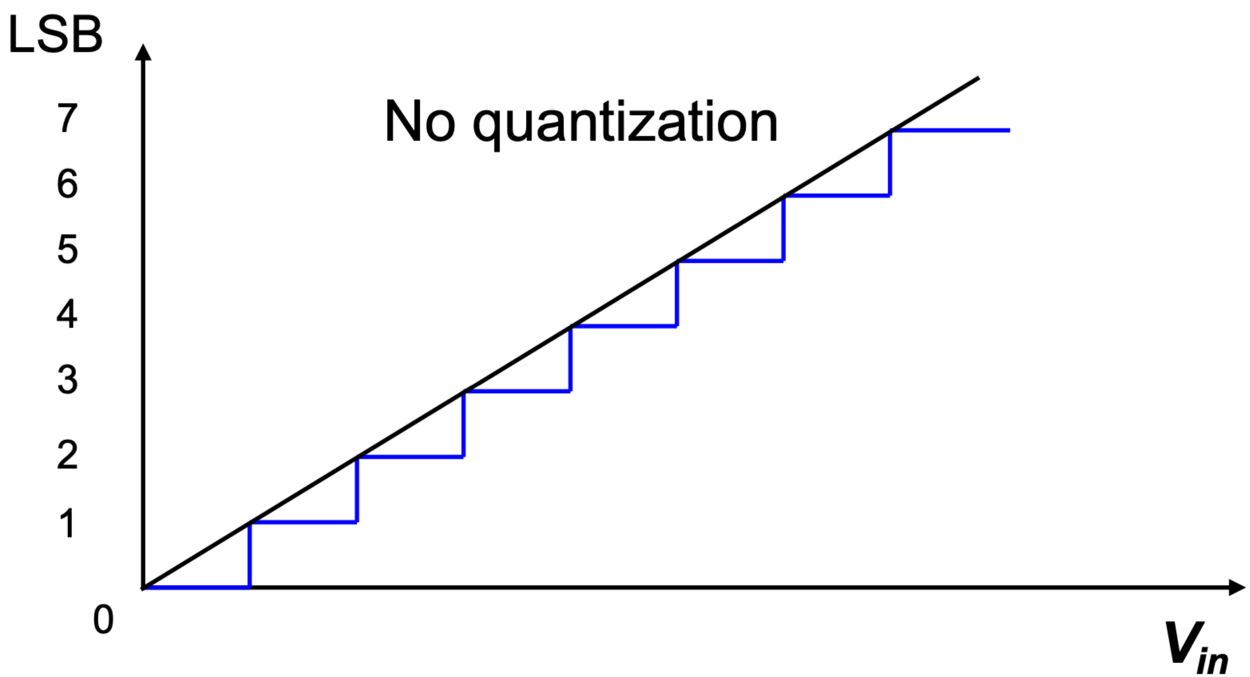
INL and DNL Plots

- **INL and DNL for an experimental 14b ADC**

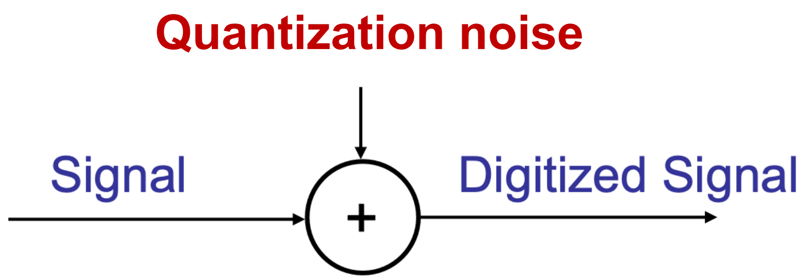


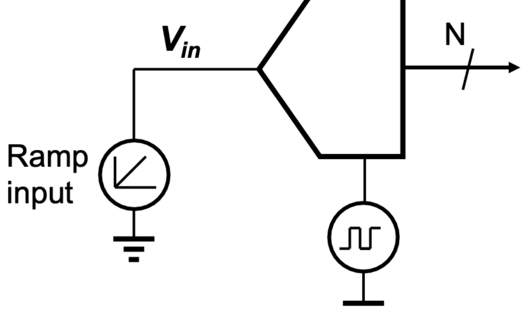
SNR, Quantization Noise

- **SNR or Signal-to-Noise ratio**: Signal power, and noise power (**quantization noise**/error and the circuit noise)
- We consider **quantization noise** as a white noise that is uncorrelated with the signal, with a uniform probability distribution
- **ENOB**: Effective Number of Bits, calculated from **SNDR**

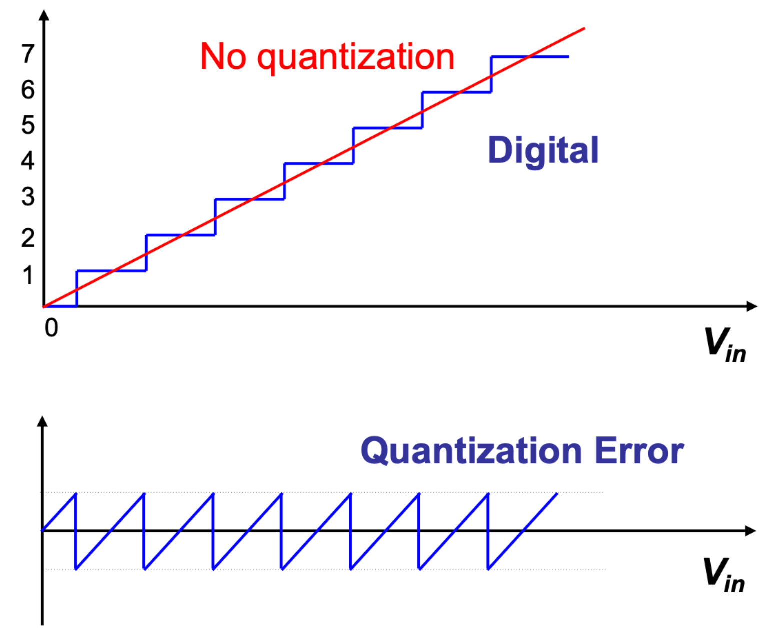


- We want to determine the mean squared value of the quantization noise



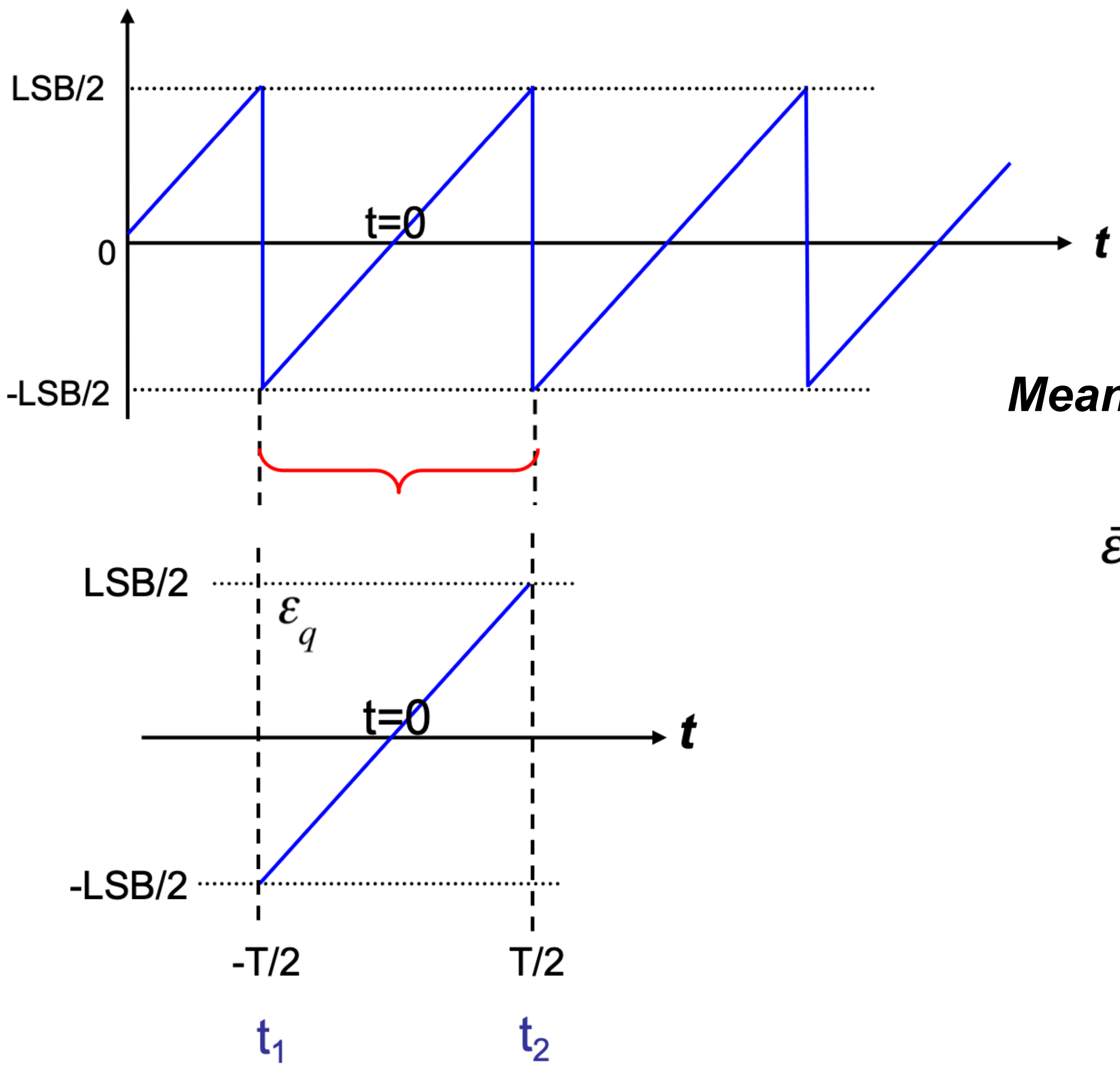


Test Setup



Quantization Noise for Ramp Input

- Concentrating on region from –T/2 to T/2



Mean squared quantization noise

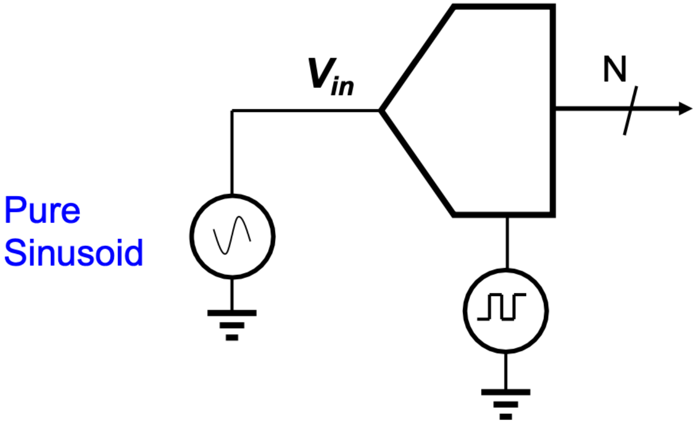
$$\bar{\varepsilon}_q^2 = \frac{1}{T}\int_{-T/2}^{T/2}\left(\frac{t}{T}LSB\right)^2 dt$$

$$= \frac{1}{3}\frac{LSB^2}{T^3}t^3 \Big|_{-T/2}^{T/2}$$

$$= \frac{LSB^2}{12}$$

SNR for Ideal ADC

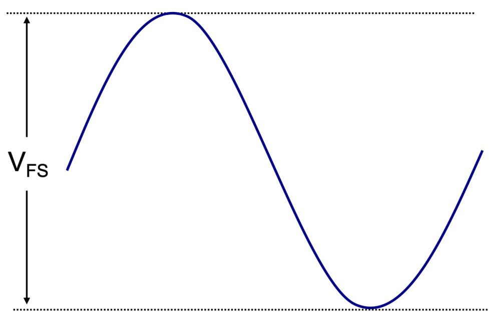
- Pure sine wave has only one frequency component, easier to generate



Signal to Noise Ratio (SNR) = $\dfrac{\textbf{Signal Power}}{\textbf{Noise Power}}$

$$SNR = 10\log_{10}\left(\frac{signal\ \ power}{noise\ \ power}\right)$$

$$= 20\log_{10}\left(\frac{\frac{2^N}{2\sqrt{2}}LSB}{\frac{1}{\sqrt{12}}LSB}\right)$$

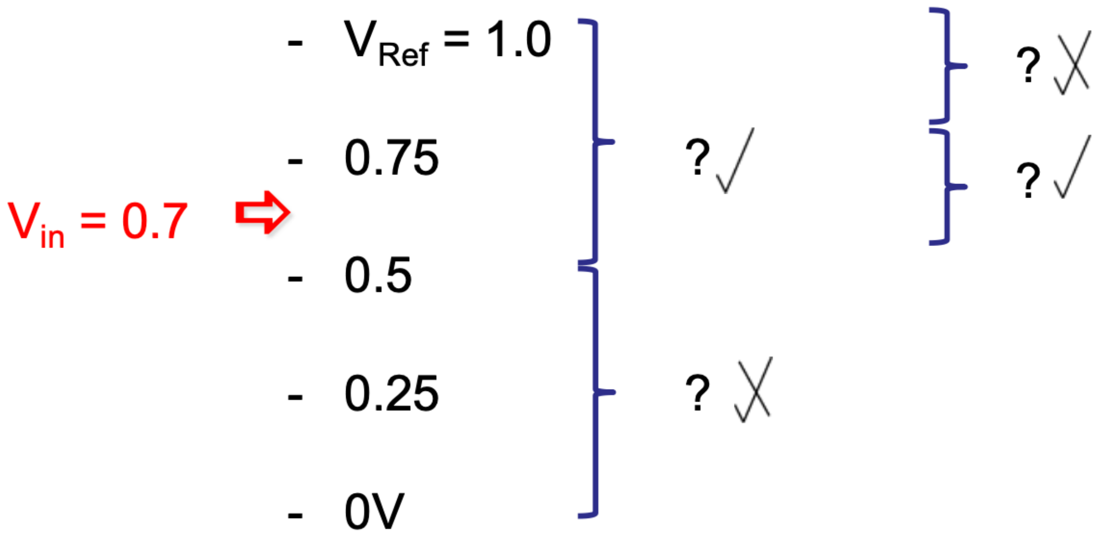


$$SNR = (6.02N + 1.76)\ dB$$

- Example: For an 8-bit ADC (N=8), the maximum SNR is 49.76 dB

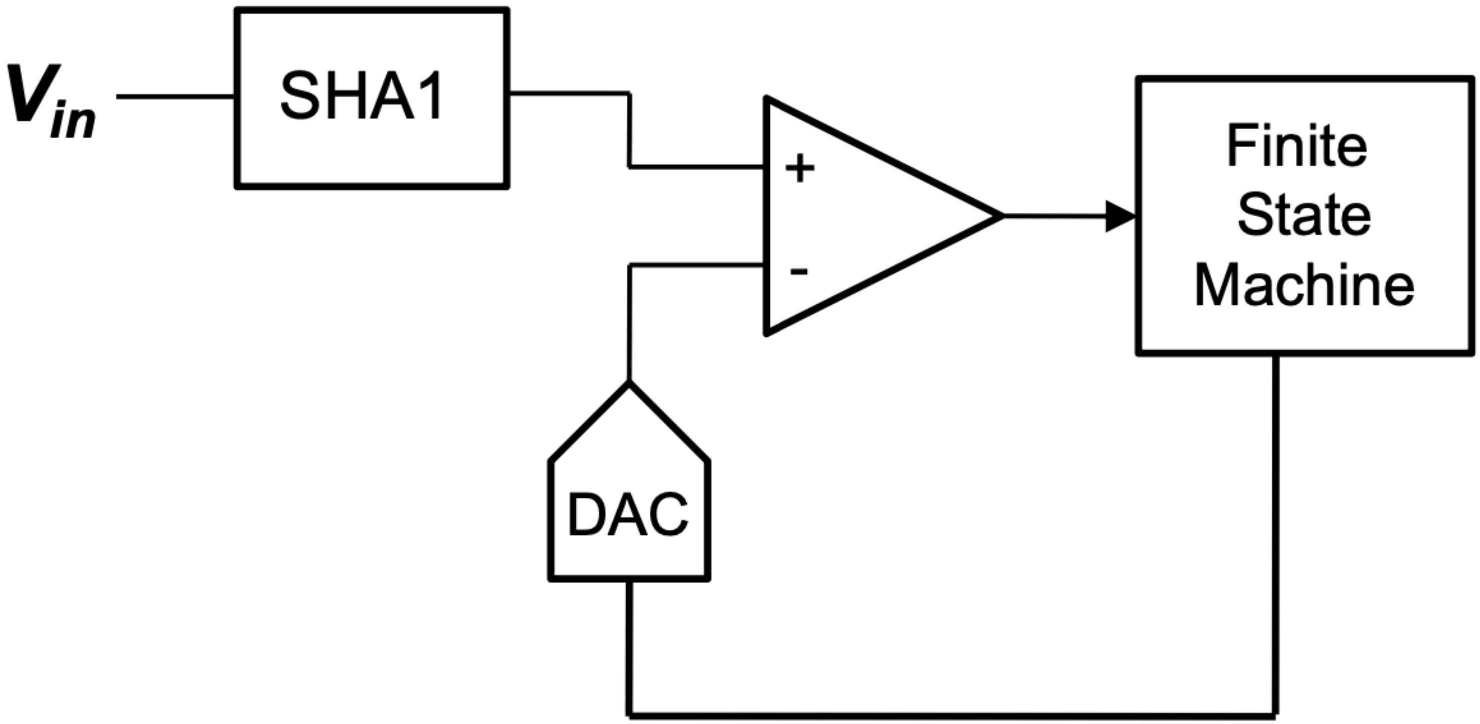
Successive Approximation

- **Key idea:** Performing a binary search, and finding 1 bit from each cycle, starting with the MSB

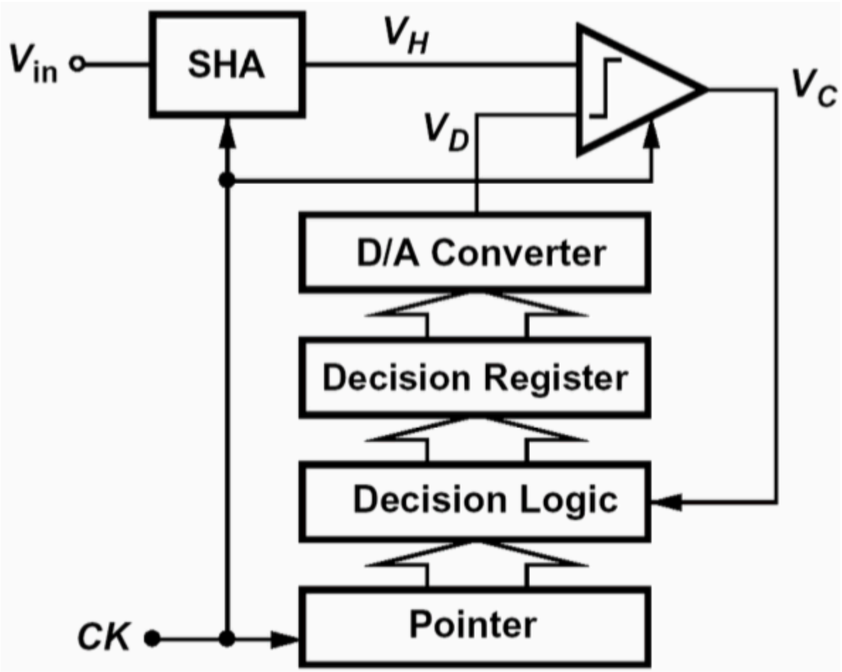


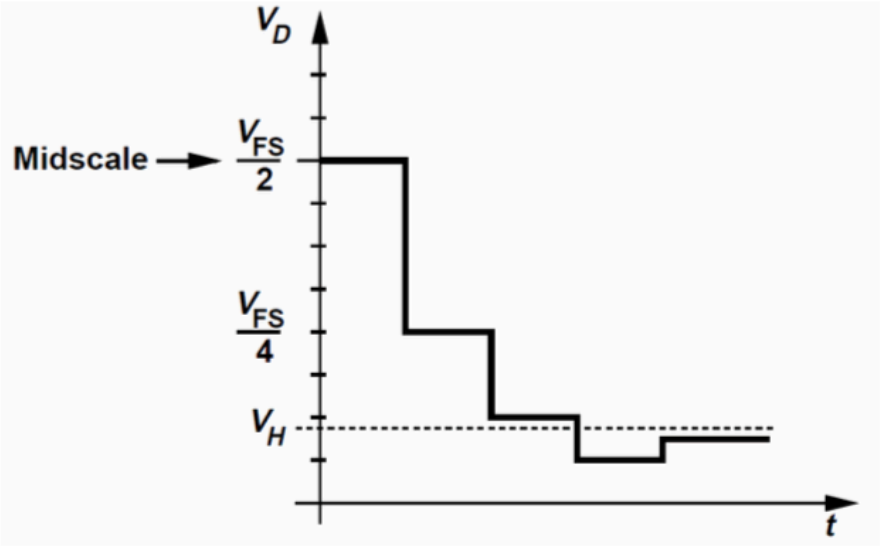
Successive Approximation Register (SAR)

- Binary search for input voltage



SAR Operation

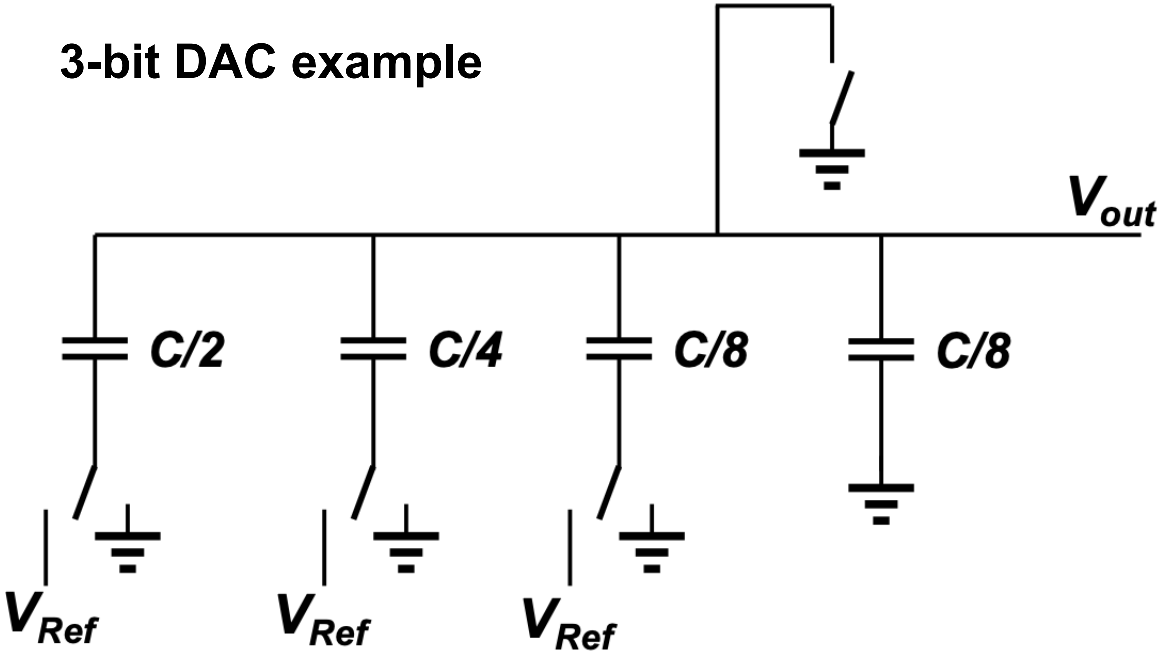




DAC

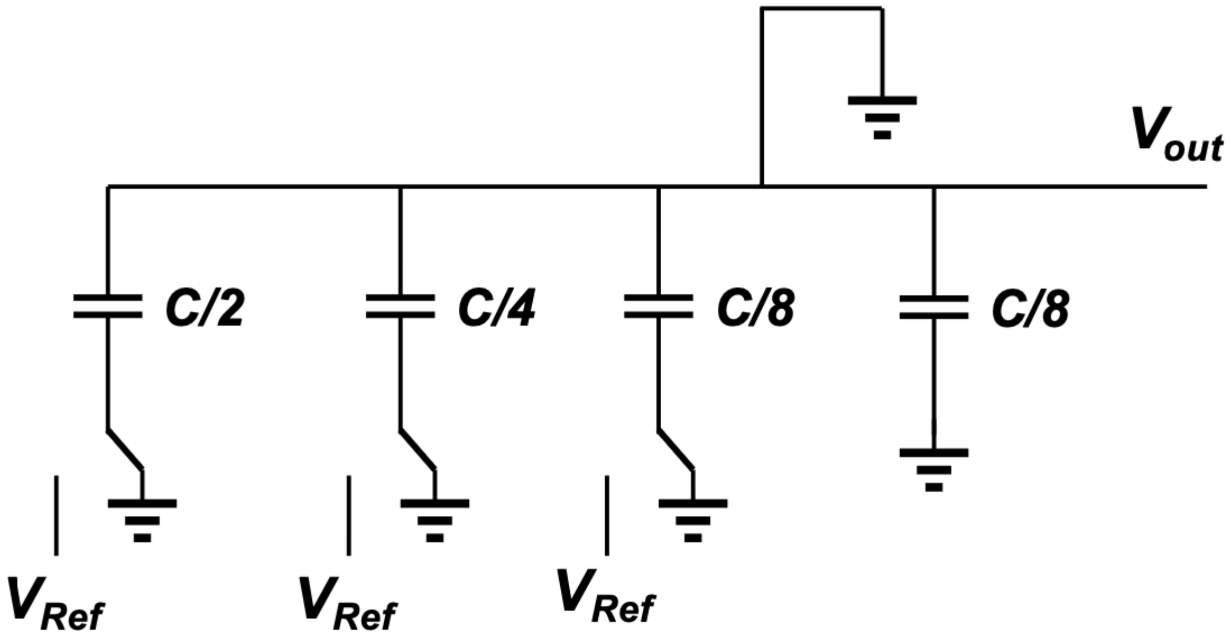
- Capacitive DACs are common in SAR ADC
- Most common: Charge Redistribution DAC
- Switches individually connect to V_{Ref} or ground

3-bit DAC example



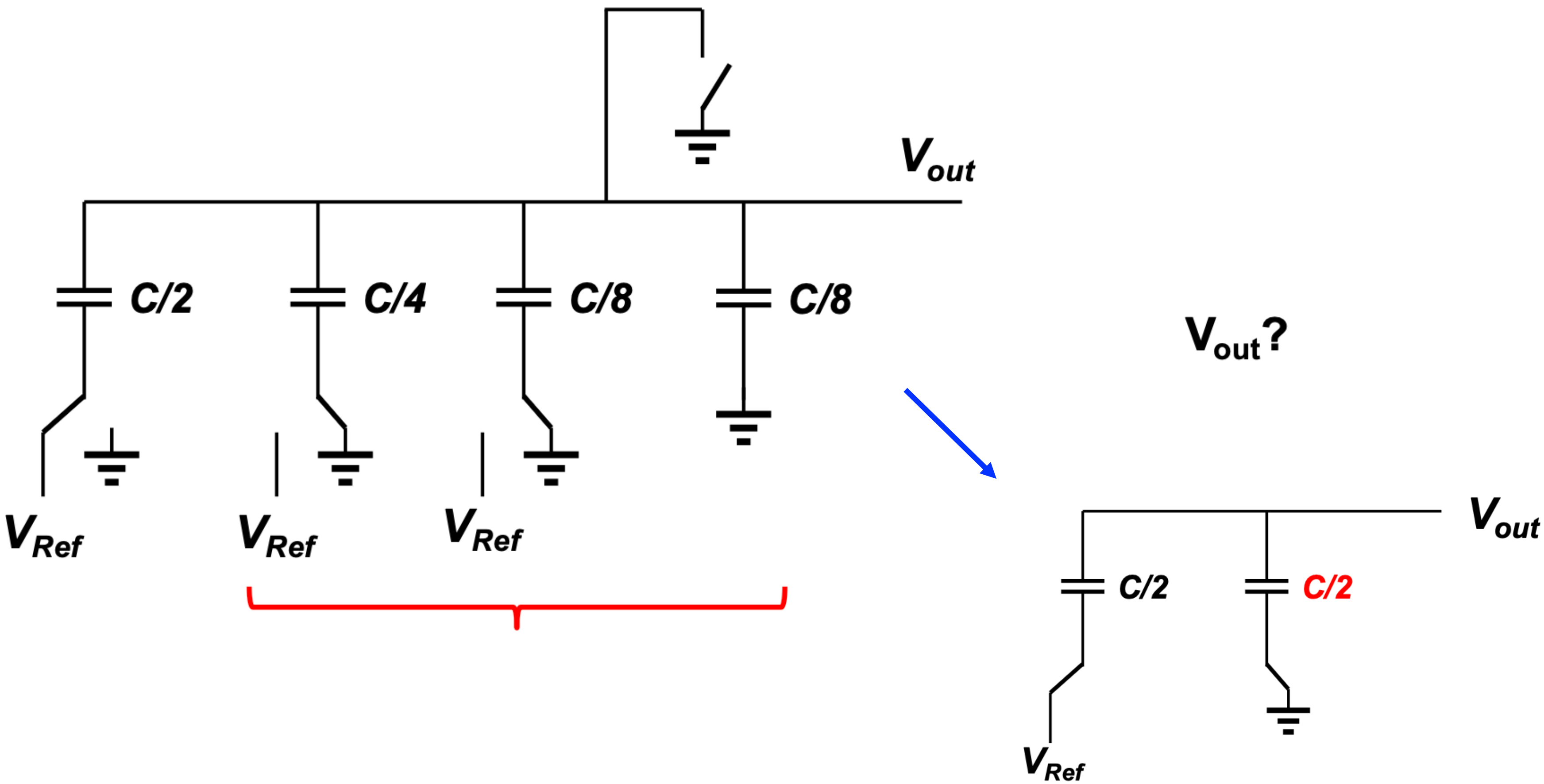
CDAC Operation (1) - Reset

- Reset charge on all caps
- Shorting top and bottom connections to GND



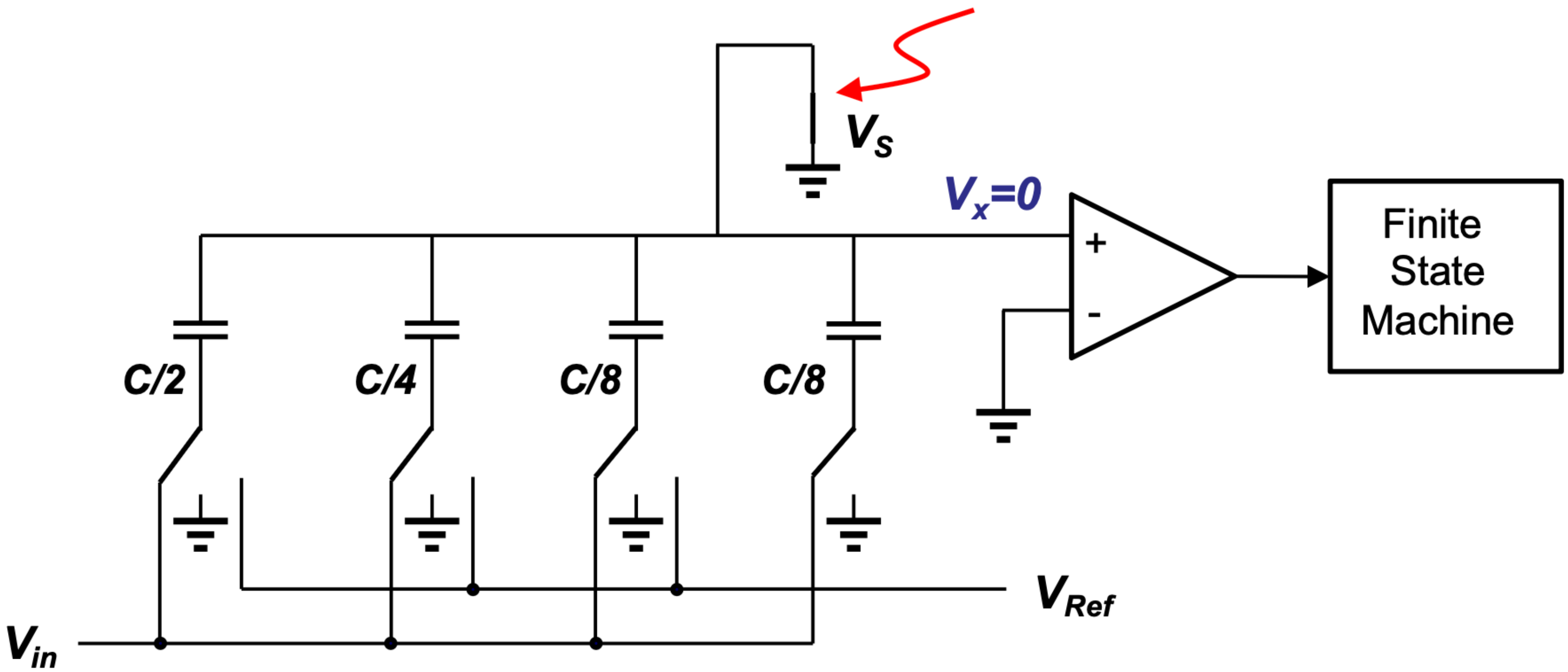
CDAC Operation (2) – Charge Redistribution

- Dial up a voltage by connecting the switches in a binary fashion to V_{Ref}
- Let's say we want code 100:



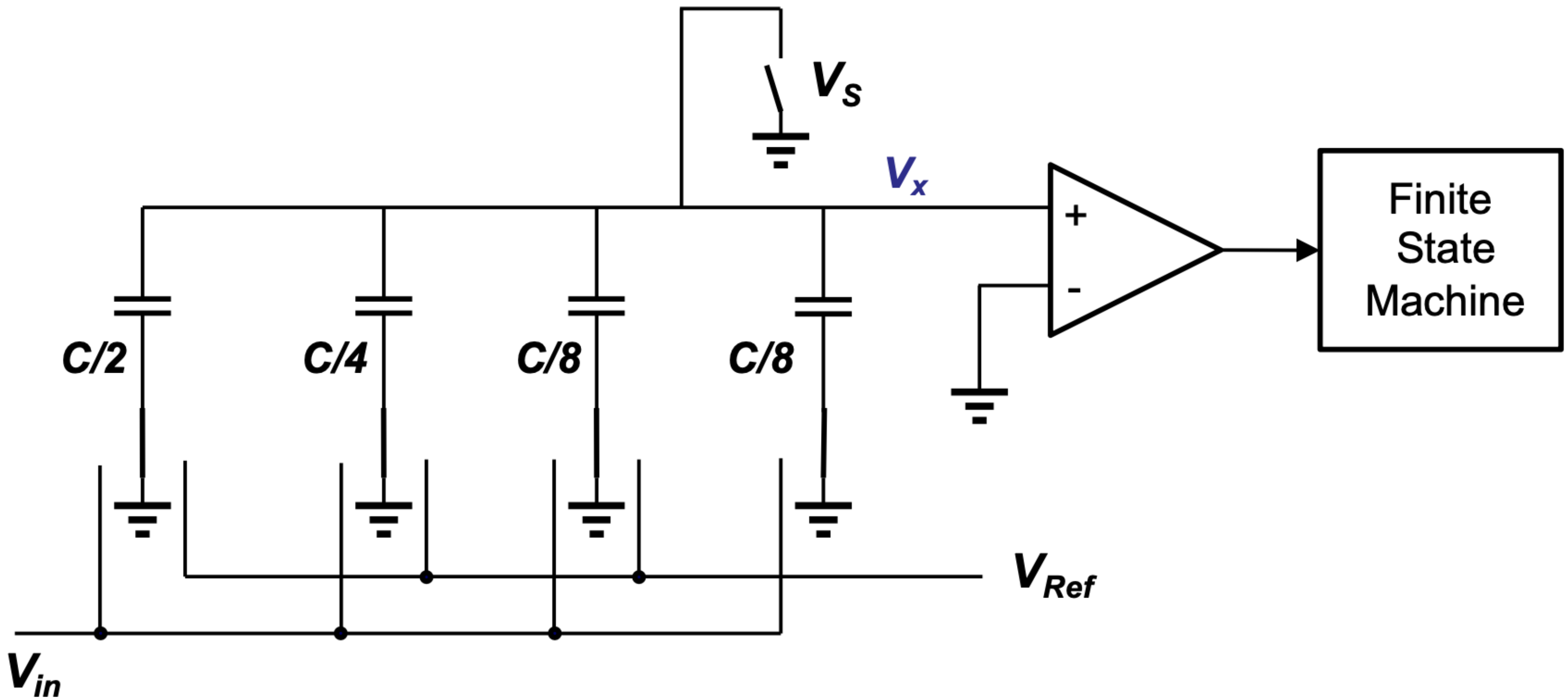
SHA combined with CDAC – Sample Phase

- It is possible to combine S/H capacitance with CDAC
- Use the same cap for sampling and DAC



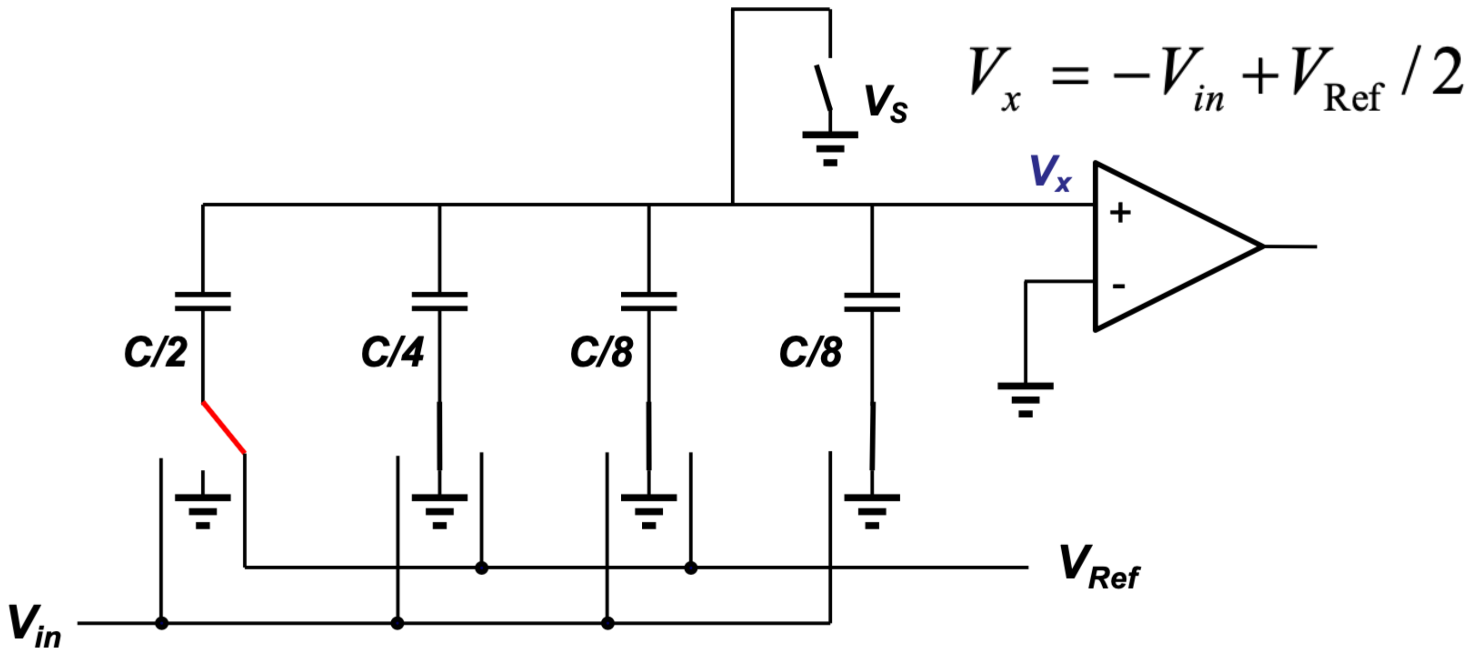
Redistribution Phase

- Sampling switches are connected to ground
- $V_x = -V_{in}$



3-bit ADC Example: MSB Trial

- Next test if Vin > Vref /2, or is MSB (b0) = 1?



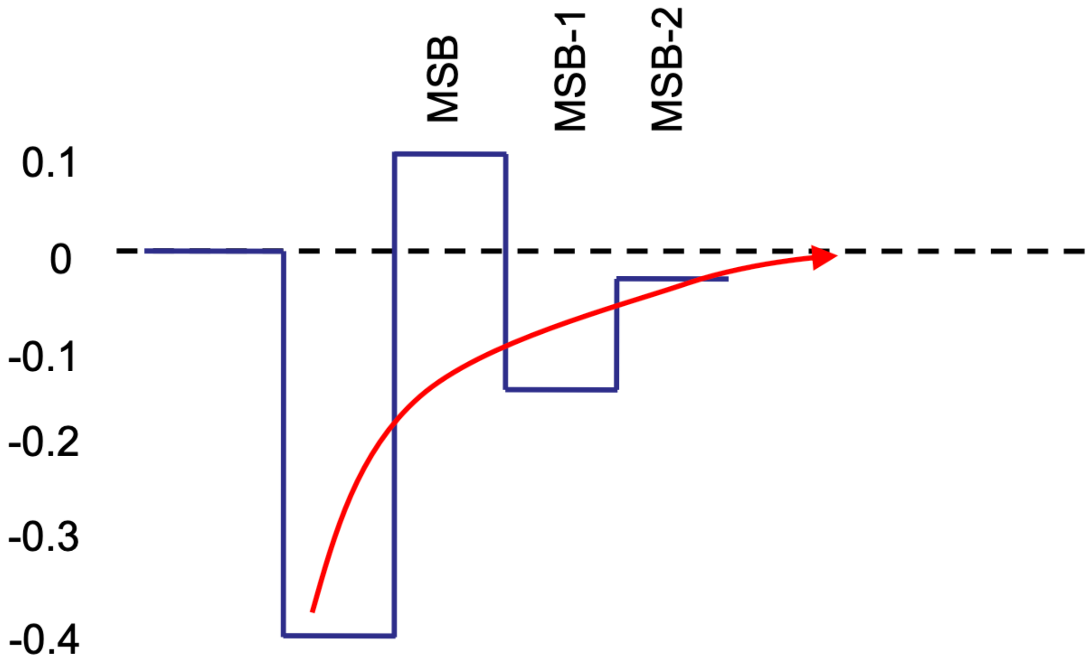
If $V_x > 0$ =>

If $V_x < 0$ =>

- Then proceed to next most significant bit (i.e., b1) and so on...

3-bit ADC Example

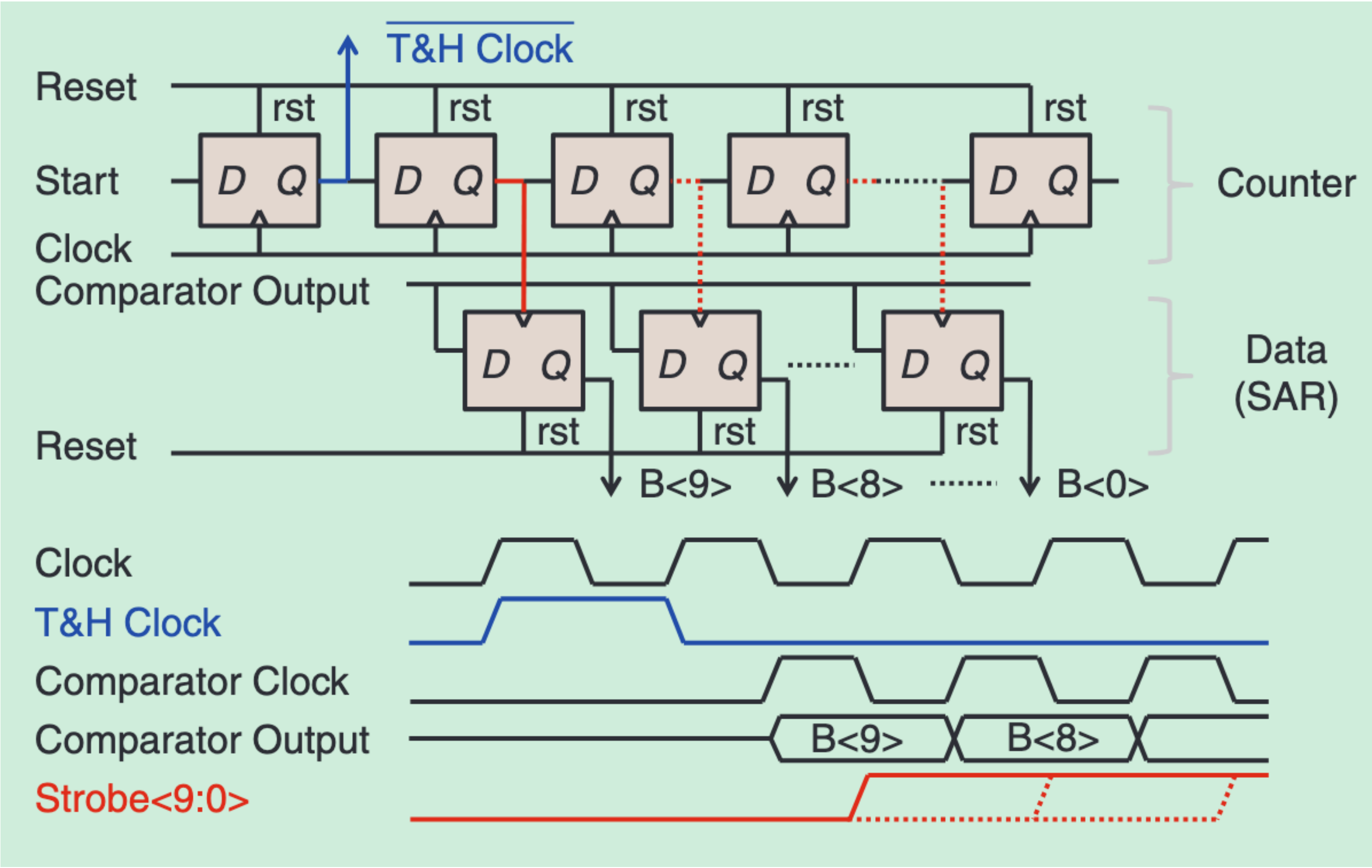
- Waveform at Vx (the comparator input) during conversion
- Vref = 1V, Vin = 0.4Vref



- Vx gets closer and closer to the ground

SAR Logic

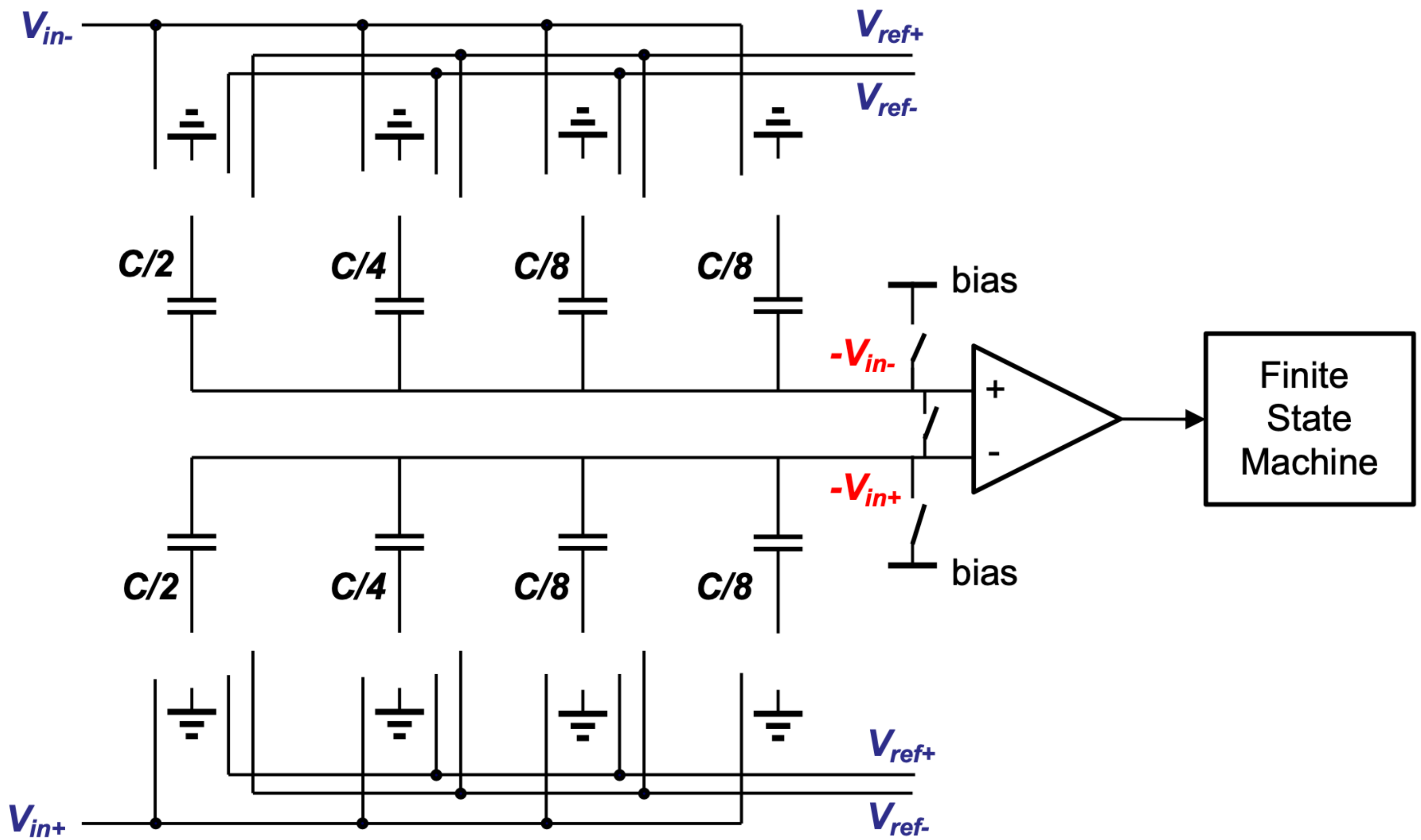
- The logic controls the operation of ADC and generates the digital output code



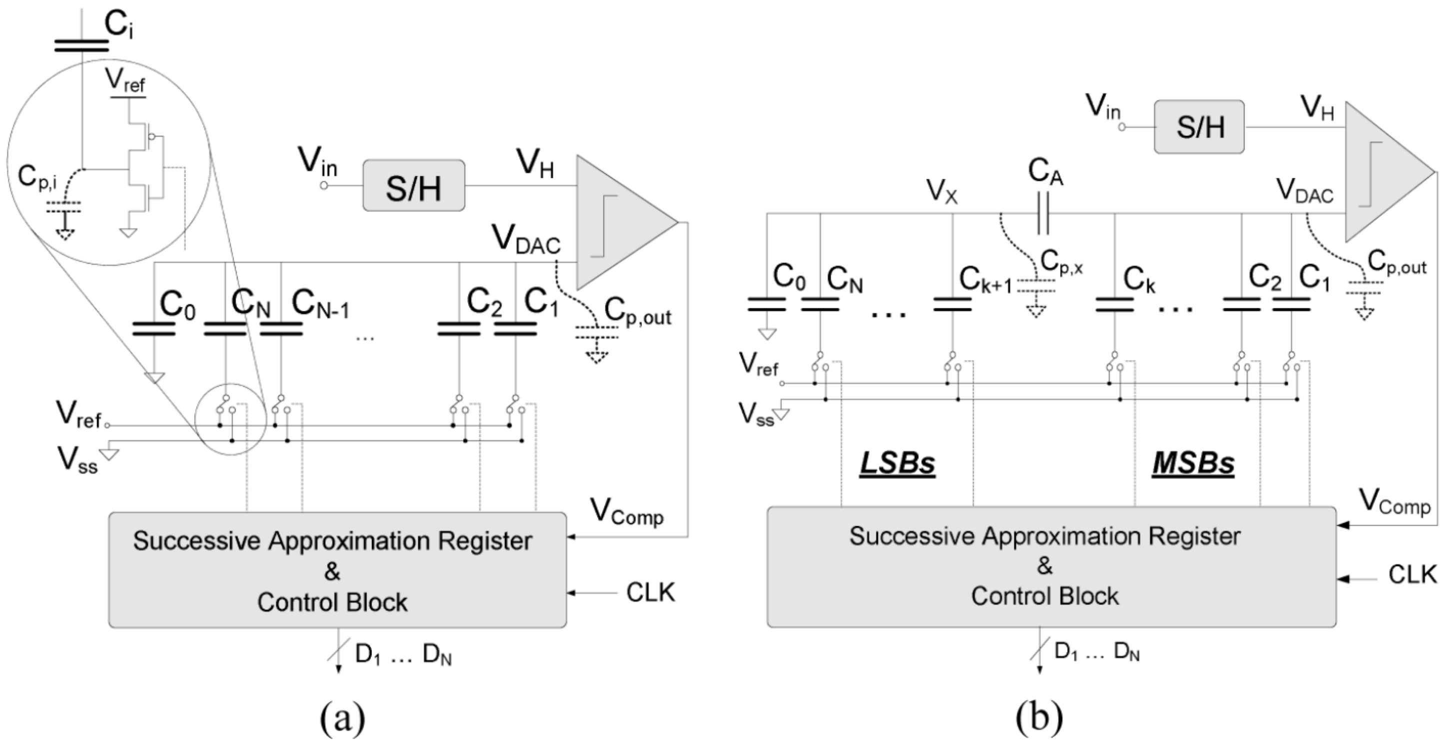
P. Harpe, *IEEE Solid-State Circuits Magazine*, 2016

Fully Differential SAR ADC

- N-bit differential SAR has 2^{N-1} unit caps on each side
- Comparator decides the sign (i.e., MSB) and 3 bits
- Connect to Vref+, Vref- depending on MSB decision, continue with other bits



CDAC Topologies



Conventional Binary Weighted (CBW)

Binary Weighted w/Attenuator Cap (BWC)

M. Saberi, et al., *TCAS-I, 2011*

StrongARM Latch Comparator

The StrongARM latch has become popular for three reasons:

- it consumes zero static power
- it directly produces rail-to-rail outputs
- its input-referred offset arises from primarily one differential pair

T. Kobayashi, et al., *VLSI Circuits Symp.*,1992

StrongARM Latch Comparator

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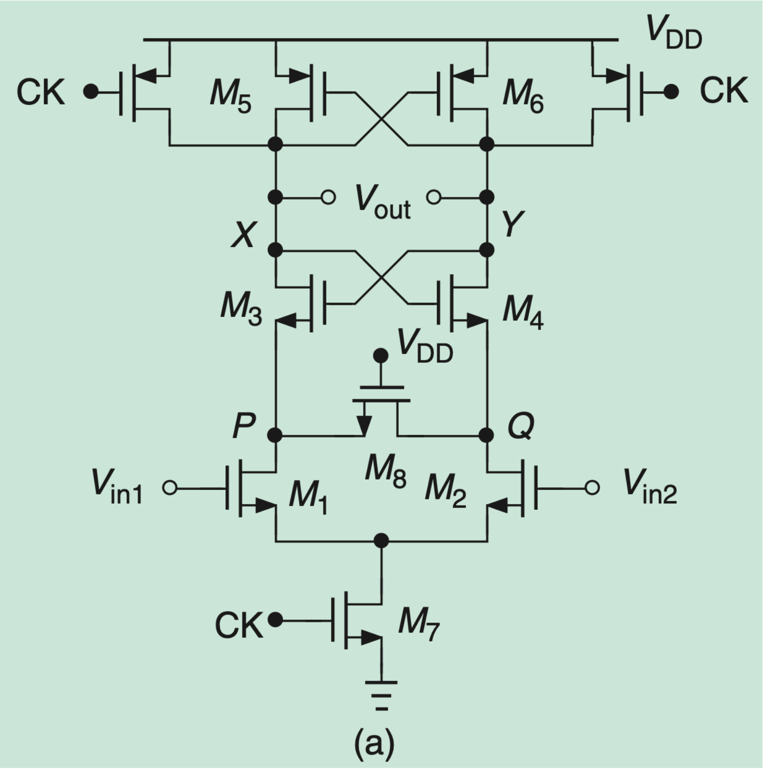
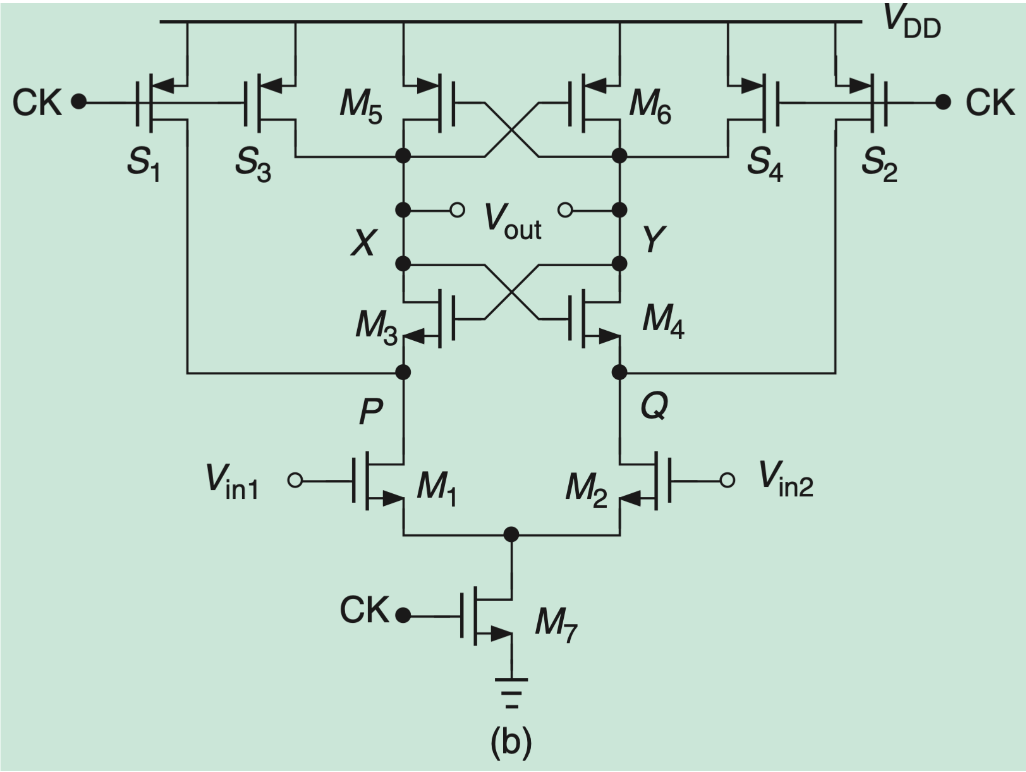
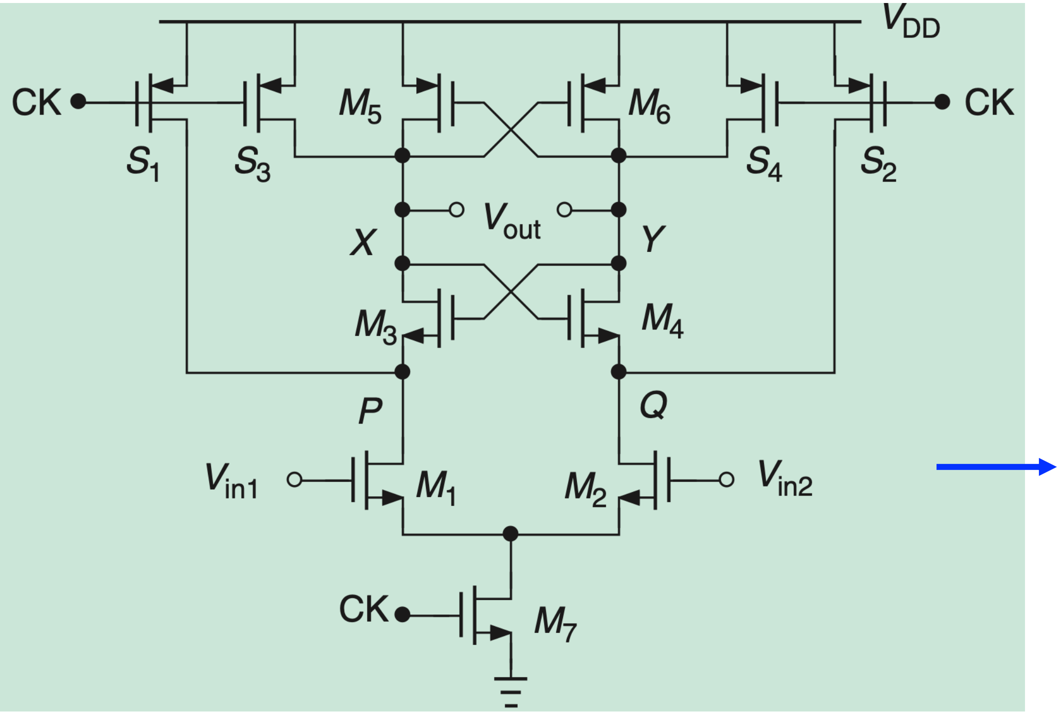
(a) The original and (b) modified StrongARM latch topologies



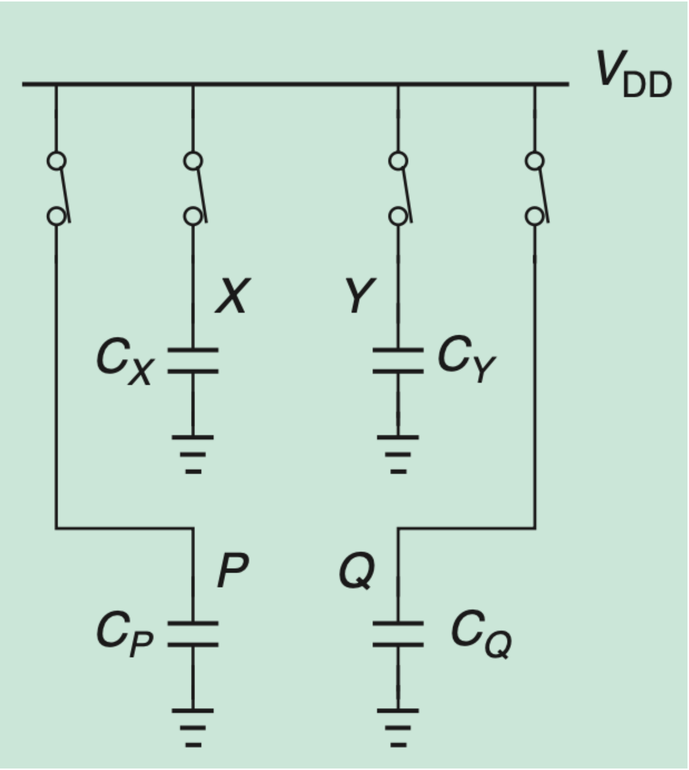


Y. T. Wang and B. Razavi, *JSSC*, 2000

StrongARM Latch Comparator: Phase 1

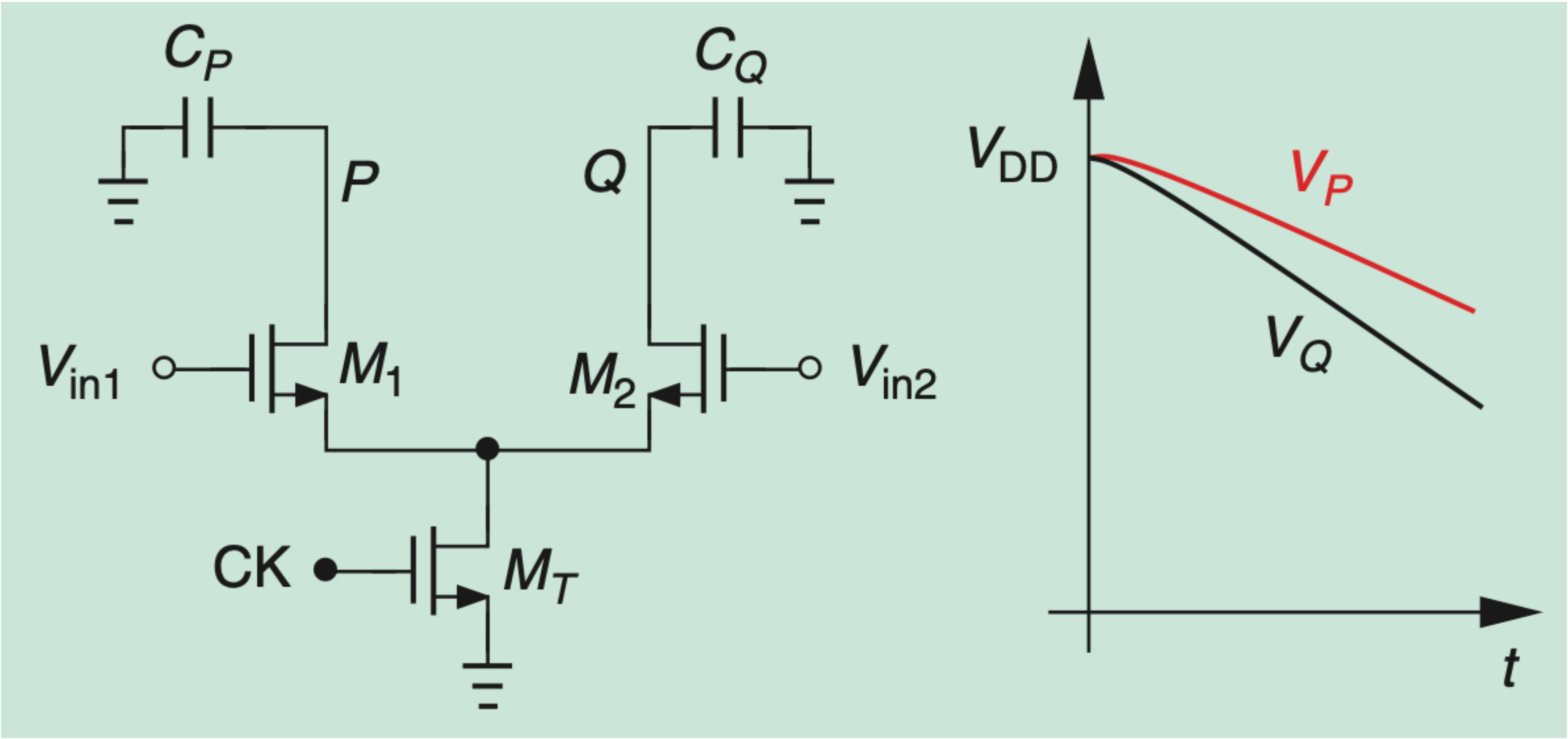


(1) Precharge



StrongARM Latch Comparator: Phase 2

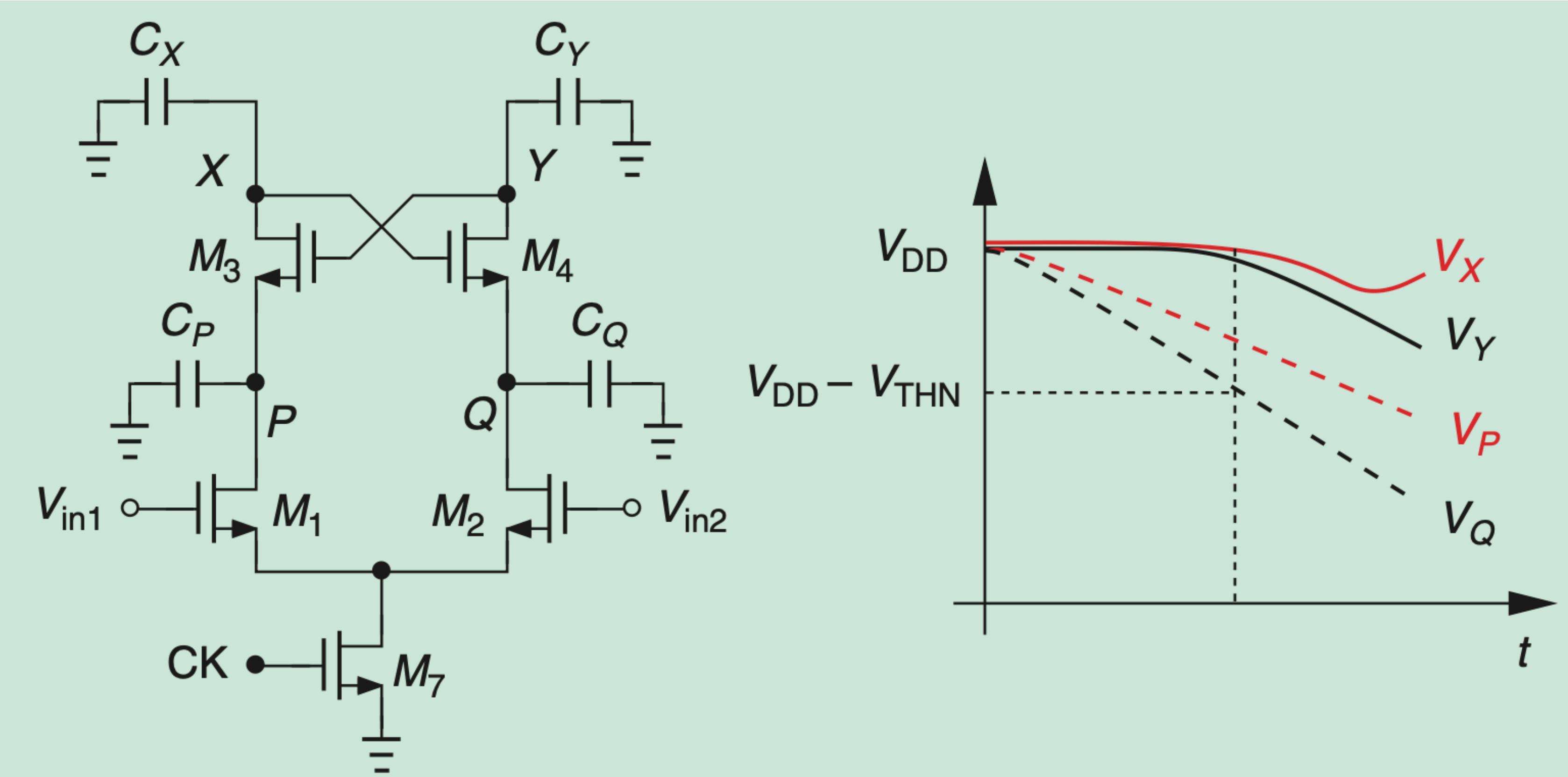
(2) Amplification



$$|V_P - V_Q| \approx (g_{m1,2}|V_{in1} - V_{in2}|/C_{P,Q})\, t$$

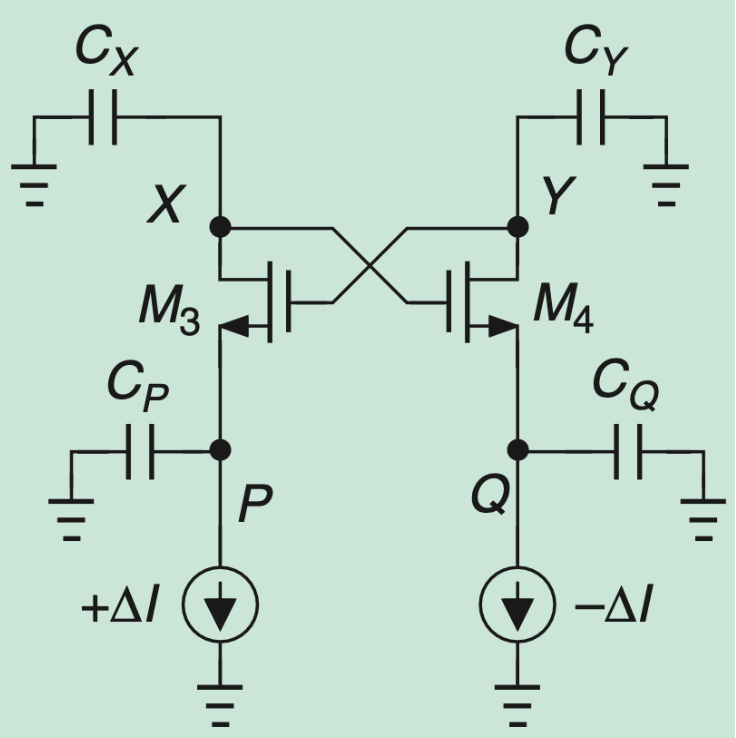
StrongARM Latch Comparator: Phase 3

(3) Turn-on of cross-coupled NMOS pair



StrongARM Latch Comparator: Phase 3

Equivalent circuit



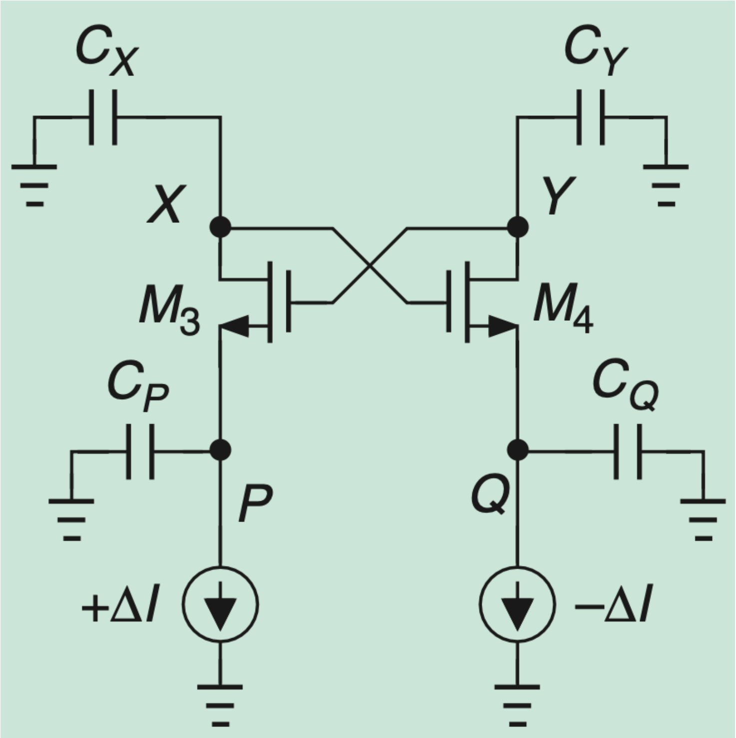
$$-C_X \frac{dV_X}{dt} = g_{m3}(V_Y - V_P)$$

$$-C_Y \frac{dV_Y}{dt} = g_{m4}(V_X - V_Q)$$

$$-C_P \frac{dV_P}{dt} = C_X \frac{dV_X}{dt} + \Delta I$$

$$-C_Q \frac{dV_Q}{dt} = C_Y \frac{dV_Y}{dt} - \Delta I.$$

Equivalent circuit



$$-C_X \frac{dV_X}{dt} = g_{m3}(V_Y - V_P)$$
$$-C_Y \frac{dV_Y}{dt} = g_{m4}(V_X - V_Q)$$
$$-C_P \frac{dV_P}{dt} = C_X \frac{dV_X}{dt} + \Delta I$$
$$-C_Q \frac{dV_Q}{dt} = C_Y \frac{dV_Y}{dt} - \Delta I.$$

$$-C_{X,Y} \frac{d(V_X - V_Y)}{dT} = g_{m3,4}(-V_X + V_Y - V_P + V_Q)$$

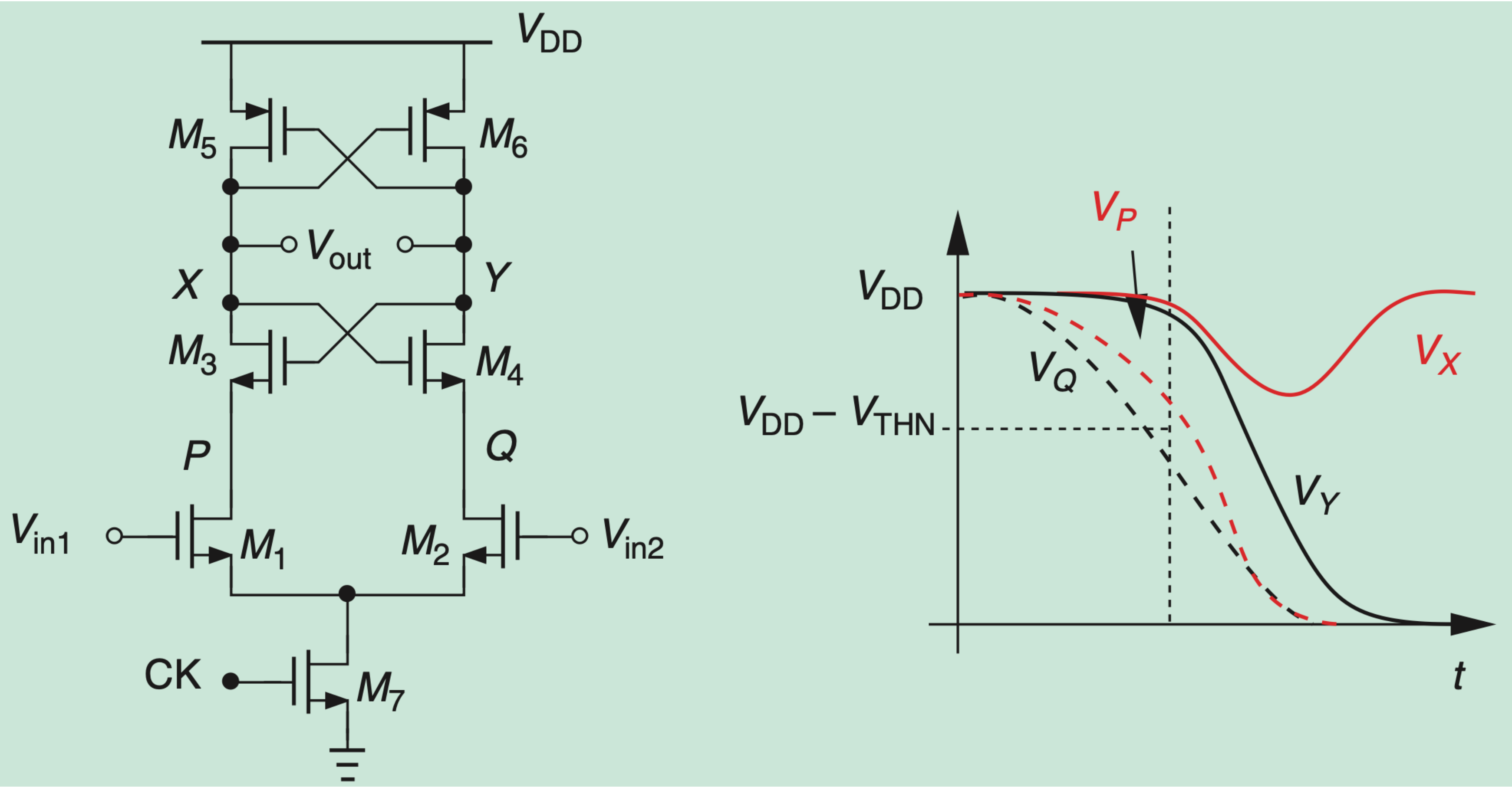
$$C_{P,Q}(V_Q - V_P) = C_{X,Y}(V_X - V_Y) + 2\Delta I t$$

$$C_{X,Y} \frac{d(V_X - V_Y)}{dt} - g_{m3,4}\left(1 - \frac{C_{X,Y}}{C_{P,Q}}\right)(V_X - V_Y) = -2 g_{m3,4} \frac{\Delta I}{C_{P,Q}} t.$$

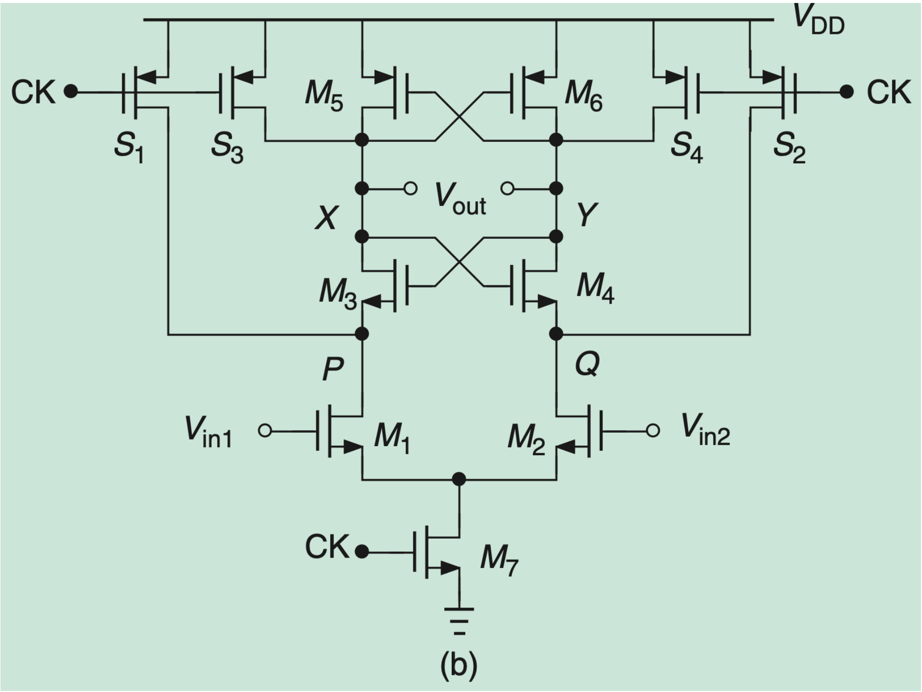
$$\tau_{reg} = \frac{C_{X,Y}}{g_{m3,4}(1 - C_{X,Y}/C_{P,Q})}$$

StrongARM Latch Comparator: Phase 4

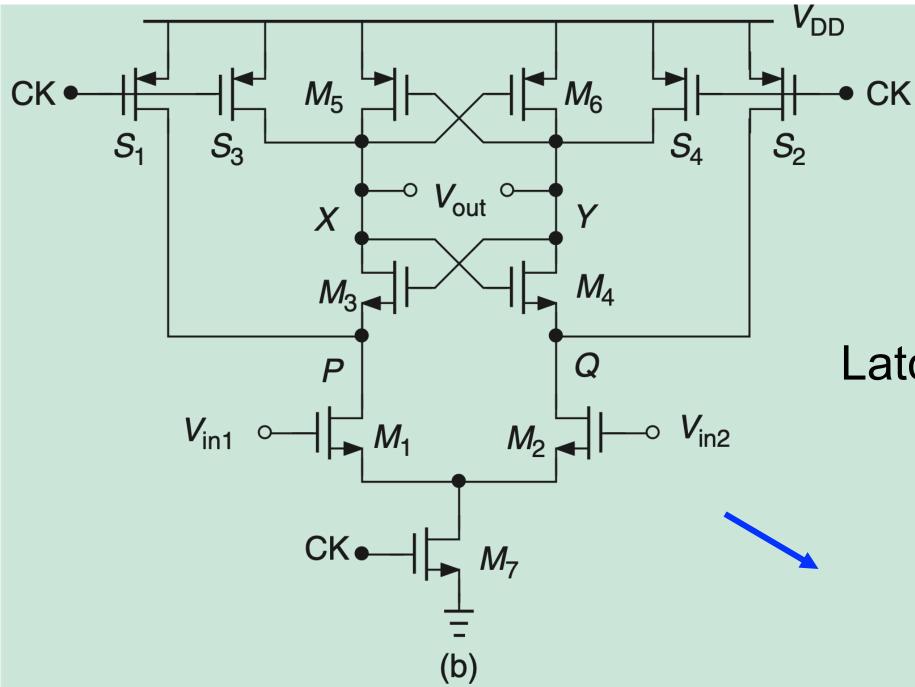
(4) Turn-on of cross-coupled PMOS pair



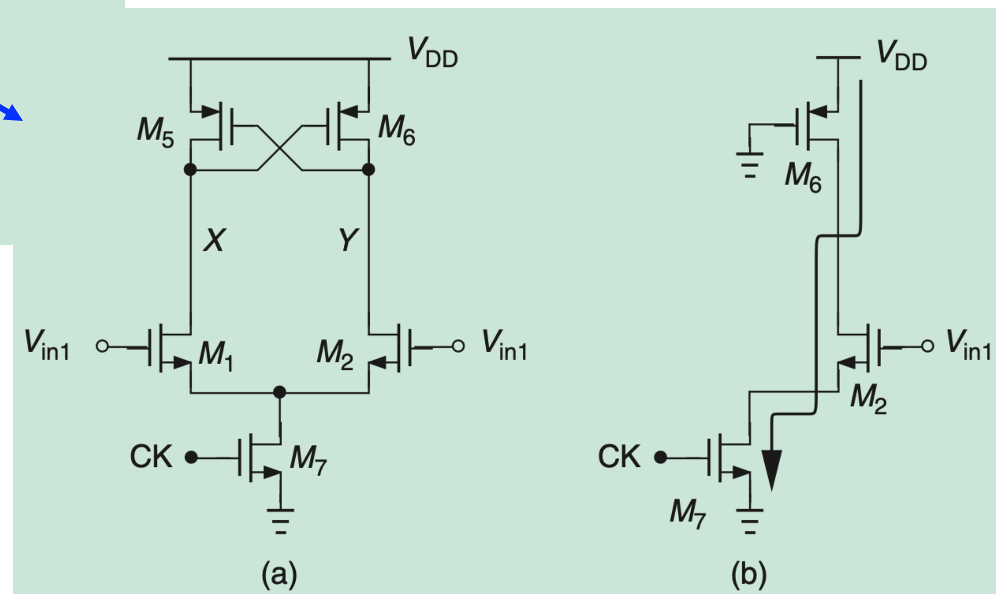
StrongARM Latch Comparator



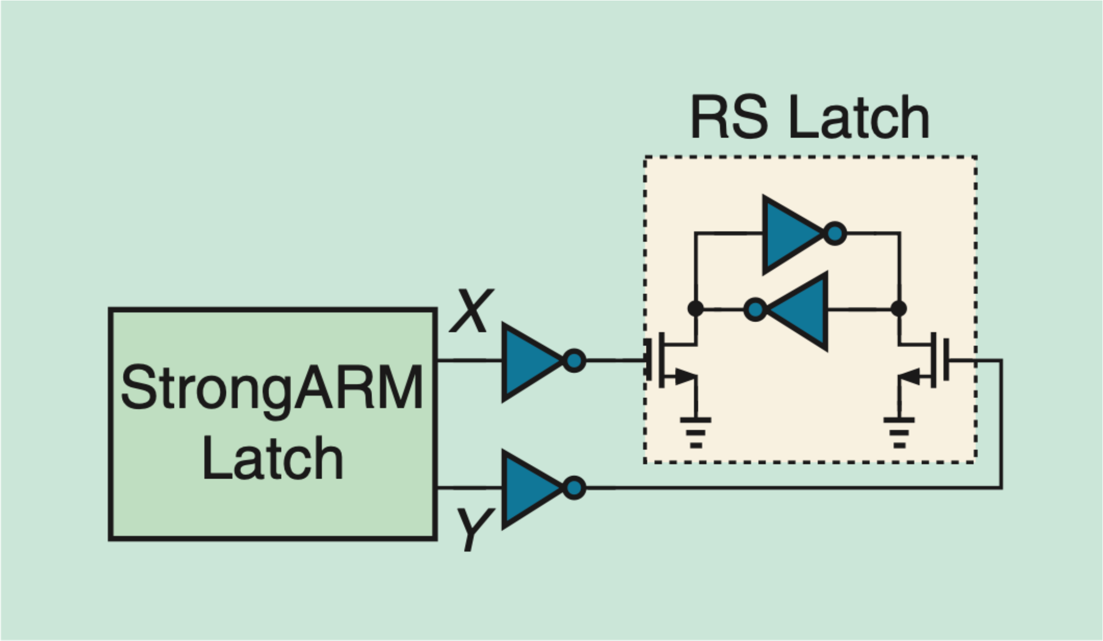
StrongARM Latch Comparator



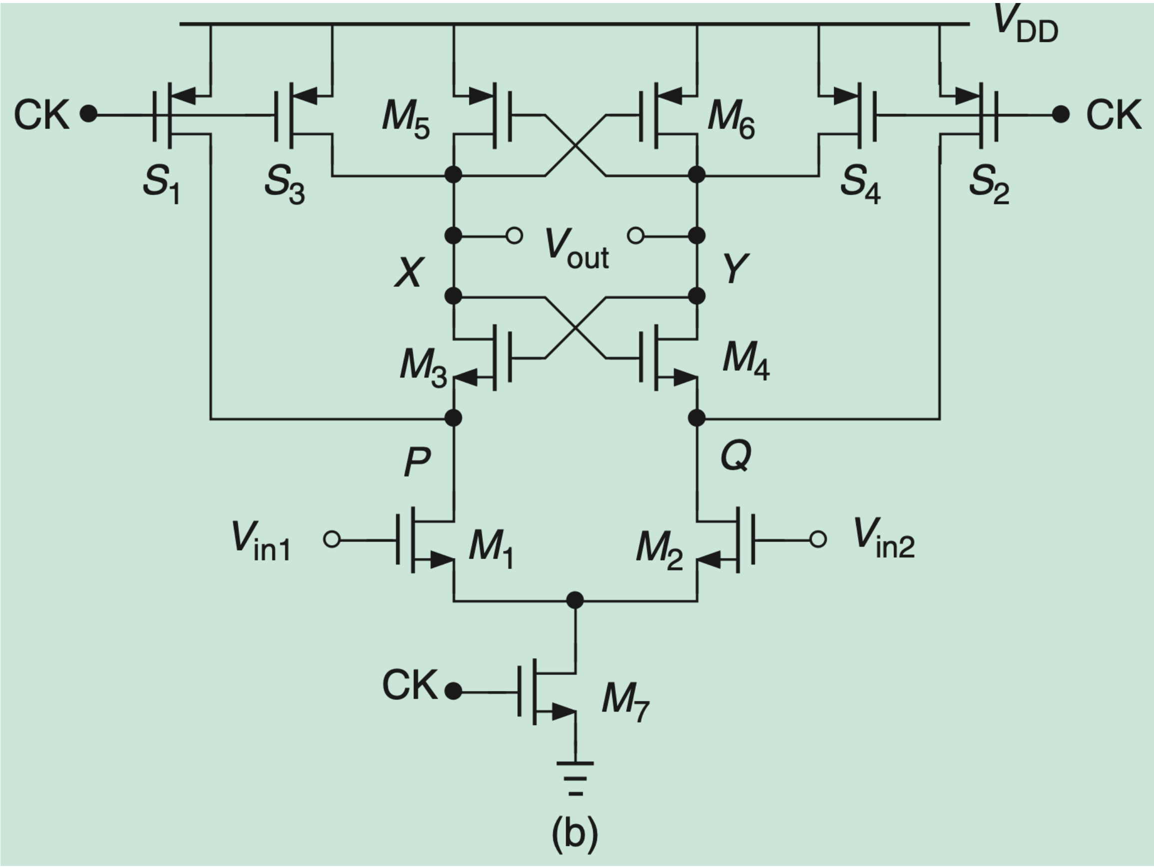
Latch without cross-coupled NMOS pair and the resulting static current



StrongARM latch followed by the RS latch



StrongARM Latch: Offset



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