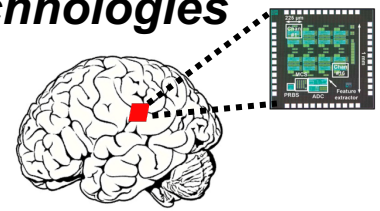
Integrated Neurotechnologies Laboratory

EPFL



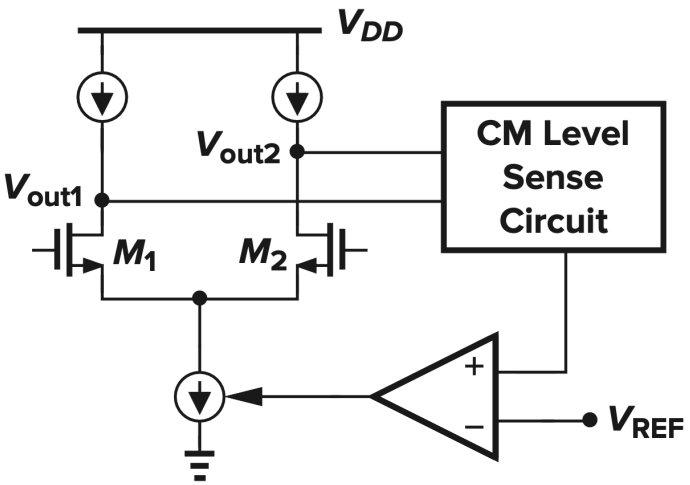
Advanced analog integrated circuit design (EE-523), Lecture 4

Prof. Mahsa Shoaran

Institutes of Electrical and Micro Engineering and Neuro-X, School of Engineering, EPFL

Recap: CMFB

- High-gain differential circuits require **“common-mode feedback” (CMFB)**



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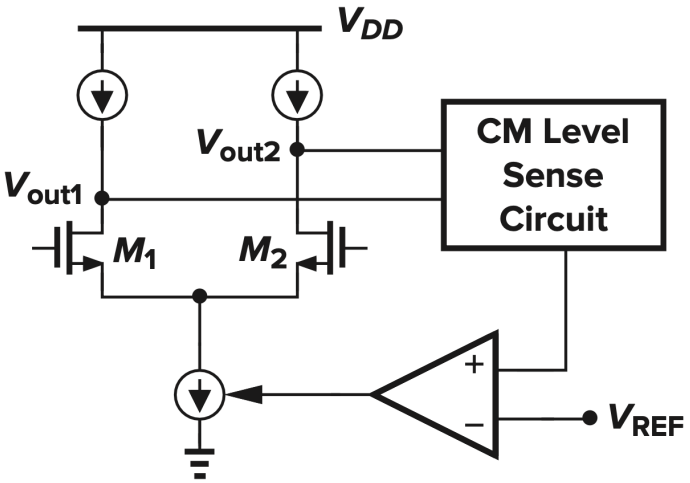
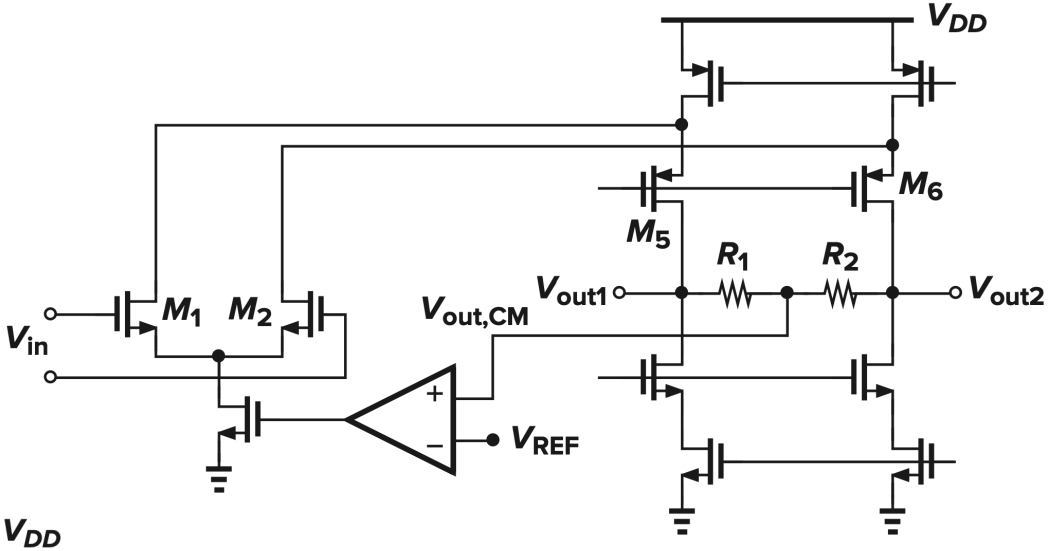
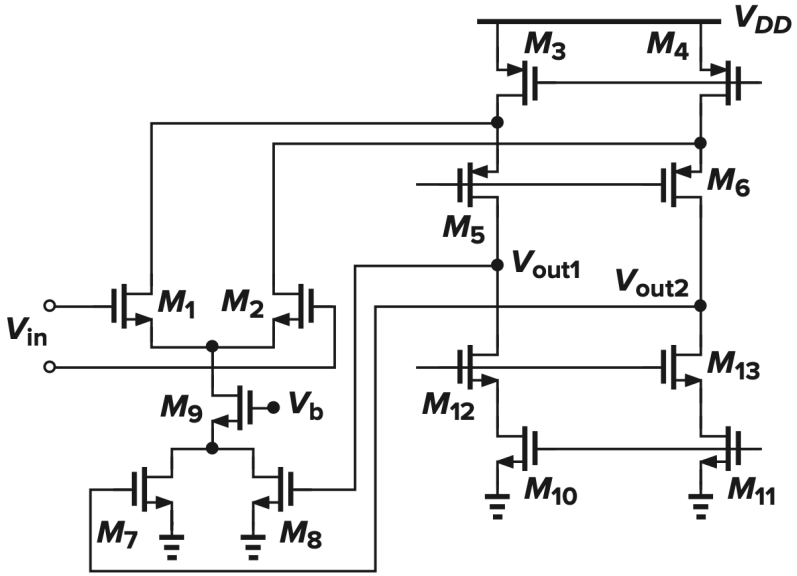
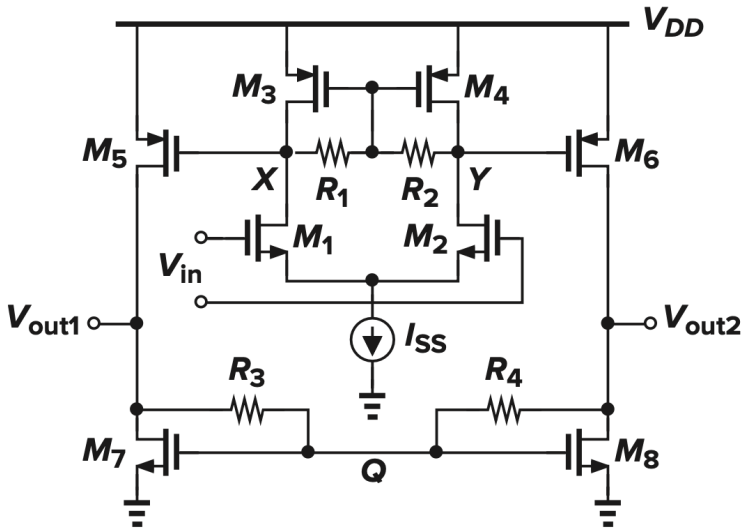
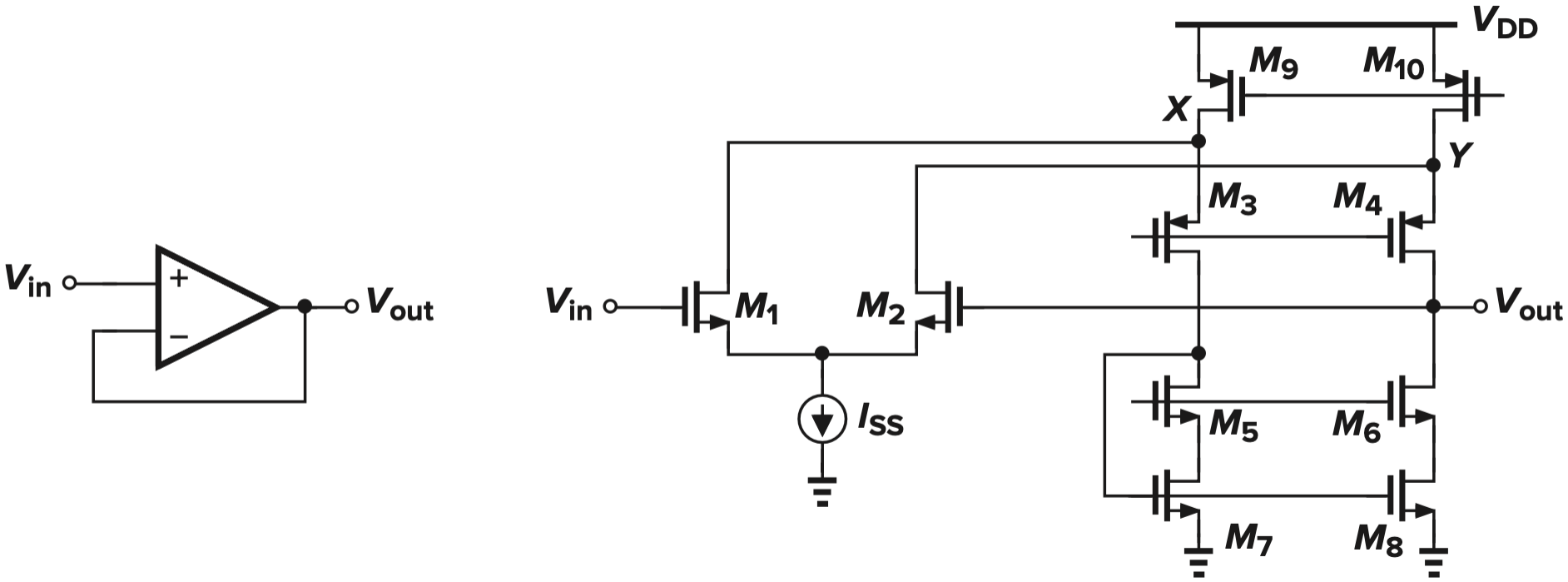






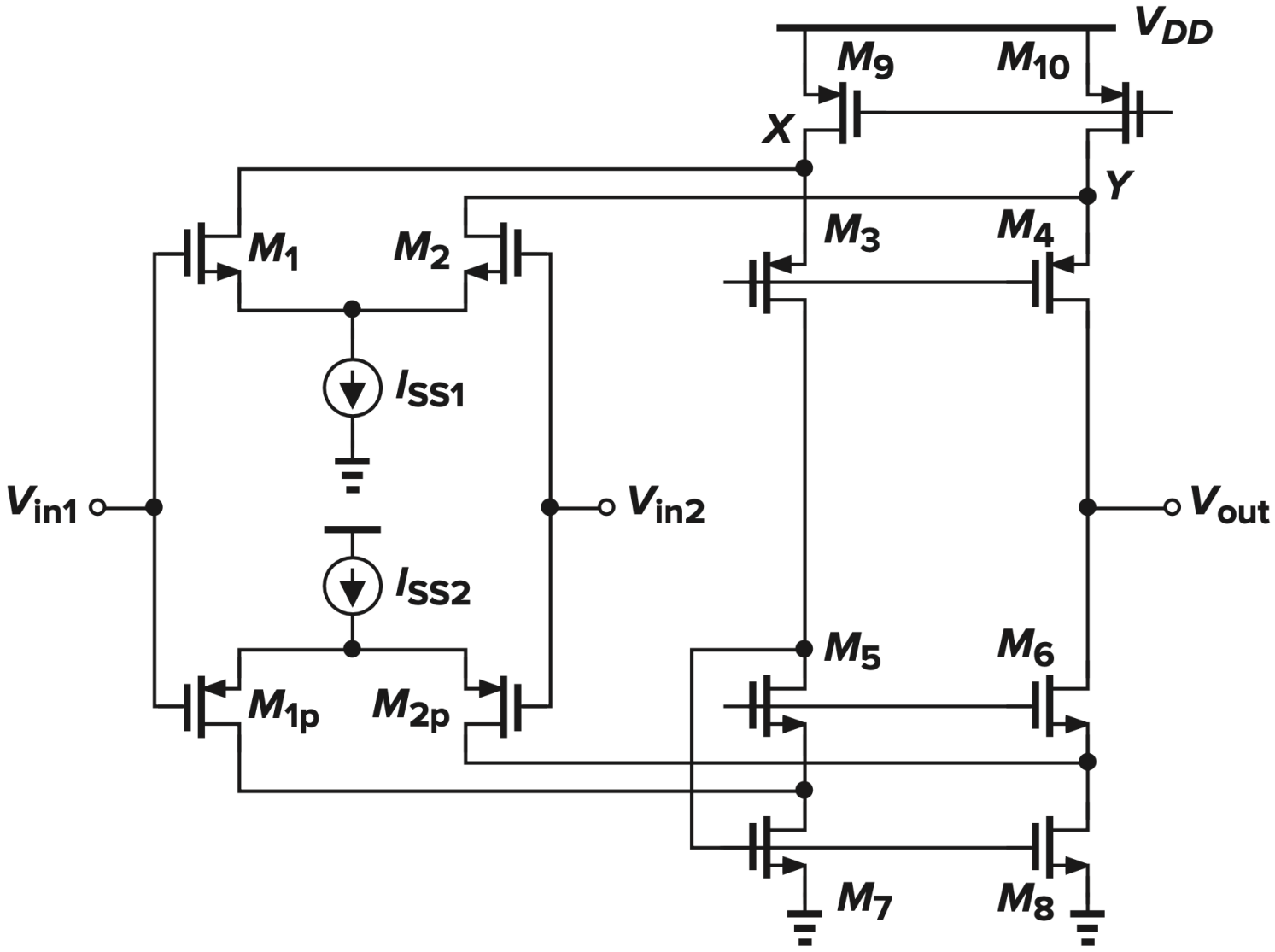


Input Range



$$V_{in,min} \approx V_{out,min} = V_{GS1,2} + V_{ISS}$$

Input Range Extension



Why Switched-Capacitor Circuits?

- **Continuous-time circuits**: Input and output are continuous signals
- **Discrete-time circuits:** Process input "at periodic instants of time and generates output at the end of each period. Example: **switched-capacitor (SC) circuits**

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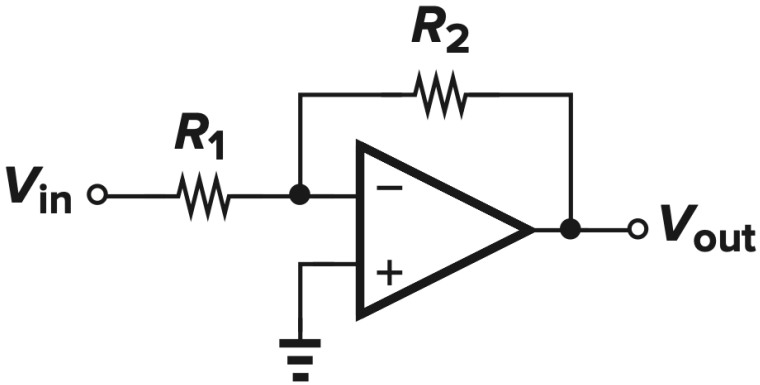
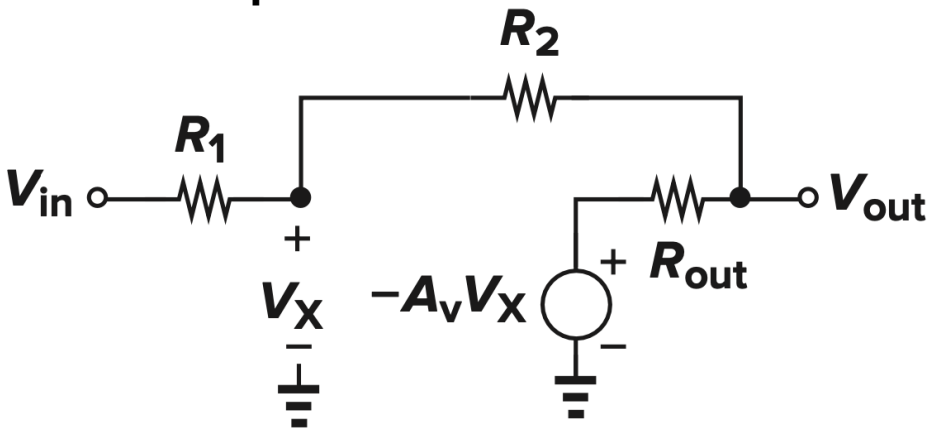
Continuous-time feedback amplifier

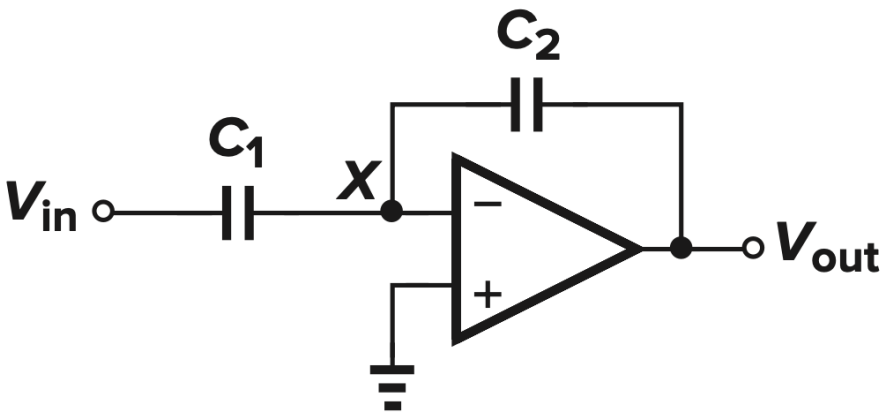




$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \cdot \frac{A_v - \dfrac{R_{out}}{R_2}}{1 + \dfrac{R_{out}}{R_1} + A_v + \dfrac{R_2}{R_1}}$$

Continuous-time Feedback Amplifier with Capacitors

- To avoid reducing the open-loop gain of the op amp, perhaps we can replace the resistors by capacitors:



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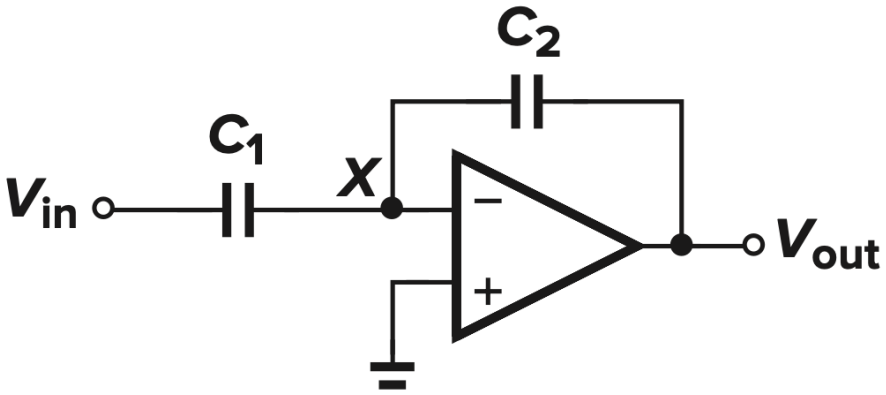
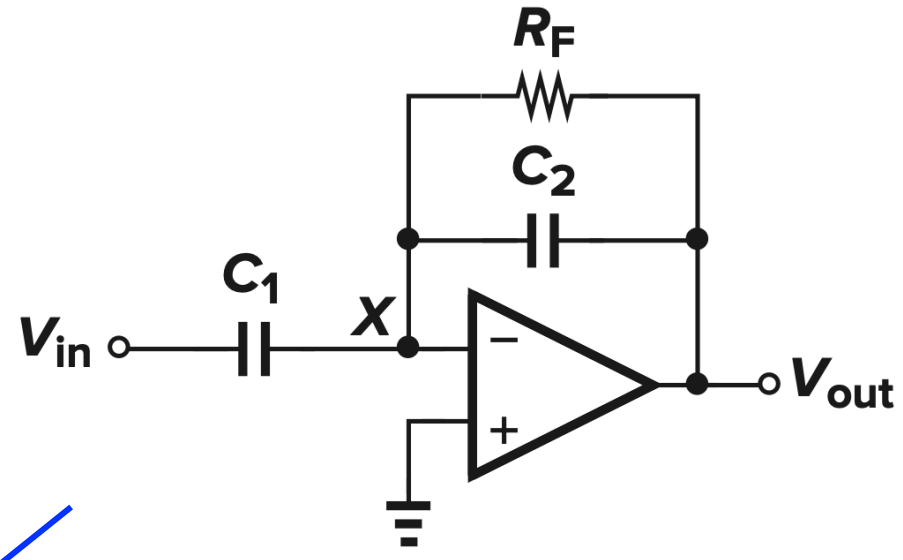


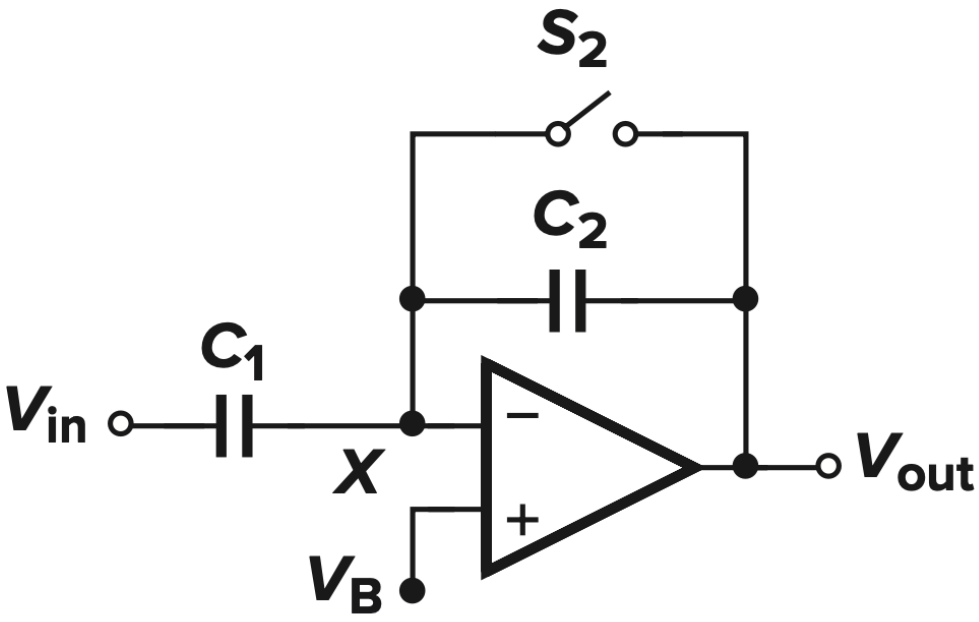


$$\frac{V_{out}}{V_{in}}(s) \approx -\frac{R_F \dfrac{1}{C_2 s}}{R_F + \dfrac{1}{C_2 s}} \div \frac{1}{C_1 s}$$

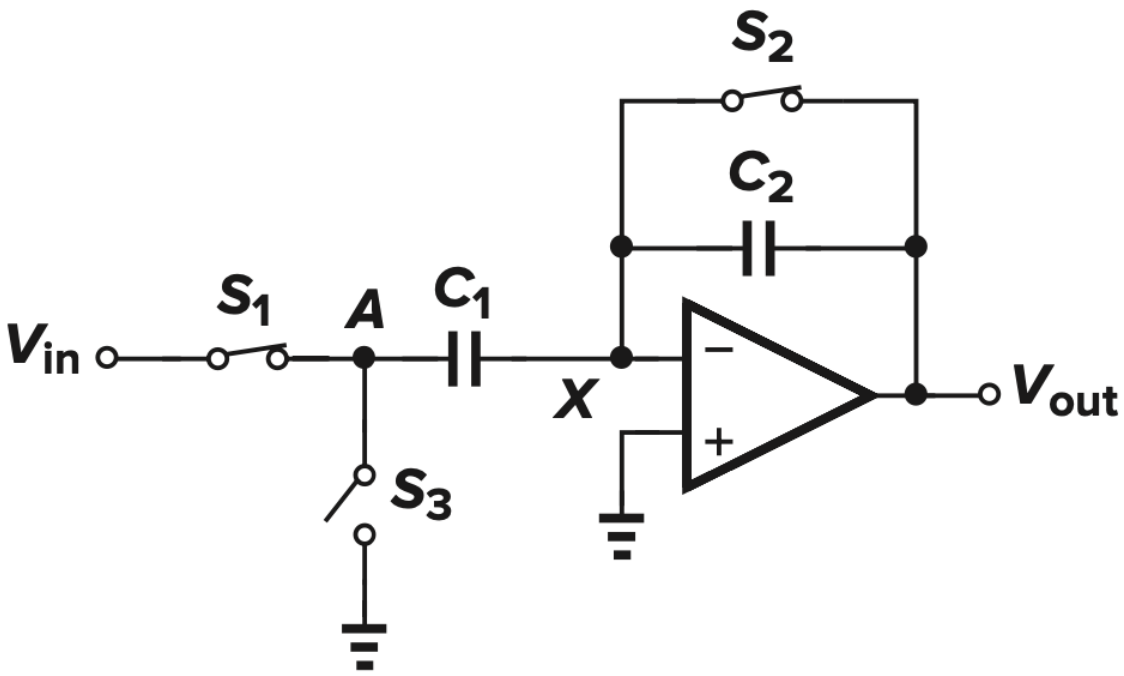
$$= -\frac{R_F C_1 s}{R_F C_2 s + 1}$$

$V_{out}/V_{in} \approx -C_1/C_2$ only if $\omega \gg (R_F C_2)^{-1}$

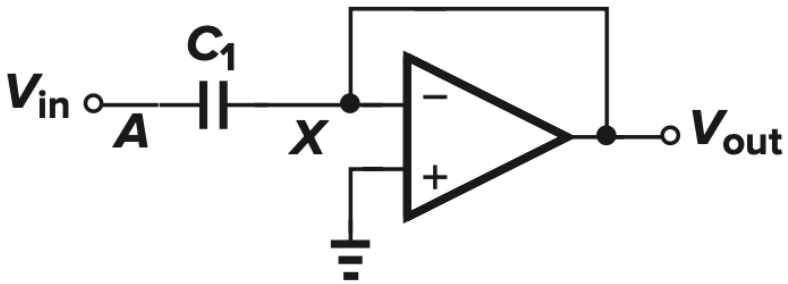
Use of Feedback Switch to Define DC Input Level



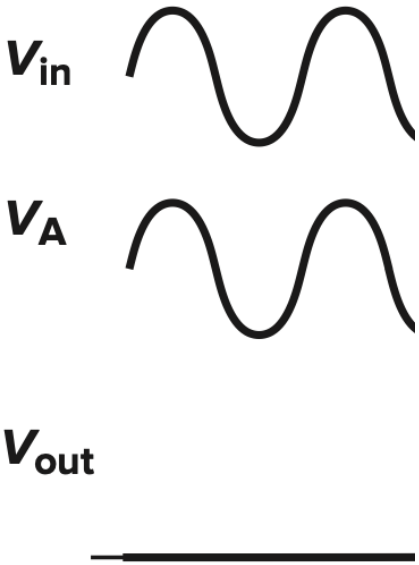
Switched-Capacitor Amplifier



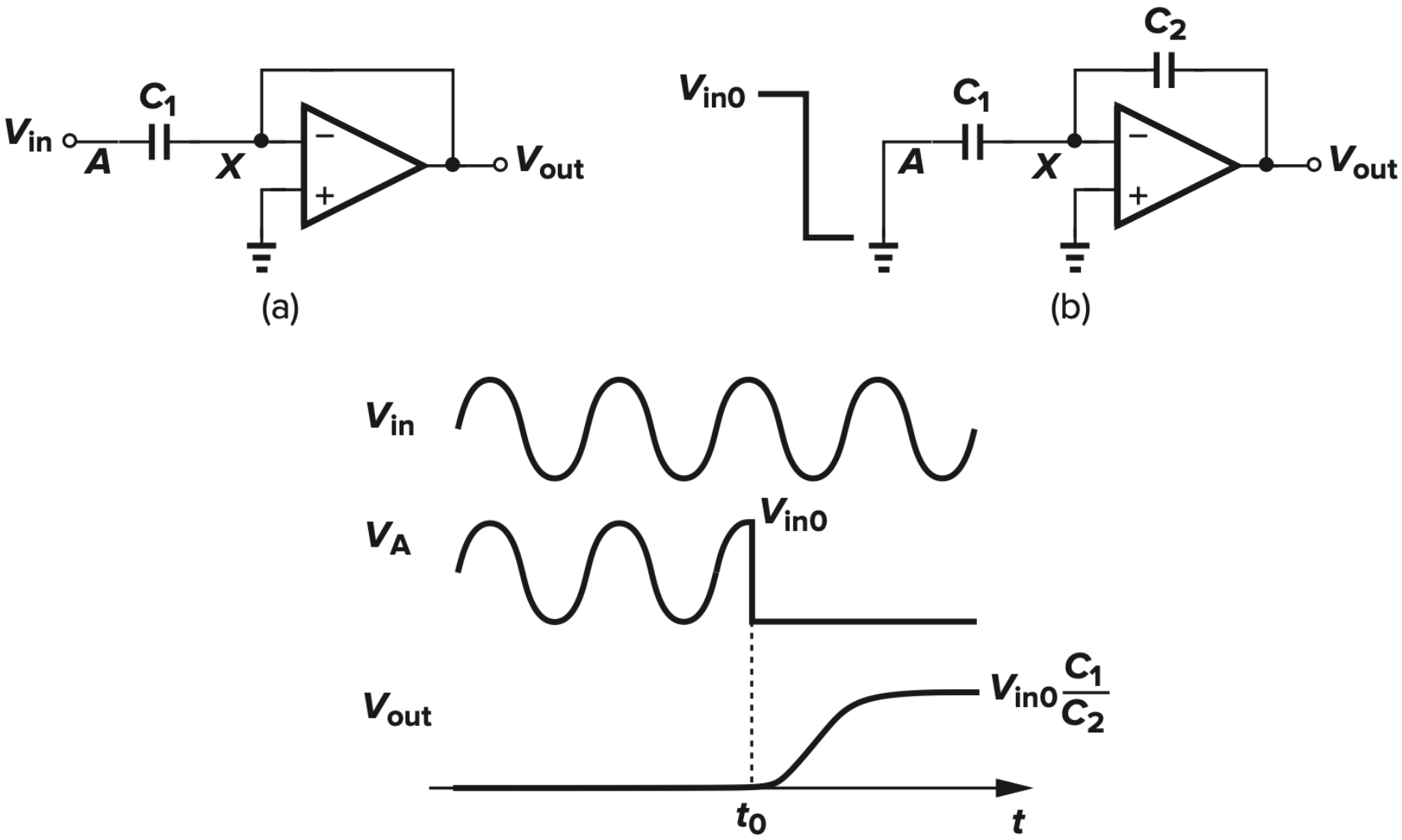
Switched-Capacitor Amplifier



(a)



Switched-Capacitor Amplifier



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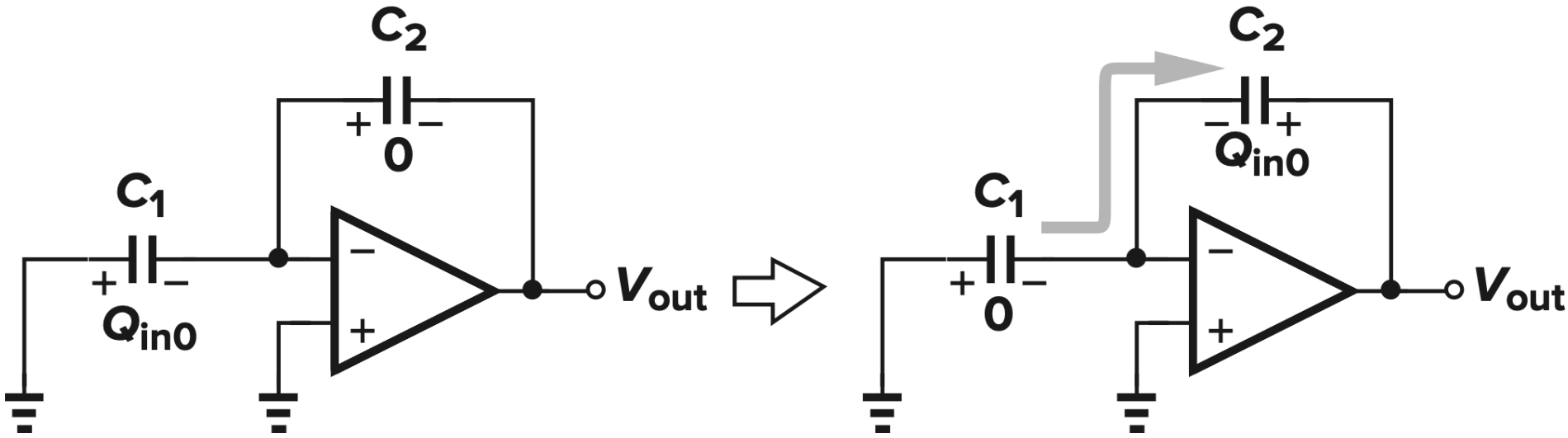
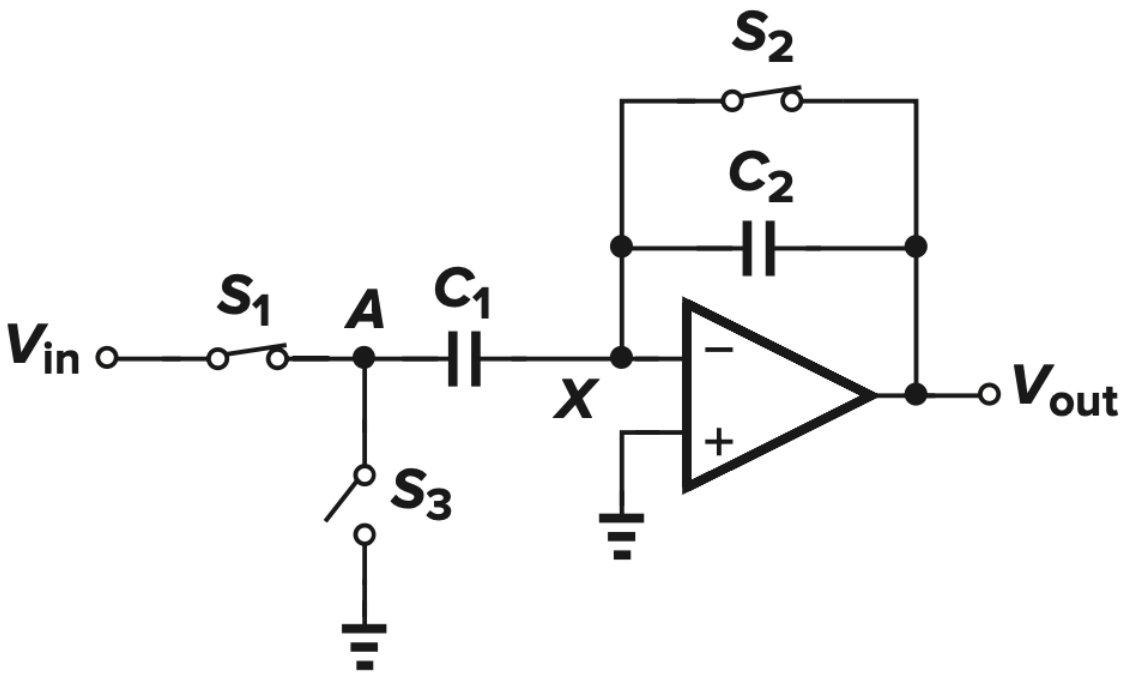
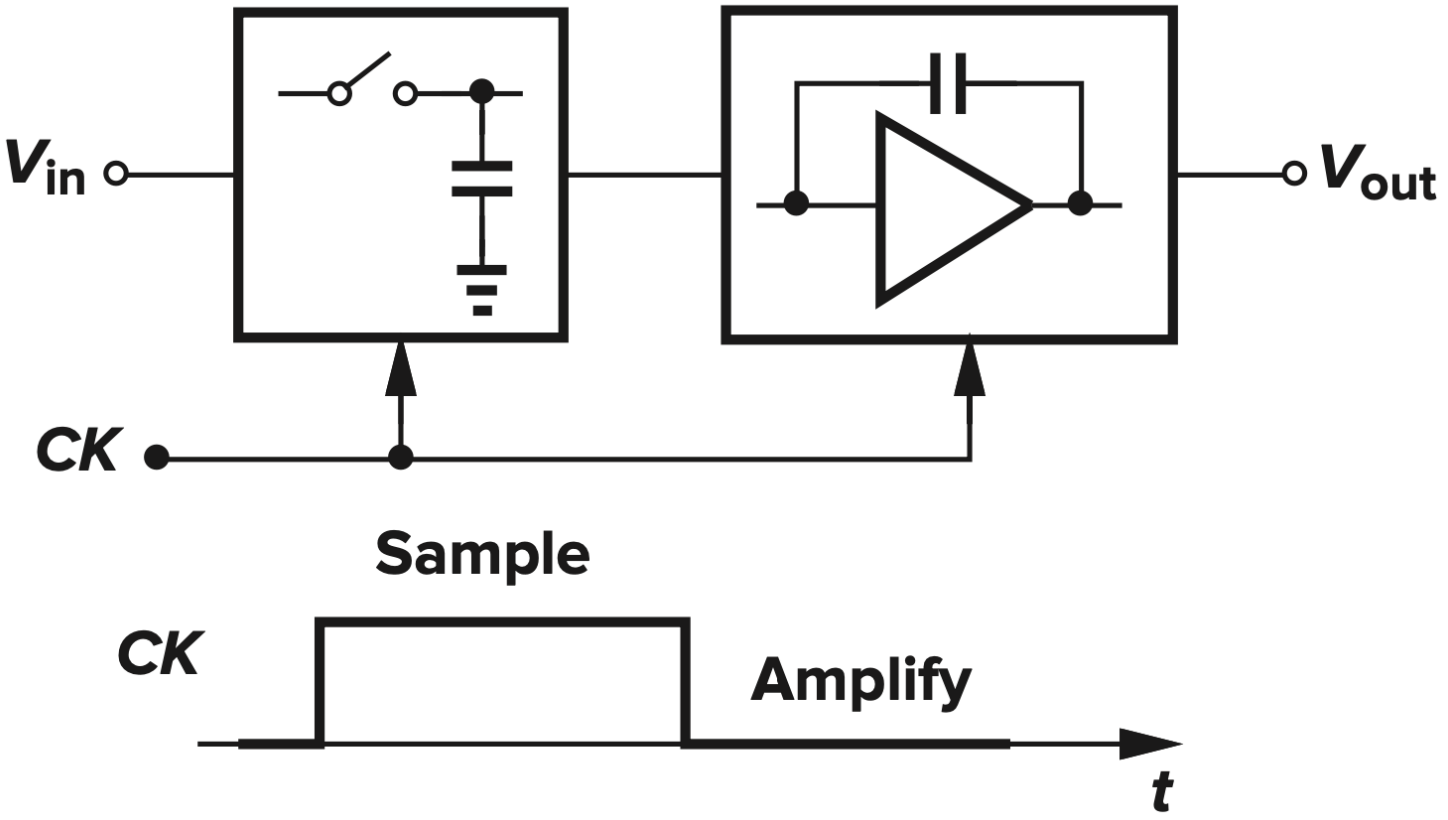


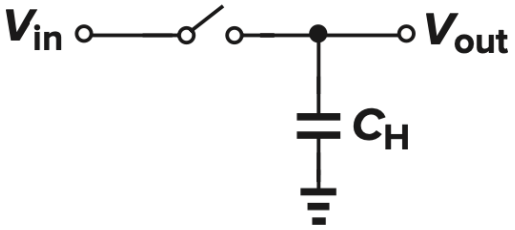
Discrete-time vs. Continuous-time

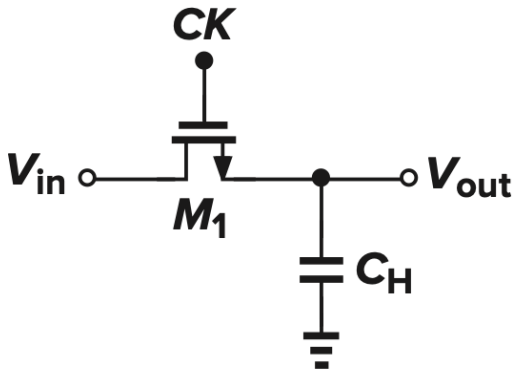


Switched-Capacitor Amplifier: General View



Simple sampling circuit





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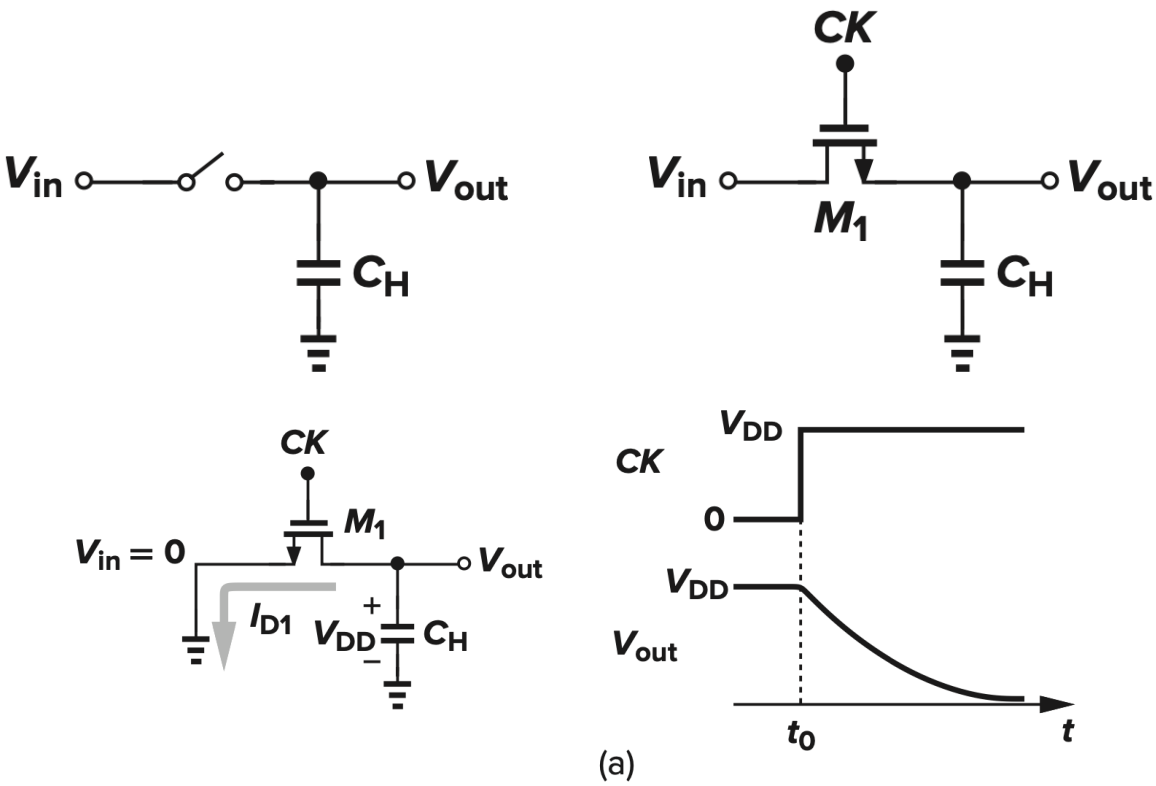

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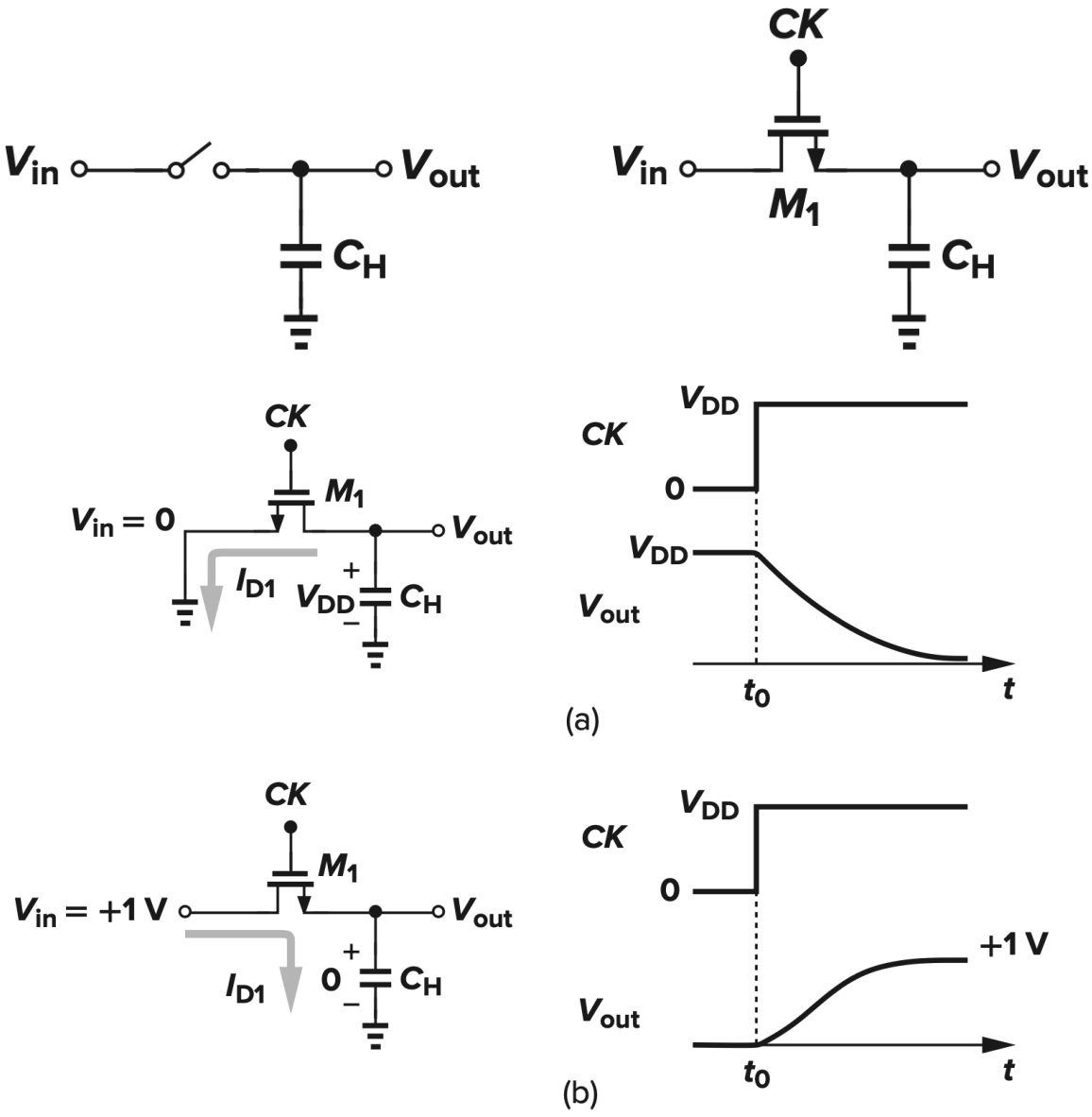
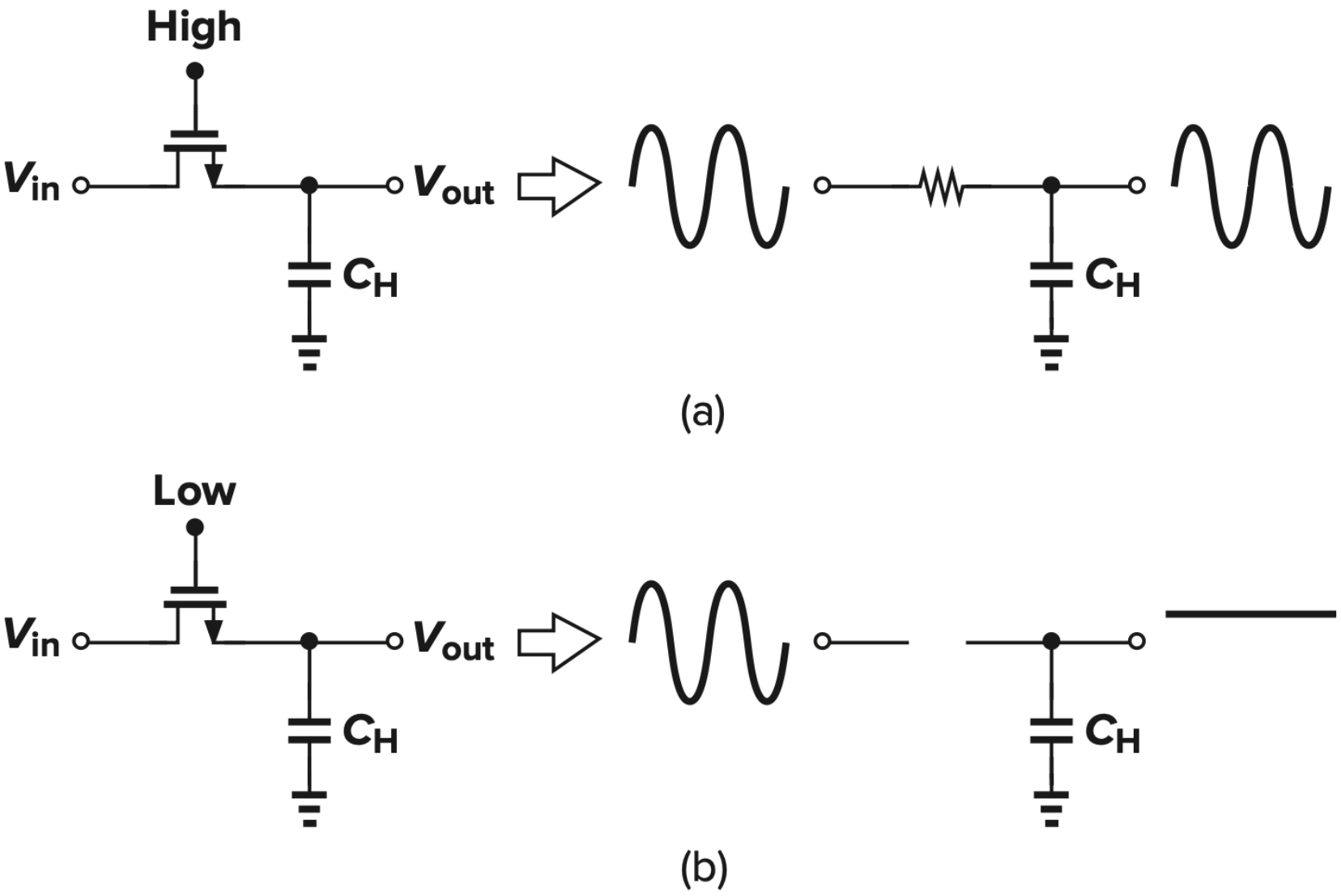
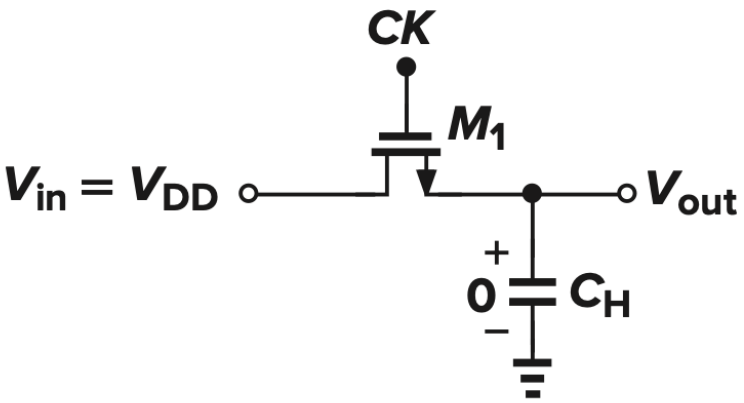
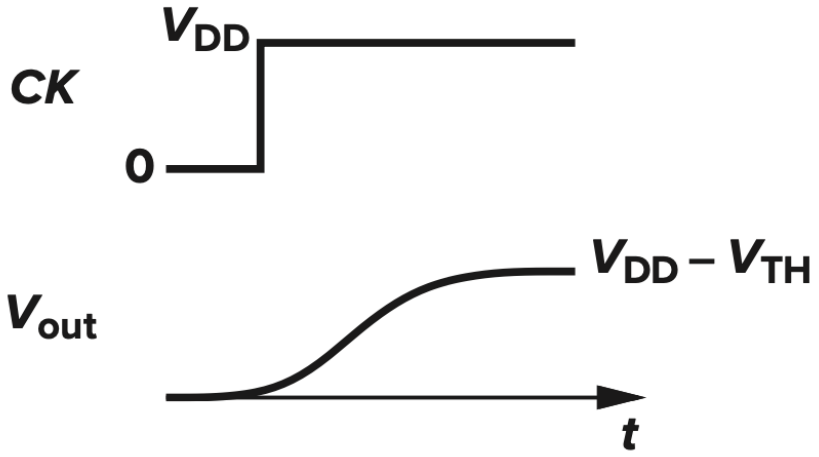


Track and hold



Maximum output level in an NMOS sampler





$$C_H \frac{dV_{out}}{dt} = I_{D1}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{out} - V_{TH})^2$$

$$\frac{dV_{out}}{(V_{DD} - V_{out} - V_{TH})^2} = \frac{1}{2}\mu_n \frac{C_{ox}}{C_H}\frac{W}{L}dt$$

$$\frac{1}{V_{DD} - V_{out} - V_{TH}}\Bigg|_0^{Vout} = \frac{1}{2}\mu_n \frac{C_{ox}}{C_H}\frac{W}{L}t\Bigg|_0^t$$

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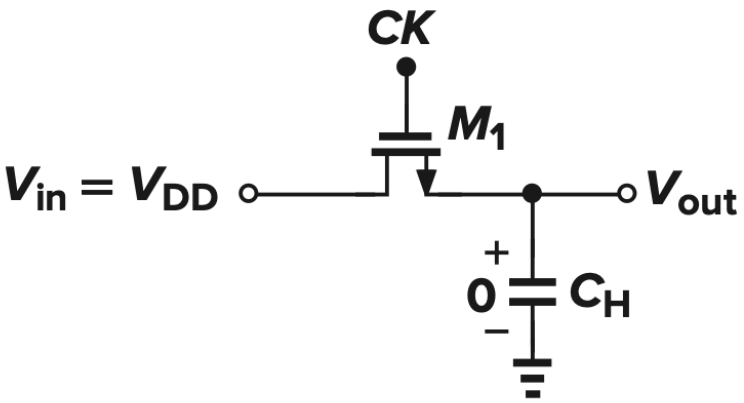

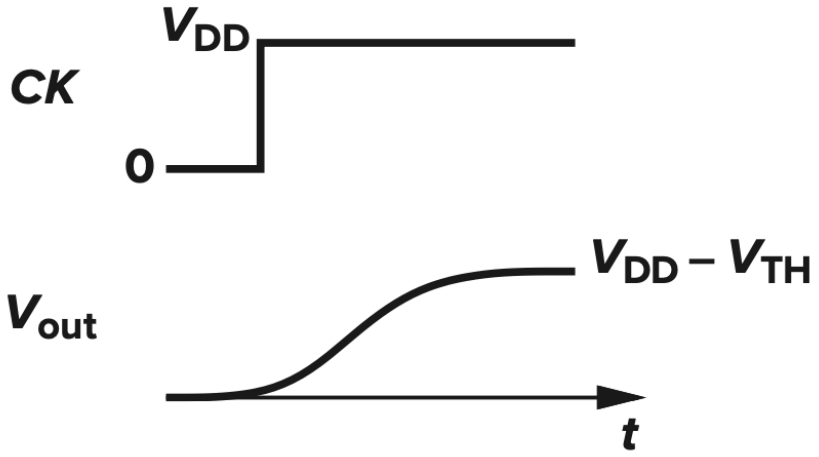

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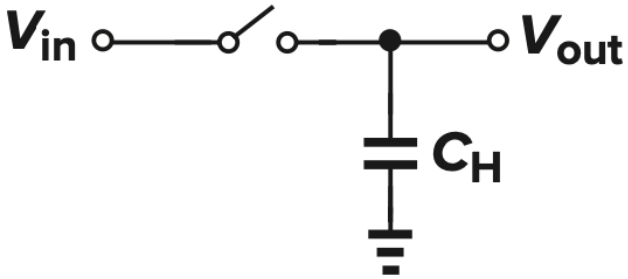
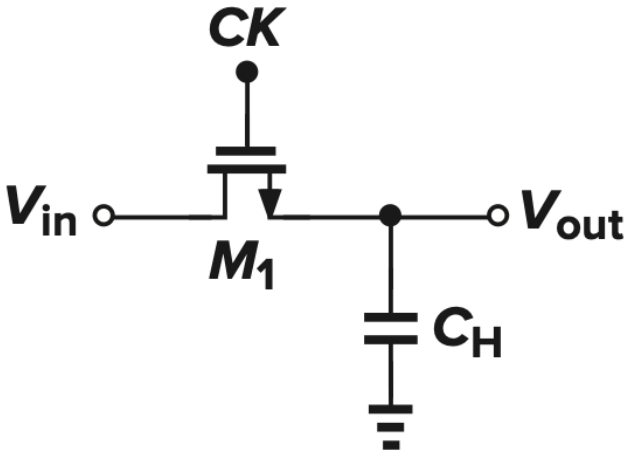
$$V_{out} = V_{DD} - V_{TH} - \frac{1}{\frac{1}{2}\mu_n \frac{C_{ox}}{C_H}\frac{W}{L}t + \frac{1}{V_{DD} - V_{TH}}}$$

NMOS and PMOS Switches





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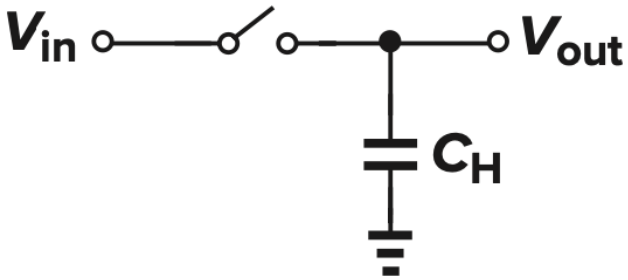
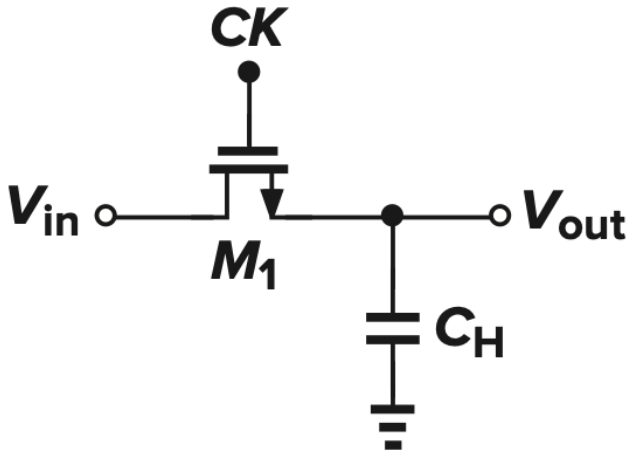
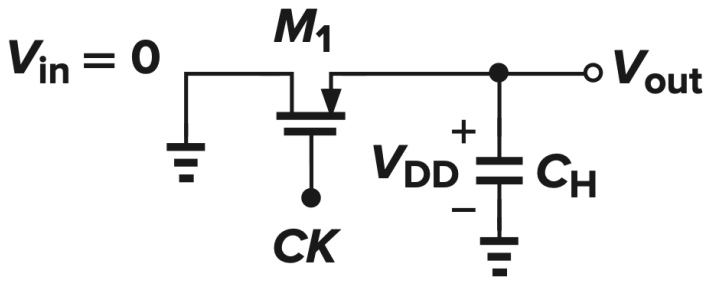
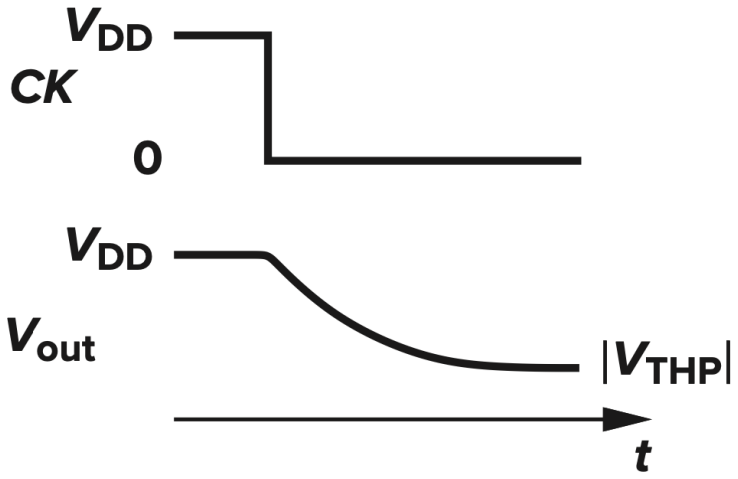
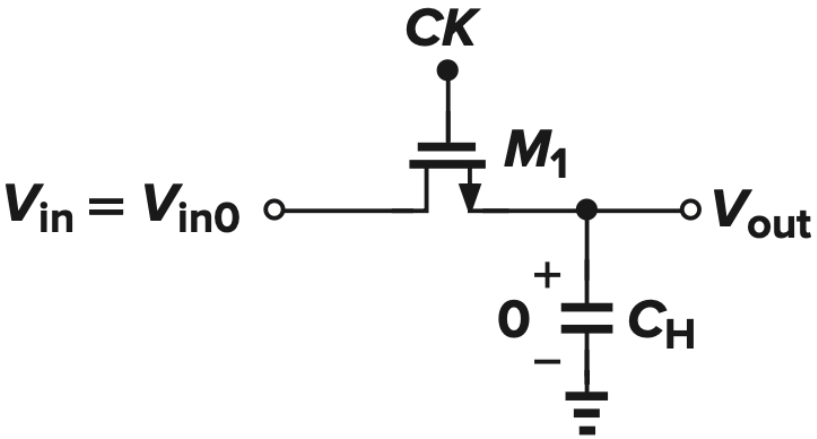


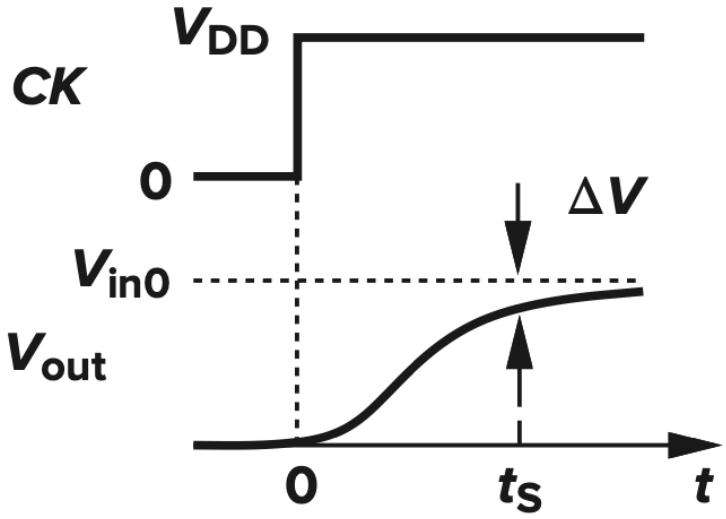






Speed Considerations





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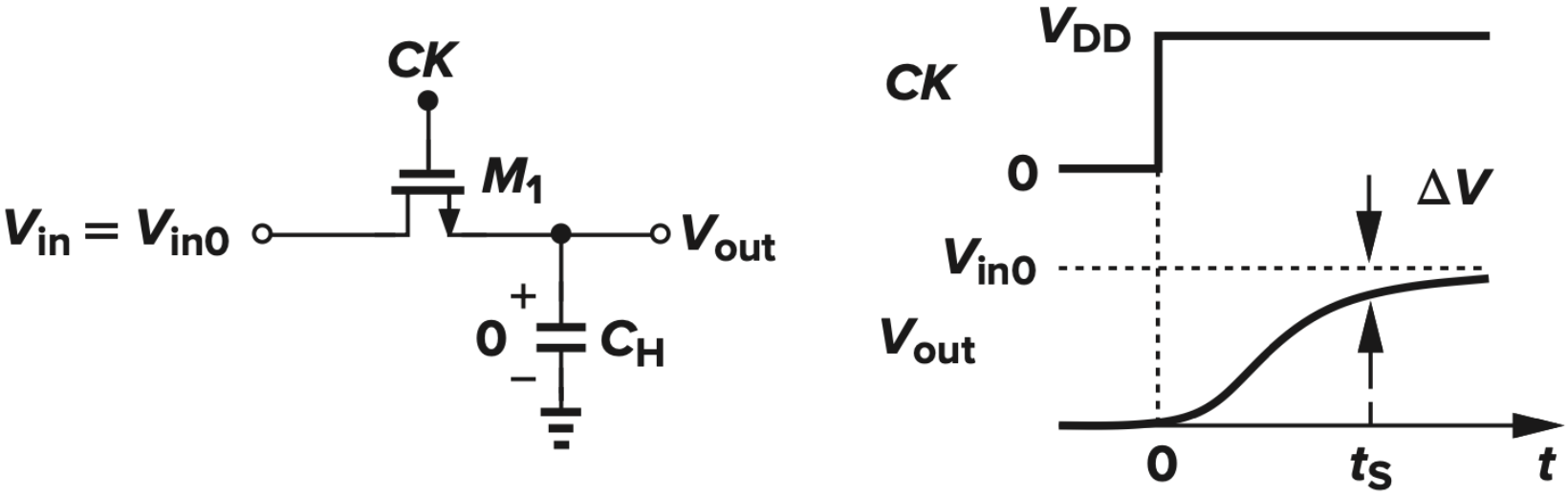
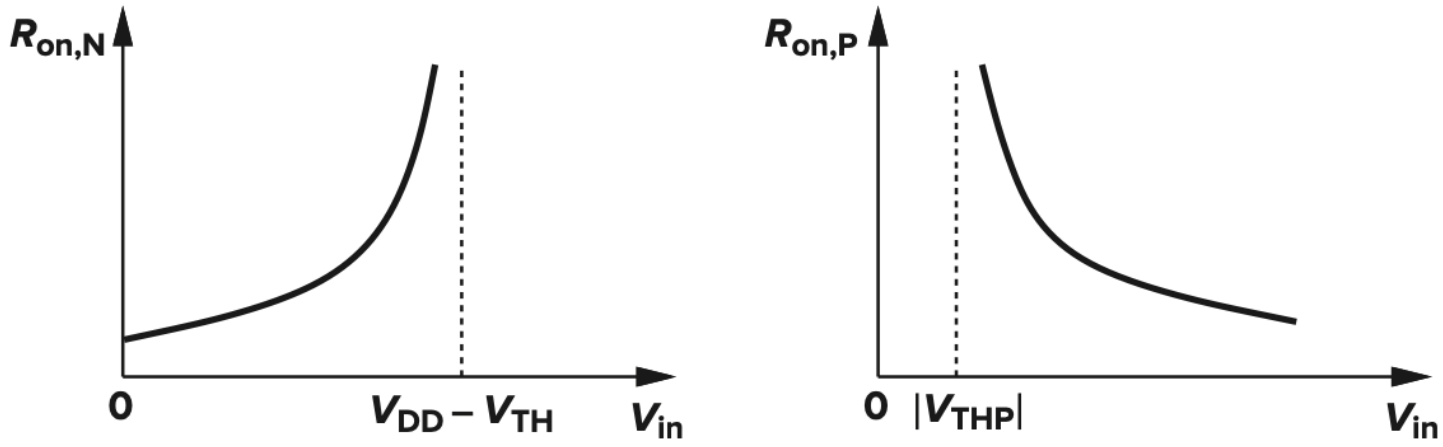
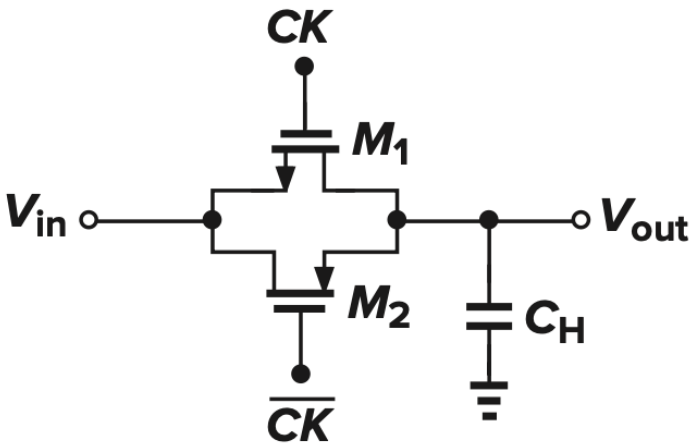


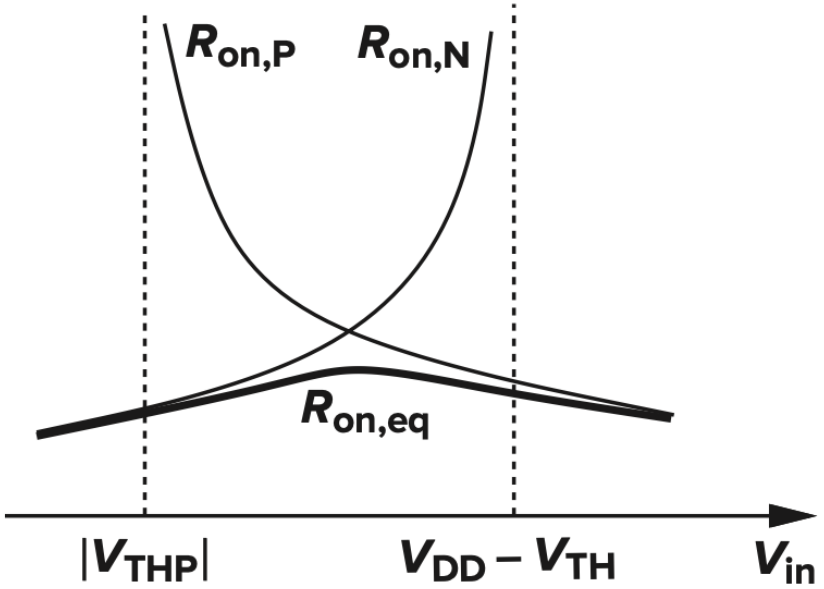
On-resistance of NMOS and PMOS devices as a function of input voltage



Speed Considerations: Complementary Switch

On-resistance of the complementary switch

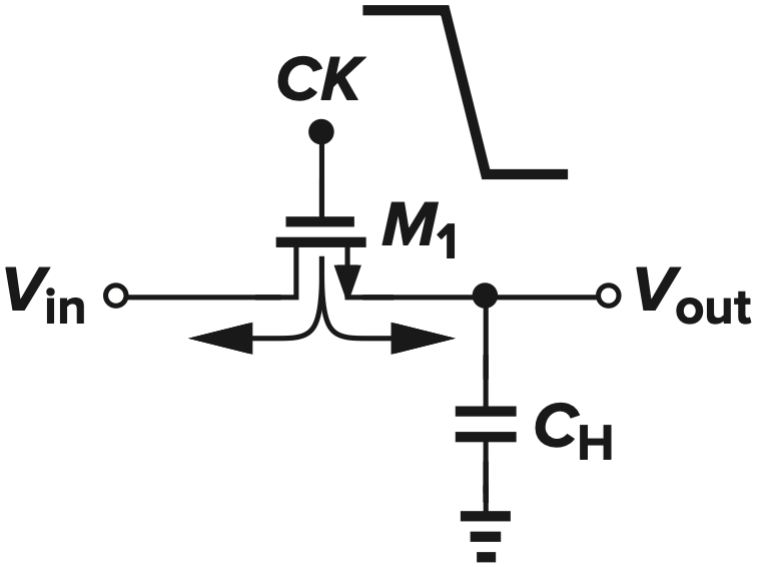




Precision Considerations

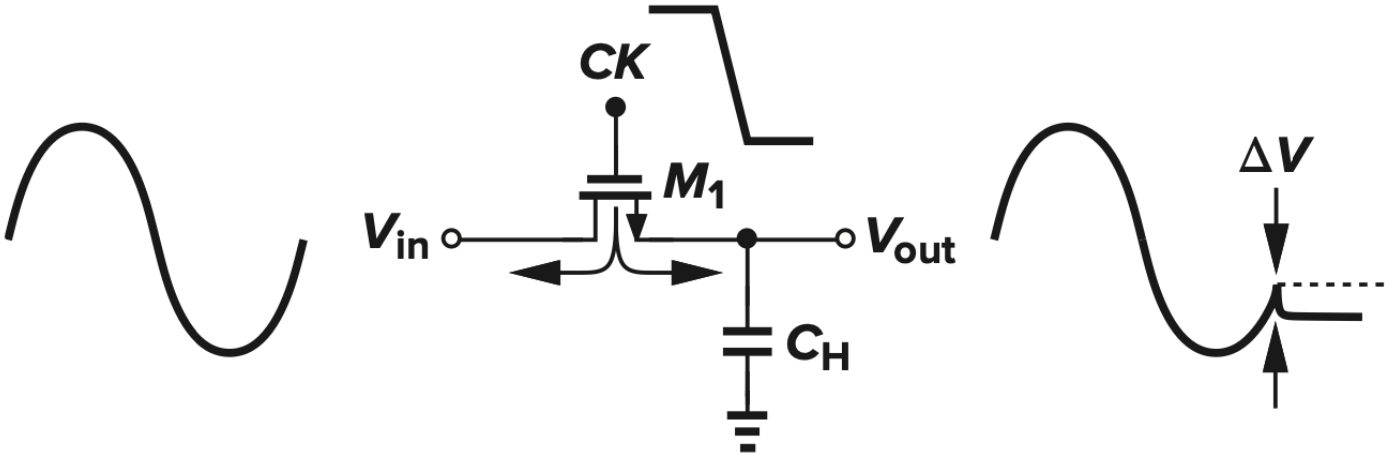
- **A larger *W*/*L* or a smaller sampling capacitor** in MOS switches results in a **higher speed**.
- However, these methods of increasing the speed **degrade the precision with which the signal is sampled**
- Three mechanisms in MOS transistor operation introduce error at the instant the switch turns off:
  - **Channel Charge Injection**
  - **Clock Feedthrough**
  - ***kT*/*C* Noise**

Channel Charge Injection



$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

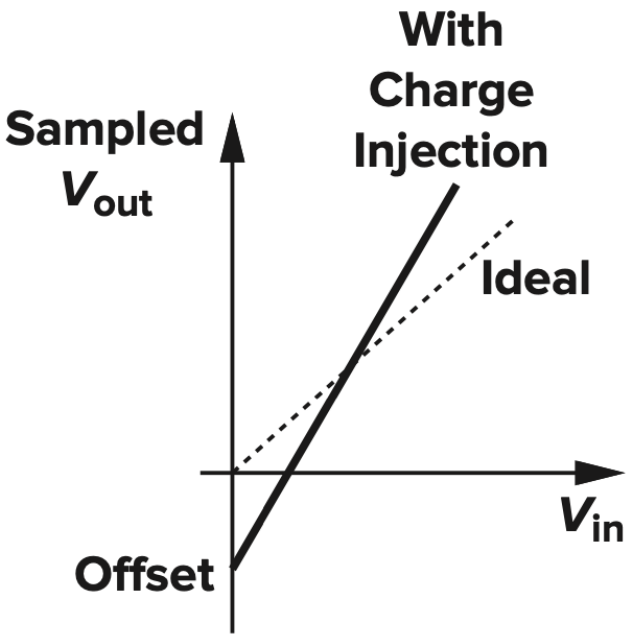
$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}$$



Channel Charge Injection

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$$



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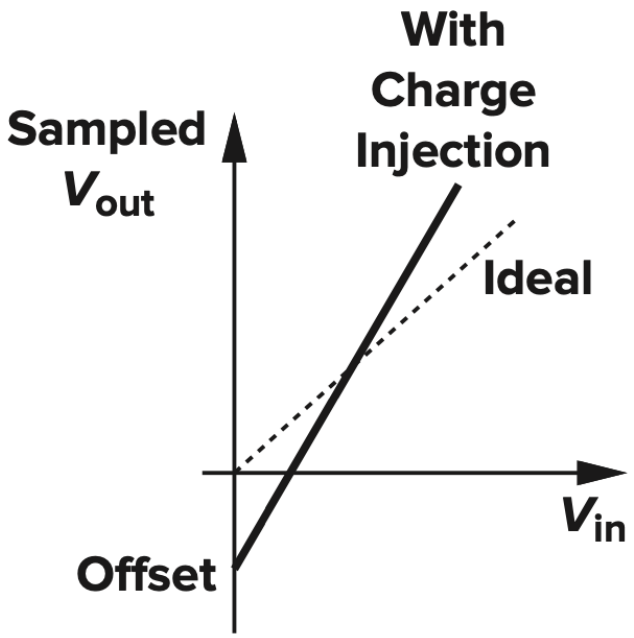


$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$$

Speed-Precision Trade-off due to Charge Injection

$$F = (\tau \Delta V)^{-1}$$

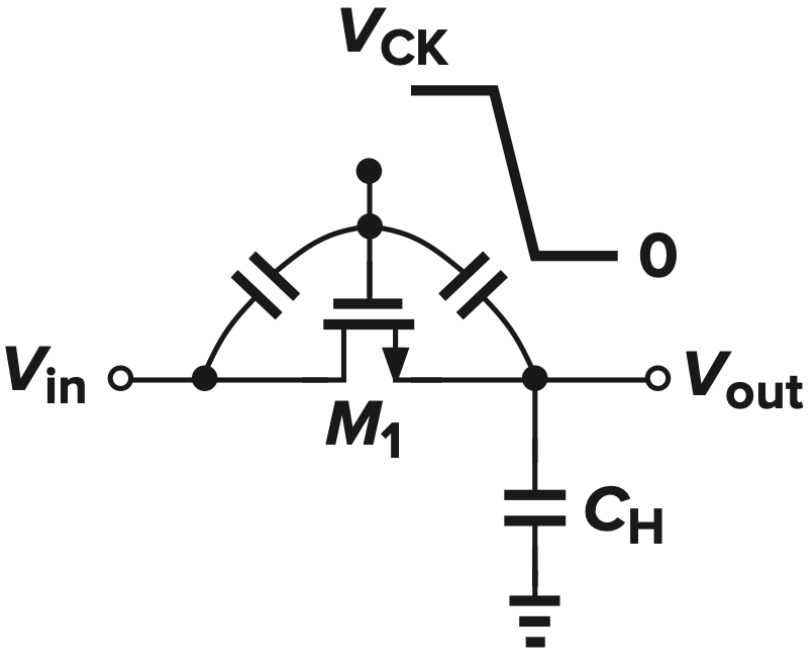
$$\tau = R_{on} C_H$$

$$= \frac{1}{\mu_n C_{ox} (W/L)(V_{DD} - V_{in} - V_{TH})} C_H$$

$$\Delta V = \frac{WLC_{ox}}{C_H} (V_{DD} - V_{in} - V_{TH})$$

$$F = \frac{\mu_n}{L^2}$$

Clock Feedthrough

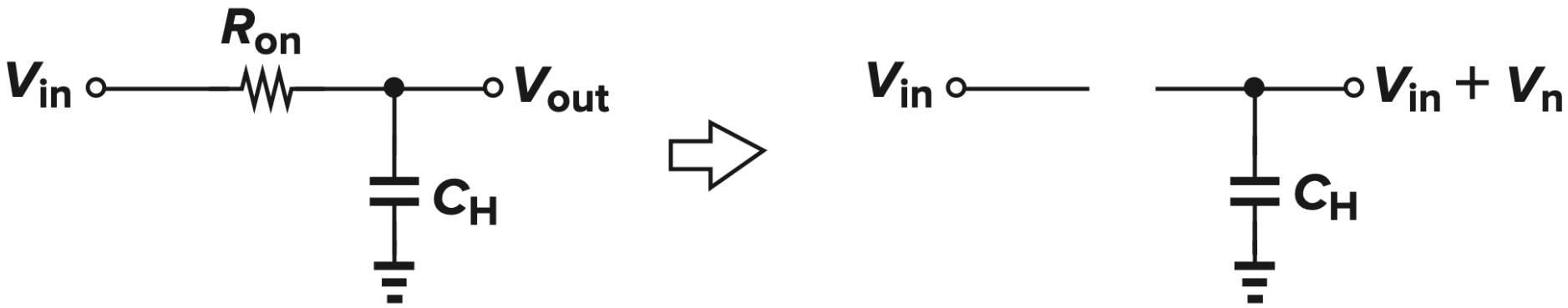


$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H}$$

kT/C Noise

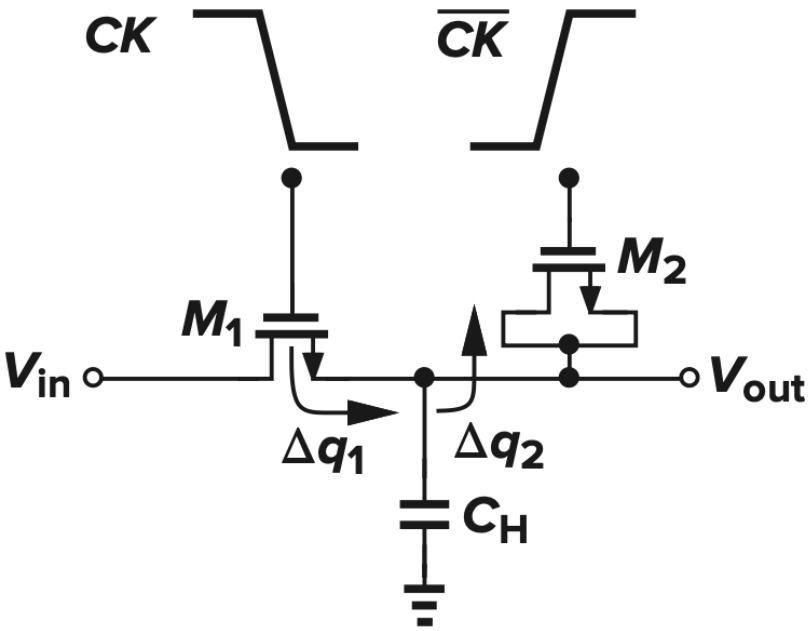
- The on-resistance of the switch introduces thermal noise at the output
- When the switch turns off, this noise is stored on the capacitor along with the instantaneous value of the input voltage

- The **rms voltage of the sampled noise is ~** $\sqrt{kT/C}$



Charge Injection Cancellation

- The charge injected by the main transistor can be removed by means of a second "dummy" transistor



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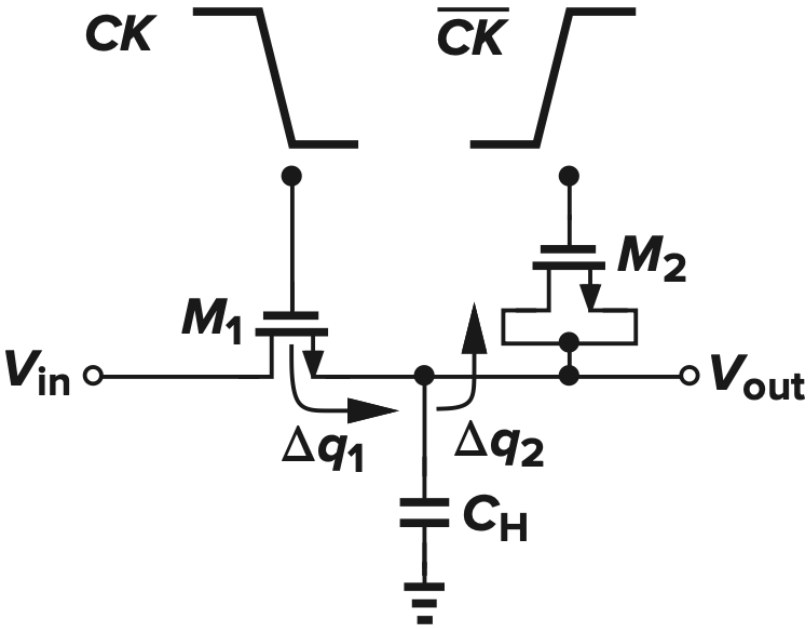
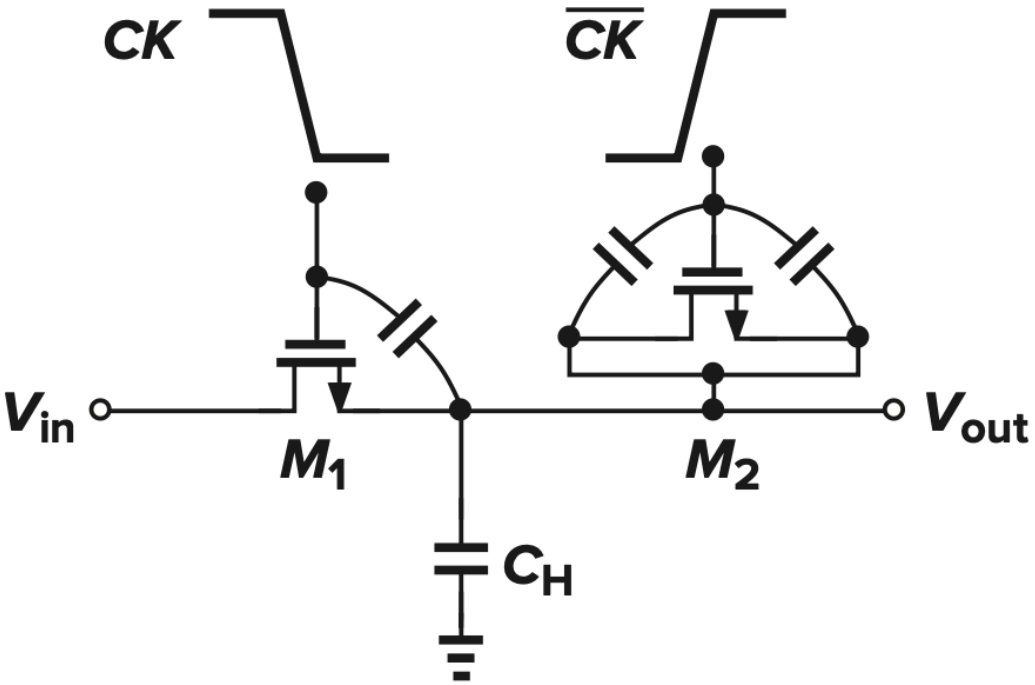


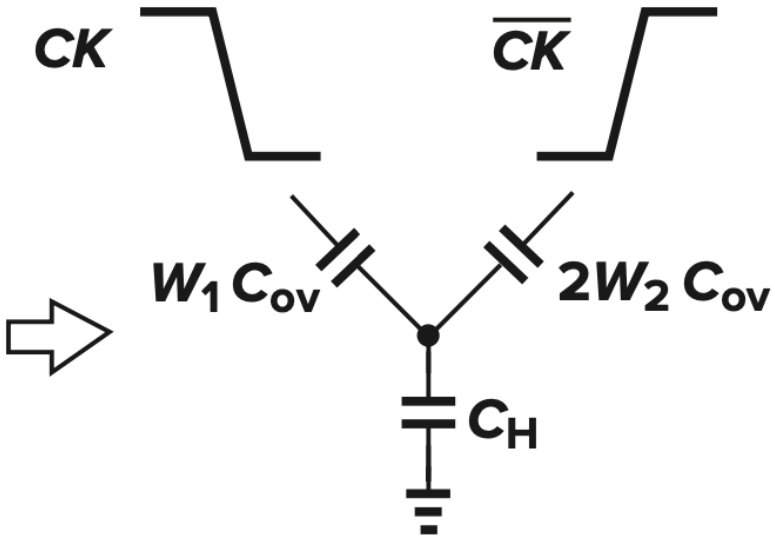
$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1})$$

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH2})$$

$W_2 = 0.5W_1$ and $L_2 = L_1$, then $\Delta q_2 = \Delta q_1$ X

Clock feedthrough suppression by dummy switch

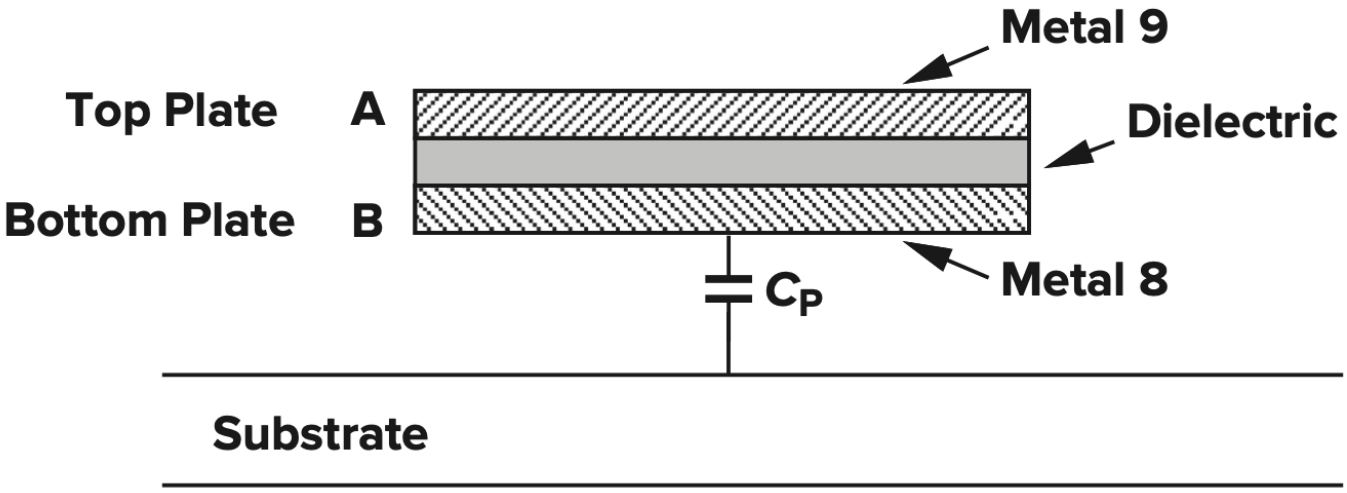


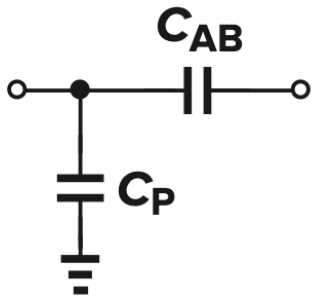


$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}+V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}=0$$

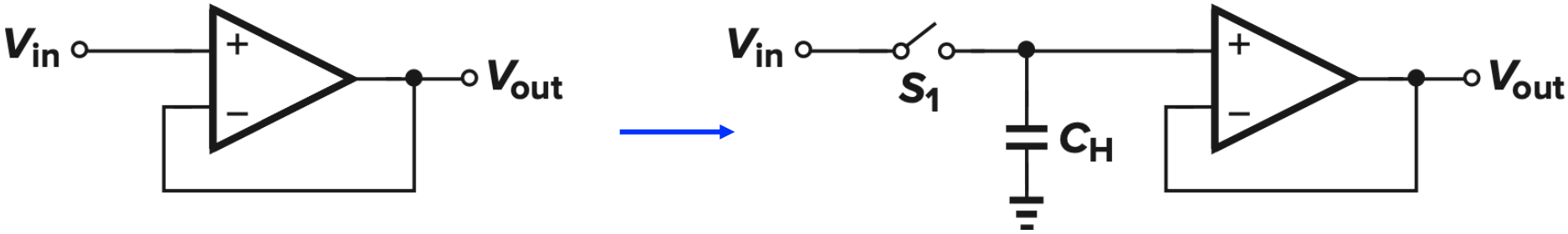
Capacitors in CMOS technology

- Capacitors in CMOS technology: The “top plate” and the “bottom plate” are realized by metal layers
- The bottom plate suffers from capacitance Cp to the underlying substrate: a value typically 5 to 10% of the main capacitance

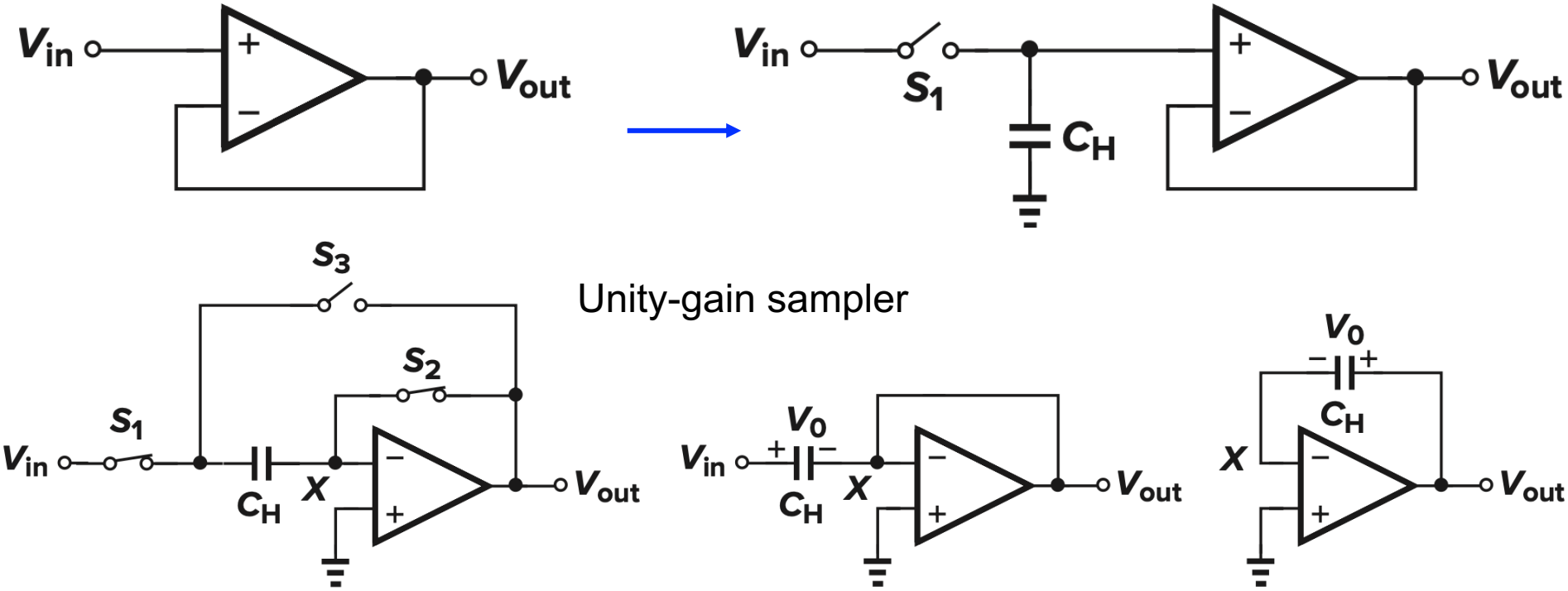




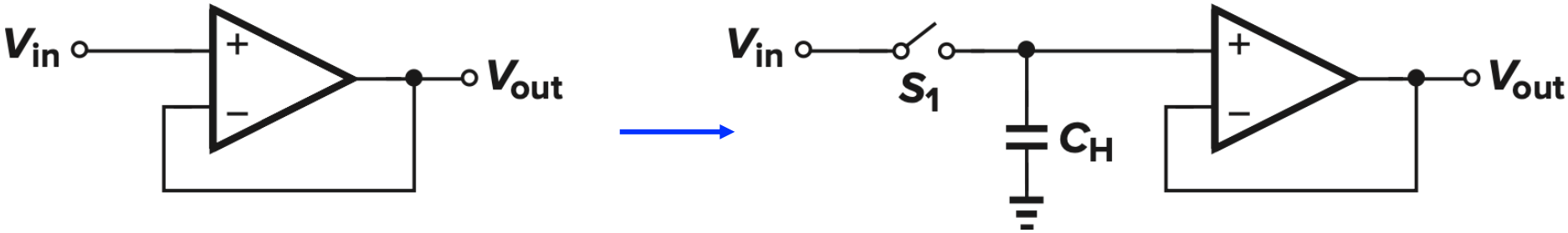
Switched-Capacitor Amplifiers



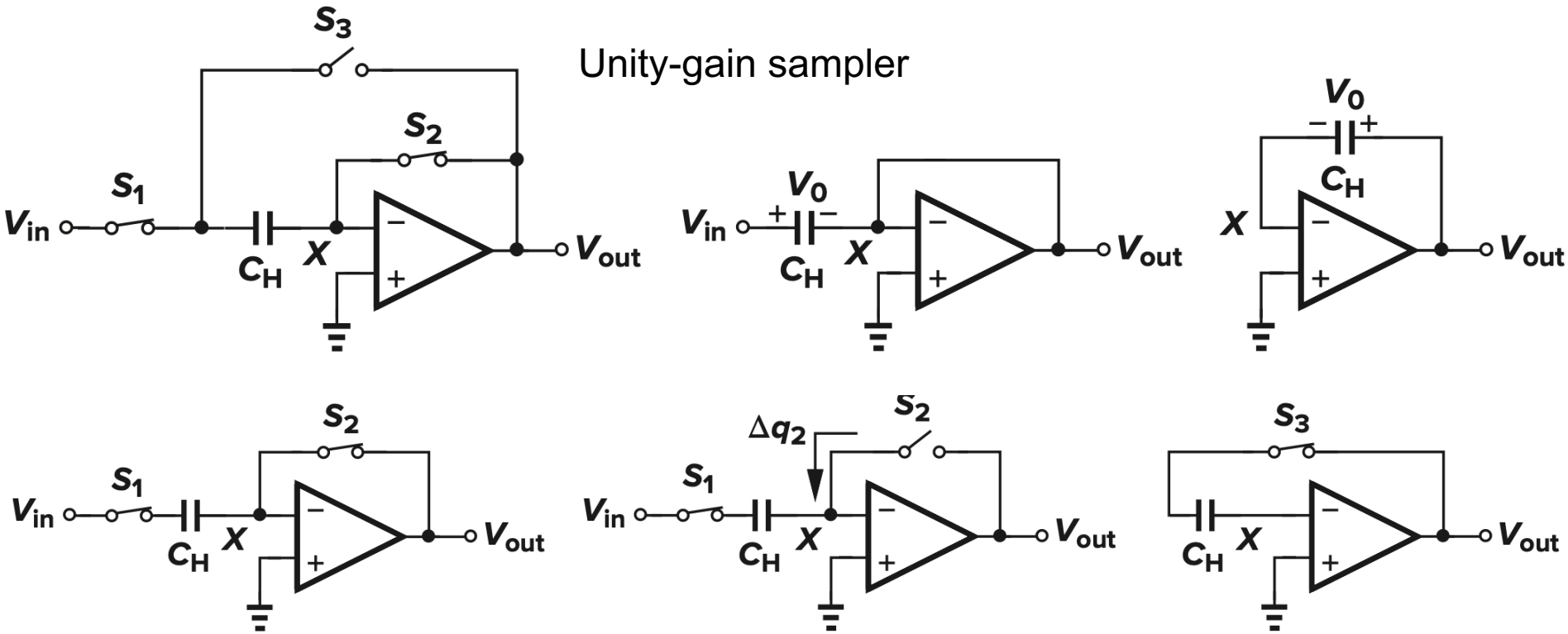
Switched-Capacitor Amplifiers



Switched-Capacitor Amplifiers

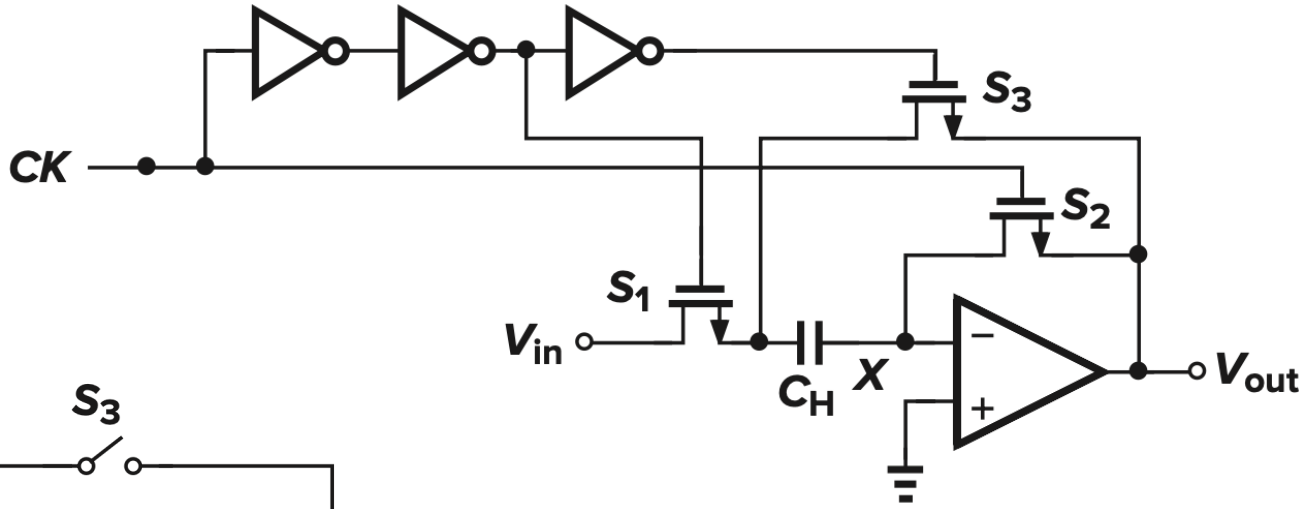


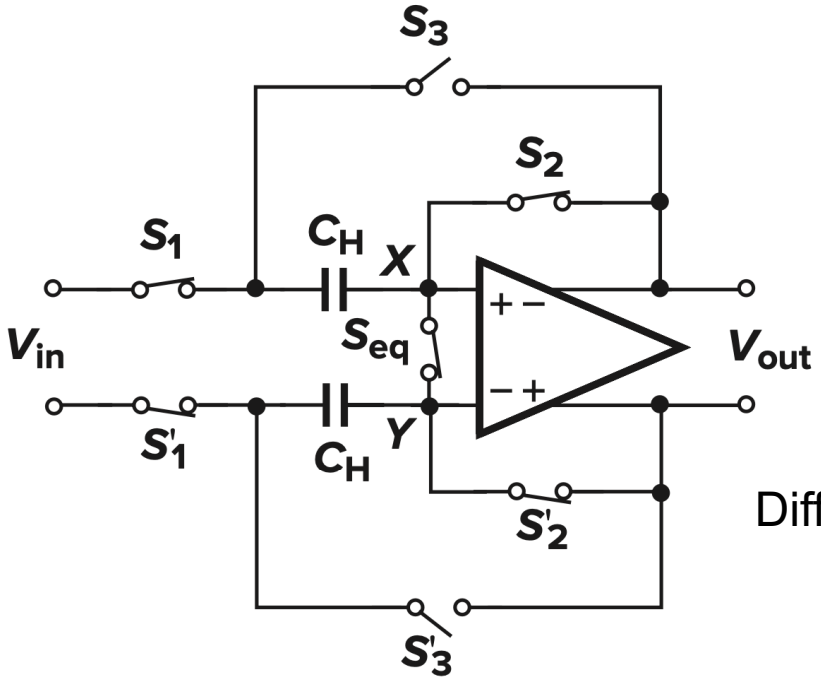
Unity-gain sampler



Unity-gain sampler

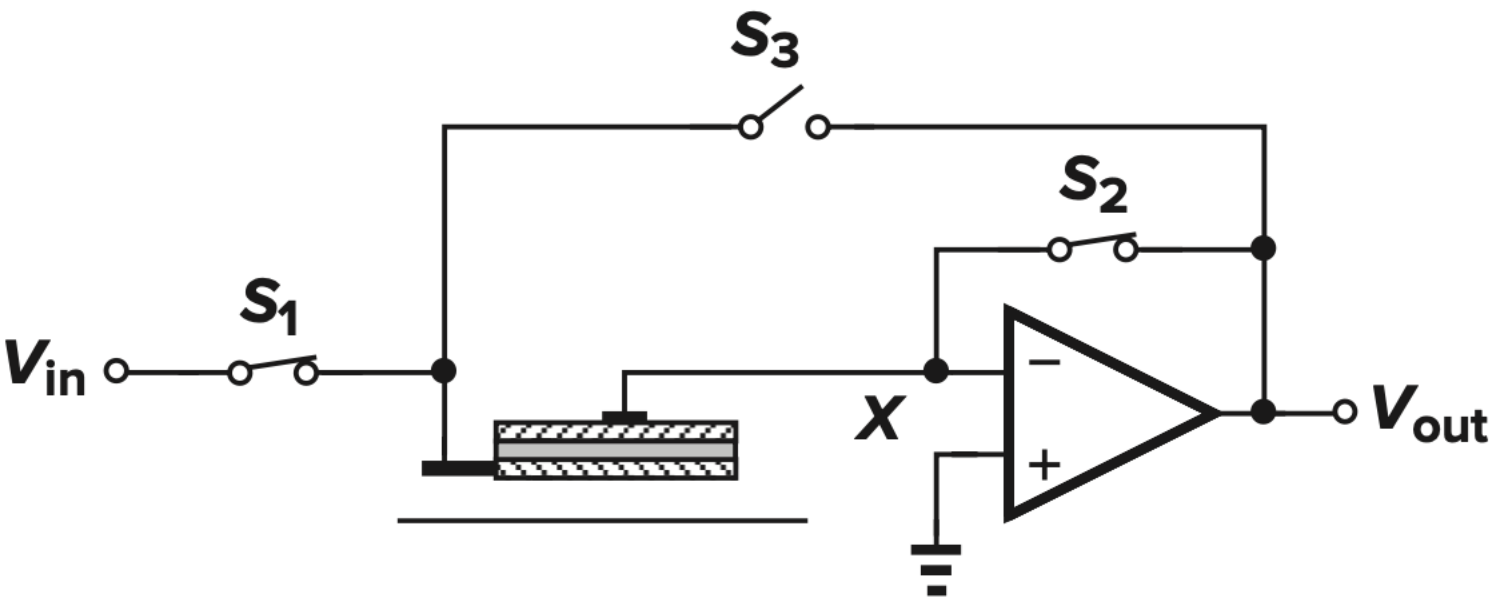
Generation of proper clock edges for unity-gain sampler



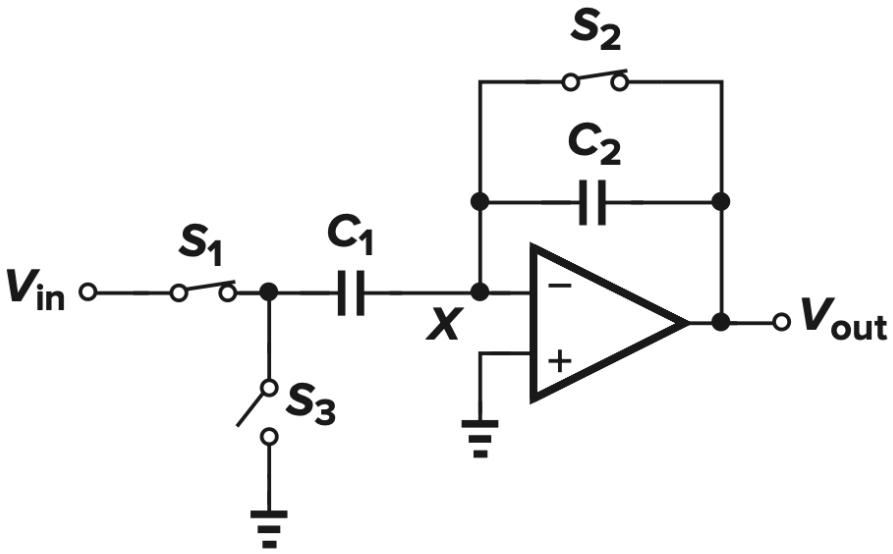


Differential realization of unity-gain sampler

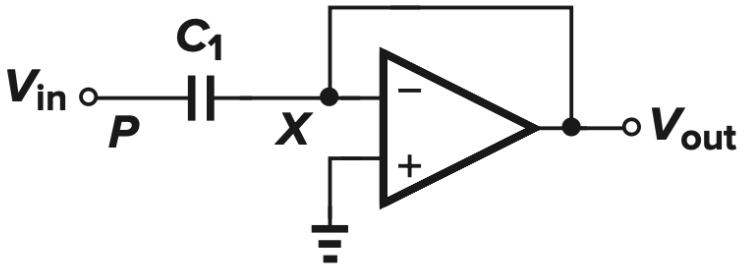
Bottom-plate sampling



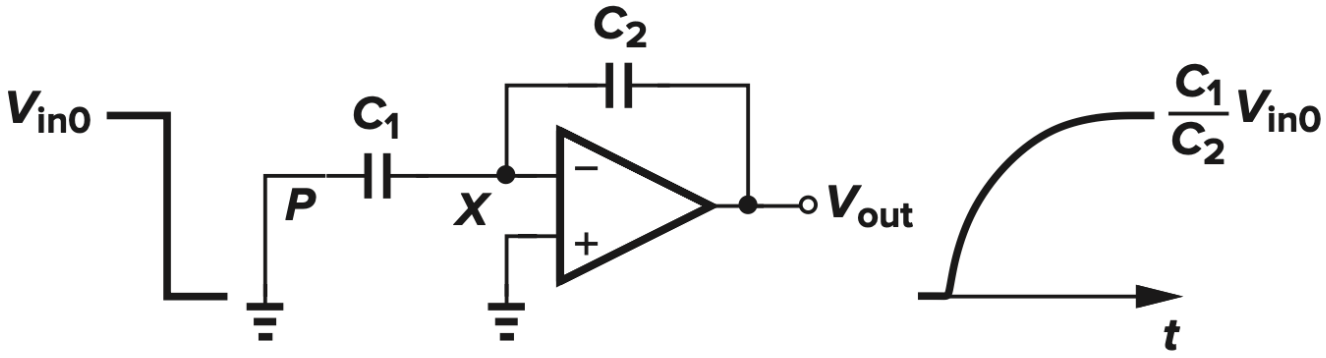
Noninverting Amplifier



(a)



(b)



(c)

Differential realization of noninverting amplifier