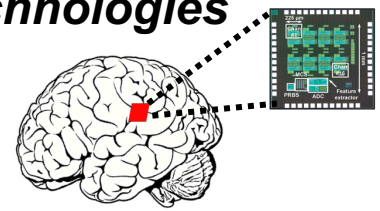
Integrated Neurotechnologies Laboratory

EPFL



Advanced analog integrated circuit design (EE-523), Lecture 1

Prof. Mahsa Shoaran

Institutes of Electrical and Micro Engineering and Neuro-X, School of Engineering, EPFL

Advanced analog integrated circuit design

EE-523 / **3 credits**

Teacher: Shoaran Mahsa

Language: English

Summary

Introduction to advanced topics in analog and mixed-signal CMOS circuits at the transistor level. The course will focus on practical aspects of IC design, quantitative performance measures, and design trade-offs to develop an intuitive understanding of circuit behavior.

Content

- Advanced topics on CMOS operational amplifiers
- Review of noise, feedback and stability
- Switched-capacitor circuits
- Design of low-power, low-noise analog front-ends

Show more

Keywords

CMOS, advanced analog integrated circuits, mixed-signal IC design, low-noise analog front-end, noise efficiency factor, biomedical circuits, biopotential amplifier

Learning Prerequisites

RECOMMENDED COURSES

- Analog IC design (EE-320)
- Fundamentals of analog & mixed signal VLSI design (EE-424)

IMPORTANT CONCEPTS TO START THE COURSE

- MOS transistor operation, large/small signal models, parasitics
- Time and frequency (Laplace) domain analysis
- Single-stage, multi-stage, and differential CMOS amplifiers
- Noise, stability, and feedback concepts

In the programs

Electrical and Electronics Engineering
2024-2025 Master semester 2

- **Semester:** Spring
- **Exam form:** Written (summer session)
- **Subject examined:** Advanced analog integrated circuit design
- **Courses:** 2 Hour(s) per week x 14 weeks
- **Exercises:** 1 Hour(s) per week x 14 weeks
- **Type:** optional

Electrical and Electronics Engineering
2024-2025 Master semester 4

Microengineering
2024-2025 Master semester 2

Microengineering
2024-2025 Master semester 4

Reference week

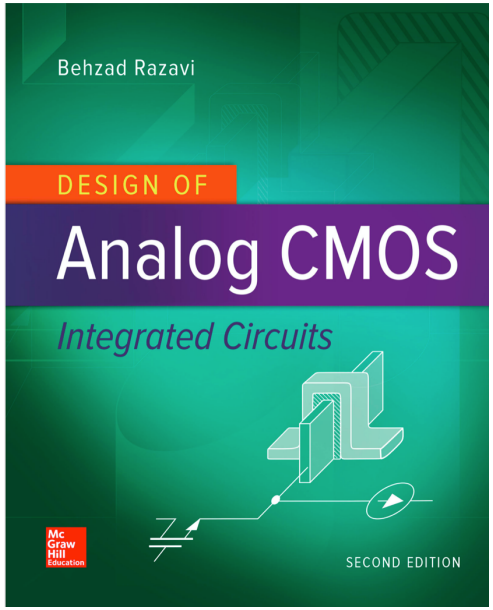
	Mo	Tu	We	Th	Fr
8-9					
9-10					
10-11					
11-12					
12-13					
13-14					BC07-08 INJ218
14-15					
15-16					BC07-08 INJ218
16-17					
17-18					

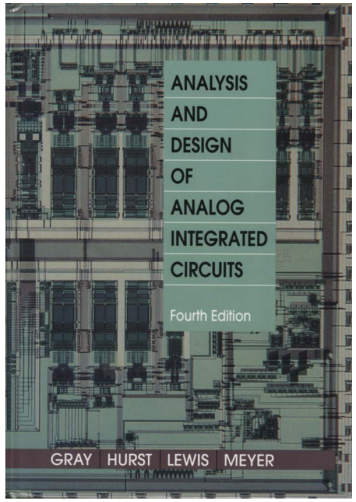
Advanced analog IC design: References, moodle

- **Design of Analog CMOS Integrated Circuits**, B. Razavi
- Analysis and Design of Analog Integrated Circuits, P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer
- Analog-to-Digital Conversion, M. Pelgrom
- Scientific papers, book chapters, …

Most figures in this set of slides are taken from the first reference

Moodle: https://moodle.epfl.ch/course/EE-523





Course requirements

- The knowledge of **EE-320 and EE-424** is required to take this course

- Students who have only taken EE-320 will need to review a few chapters of Prof. Razavi's CMOS book. In general, the prerequisite chapters include:
  - Basic MOS Device Physics (Chapter 2)
  - Single-Stage Amplifiers (Chapter 3)
  - Differential Amplifiers (Chapter 4)
  - Current Mirrors (Chapter 5)
  - **Frequency Response of Amplifiers (Chapter 6)**
  - **Noise and Feedback (Chapter 7, 8)**

- Alternative courses may count as prerequisites on a case-by-case basis

Aims of the course

- **This is a new course!**
- **We will learn, adjust and improve**

- **We want you to learn:**
  - The **essential topics in CMOS design**
  - Gain an **intuitive understanding** of circuit design and behavior
  - Learn **actual IC design** in Cadence Virtuoso

This week;

- **First lecture (1:15-2pm) in INJ218**
- **First TP session (2:15pm-4pm) in BC07-08**

- **Next week (March 7): Lecture and exercise sessions in INJ218**

- **Important:** Complete the **EDA assignment for the TPs**

Questionnaire and quiz summary

- ✓ Some students have the necessary background, but may have forgotten basic concepts, this will be refreshed throughout the course
  - ✓ **Intuition-based design**, hard to forget!
  - ✓ **This will be the focus, rather than covering many topics**
- ✓ Some students have not seen some key concepts (frequency response, noise, …). They will need to read extra materials.
- ✓ **Most students do not have experience of analog design in Cadence**, some have done simple digital or very simple analog modules
- ✓ Some students are exchange and have taken courses elsewhere, they would still need actual IC design experience in Cadence for their projects
- Students who have not seen the key concepts such as small-signal model, amplifiers and differential pairs will need to study significantly to catch up

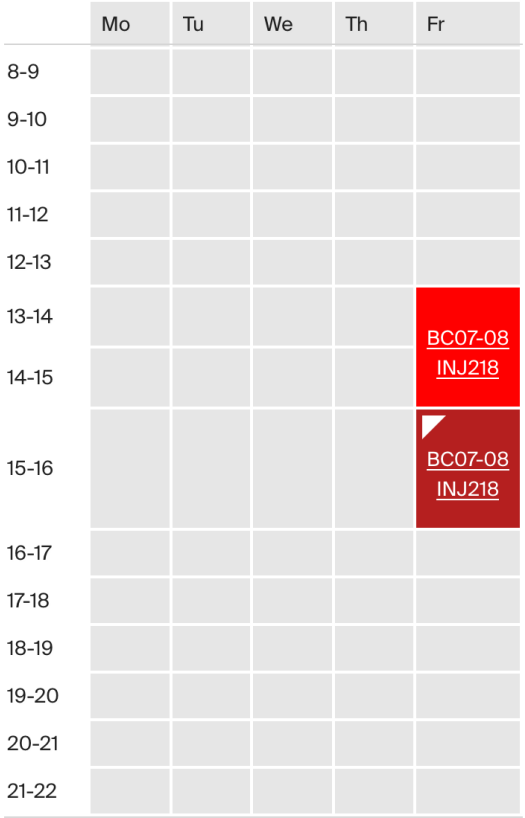
Course structure

- **In-person lectures**: 2 hours or 3 hours per week (scheduled weeks) in **INJ218**
- **Exercise sessions**: 1 hour per week (scheduled weeks) in **INJ218**
- **TP (Cadence) sessions:** 3 hours per week (scheduled weeks) in **BC07-08**

- Questions through moodle forum
- On-demand office hours (Professor and TAs)
  - TA: Yiheng Fu (yiheng.fu@epfl.ch)
  - TA: Alin Thomas Tharakan (alin.tharakan@epfl.ch)
  - TA: Cong Huang (cong.huang@epfl.ch)
  - TA: Yasemin Engur (yasemin.engur@epfl.ch)

Make sure to

- Attend the lecture and exercise sessions
- Allocate time for exercises and TP sessions



Weekly Schedule and Grading

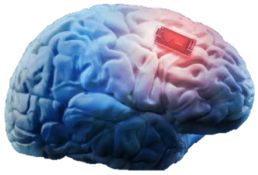
Week (day)	Subject by week – EE-523: Advanced analog integrated circuit design – Spring 2025	Materials
Week 1: 17.02 to 23.02 (2.21)	**Questionnaire about background, EDA statement, Quiz**	**Slides on Moodle**
Week 2: 24.02 to 02.03 (2.28)	**Introduction + TP1: Review of basics, single-stage amplifiers, diff pair, dc/ac analysis**	**Slides + Tutorial**
Week 3: 03.03 to 09.03 (3.7)	**Op amp: advanced topologies, design considerations + Exercise1**	**Slides on Moodle**
Week 4: 10.03 to 16.03 (3.14)	**TP2: Op amp, frequency response, noise, design procedure**	**Tutorial on Moodle**
Week 5: 17.03 to 23.03 (3.21)	**Op amp: advanced topologies, gain boosting, CMFB + Exercise2**	**Slides on Moodle**
Week 6: 24.03 to 30.03 (3.28)	**Switched-cap circuits: Introduction to SAR ADC + Exercise3**	**Slides on Moodle**
Week 7: 31.03 to 06.04 (4.4)	**TP3: SC circuits, S/H for ADC – Design homework announcement and team building**	**Tutorial on Moodle**
Week 8: 07.04 to 13.04 (4.11)	**TP4: Comparator, design specifications: power, offset, noise, Monte Carlo simulations**	**Tutorial on Moodle**
Week 9: 14.04 to 20.04 (4.18)	Holiday – No class	
Week 10: 21.04 to 27.04 (4.25)	Holiday – No class	
Week 11: 28.04 to 04.05 (5.2)	**Nonlinearity, mismatch, layout + Exercise4**	**Slides on Moodle**
Week 12: 05.05 to 11.05 (5.9)	**SAR ADC (continued) + Exercise5**	**Slides on Moodle**
Week 13: 12.05 to 18.05 (5.16)	**TP5: Layout, DRC/LVS, post-layout simulations**	**Tutorial on Moodle**
Week 14: 19.05 to 25.05 (5.23)	**Guest lecture: Delta Sigma ADC + integrated exercise**	**Slides on Moodle**
Week 15: 26.05 to 01.06 (5.30)	**TP6: Project on SAR comparator design and layout**	**Tutorial on Moodle**

Assessment:

- **Written final exam**: 60% or 70% of the final grade
- **Design homework**: 40% or 30% of the final grade
- We will use the grading scheme that produces the highest grade for each student!
- No mid-term exam

The Instructor

- Prof Mahsa Shoaran
  - **Integrated Neurotechnologies Lab (INL)**
    - Institute of Electrical and Micro Engineering (IEM)
    - Neuro-X Institute (Campus Biotech)
  - 2017-2019: Assistant Prof at **Cornell University**, NY, USA



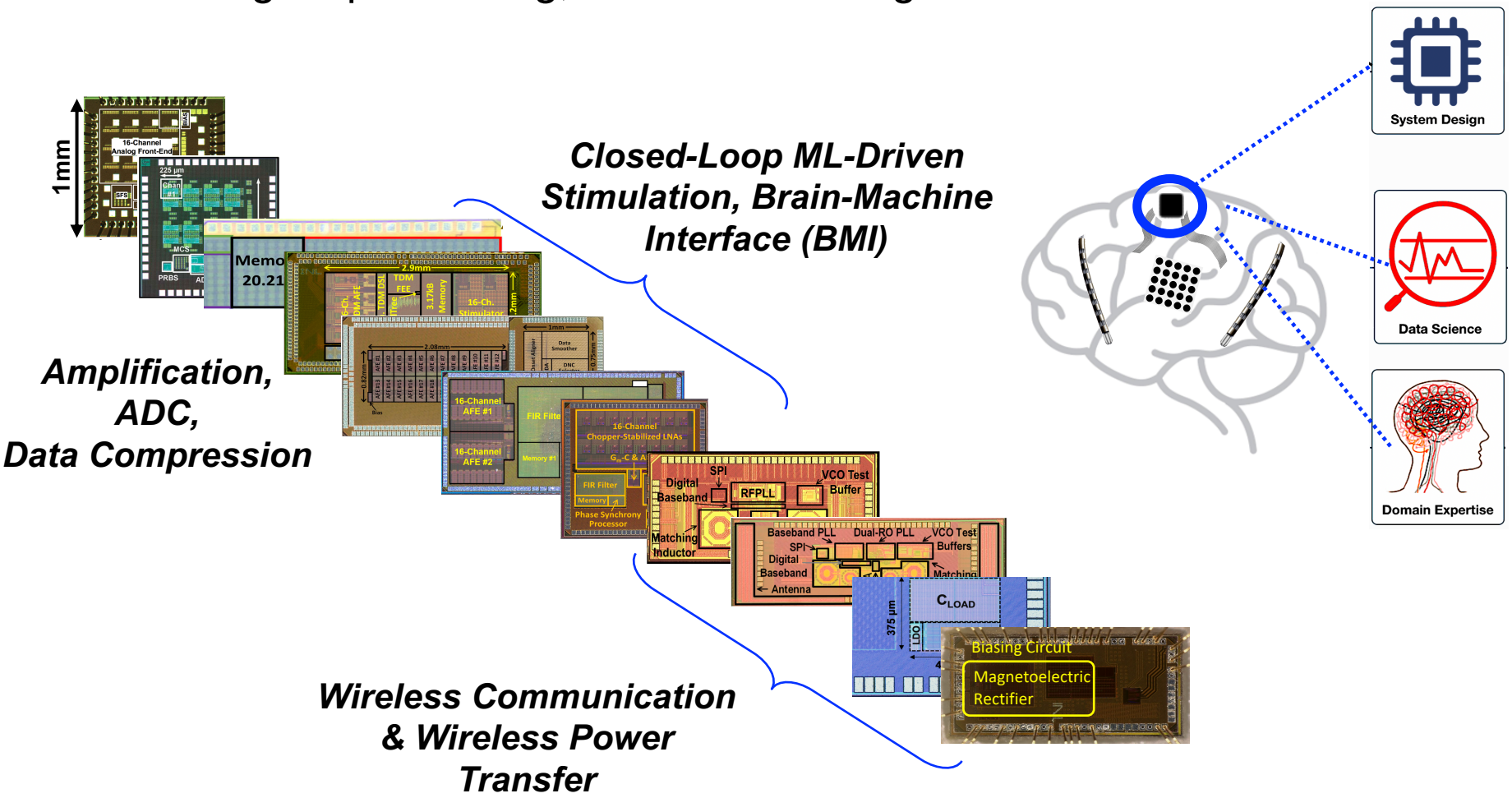
EPFL SCHOOL OF ENGINEERING
ELECTRICAL ENGINEERING

Institute of Electrical and Micro Engineering

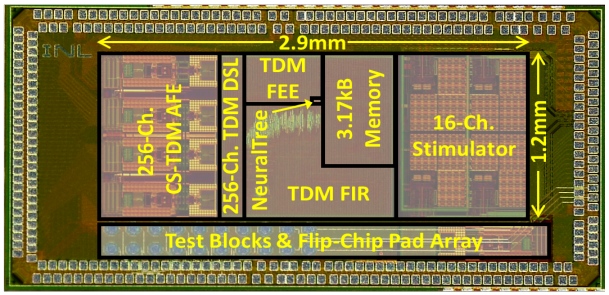
Neuro-X Institute

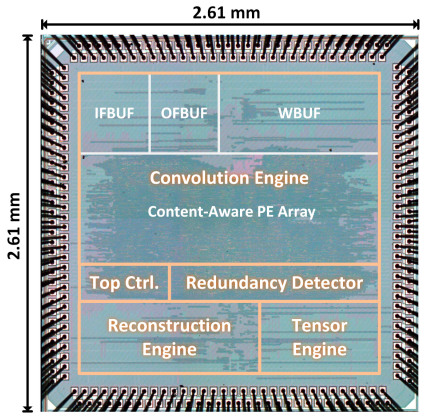
What we do: Neural Interface Chip Design

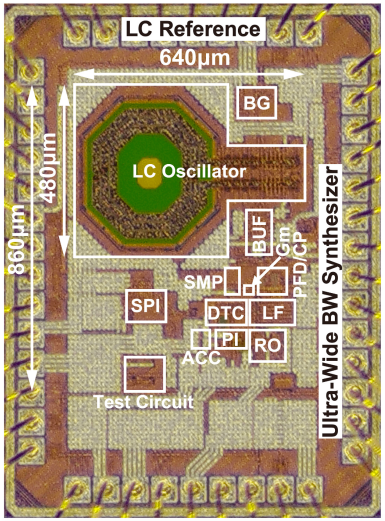
- **Analog/digital/mixed-signal IC design**
- Neural signal processing, machine learning

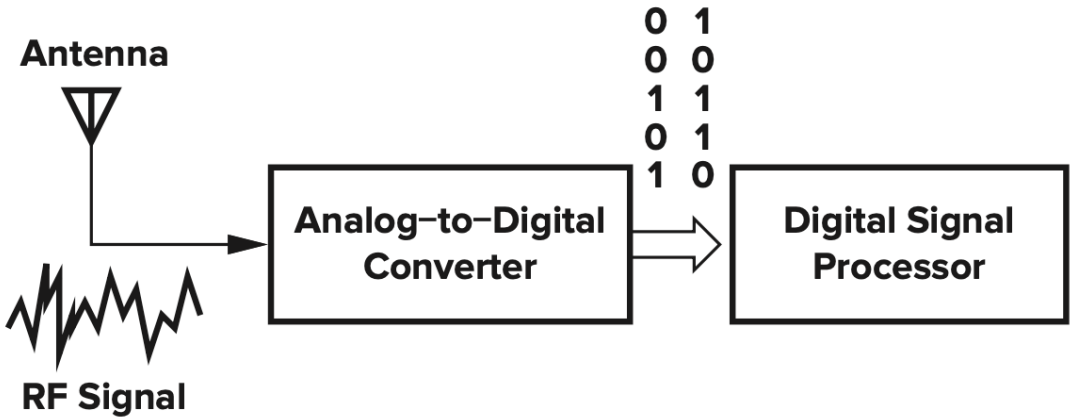


The Art of Chip Design!







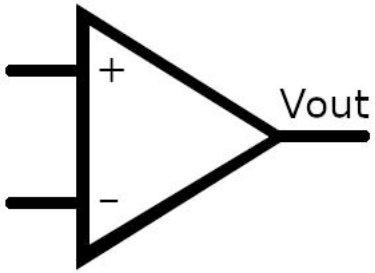


- Today's complex ASICs demand **both analog and digital IC design**

Operational amplifiers (op amps)

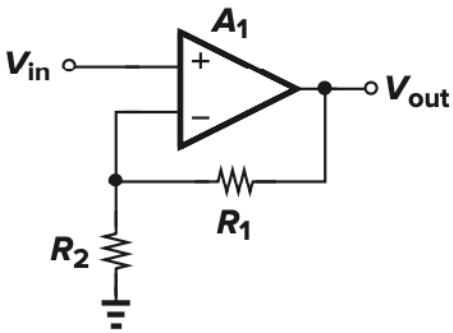
Key specs for an op amp:

- DC **Gain**
- Small signal output drive (**Rout**)
- **CMRR**
- **PSRR**
- **Zin**
- **Bandwidth**/pole-zero location
- Large signal output drive (max current)
- Input voltage range (common mode)
- **Output voltage swing**
- **Current consumption**
- **Power supply (VDD)**
- **Noise**
- **Offset**
- **Linearity**
- Temperature dependence
- Process dependence



Op amp: Gain Error

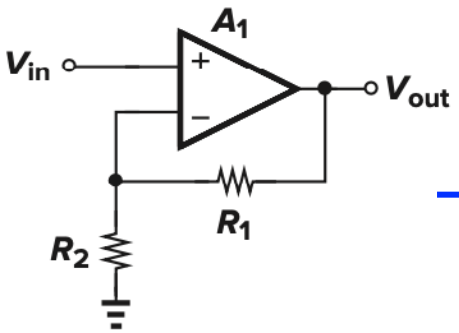
- **High open-loop gain**



- For a nominal gain of 10, determine the minimum value of A_1 for a gain error of 1%?

Op amp: Gain Error

- **High open-loop gain**



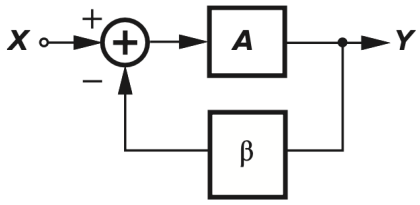
$$1 + R_1/R_2 = 10$$

$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1}$$

$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right)\left(1 - \frac{R_1 + R_2}{R_2}\frac{1}{A_1}\right)$$

A_1 > 1000 for a gain error <1%

- For a nominal gain of 10, determine the minimum value of A_1 for a gain error of 1%?



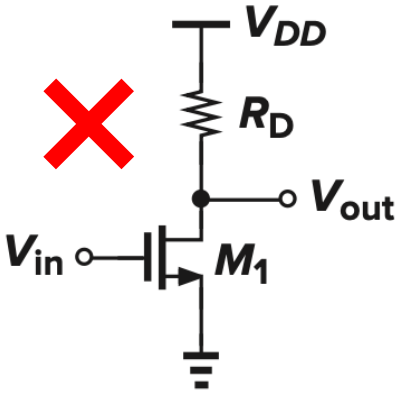
$$\frac{Y}{X} = \frac{A}{1 + \beta A}$$

$$\approx \frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right)$$

$$\beta A \gg 1$$

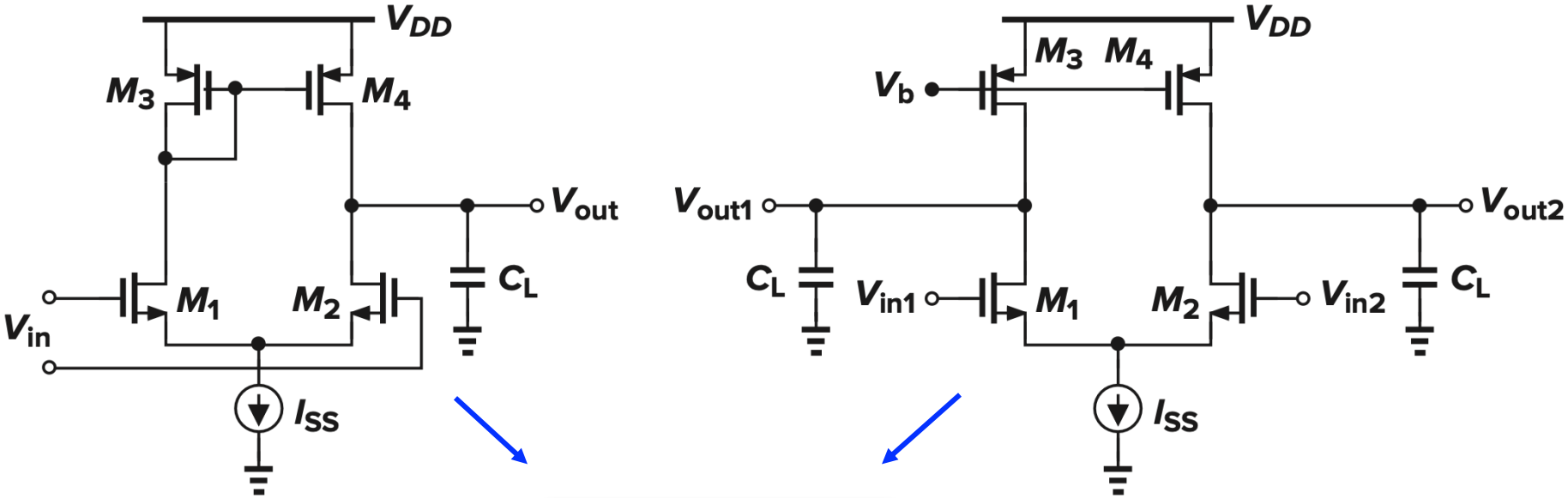
We will discuss:

- Telescopic and folded-cascode topologies
- Two-stage and gain-boosting configurations
- Common-mode feedback



One-Stage Op amps

- Differential amplifier with **single-ended** and **differential** outputs
- The **low-frequency gain** hardly exceeds 10 in nanometer technologies
- The **bandwidth** is usually determined by the load capacitance C_L
- Both suffer from **noise contributions** of $M1$–$M4$



$$g_{mN}(r_{ON} \| r_{OP})$$

Example: Input CM Range and Output Impedance

- Find the input common-mode voltage range and closed-loop output impedance of the unity-gain buffer shown below. Assume V_{th} = 0.3V and V_{od} = 0.1V.