EE-523 – Exercise 1

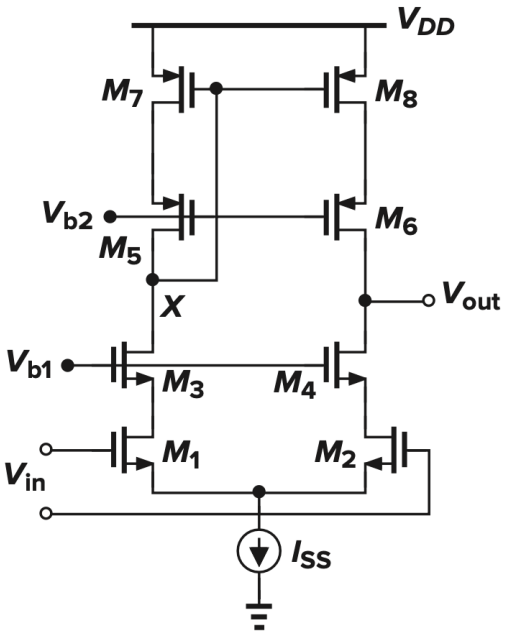
1. In the op amp shown below, $(W/L_{eff})_{1-8} = 100/0.34$, $I_{SS} = 1mA$, $V_{b1} = 1.7V$. Assume $\gamma=0$, $V_{TH,P} = 0.8V$, $V_{TH,N} = 0.7V$, $\mu_n C_{ox} = 0.134\ mA/V^2$, $\mu_p C_{ox} = 0.038\ mA/V^2$, $\lambda=0$, and $V_{DD} = 3V$.

(a) What is the maximum allowable input CM level?

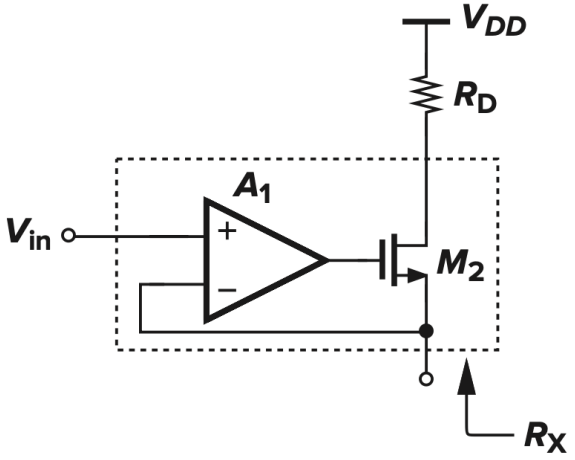
(b) What is the value of V_X (voltage at node X)?

(c) What is the maximum allowable output swing if the gate of M_2 is connected to output?

(d) What is the acceptable range of V_{b2}?



2. Determine the resistance seen at the source of M_2 if $\gamma = 0$.



3. Suppose that in the circuit below, I_1 = 100μA, I_2 = 0.5mA, and $(W/L_{eff})1-3$ = 100/0.34, $V_{TH,N}$ = 0.7V, $\mu_n C_{ox}$ = 0.134 mA/V^2, $\mu_p C_{ox}$ = 0.038 mA/V^2, λ=0. Assuming that I_1 and I_2 are implemented with PMOS devices having $(W/L_{eff})_P$ = 50/0.32

(a) Calculate the gate bias voltages of M_2 and M_3.

(b) Determine the maximum allowable output voltage swing.

(c) Calculate the overall voltage gain, assuming λ=0.2.