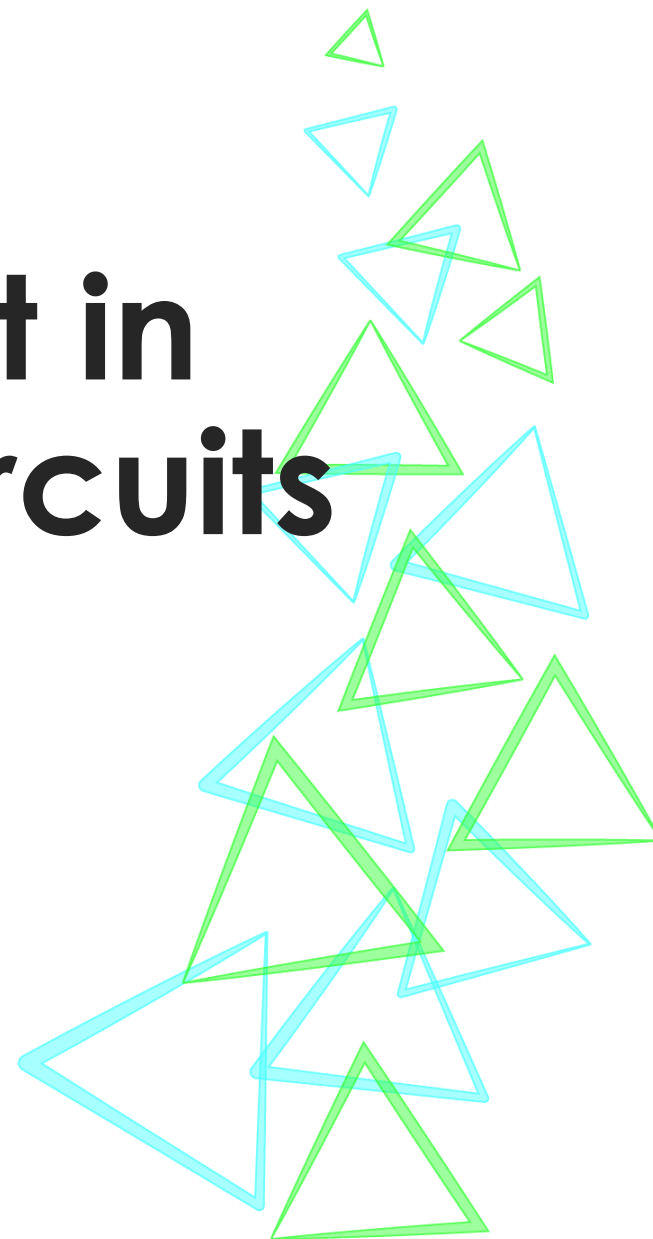


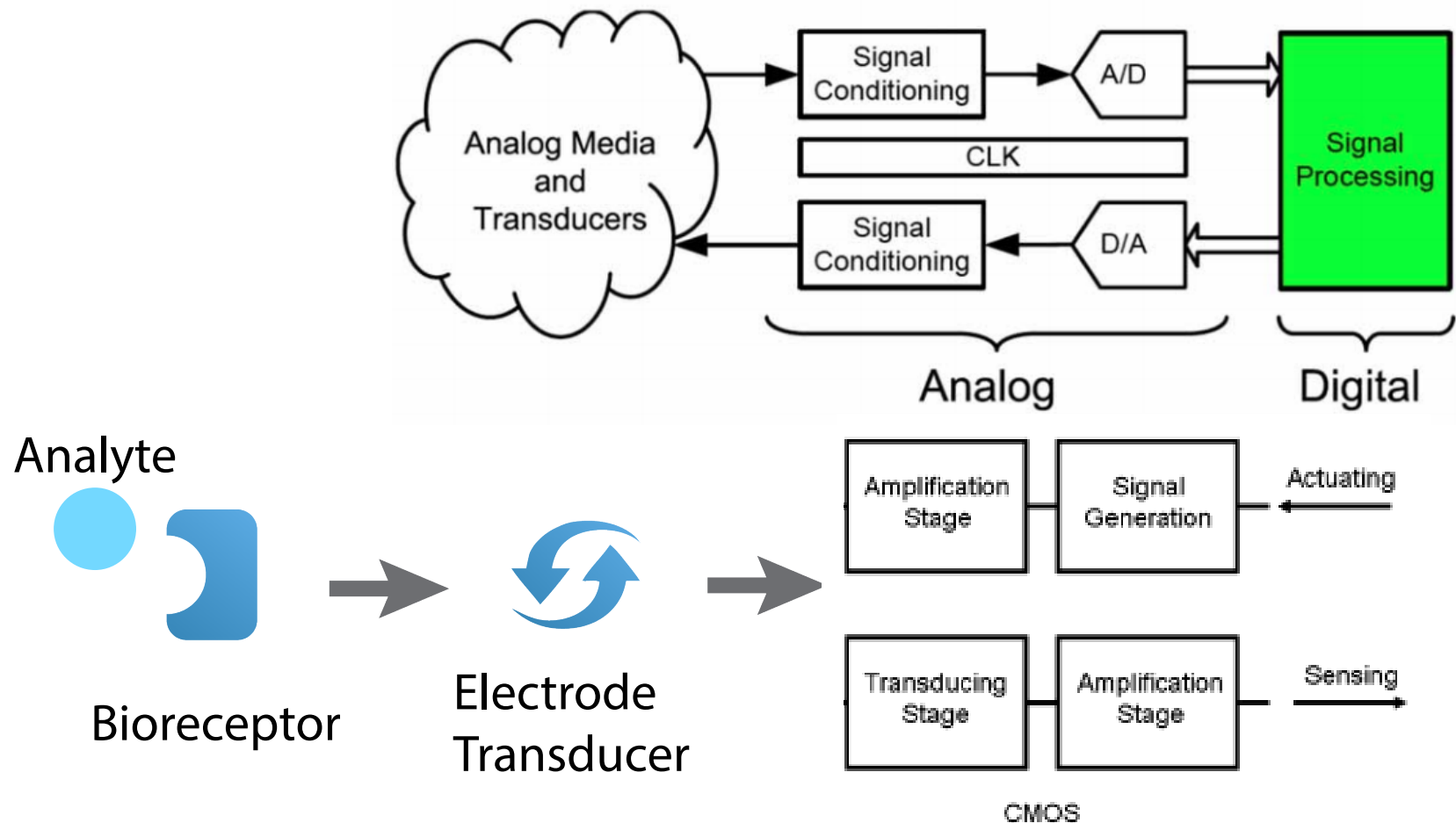
# Practical Aspect in Mixed Signal Circuits

Francesca Stradolini

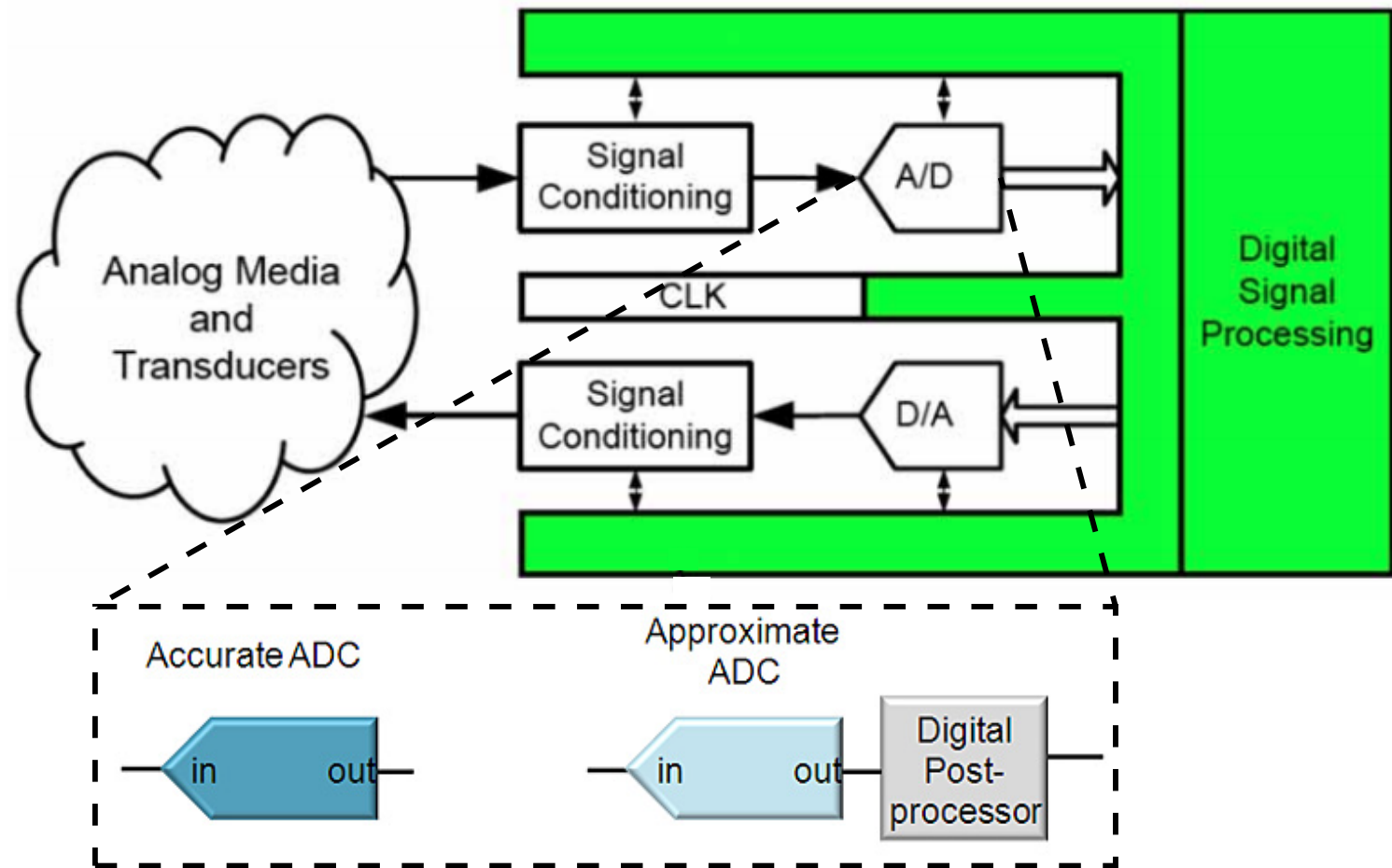
12.12.2017



# Parallelism: mixed signal & biosensor

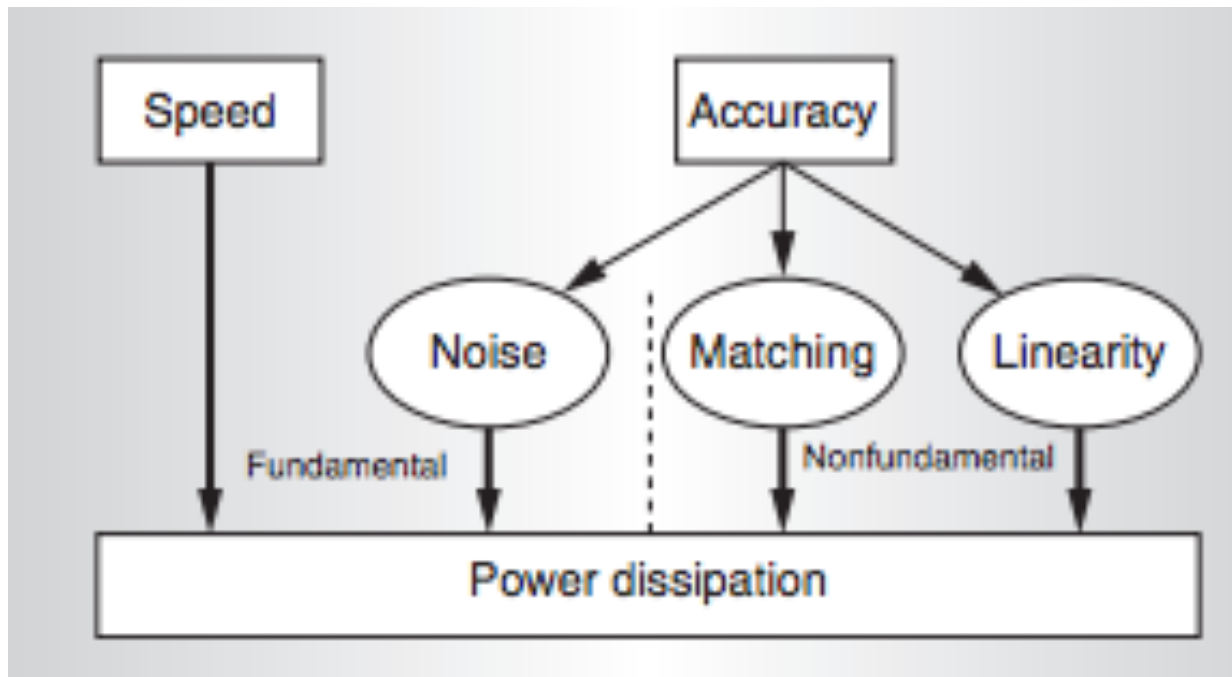


# Digital Assisted Analog (DDA)



# Analog Circuit Trade-off

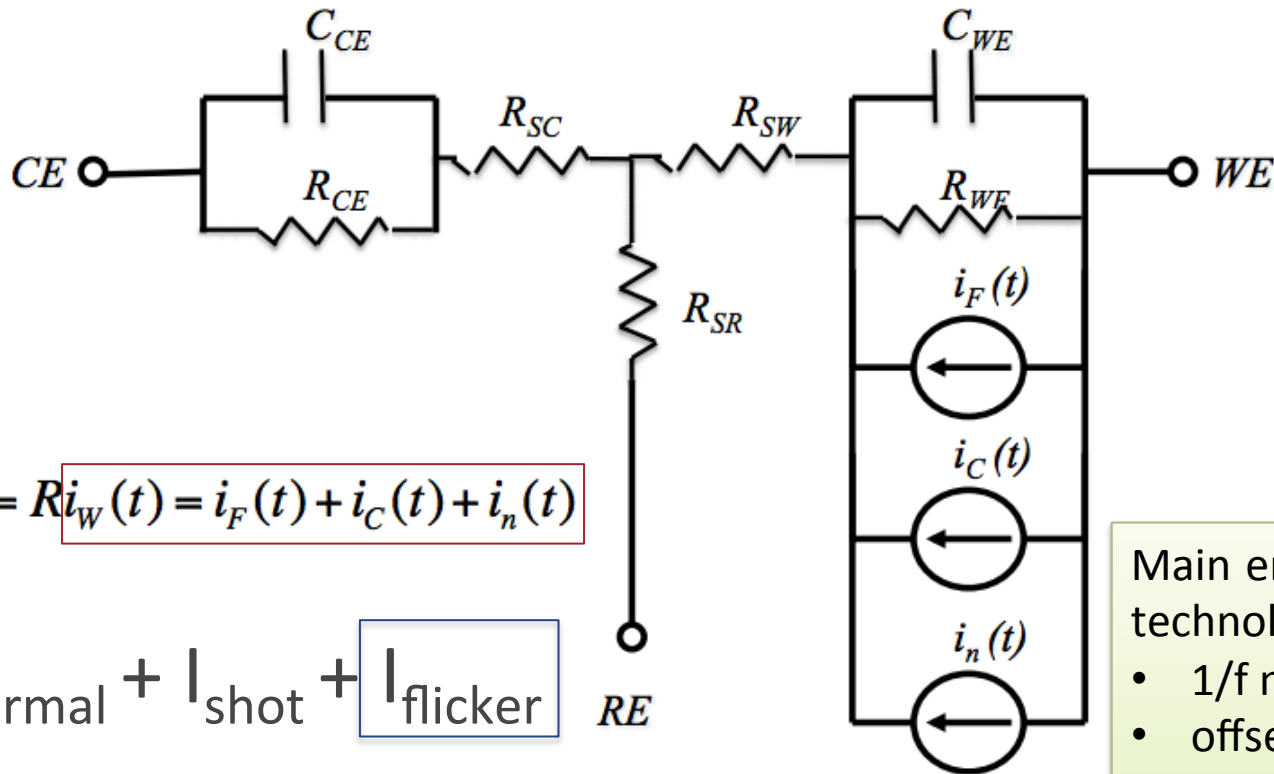
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- Power tends to increase linearly with speed
- Precision is affected by:
  1. thermal noise (caused by random carrier motion),
  2. component matching (inversely proportional to component area),
  3. high linear amplification (sub-optimal in terms of speed and noise).

# Total noise in Bio-Application

$$I_w = I_f + I_c + I_n$$



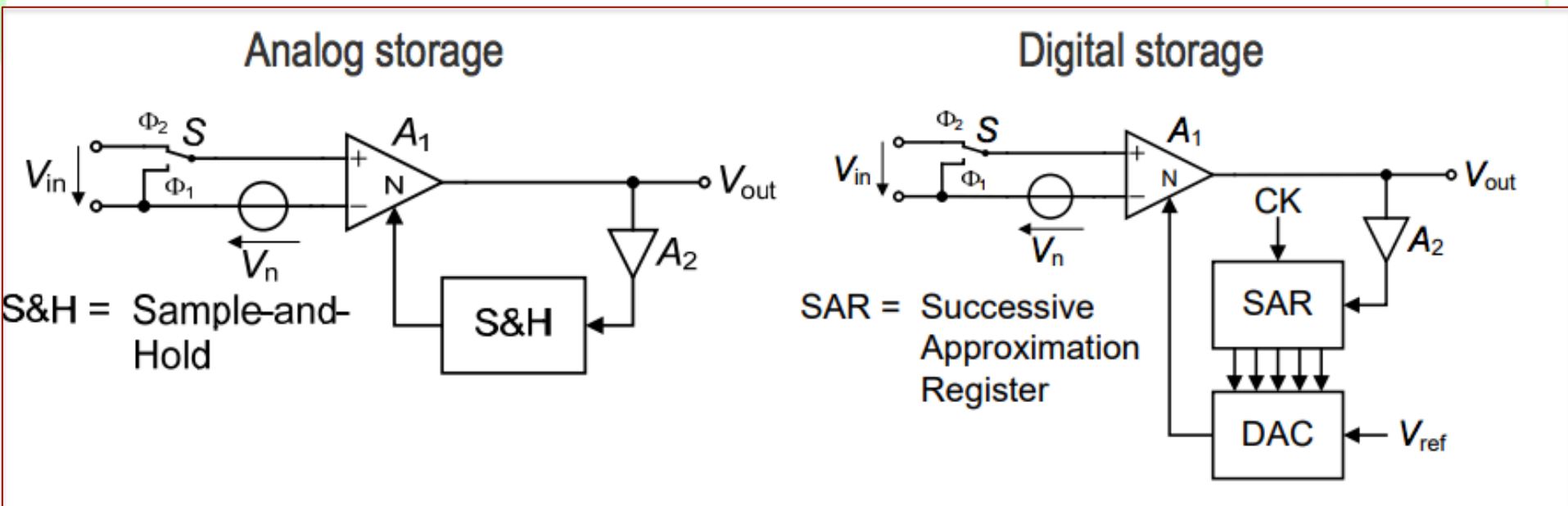
$$I_n = I_{\text{thermal}} + I_{\text{shot}} + I_{\text{flicker}}$$

Main errors in CMOS technology (opAmp)

- 1/f noise
- offset
- drift

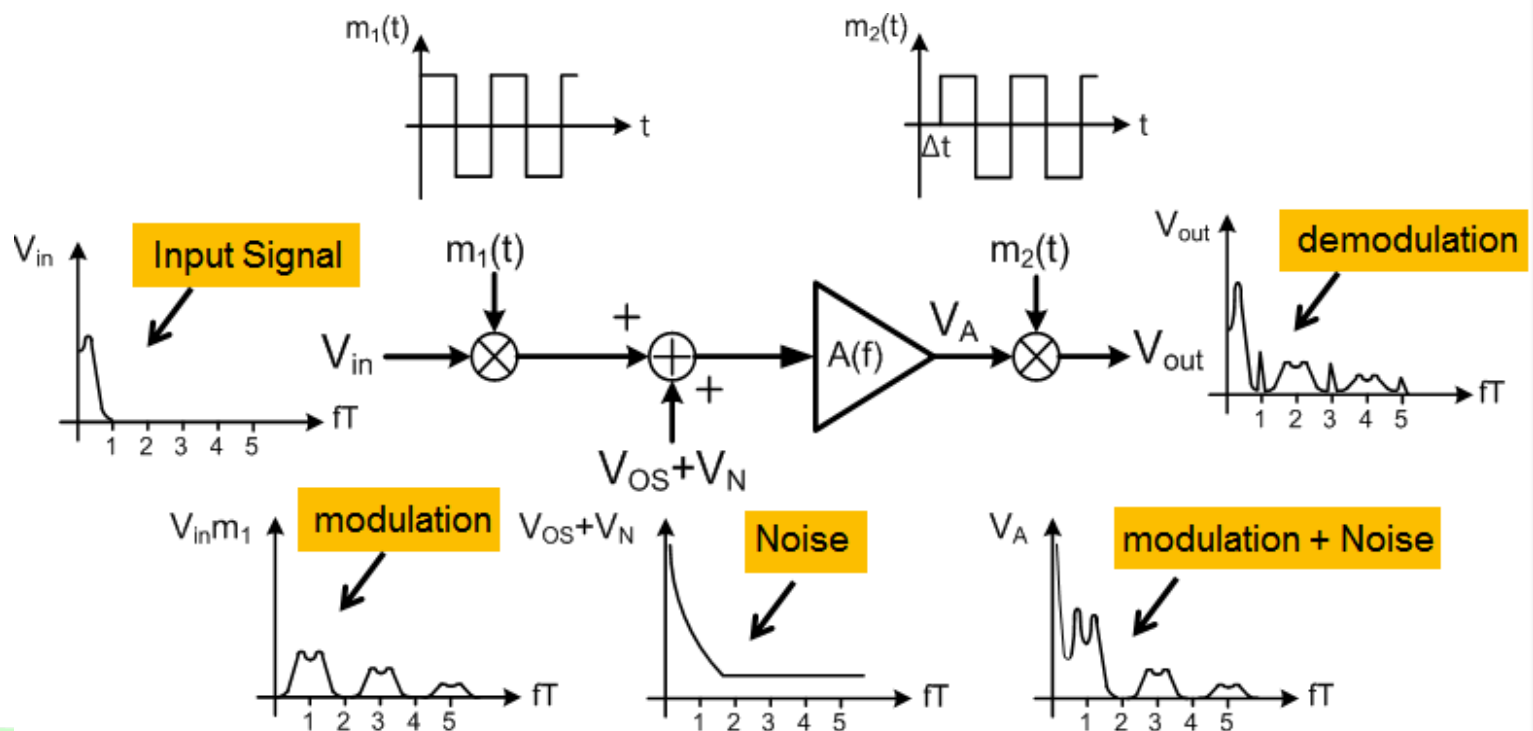
# Offset Cancellation

- ▲ **Trimming** usually performed during production.
- ▲ **AutoZeroing (AZ)**
- ▲ **Chopper Stabilization (CS)**



# Offset Cancellation

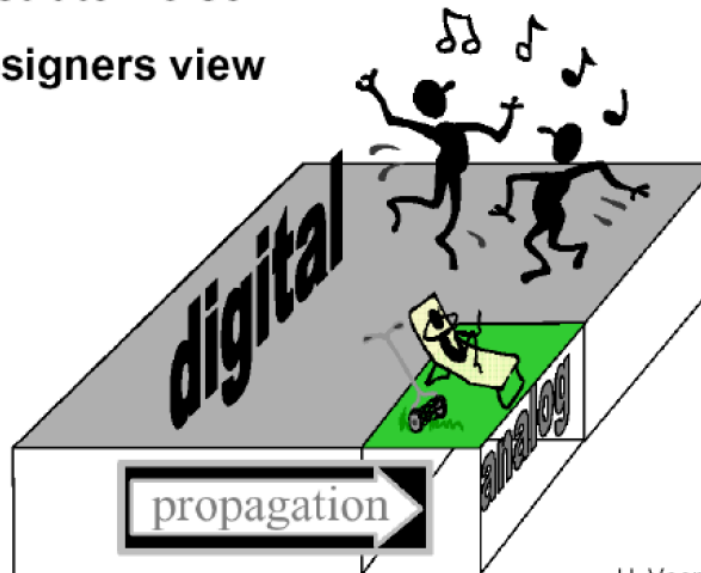
- ▲ Trimming
- ▲ AutoZeroing (AZ)
- ▲ Chopper Stabilization (CS)



# Generalize good co-designing

- ▲ Quiet the talker (reduce noise generation)
- ▲ Isolate the listener (sensitive circuit by shielding, guarding rings etc)
- ▲ Close the listener's ears (make more noise-tolerant)

Substrate Noise:  
A designers view



Important to make right decisions regarding

- placement of components,
- I/Os
- Routing
- Powering
- Decoupling...



# ElectroMagnetic Compatibility

## EMC

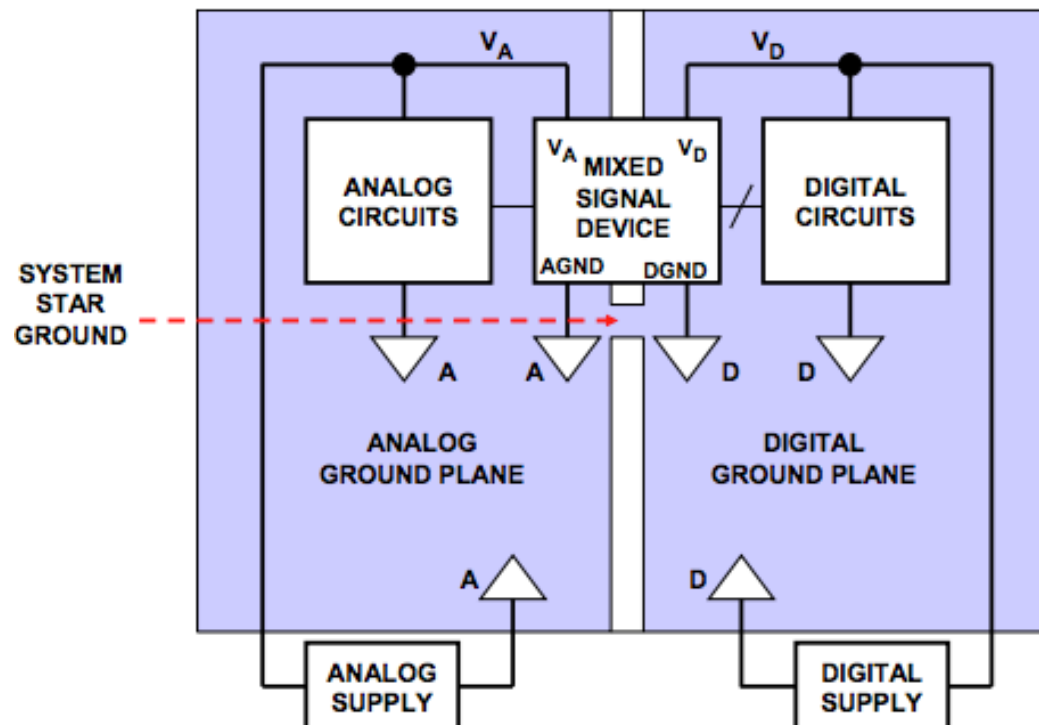
Two main principles

1. Current should be returned to their sources locally to avoid loop-antenna.
2. A system should have only one reference plane to not create dipole antenna.

## Grounding

# PCB Grounding

- ▲ split analog (AGND) and digital ground (DGND), not overlapping each other (to minimize coupling)
- ▲ connect the GND plane to a single point, normally the power supply -> **STAR GND configuration**



# Routing Suggestions

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- ▲ **minimize** long parallel lines and close proximity of signal traces to reduce inductive coupling,
- ▲ minimize long traces on adjacent layer to prevent capacitive coupling,
- ▲ route on separate layers signal traces requiring high isolation. If not possible, make them run orthogonally to one another with GND plane in between to minimize capacitive coupling (GND acts as shielding).

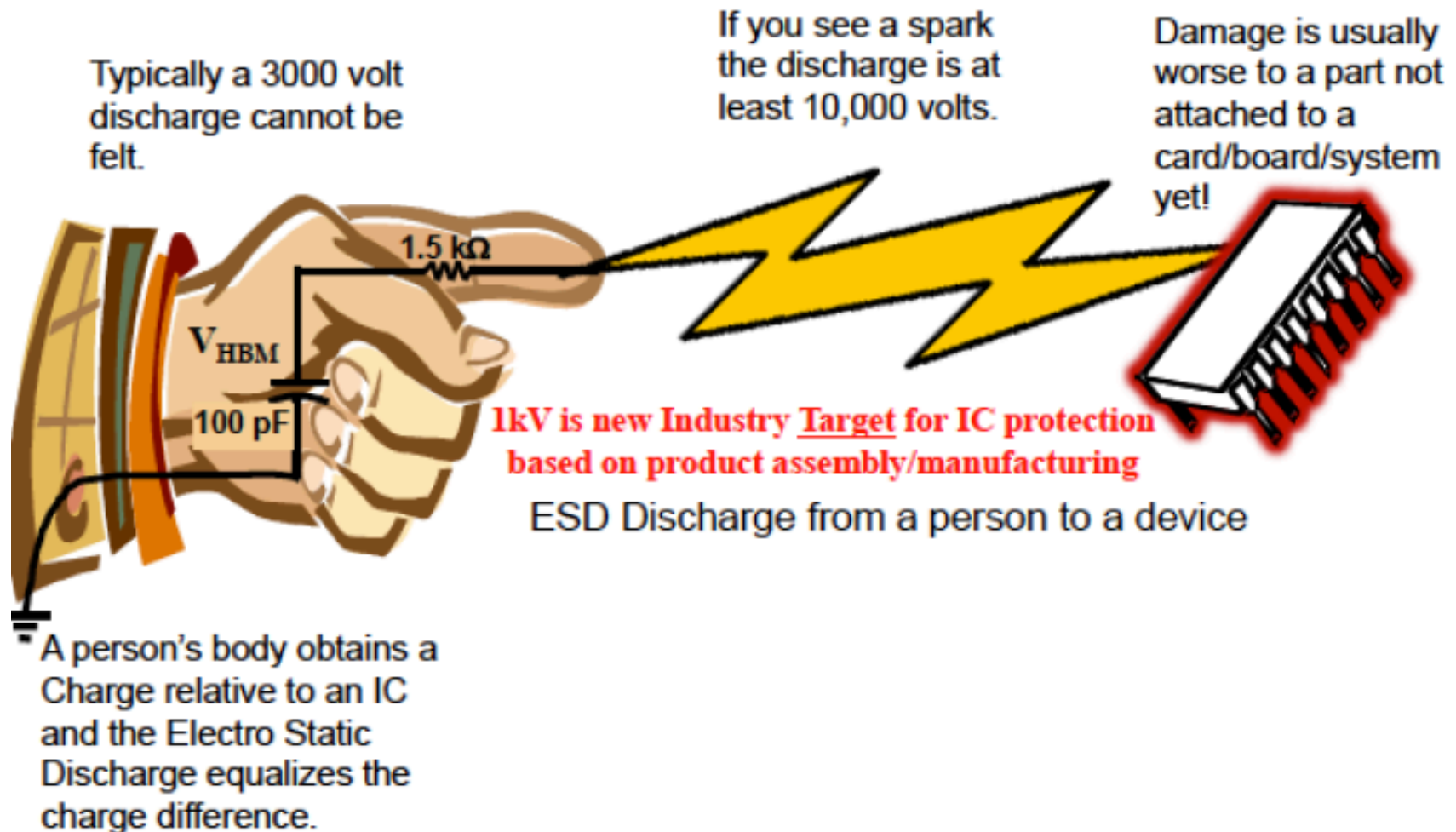
# Circuit decoupling:

## Power Supply Rejection Ratio (PSRR)

PSRR = sensitivity of an analog circuit to power supply variations

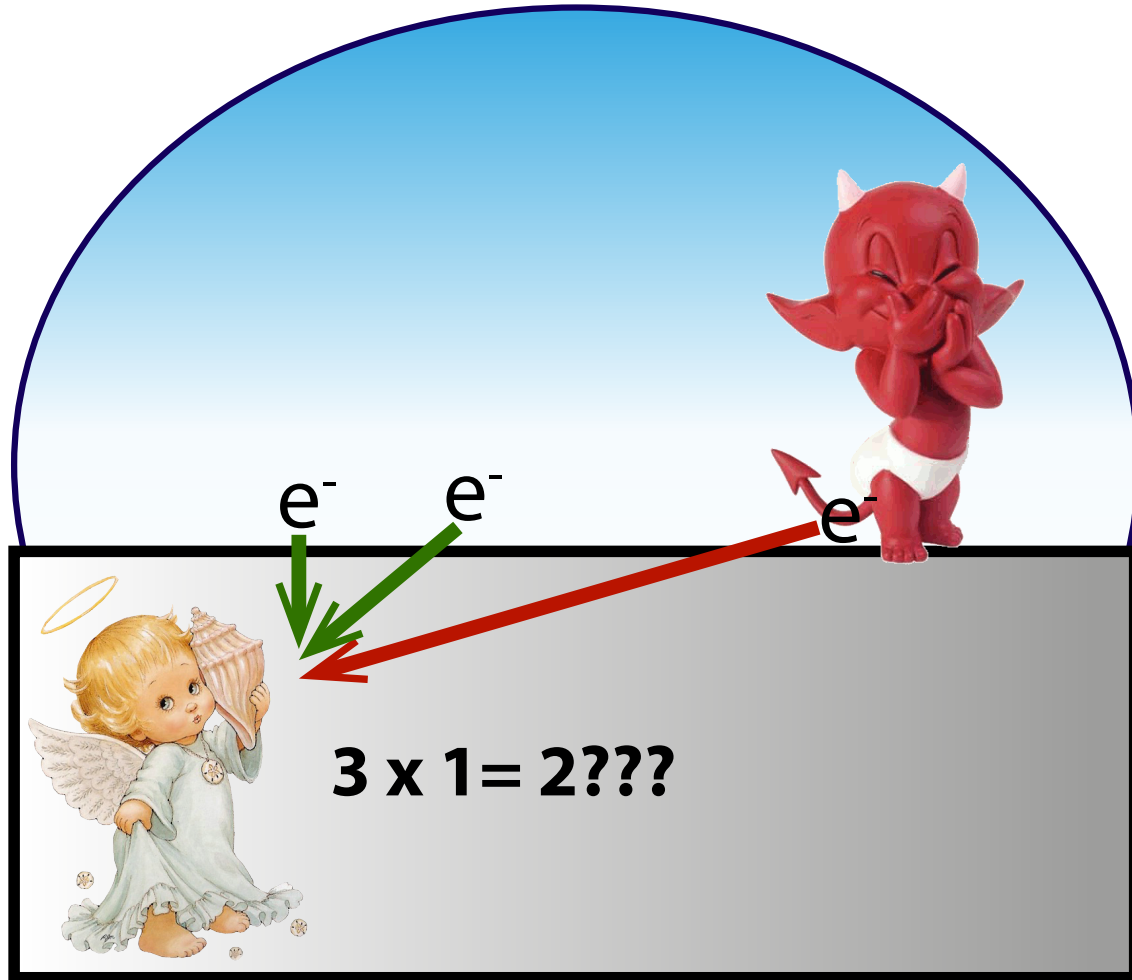
- ▲ Check the **application section in the datasheet** of each component to follow power supply decoupling recommendations.
- ▲ Main rules are:
  - ▽ **large electrolytic C** (10-100 $\mu$ F) close to chip (reservoir)
  - ▽ **small C** (0.01-0.1 $\mu$ F) physically close to power pins (short the high f away from chip),
  - ▽ decoupling Cs connected to a large-area low-impedance GND plane through via or short trace,
  - ▽ **Optional:** small ferrite bead in series with supply pin (localize the noise, keep external high f noise, keep internally generated noise from propagation to the rest of circuit).

# ElectroStatic Discharge (ESD)



# keep care 😊

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