SECTION OF ELECTRICAL ENGINEERING

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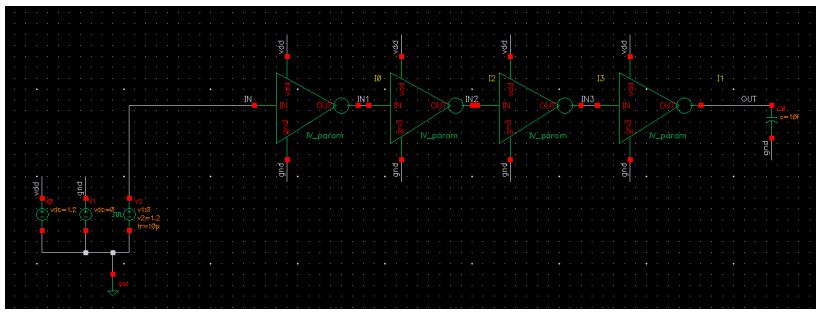
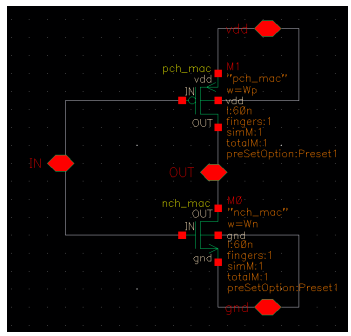
Advanced VLSI design
How to properly size a design using Virtuoso and ADE?

1. SETTING UP THE DESIGN UNDER TEST

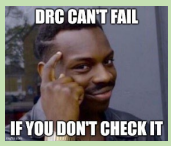
Here, for the example, we consider a simple chain of inverters in 65ll UMC CMOS technology.





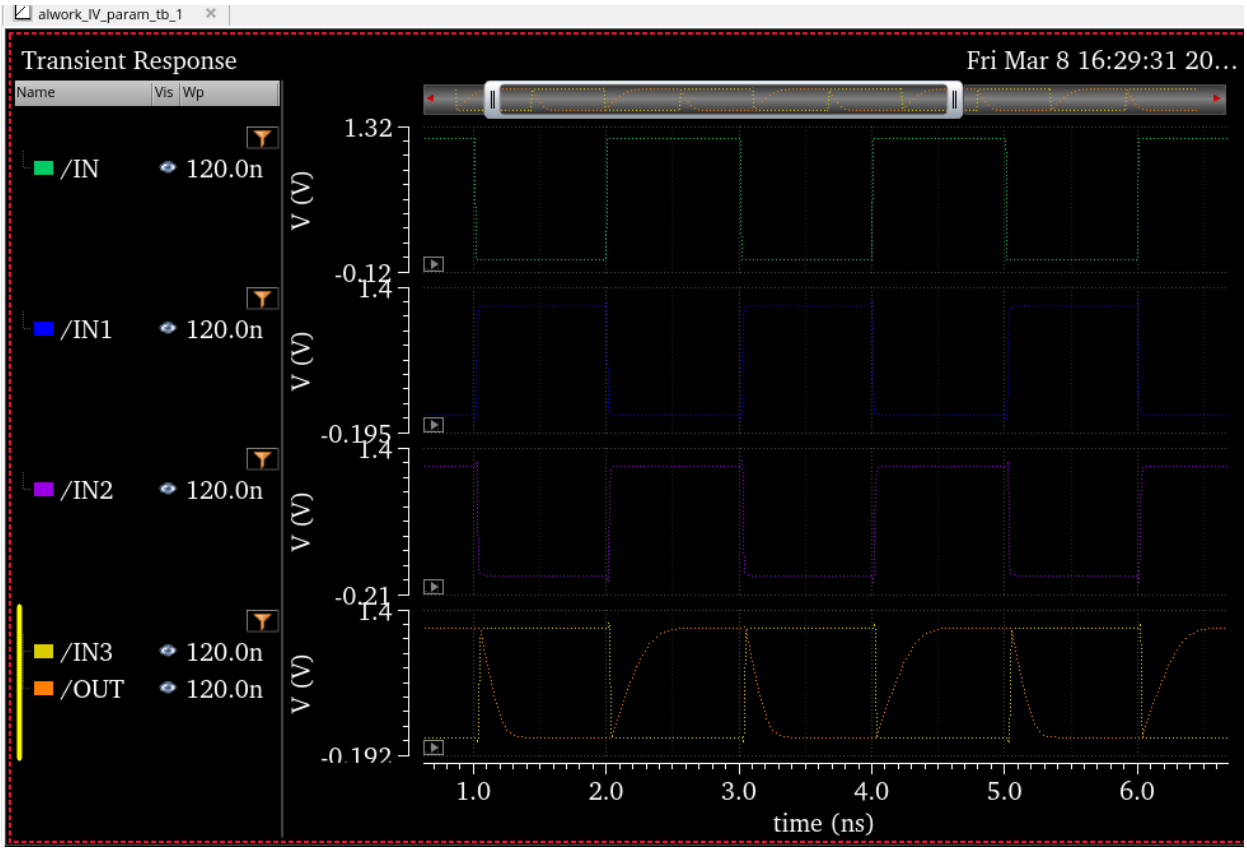
Each inverter is composed of 1pmos and 1nmos transistor (here we use nch_mac and pch_mac). We set the nmos and pmos W parameter to Wn and Wp respectively.

The input source (IN) generates a 50% 1ns period square signal between 0 and 1.2V with a rise and fall time of 10ps. The output capacitor is 10fF, and we chain several inverters to avoid capacitive coupling with the input signal.



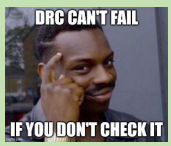
Special teacher tips: We generally advise to use “mac” devices for mos transistors as they have 4 terminal and the designer has explicit control over the bulk. In non-mac mos devices, the bulk terminal is generally connected to GND!/VSS! or VDD! using a global variable. Explicit declaration is always a good way to not make mistakes.

Create an ADE assembler view for it, set measures probes on IN, IN1, IN2, IN3 and OUT signals. Set a 10ns transient analysis. Define global variables Wn and Wp to 120n (no need to put the unit there – it’s obviously meters). Run the simulation and check that everything works properly.



Here we are particularly interested in the transmission time through the last inverter. So the delay between IN3 and OUT.

Open the calculator (tools > calculator) and use the special function delay to extract the time transmission time of the last inverter (I3) on the second rising and falling edges of OUT (here we are checking the transition at 2ns and 3ns). Call these expressions FallingOUT and RisingOUT. As we are characterizing an inverter, so one signal is falling while the second is rising (and inversely).



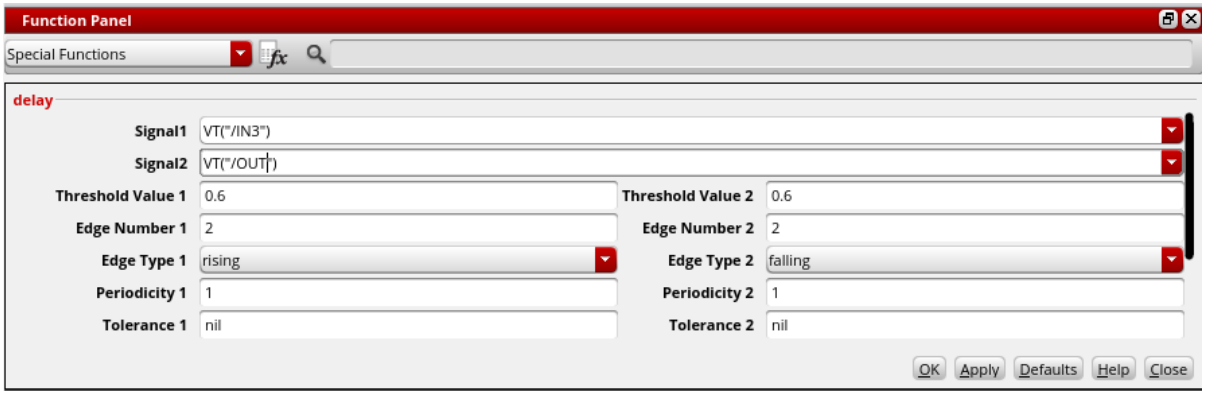
Special teacher tips: when measuring a timing, power or energy from a transient simulation, it is a good practice to not take the first switching. Typically a transient analysis starts from the state to which the DC analysis converged to. One has no guarantee that the resulting state is correct and that no nodes are stuck in some metastable states. Running a few cycles is never bad to reach some kind of "steady state" situation. Also, the measurement conditions one may want to reach are rarely the ones from the dc analysis.

Here is an example of expression :

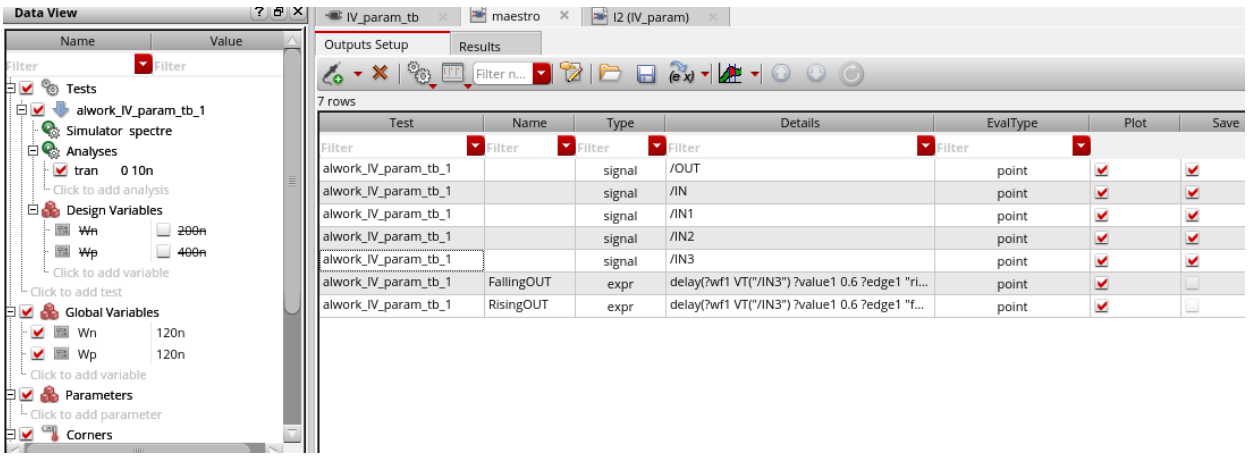
delay(?wf1 VT("/IN3"), ?value1 0.6, ?edge1 "rising", ?nth1 2, ?td1 0.0, ?tol1 nil, ?wf2 VT("/OUT"), ?value2 0.6, ?edge2 "falling", ?nth2 2, ?tol2 nil, ?td2 nil , ?stop nil, ?multiple nil)

here we consider 50-50 at 0.6V

and the corresponding calculator window :



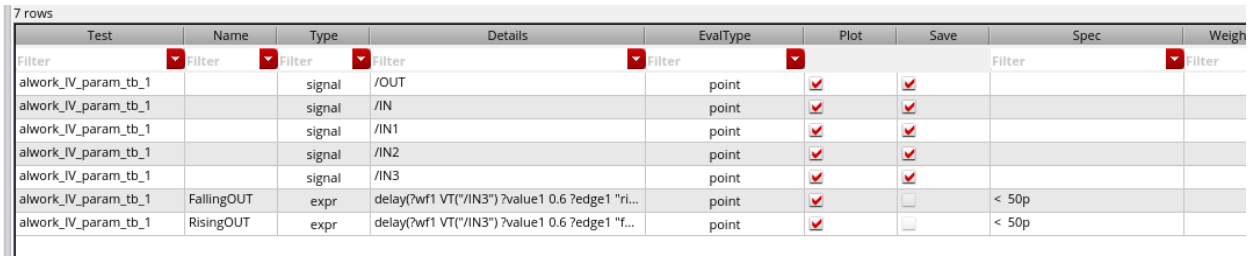
Here is a few of the ADE assembler view with all the signals and expressions.



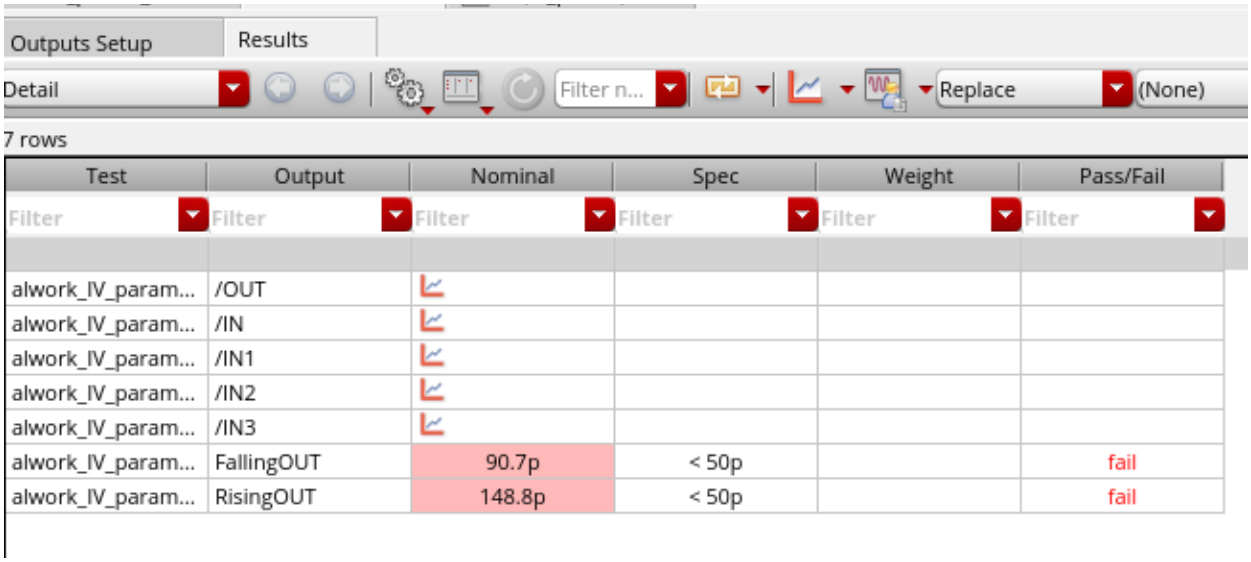
Run the simulation and check the timing you get for the falling and rising times. With such an unbalanced sizing (120nm for both Wn and Wp), you should get a much slower rising than falling as the pmos is much weaker than the nmos. Something around 90ps for falling and 150ps for rising.

2. DEFINING TARGETS

In the FallingOUT and RisingOUT expressions, define timing targets at <50ps.



Note how both of them are in red and marked as failed in the results panel after you run the simulation

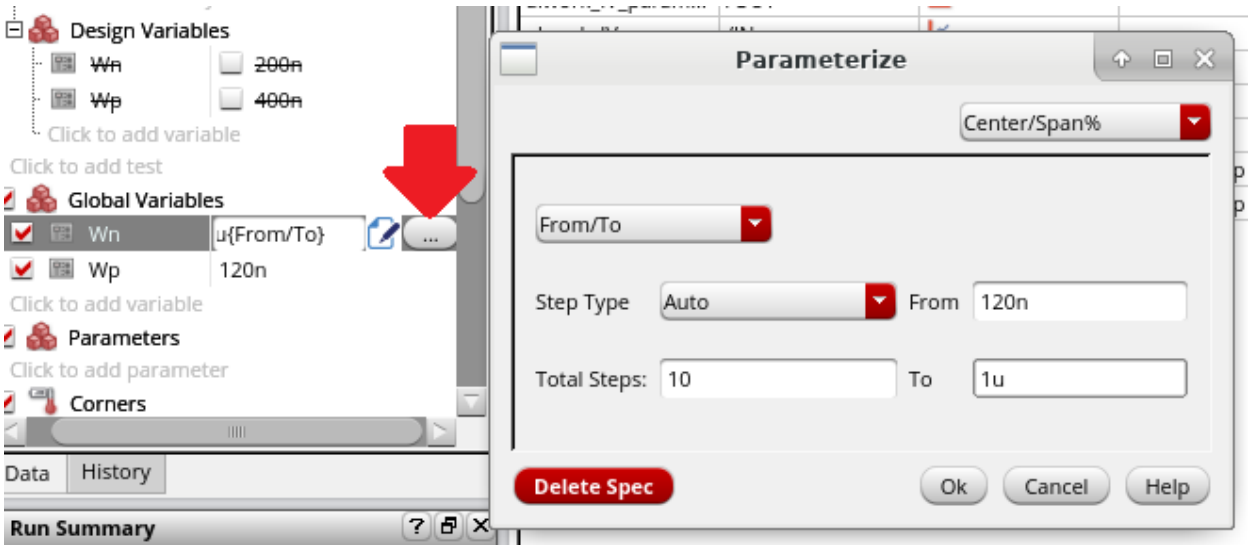


3. RUNNING A PARAMETRIC ANALYSIS

Let's analysis Wn first.

To set a parametric analysis, define a parameter, and set a from/to analysis.

- In the dataview panel in the Wn global variable, click on the "…" button
- Click delete spec to remove the current 120nm sizing
- Select from/to in the dropdown menu, and select 10 step, auto, from 120n to 1u.



This will run 10 simulations with various sizes of Wn from 120nm to 1u.

In the results panel, note that the dropdown menu has a lot of options. The Detail-transpose is generally the easier to read. Here Wp is constant and Wn varies.

Outputs Setup | Results

Detail - Transpose | Filter n... | Replace | (None)

10 rows

Point	Corner	Wn
1	nom	120n
2	nom	217.8n
3	nom	315.6n
4	nom	413.3n
5	nom	511.1n
6	nom	608.9n
7	nom	706.7n
8	nom	804.4n
9	nom	902.2n
10	nom	1u

10 rows

Pass/Fail	/OUT	/IN	/IN1	/IN2	/IN3	FallingOUT	RisingOUT
fail						90.7p	148.8p
fail						59.36p	148.9p
fail						46.77p	150.2p
fail						39.87p	152.7p
fail						36.06p	154.6p
fail						33.8p	155.2p
fail						32.04p	157.5p
fail						30.97p	158.8p
fail						30.09p	160.3p
fail						29.51p	161.9p

Counterintuitive remarks: Note that RisingOUT increases when Wn increases (think about it 😉). And if you can't find the answer, it's in the EDALABS material session 2.

Do the same with both Wn and Wp. Note that now virtuoso has to do 100 simulations. It's a lot. One way to go faster is to run several simulations in parallel.

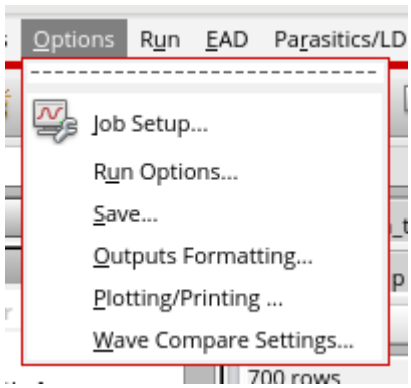
Options>Job Setup…

There you can define the number of jobs that can run simultaneously. You can put 2 in "max jobs"

Options>Run Options…

Tick "parallel"

PLEASE, be gentle with the resources. Remember that you generally work in a shared infrastructure with other users, and a limited amount of licenses.

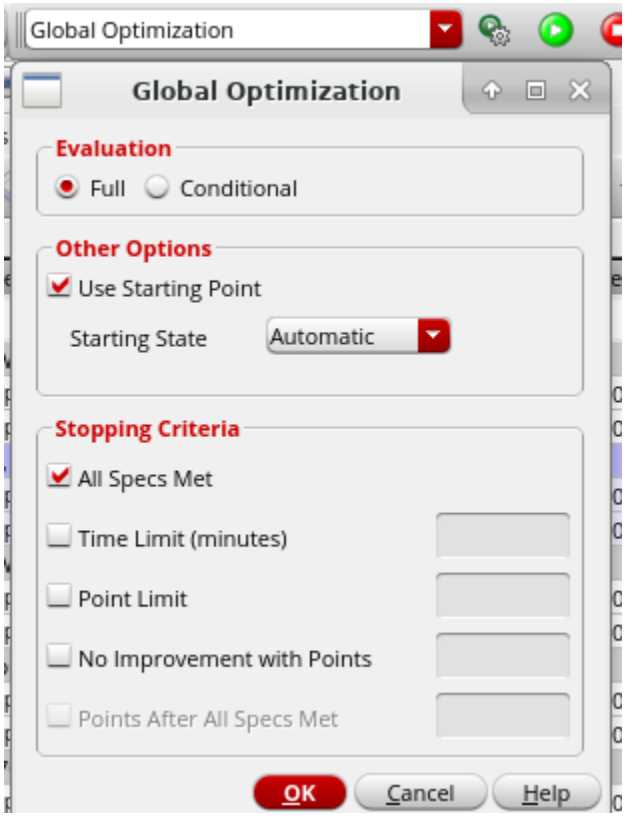


Check the result. You should find that sizes of Wn=315n and Wp=610n are good.

This highlights how design space explorations can become complex particularly when involving constrains pulling in different directions.

4. AUTOMATING PARAMETRIC ANALYSIS WITH VIRTUOSO

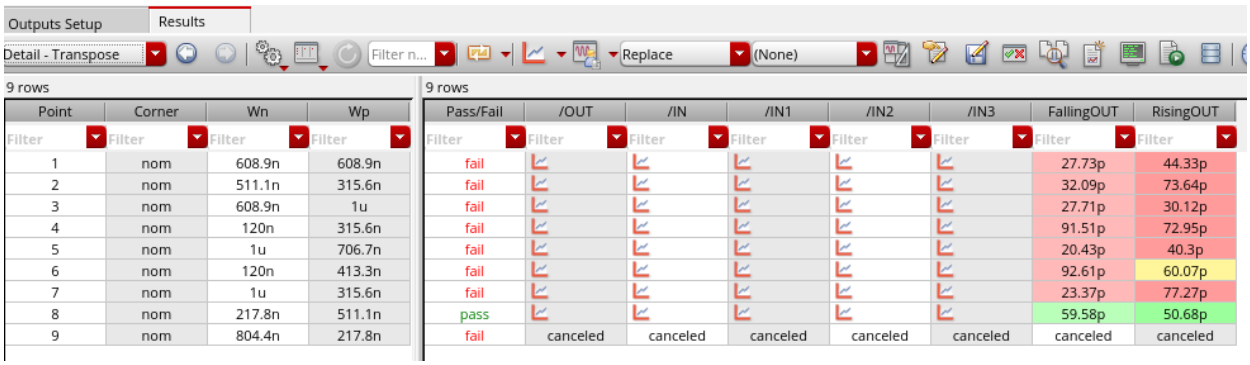
Virtuoso embeds an optimization tool that enables you to explore a design space faster. It does a pre-screening of the design space, identifies trends, and then try to find an optimum that matches with the defined targets. Note that you can also weight them to help it converge.



Select “Global optimization” and click on  . There are many options in there, here we pick a configuration, but depending on your needs you may want :

- To change parameters
- To read about it on support.cadence.com

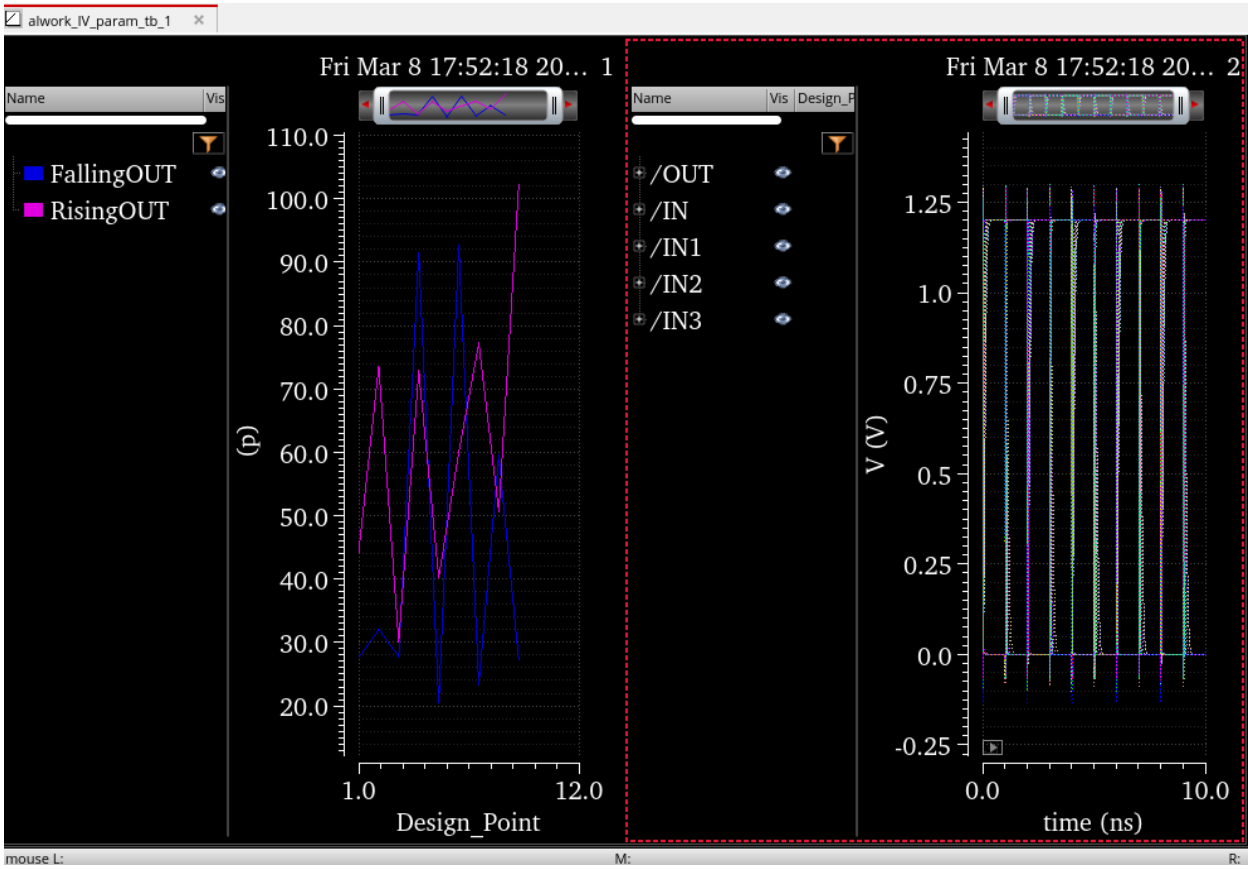
Selecting a starting point will force it to start from the middle of the range defined in the global variable panel (here approx. Wp=Wn=600nm). For the example, we updated the constraints to a range between 50p and 60ps for the target, to force the optimizer to explore the design space.



Point	Corner	Wn	Wp	Pass/Fail	/OUT	/IN	/IN1	/IN2	/IN3	FallingOUT	RisingOUT
1	nom	608.9n	608.9n	fail						27.73p	44.33p
2	nom	511.1n	315.6n	fail						32.09p	73.64p
3	nom	608.9n	1u	fail						27.71p	30.12p
4	nom	120n	315.6n	fail						91.51p	72.95p
5	nom	1u	706.7n	fail						20.43p	40.3p
6	nom	120n	413.3n	fail						92.61p	60.07p
7	nom	1u	315.6n	fail						23.37p	77.27p
8	nom	217.8n	511.1n	pass						59.58p	50.68p
9	nom	804.4n	217.8n	fail	canceled	canceled	canceled	canceled	canceled	canceled	canceled

It took 8 iterations to converge to an acceptable solution, relatively similar to the one we got with a complete design space exploration.

Clicking on  will show you the iterative process to converge.


alwork_IV_param_tb_1
Fri Mar 8 17:52:18 20... 1
Name
Vis
FallingOUT
RisingOUT
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
(p)
1.0
12.0
Design_Point
Fri Mar 8 17:52:18 20... 2
Name
Vis
Design_F
/OUT
/IN
/IN1
/IN2
/IN3
1.25
1.0
0.75
0.5
0.25
0.0
-0.25
V (V)
0.0
10.0
time (ns)
mouse L:
M:
R: