SECTION OF ELECTRICAL ENGINEERING

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ADVANCED VLSI DESIGN

Content of the MidTerm Presentation (GRADED)

Duration: 10 minutes for presenting, 5 minutes for questions and answers

Note that you have to upload your presentation on the Moodle web-site **one hour before the start of the first presentation** by using the "MidTerm Presentation" upload link. A computer with the presentation will be available in the examination room.
In your MidTerm presentation, you are expected to discuss the following content (Note that points 1,2,3 have many sub-items).

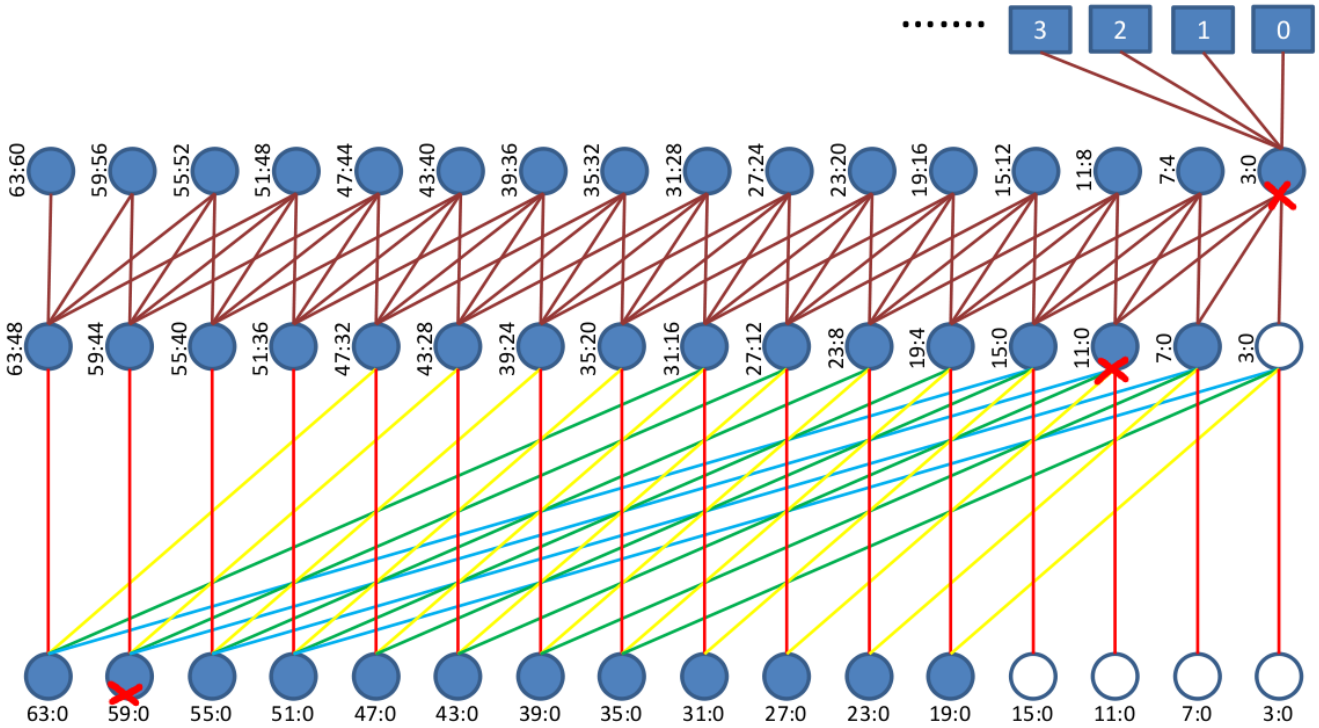
1. **Top Level Block Diagram of the 64-Bit Accumulator with Parallel-Prefix Adder**
   1.1. Give a very quick overview of the design status for each block.
   1.2. Does the accumulator pass the functionality verification with the provided tester?

2. **Discussion of the individual building blocks, focusing on the blocks that are based on dynamic logic (PG Generator, Carry Merge Block and its building blocks), you may also include and discuss relevant CMOS circuits as well if needed.**
   2.1. Boolean expression of the implemented logic functions (Inputs, Outputs) and the corresponding block diagram.
   2.2. The used logic type (Domino Logic, NP-Domino Logic; footed/unfooted etc.)
   2.3. The type of logic tree selected (N only, P only, N followed by inverter, P followed by inverter etc.)
   2.4. Transistor level schematics, indicating the inputs and the outputs clearly with the signal names at the inputs and the outputs
   2.5. Discuss the necessary solutions to the problems that have been debugged during the previous weeks. You can draw the static inverter at the output, if used, with an inverter symbol instead of a transistor level schematic.
   2.6. Justification of the reason of your choice for the Parts 2.1, 2.2, 2.3 and 2.4

3. **Design/architecture and discussion of your clock distribution and clock tree**

4. **Analysis and discussion of the critical path of the design and Signal Integrity Analysis (data and clock), based on the provided testbench that excites the critical path**
   4.1. You are expected to provide some information about the critical path of your entire design:
   - The voltage waveforms of some nodes on the critical path when the critical path is triggered

by its corresponding input vector on a single plot. In case your design is similar to the one on page 9 of the Project Description document, the signals CLK, G3:0, G11:0, G59:0 and Sum<63> (or the negated versions of some of them instead) are on the critical path.
Do not confuse G59:0 with G<59:0>. G59:0 is the combined (merged) generate signal and it is a 1-bit signal (i.e. it is not a bus representation); on the other hand, G<59:0> is the 60 bit generate signal bus where G<n> = A<n>•B<n>. The signals G3:0, G11:0, G59:0 are highlighted with a red crosses (x) in the picture below.



- The delay times between the consecutive nodes on the critical path when the critical path is triggered by its corresponding input vector on the same plot. In particular, indicate the delay times between the following signals when the critical path is triggered (show them on the voltage waveform figure):
  - CLK-G3:0
  - G3:0-G11:0
  - G11:0-G59:0
  - G59:0-Sum<63>
  - CLK-G59:0
  - CLK-Sum<63>

The provided testbench with the tester can be used for the analysis of the critical path. Here you have instructions for this analysis:

- Few vectors have been added at the beginning of vectors.txt that is used in the simulation to excite the critical path of your design. Note: if you have modified vectors.txt, please overwrite it by executing 'git checkout vectors.txt'.
- Run the simulation with the updated vectors.txt
- Make sure this test passes with no errors.
- Reminder: all the nodes are precharged during the precharge phase. The critical path is

triggered and all the nodes are toggling during the evaluation phase.
- For your presentation, we expect you to report the waveforms mentioned above during the evaluation phase (not precharge) of your circuit. In particular, you need to show that G3:0, G11:0, G59:0 and Sum<63> are all switching during this phase, therefore proving that the critical path has been excited.
- Having a functionally correct design, the critical path is expected to be excited in one of the first 5 input vectors. However, this highly depends on your design, therefore if the provided vectors do not excite the critical path of your circuit, they need to be changed accordingly. In case you have difficulties completing this task, feel free to contact the TAs for support.
- Hint: during testing, you can use 'liberal' as accuracy option for your simulator. This saves you time during the investigation/debug. However, ideally, when you have a stable working environment, you might evaluate the delays of the nodes involved in your critical path using the 'conservative' accuracy option. If this results in a very large simulation time (i.e. >>1h), you can still provide delay values from the 'liberal' simulation.

4.2. Show the waveforms of the clock signals that drive the dynamic gates that output the signals (see list above) on the critical path. Comment on the signal quality (i.e. transition times, skew...) and the timing relation between corresponding clocks and data.

4.3. Show the waveforms of: one primary input, the root of the clock tree, the clock input of the last bit of the accumulator register, and the input and output of that accumulator register (to check that timing is met).

Some recommendations for a High Quality Presentation:

1. To show your schematics, do NOT take screenshots of the Cadence schematic window. You can draw quite good-looking schematics by using the software like Visio etc. (there are tons of online tools and epfl-sponsored licenses). If you take virtuoso window screenshots, present your circuit in an understandable way and convert the colors so that the background is white and the circuit is dark (there is an option in virtuoso to change the background in white for screenshots).
2. Convert the background color of the waveform window to white and increase the thickness of the waves to make them visible. Change the colors of the waves so that they can be distinguished well.
3. Do NOT use a lot of written explanation; instead, prefer to show pictures, blocks, schematics, waveforms, arrows etc. Talk instead of reading what is written on the slides.

Good luck.