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EDA-BASED DESIGN TP-2021/2022 EDABD2020-TP04.doc

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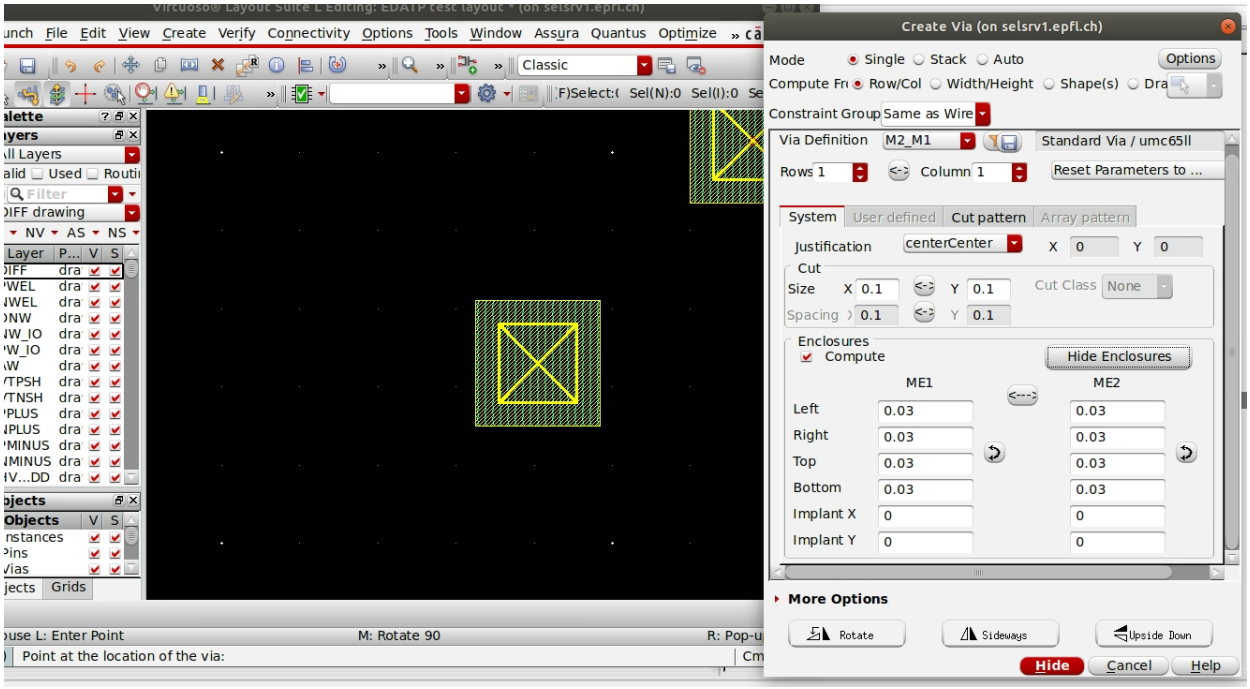
EDA-BASED DESIGN
Optimizing your design with min-size Vias

1. DEFAULT OPTIONS

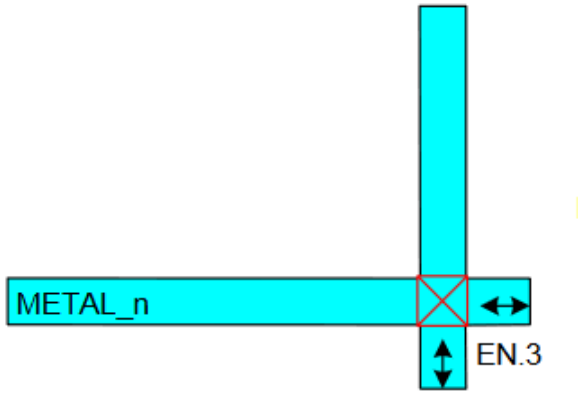
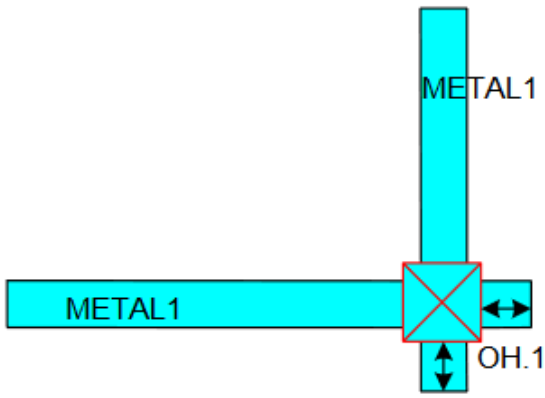
When instantiating a via with the layout default ‘o’ key, the following window appears :



PDK sometimes configure virtuoso more or less. In some PDKs, if you click on “reset parameters to…” dropdown menu, you will be able to select different configurations for the PDK. Though, here, it is not configured.

The default via does not consider the most aggressive possibilities described in the TRL (pages 61 to 64). But rather a general design structure with large spacings that will pass the DRC tests whatever are the conditions (30nm on all the sides).

Still, the TLR tells you that you can do the following :

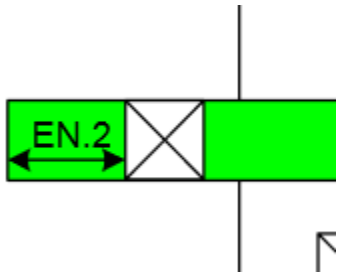
	
For Metal 2 and above	For Metal 1

The only constraints being EN.3 that must be :

1XMn-1XVn.EN3	METAL_n line end enclosure of MVIA_n at METAL_n outer corner (for two adjacent sides, at least one side should be treated as metal line end) (n=2,3,4,5)	EN.3	≧	0.03

Basically, while you respect EN.3 (30nm) on both sides of the via, you can make its enclosure 0nm for M2 and above, or have the via 5nm larger than M1. Note that M2 and above min width is 100nm while it is 90nm for M1 in this technology.

You can apply the same approach for CT (M1 to Polysilicon contact). TLR tells you, page 40 that you can have the contact on the edges of the polysilicon on 2 sides, if you respect 40nm on two sides.

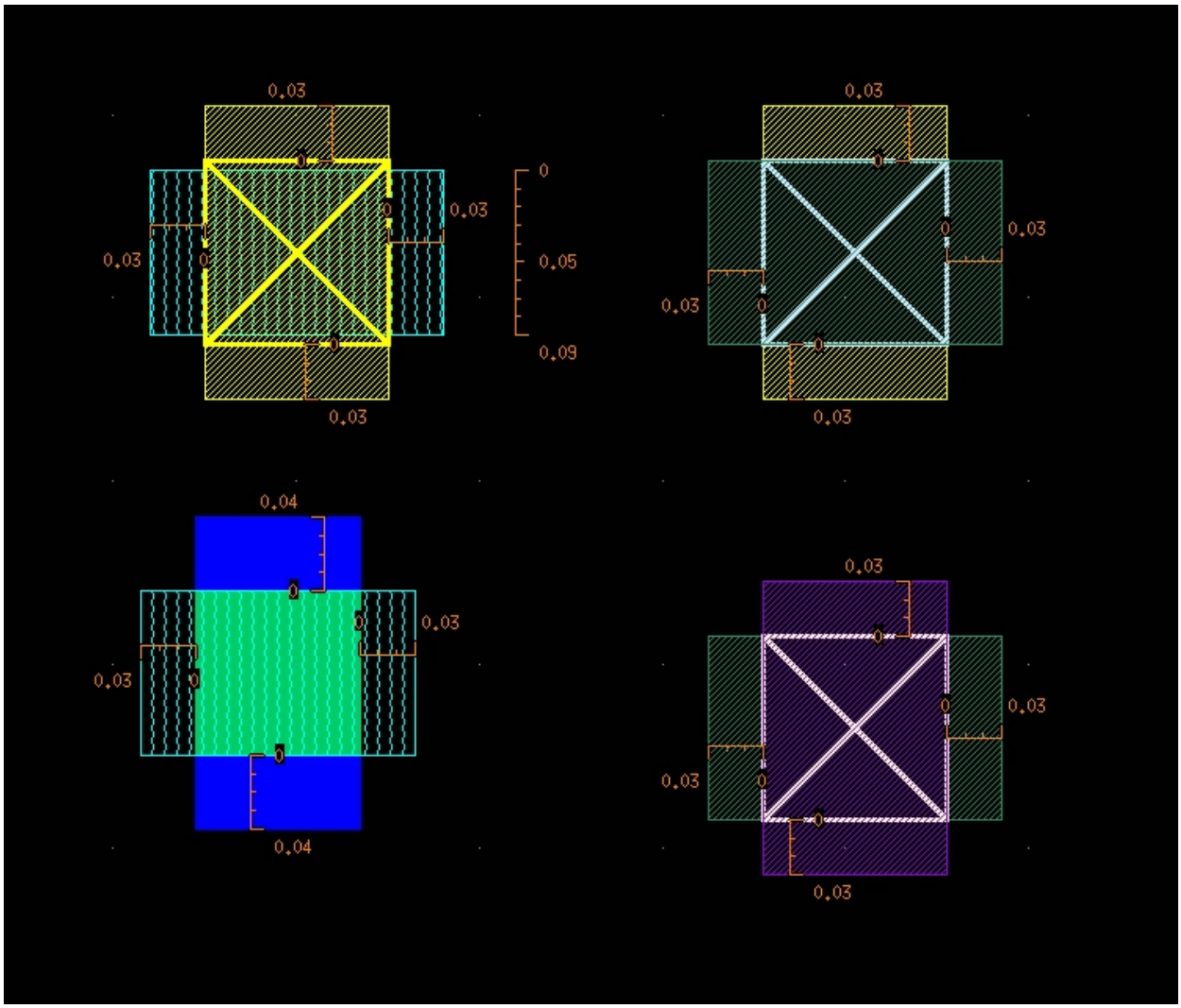


The corresponding rule is also described page 40:

PLY-CT.EN2	POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero if PLY-CT.EN1 is not fulfilled	EN.2	≧	0.04

Just keep in mind that a contact is 90nm wide. So even with that, you would need to make sure that you enlarge slightly your polysilicon line to have your contact. Note that in advanced technologies (sub30), some technologies allow the contact to be larger than the polysilicon line.

That said, the following designs are viable and will not generate DRC errors besides minimum area errors for the involved metals.



This approach will allow you to have a better density for your design and respect the horizontal and vertical routing orientation as it keeps your lines minimum size in the orientation you chose for it.

You can create these cells by using the “r” key and the ruler (“k”).

Still, you can run the following command in your CDS_VISO folder (run it only once):

> tar -zxvf /softs/classroom/tutorials/vias_65nm_UMC.tar.gz

It will extract a lib called VIAS_65nmUMC (you will see a folder called like that), and you can import it in your design by adding one line in your cds.lib file, or through virtuoso (tools>Library path editor). We describe this procedure in one of the tutorials.

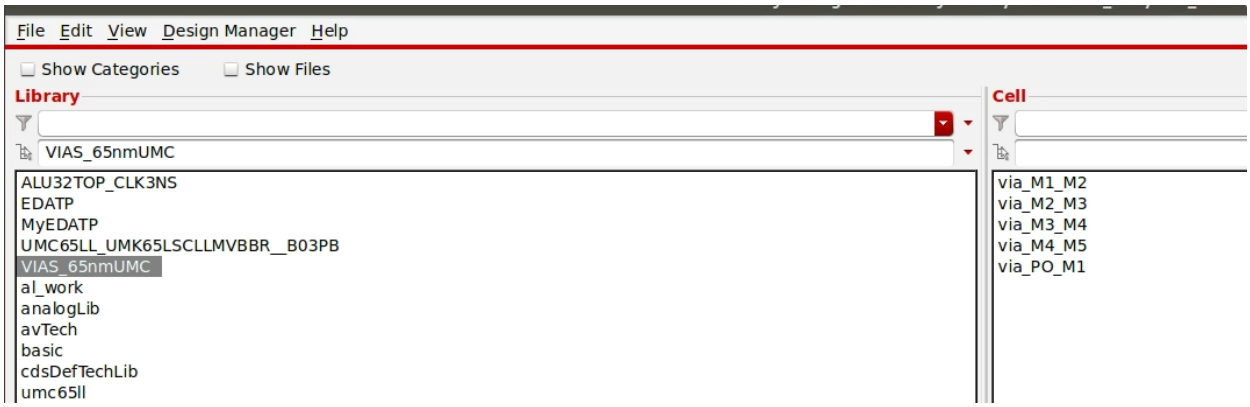
The resulting line in your cds.lib would be :

DEFINE VIAS_65nmUMC *path_to_the foder*

If the folder is inside your CDS_VISO folder, the following line will work :

DEFINE VIAS_65nmUMC VIAS_65nmUMC

The resulting view in virtuoso will be the following :



Each via can be instantiated in your design if you want to use it like that. Rotate it based on your needs.