UMC

* BEGIN *

65 nm Logic and Mixed-Mode Low Leakage Process Topological Layout Rule

(Ver.1.19_P. 1)

P-Sub, Logic and Mixed-Mode Process

1. Contents Page

2. Revision History

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
1.19	1	06/16/2015	**6.A.2.1 DC Rules** mA/um..	**6.A.2.1 DC Rule** mA/Via	
			6.E Pulse Rule None	**6.E Pulse Rule** Add Metal Width and Thickness.and figures	

3. Mask Layer Definitions

Mask ID	Layer	Description Digitized	Digitized Area Pattern	(Dark/Clear)
P20	DIFFUSION	Define active region	DIFFUSION	D
P92	N_WELL	Define N_WELL implant region	N_WELL	C
PC0	DEEP_N_WELL	Define DEEP N_WELL region	DEEP_N_WELL	C
P91	P_WELL	Define P_WELL implant region	(*1)	D
P10	P-	Define 1.8V/2.5V /3.3V PMOS Device	(*1)	C
P33	N-	Define 1.8V/2.5V/3.3V NMOS Device	(*1)	C
P1T	VTP_LL	Define LL_RVT PMOS Device	(*1)	C
P1S	VTN_LL	Define LL_RVT NMOS Device	(*1)	C
P1V	VTP_LLH	Define LL_HVT PMOS Device	(*1)	C
P1U	VTN_LLH	Define LL_HVT NMOS Device	(*1)	C
P1R	VTP_LLL	Define LL_LVT PMOS Device	(*1)	C
P1Q	VTN_LLL	Define LL_LVT NMOS Device	(*1)	C
P21	TG	Define thick gate oxide formation	TG	D
P87	N+_POLY_IMP	Define N+ Poly implant region	(*1)	C
P30	POLY1	Define Poly layer	POLY1	D
PA3	HV_NLDD	Define 1.8V/2.5V/3.3V NMOS Device &1.8V/2.5V/3.3V NATIVE Device	(*1)	C
P1N	LL_PLDD	Define LL family PMOS Devices	(*1)	C
P1M	LL_NLDD	Define LL family NMOS devices and 1.2V NATIVE Device	(*1)	C
P98	N+	Define N+ implant region	N+	C
P97	P+	Define P+ implant region	(*1)	C
P99	PESD	Define PESD Implant Region	PESD	C
P29	SAB	Define non-salicide region	(*1)	D
P31	HR	Define high resistance Poly resistors	HR	C
P3M	MR	Define medium resistance Poly resistors	MR	C
P56	CONTACT	Define Poly and Diffusion Contact	CONTACT	C
P60	METAL1	Define 1st Metal	METAL1	C
P66	MVIA1	Define 1st and 2nd Metal Contacts	MVIA1	C
P67	METAL2	Define 2nd Metal	METAL2	C
P68	MVIA2	Define 2nd and 3rd Metal Contacts	MVIA2	C
P69	METAL3	Define 3rd Metal	METAL3	C
P70	MVIA3	Define 3rd and 4th Metal Contacts	MVIA3	C
P71	METAL4	Define 4th Metal	METAL4	C
P72	MVIA4	Define 4th and 5th Metal Contacts	MVIA4	C
P73	METAL5	Define 5th Metal	METAL5	C
P74	MVIA5	Define 5th and 6th Metal Contacts	MVIA5	C
P75	METAL6	Define 6th Metal	METAL6	C
P76	MVIA6	Define 6th and 7th Metal Contacts	MVIA6	C
P77	METAL7	Define 7th Metal	METAL7	C
P61	MIMAM	Define MIM alignment mark	MIMAM	C
P7G	MIMTP	Define top plate of MIM	MIMTP	D
P65	MIMBP	Define bottom plate of MIM	MIMBP	D
PF2	MVIA7	Define 7th and 8th Metal Contacts	MVIA7	C
PF3	METAL8	Define 8th Metal	METAL8	C
PF6	MVIA8	Define 8th and 9th Metal Contacts	MVIA8	C
PF7	METAL9	Define 9th Metal	METAL9	C
PF8	MVIA9	Define 9th and 10th Metal Contacts	MVIA9	C
PF9	METAL10	Define 10th Metal	METAL10	C
PL1	TMV_RDL	Define 10th Metal and Al-Pad Contacts	TMV_RDL	C
PL2	AL_RDL	Define Al-Pad	AL_RDL	D
PL3	PASV_RDL	Define Al-Pad Window region	PASV_RDL	C
PL6 (*2)	CU_FUSE_PAD	Define Copper-Fuse Window region	CU_FUSE_PAD	C

Note: *1, Please refer to 65nm CMOS platform mask tooling rule:
2, An additional PL6 layer is required for products with copper fuse.

4. Topological Layout Rules

The following TLR is organized into two major sections: Section 4A, "FEOL Layout Rules," and Section 4B, "BEOL Layout Rules."

All layout rules are given in um or um^2 and minimum design grid is 5nm. For DIFFUSION, POLY1, N+, P+, CONTACT, METAL1, MVIA1, 1X pitch METAL, 1X pitch MVIA, 2X pitch METAL and 2X pitch MVIA layer, 1nm grid is allowed. Most of these dimensions are the target dimensions on wafer, excluding mask biases, OPC, Poly trimming, etc.

a. UMC offers the L55SP process, which is a 10% linear shrink of the L65SP process. However, L65LL does not offer 10% shrinkage path due to process concern.
b. The intention for L65LL layers is to be compatible with L65SP. For customers with intention to have L55SP compatible design in L65LL process, additional L55SP compatible rules are provided in this document as reference.
c. 1nm grid is allowed for 4X pitch METAL, 4X pitch MVIA, 6X pitch METAL, 32.5KA METAL, 32.5KA MVIA and AL_RDL, TMV_RDL, PASV_RDL over SEAL_RING_MARK area.
d. Verified SRAM layouts should be waived to their corresponding SRAM rules. Customer who changes the layouts should take all risks. For logic layouts at the boundary between SRAM and logic areas, logic rules need to be followed.

Rules that vary between L55SP and L65LL processes

Rule No.	Description		L65LL	L55SP compatible
NT-DF.S2	Spacing of NATIVE to unrelated DIFFUSION	≧	0.25	0.28
NT-DF.EN1	NATIVE enclosure of DIFFUSION	=	0.25≦EN1 ≦ 0.28	0.28
PLY_NT.W2	POLY1 width for NATIVE device over NATIVE but not over TG	≧	0.20	0.22
PLY_NT.W3.TG18	POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device	≧	1.0	1.1
PLY_NT.W3.TG25	POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device	≧	1.2	1.33
PLY_NT.W3.TG33	POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device	≧	1.2	1.33
PLY_NT.W4.TG25_OD33	POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS	≧	1.4	1.55
PLY_G.S1	Spacing of parallel POLY1 gates	≧	0.13	0.15
PLY.W.TG18	POLY1 width over TG of 1.8V device (for 1.8V+/-10% voltage tolerance)	≧	0.18	0.20
PLY.W.TG25	POLY1 width over TG of 2.5V device (for 2.5V+/-10% voltage tolerance)	≧	0.24	0.26
PLY.W.TG33	POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance)	≧	0.37	0.41
PLY_PG.W.TG25_OD33	POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS	≧	0.4	0.42
PLY.W.TG25_UD18	POLY1 width over TG and CAD_UD_MARK of 2.5V underdrive 1.8V device (for 1.8V+/-10% voltage tolerance)	≧	0.22	0.24
PLY-DF.OH3	POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um	≧	NA	0.16
Die Seal Ring Rules	Please refer to the Spec. No. G-03DSR-GENERATION65N-TLR/DIE_SEAL_RING			
ESD rules	Please refer to the Spec. No. G-03E-GENERATION65N-TLR/ESD			
FLIP CHIP rules	Please refer to the Spec. No. G-03FC-GENERATION65N-TLR/FLIP_CHIP			
BOAC rules	Please refer to the Spec. No. G-03B-GENERATION65N-TLR/BOAC			
Cu Fuse rules	Please refer to the Spec. No. G-03F-GENERATION65N-CU-TLR/FUSE			
MIM Capacitor rules	Please refer to section 4B.a.11.1 MIM capacitor			
Generic Pad rules	Please refer to section 4B.a.7.2 & 4B.b.7.2 Generic Pad Related Layout Guidelines			
1XMn.A1	METAL_n area (n=2,3,4,5,6)	≧	0.046um^2	0.052um^2

4.0 Figures and Rules Definition

4.0.1 Rule Definitions

For the following section, "A" and "B" refer to shapes on layer A and layer B respectively.

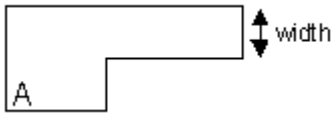
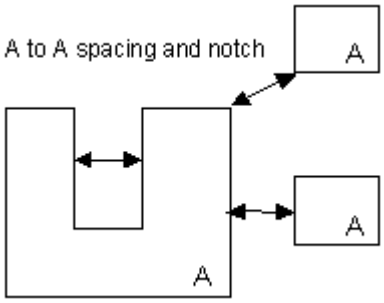
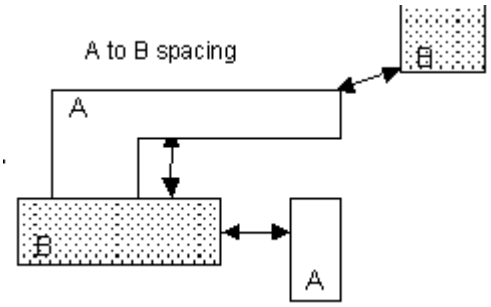
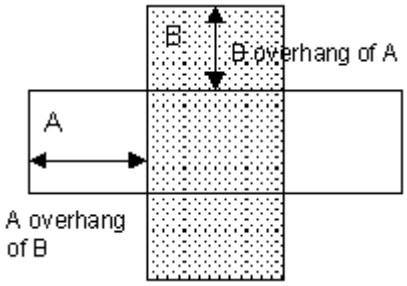
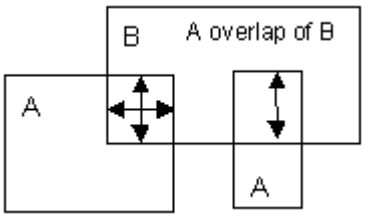
Width	Distance between inside edges of an individual shape. Width is measured between edges that are parallel or form an angle < 90deg.
Exact size	Exact size of an individual shape, Shape must be rectangular.
Length	Length of an individual shape. Shape must be rectangular. Length is the longer side of the rectangle.
Space and notch	Distance between all parallel outside edges of all shapes.
Area	Area of each individual shape.
Enclosed area	Enclosed area of each individual shape.
Density	Density of A. Specified as a window of a given size which is stepped in x increments across the chip.
A shapes must be orthogonal	All edges of A must be parallel to the x or y axis
A shapes must be rectangular	All shapes of A must be rectangles (or squares). Any angle of the edges in respect to the x- or y-axis is allowed.
Spacing of A to B	Distance between all outside edges of A and outside edges B.
Maximum space	Maximum distance in the well to the next well contact. Used for latch-up checks only
A overlap of B	Spacing of all inside edges of shapes on layer A and B if those shapes intersect.
A overhang of B	Spacing of all inside edges of shapes A to outside edges of shapes B if not shielded by outside edges of shape B.
A enclosure of B	All shapes on layer B which touch shapes on layer A (a). must be entirely covered by shapes of layer A. AND (b). All outside edges of shapes B must have a minimum spacing to all inside edges of shapes A. (c) Shapes on B that do not touch A are not checked.
A and B common run length	Cumulative sum of length of parallel adjacent outside edges of shapes of layer A and B
A or B	Result is the geometrical union of shapes on layer A with shapes on layer B.
A over B	Result is the geometrical intersection of shapes on layer A with shapes on layer B.
A not over B	Result is the geometrical intersection of shapes on layer A with the complement of shapes on layer B.
A touching B	All shapes on A that have either common edges and/or common area and/or common corners with shapes on level B.
A not allowed over B	Geometrical intersection of shapes on layer A with shapes on layer B is not allowed.
A rule (B1, B2, B3 ...)	The rule assigns A to all B: A rule B1, A rule B2,...
(A1, A2 ...) rule B	The rule assigns all A's to B: A1 rule B, A2 rule B, ...

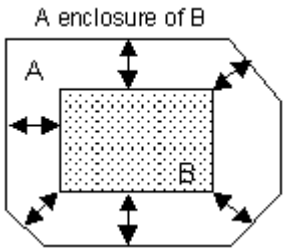
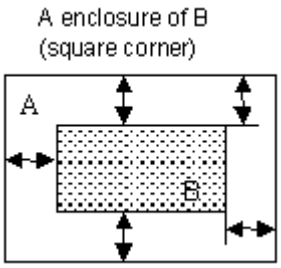
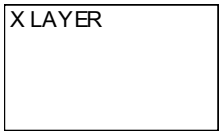
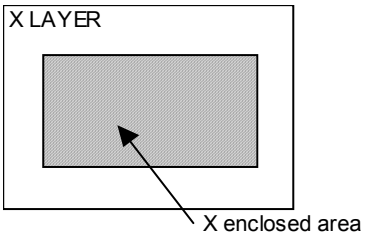
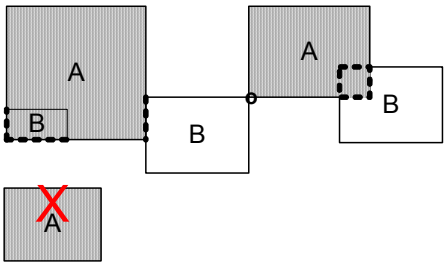
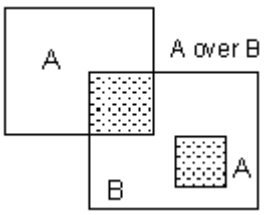
4.0.2 Abbreviations

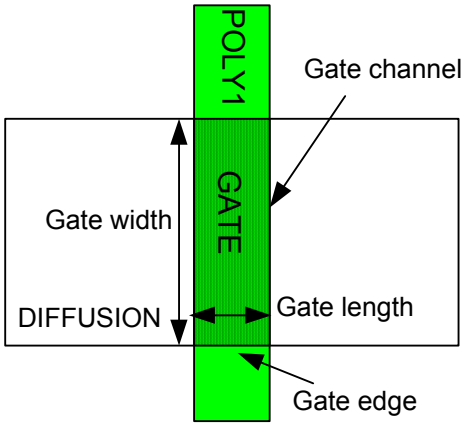
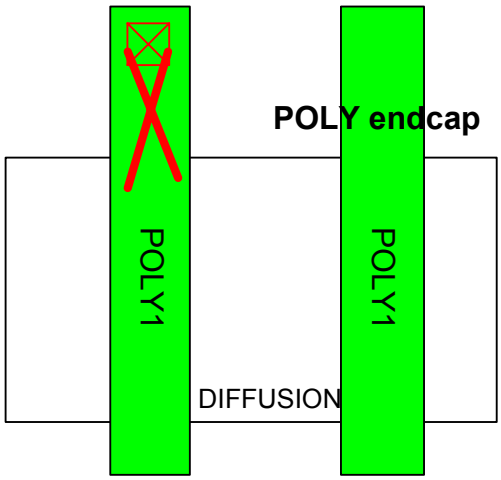
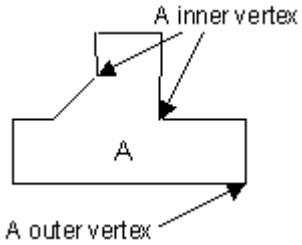
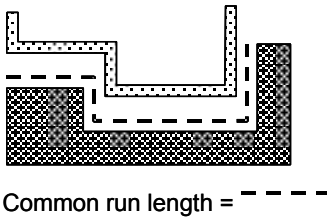
The following abbreviations are used to make the TLR document more readable.

TERM	DEFINITION
Gate	POLY1 over DIFFUSION
NMOS Gate	Gate not over N_WELL
PMOS Gate	Gate over N_WELL
Core Device	Gate not over TG
I/O Device	Gate over TG
NATIVE Device	Gate over NATIVE layer
NCAP /MIS_VAR Device	Gate over MIS_IMPLANT_BLOCK
N+ DIFFUSION	DIFFUSION over N+
P+ DIFFUSION	DIFFUSION over P+
Poly on field	POLY1 not over DIFFUSION
P_WELL	Not N_WELL
DIFFUSION Contact	CONTACT over DIFFUSION
Poly CONTACT	CONTACT over POLY1
N+ CONTACT	CONTACT over N+ DIFFUSION
P+ CONTACT	CONTACT over P+ DIFFUSION
N_WELL pick up	(N+ DIFFUSION not touching POLY1) over N_WELL
P_WELL pick up	(P+ DIFFUSION not touching POLY1) over P_WELL
Soft CONTACT	CONTACT on one side of a butted junction when other side of butted junction does not enclose a CONTACT.
N+ DIFFUSION non-salicide resistor	(N+ DIFFUSION touching SAB and touching CONTACT) not touching POLY1
P+ DIFFUSION non-salicide resistor	(P+ DIFFUSION touching SAB and touching CONTACT) not touching POLY1
N+ DIFFUSION salicide resistor	(N+ DIFFUSION over CAD_DIFFUSION_RESISTOR_SYMBOL) not touching SAB
P+ DIFFUSION salicide resistor	(P+ DIFFUSION over CAD_DIFFUSION_RESISTOR_SYMBOL) not touching SAB
N+ POLY1	POLY1 over N+
P+ POLY1	POLY1 over P+
N+ POLY1 non-salicide resistor	(N+ POLY1 not touching DIFFUSION) touching SAB
P+ POLY1 non-salicide resistor	(P+ POLY1 not touching DIFFUSION) touching SAB
N+ POLY1 non-salicide resistor body	(N+ POLY1 not touching DIFFUSION) over SAB
P+ POLY1 non-salicide resistor body	(P+ POLY1 not touching DIFFUSION) over SAB
N+ POLY1 salicide resistor	(N+ POLY1 over CAD_POLY_RESISTOR_SYMBOL) not touching SAB
P+ POLY1 salicide resistor	(P+ POLY1 over CAD_POLY_RESISTOR_SYMBOL) not touching SAB
MOS	Transistor structure consists of drain/source/gate/substrate
MOM Capacitor	Metal oxide metal capacitor
Poly endcap	POLY1 Region overhanging DIFFUSION without a CONTACT

4.0.3 Figures of Rule Definitions

Geometrical Terminology	Figures	Rule No.
Width		A.W
Spacing and notch		A.S
Spacing		A-B.S or B-A.S
Overhang		A-B.OH (A overhang of B) or B-A.OH (B overhang of A)
Overlap		A-B.OL or B-A.OL

Geometrical Terminology	Figures	Rule No.
Enclosure	 	A-B.EN
Area		X.A
Enclosed area		X.EA
A touching B	A touching B 	A.R1 or B.R1
A over B		

Geometrical Terminology	Figures	Rule No.
Gate		
POLY endcap		
Inner/outer vertex		
Common run length		

4.0.4 Rule Descriptions

Category	Rule #	Descriptions (examples)
Size	$.SZ	Exact $ size
Min Width	$.W	$ Width
	$.W.%	$ Width over %
		$ Width for interconnect
		$ Width over % but not over %2
		$ Width over % and %2
Max Width	$.WX	$ Max Width
Length	$.L	Length of $
	$.S	Spacing and notch of $
	$.S.%	Spacing and notch of $ to [$ over %]
		Spacing and notch of $ to [$ touching %]
	$-&.S	Spacing of $ to &
		Spacing of $ to & with common run length ≧ ??um
		Spacing of $ to & without common run length
		Spacing of $ to [& with width > ??um]
		Spacing of $ to [& of non-equal-potential]
		Spacing of $ to & edge
		Spacing of $ to & channel
		Spacing of $ to & for ≧?X? MVIA1 array
Overhang	$-&.OH	$ overhang of &
	$-&.OH.%	$ overhang of & over %
Overlap $	&.OL	$ overlap of &
Enclosure	$-&.EN	$ enclosure of &
	$-&.EN.%	$ enclosure of [& over %]
		$ enclosure of [& touching %]
Area	$.A	$ Area
Max Area	$.AX	$ Max area
Enclosed Area	$.EA	$ Enclosed area
Density	$.D	$ Density over ??um x ??um area (stepped in ??um increments across the chip)
		Density over ??um x ??um area within & or &2 stepped in ??um increments across the chip
Rule	$.R	$ patterns must be orthogonal
		$ must be within &
		$ must touch &
		45 degrees $ is not allowed
Recommended	$.RCM	It is recommended to put as many CONTACTs as possible in the DIFFUSION region to avoid current drop due to DIFFUSION resistance

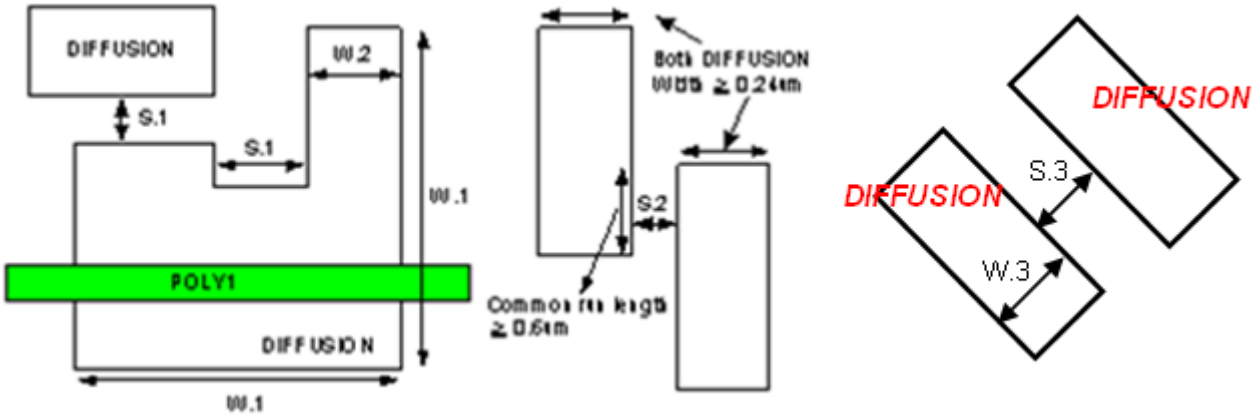
Note: This table is a reference for the automatic generation of DRC.

4A FEOL Layout Rules

4A.1 DIFFUSION (DF) Layer Layout Rules

(unit : um)

Rule No.	Description	Label		Rule
DF.W1	DIFFUSION width for device	W.1	≧	0.08
DF.W.TG18	DIFFUSION width [over TG of 1.8V device]		≧	0.24
DF.W.TG25	DIFFUSION width [over TG of 2.5V device]		≧	0.32
DF.W.TG33	DIFFUSION width [over TG of 3.3V device]		≧	0.32
DF.WX	DIFFUSION maximum width		≦	100.00
DF.W2	DIFFUSION width	W.2	≧	0.08
DF.S1	Spacing and notch of DIFFUSION	S.1	≧	0.11
DF.S.TG	Spacing and notch of DIFFUSION to [DIFFUSION touching TG]		≧	0.18
DF.S2	Spacing and notch of DIFFUSION patterns with common run length ≧ 0.60um and the width of both DIFFUSION patterns ≧ 0.24um	S.2	≧	0.12
DF.A	DIFFUSION area		≧	0.054
DF.EA	DIFFUSION enclosed area		≧	0.085
DF.D	DIFFUSION density within DIFFUSION_DUMMY_BLOCK over 150um x 150um area (stepped in 50um increments across the chip) Note1: Customers who don't need UMC to add dummy are required to draw DIFFUSION_DUMMY_BLOCK over the whole chip, such that UMC dummy insertion will be excluded and this rule can check DIFFUSION density over the whole chip. Note2: Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside DIFFUSION_DUMMY_BLOCK area after the IP mergence.		≧	20%
DF.DX	DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)		≦	80%
DF.W3	Width of 45 degree DIFFUSION	W.3	≧	0.18
DF.S3	Spacing of 45 degree DIFFUSION	S.3	≧	0.18



The following two layers are customer diffusion dummy, DIFFUSION_CUSTOMER_DUMMY (GDS no : 70(8))

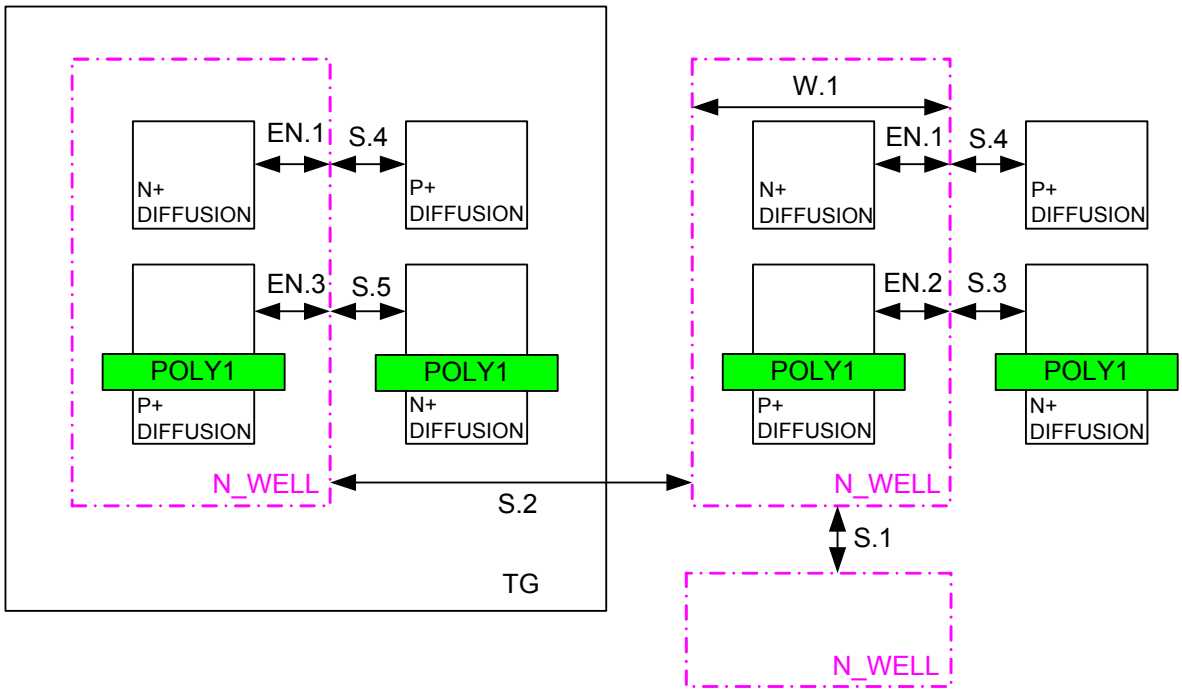
(unit : um)

Rule No.	Description	Label		Rule
DFDM.W4	DIFFUSION_CUSTOMER_DUMMY width		≧	1.5
DFDM.S4	Spacing and notch of DIFFUSION_CUSTOMER_DUMMY		≧	0.5
DFDM-NW.S5	Spacing of DIFFUSION_CUSTOMER_DUMMY to N_WELL		≧	0.4
DFDM-NW.EN1	N_WELL enclosure of DIFFUSION_CUSTOMER_DUMMY		≧	0.4
DFDM-AW.S6	Spacing of DIFFUSION_CUSTOMER_DUMMY to AW		≧	0.4
DFDM-AW.EN2	AW enclosure of DIFFUSION_CUSTOMER_DUMMY		≧	0.4
DFDM-DF.S8	Spacing of DIFFUSION_CUSTOMER_DUMMY to DIFFUSION		≧	1.0
DFDM-PLY.S9	Spacing of DIFFUSION_CUSTOMER_DUMMY to POLY1		≧	1.0
DFDM-NWR.S10	Spacing of DIFFUSION_CUSTOMER_DUMMY to N_WELL_RESISTOR		≧	1.0
DFDM- DFDM.S11	Spacing of DIFFUSION_CUSTOMER_DUMMY to DIFFUSION_DUMMY_BLOCK		≧	1.0
DFDM-FM.S12	Spacing of DIFFUSION_CUSTOMER_DUMMY to FUSE_MARK		≧	1.0

4A.2 N_WELL (NW) Layer Layout Rules

(unit : um)

Rule No.	Description	Label		Rule
NW.W1	N_WELL width	W.1	≧	0.45
NW.S1	Spacing and notch of N_WELL to [N_WELL of equal-potential]	S.1		0 or≧ 0.45
NW.S2	Spacing and notch of N_WELL to [N_WELL of non-equal-potential]	S.2	≧	0.90
NW-N_DF.S3	Spacing of N_WELL to N+ DIFFUSION	S.3	≧	0.15
NW-P_DF.S4	Spacing of N_WELL to P+ DIFFUSION	S.4	≧	0.14
NW-N_DF.S5.TG	Spacing of N_WELL to [N+ DIFFUSION touching TG]	S.5	≧	0.31
NW-N_DF.EN1	N_WELL enclosure of N+ DIFFUSION	EN.1	≧	0.14
NW-P_DF.EN2	N_WELL enclosure of P+ DIFFUSION	EN.2	≧	0.15
NW-P_DF.EN3.TG	N_WELL enclosure of [P+ DIFFUSION touching TG]	EN.3	≧	0.31
NW.R	N_WELL patterns must be orthogonal			Yes

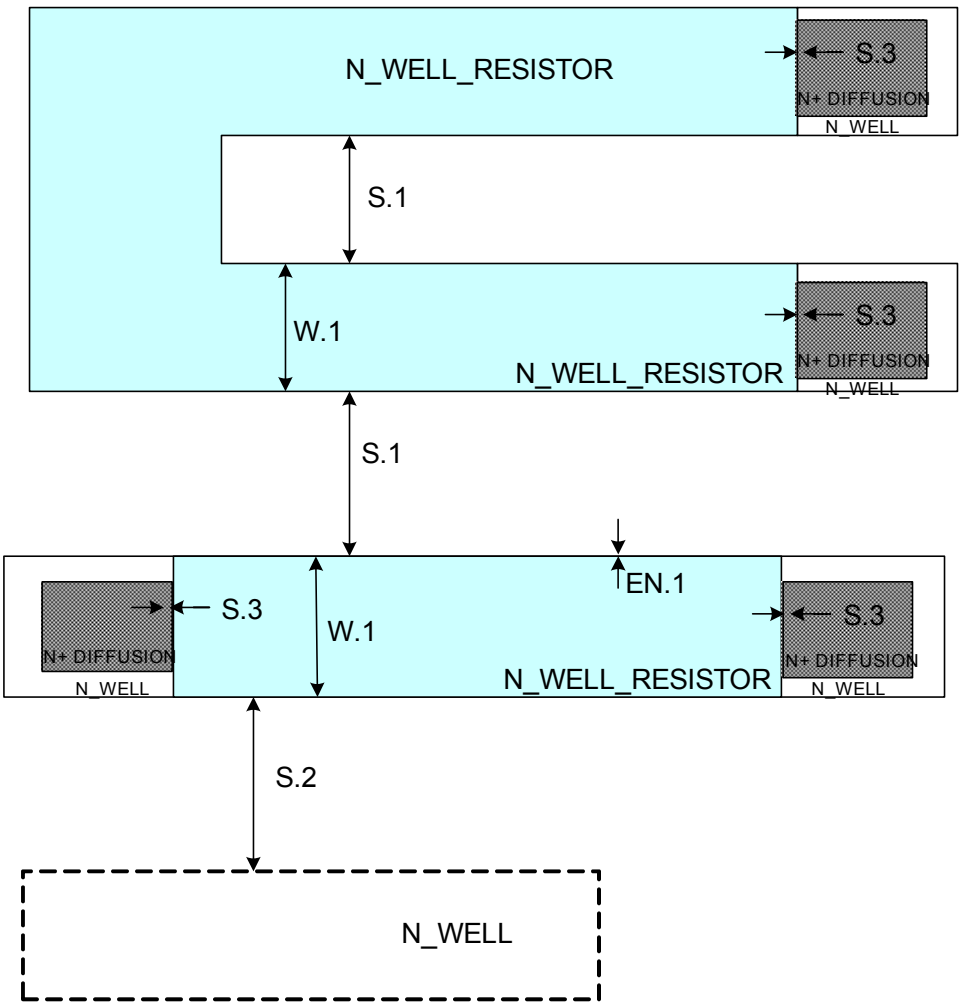


4A.2.1 N_WELL_RESISTOR(NWR) Layer Layout Rules (Non-tooling)

N_WELL_RESISTOR Layer defines N_WELL Resistor. It shall not have any DIFFUSION dummy pattern drawn within.

(unit : um)

Rule No.	Description	Label		Rule
NWR.W1	N_WELL_RESISTOR width	W.1	≧	1.50
NWR.WX	N_WELL_RESISTOR maximum width		≦	20.00
NWR.S1	Spacing and notch of N_WELL_RESISTOR	S.1	≧	0.9
NWR-NW.S2	Spacing of N_WELL_RESISTOR to N_WELL	S.2	≧	0.9
NWR-N_DF.NW.S3	Exact spacing of N_WELL_RESISTOR to N+ DIFFUSION within the same N_WELL (for N_WELL tap)	S.3	=	0
NW-NWR.EN1	Exact N_WELL enclosure of length of N_WELL RESISTOR	EN.1	=	0



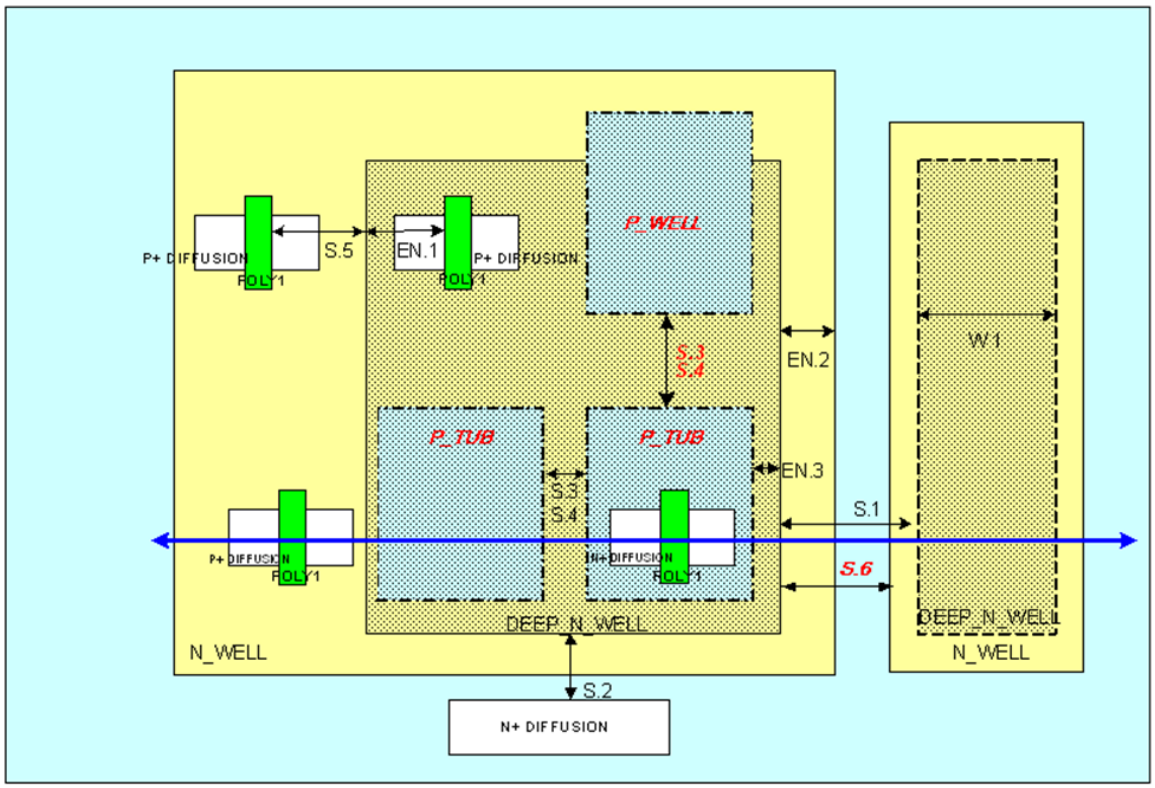
4A.3 DEEP_N_WELL (DNW) Layer Layout Rules

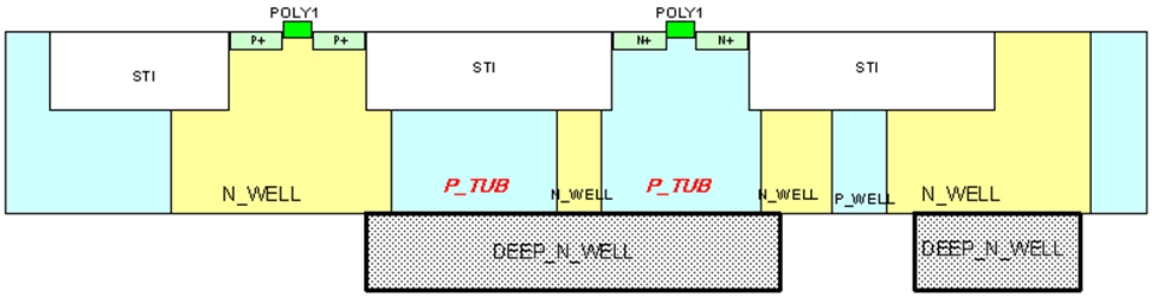
(unit : um)

Rule No.	Description	Label		Rule
DNW.W1	DEEP_N_WELL width	W.1	≧	3.00
DNW.S1	Spacing and notch of DEEP_N_WELL to DEEP_N_WELL	S.1	≧	3.50
DNW-N_DF.S2	Spacing of DEEP_N_WELL to N+ DIFFUSION outside N_WELL	S.2	≧	1.40
PW.S3	Spacing of P_TUB to (P_TUB or P_WELL of non-equal-potential) within DEEP_N_WELL	S.3	≧	1.00
PW.S4.TG	Spacing of P_TUB to (P_TUB or P_WELL of non-equal-potential) within (DEEP_N_WELL touching TG)	S.4	≧	1.20
DNW-PG.S5	Spacing of DEEP_N_WELL to PMOS gate	S.5	≧	1.00
DNW-NW.S6	Spacing of DEEP_N_WELL to N_WELL of non-equal potential	S.6	≧	1.90
DNW-PG.EN1	DEEP_N_WELL enclosure of PMOS gate	EN.1	≧	1.00
NW-DNW.EN2	N_WELL enclosure of DEEP_N_WELL (P_WELL cross DEEP_N_WELL edge is allowed)	EN.2	≧	1.00
DNW-PW.EN3	DEEP_N_WELL enclosure of P_TUB	EN.3	≧	0.40
DNW.R	N_WELL within DEEP_N_WELL must be at the same potential			Yes
DNW.R2	MOAT is not allowed within DEEP_N_WELL			Yes
DNW.R3	DEEP_N_WELL patterns must be orthogonal			Yes
DNW.R4	N_WELL_RESISTOR within DEEP_N_WELL is not allowed			Yes

Note:

1. P_TUB = (REVERSE (N_WELL)) fully within DEEP_N_WELL
2. P_WELL = (REVERSE (N_WELL)) not fully within DEEP_N_WELL
3. P_TUB can be used in designs for better noise isolation or various back-bias conditions for performance and power optimization.


P+ DIFFUSION
POLY1
S.5
EN.1
P+ DIFFUSION
POLY1
P_WELL
S.3
S.4
EN.2
W.1
P_TUB
P_TUB
EN.3
S.3
S.4
S.1
P+ DIFFUSION
POLY1
N+ DIFFUSION
POLY1
S.6
DEEP_N_WELL
DEEP_N_WELL
N_WELL
N_WELL
S.2
N+ DIFFUSION


POLY1
POLY1
P+
P+
N+
N+
STI
STI
STI
N_WELL
P_TUB
N_WELL
P_TUB
N_WELL
P_WELL
N_WELL
DEEP_N_WELL
DEEP_N_WELL

4A.4 LL_HVT (LLH) Layer Layout Rules (Non-tooling)

LL_HVT layer defines LL_HVT device for Boolean operation only.

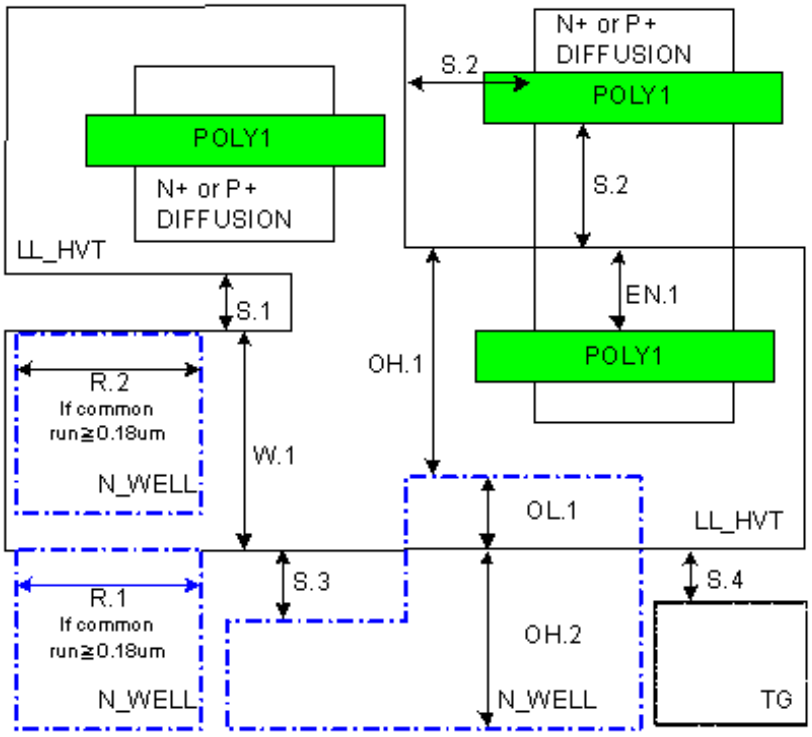
(unit : um)

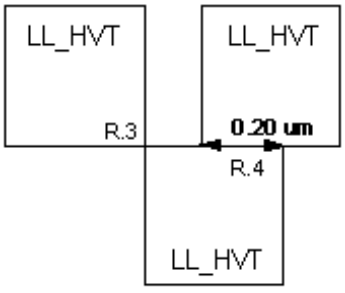
Rule No.	Description	Label		Rule
LLH.W1	LL_HVT width	W.1	≧	0.36
LLH.S1	Spacing and notch of LL_HVT	S.1	≧	0.20
LLH-PLY_G.S2	Spacing of LL_HVT to Gate	S.2	≧	0.15
LLH-PLY_G.EN1	LL_HVT enclosure of Gate	EN.1	≧	0.15
LLH.R	LL_HVT shapes must be orthogonal			Yes

The following layout rules are to prevent narrow lines or spaces existing on mask layers generated by Boolean operations with database of this layer, which will have resolution problems in mask making or in wafer processing.

(unit : um)

Rule No.	Description	Label		Rule
LLH-NW.S3	Spacing of LL_HVT to N_WELL	S.3	≧	0.18
LLH-TG.S4	Spacing of LL_HVT to TG	S.4	≧	0.18
LLH-NW.OH1	LL_HVT overhang of N_WELL	OH.1	≧	0.18
NW-LLH.OH2	N_WELL overhang of LL_HVT	OH.2	≧	0.18
NW-LLH.OL1	N_WELL overlap of LL_HVT	OL.1	≧	0.18
LLH-NW.R1	If LL_HVT and N_WELL have a common run ≧ 0.18um, then a spacing of zero is allowed along the common run	R.1		Yes
LLH-NW.R2	If LL_HVT and N_WELL have a common run ≧0.18um, then a overhang of zero is allowed along the common run	R.2		Yes
LLH.R3	Point touch of LL_HVT regions is allowed.	R.3		Yes
LLH.R4	Butting cell with common run length 0.20um is allowed	R.4		Yes





4A.5 LL_LVT (LLL) Layer Layout Rules (Non-tooling)

LL_LVT layer defines LL_LVT device for Boolean operation only.

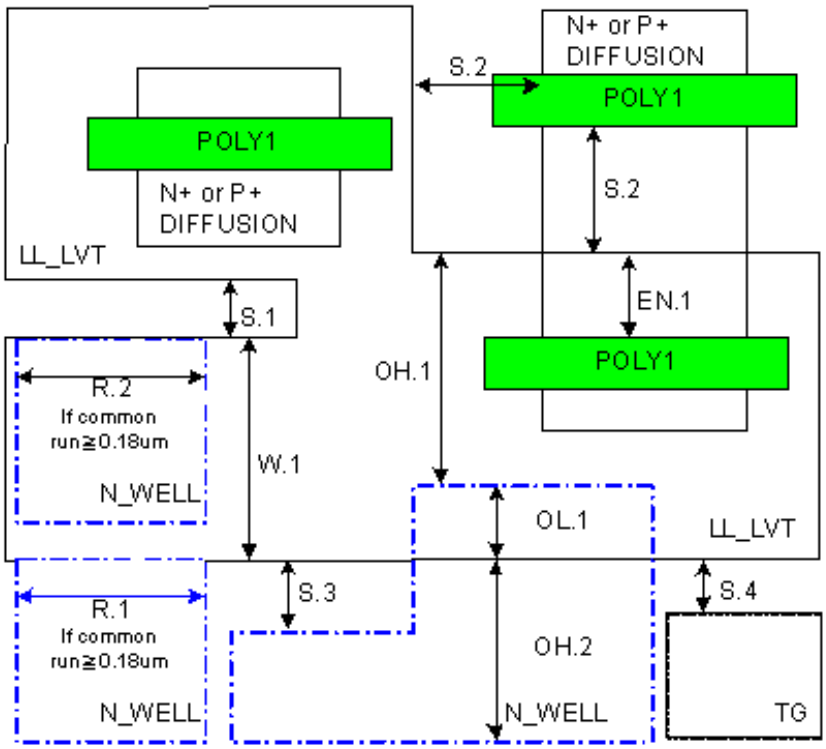
(unit : um)

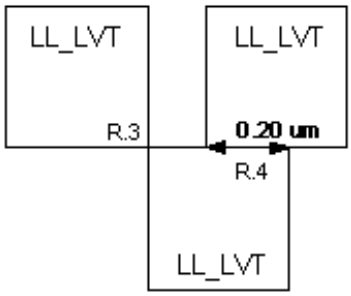
Rule No.	Description	Label		Rule
LLL.W1	LL_LVT width	W.1	≧	0.36
LLL.S1	Spacing and notch of LL_LVT	S.1	≧	0.20
LLL-PLY_G.S2	Spacing of LL_LVT to Gate	S.2	≧	0.15
LLL-PLY_G.EN1	LL_LVT enclosure of Gate	EN.1	≧	0.15
LLL.R	LL_LVT shapes must be orthogonal			Yes

The following layout rules are to prevent narrow lines or spaces existing on mask layers generated by Boolean operations with database of this layer, which will have resolution problems in mask making or in wafer processing.

(unit: um)

Rule No.	Description	Label		Rule
LLL-NW.S3	Spacing of LL_LVT to N_WELL	S.3	≧	0.18
LLL-TG.S4	Spacing of LL_LVT to TG	S.4	≧	0.18
LLL-NW.OH1	LL_LVT overhang of N_WELL	OH.1	≧	0.18
NW-LLL.OH2	N_WELL overhang of LL_LVT	OH.2	≧	0.18
NW-LLL.OL1	N_WELL overlap of LL_LVT	OL.1	≧	0.18
LLL-NW.R1	If LL_LVT and N_WELL have a common run ≧0.18um, then a spacing of zero is allowed along the common run	R1		Yes
LLL-NW.R2	If LL_LVT and N_WELL have a common run ≧0.18um, then a overhang of zero is allowed along the common run	R2		Yes
LLL.R3	Point touch of LL_LVT regions is allowed.	R.3		Yes
LLL.R4	Butting cell with common run length 0.20um is allowed	R.4		Yes



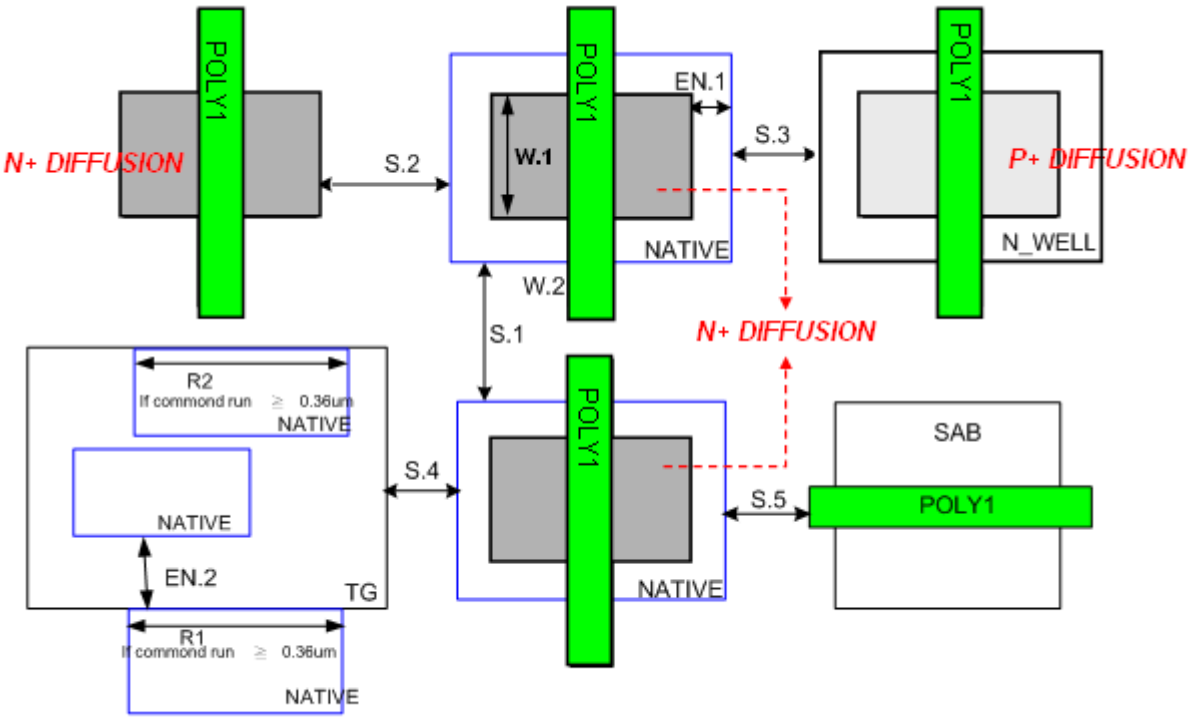


4A.6 NATIVE DEVICE (NT) Layer Layout Rules (Non-tooling)

This layer defines 1.2V, 1.8V, 2.5V, 2.5VOD3.3V and 3.3V NMOS-like NATIVE devices for Boolean operation only. All 65LL NATIVE devices can be either drawn over P-sub and receive no P_WELL implant, or drawn within DEEP_N_WELL and receive P_WELL implant. Instead, all NATIVE devices receive NMOS extension implant as well as standard N+ source/drain implant.

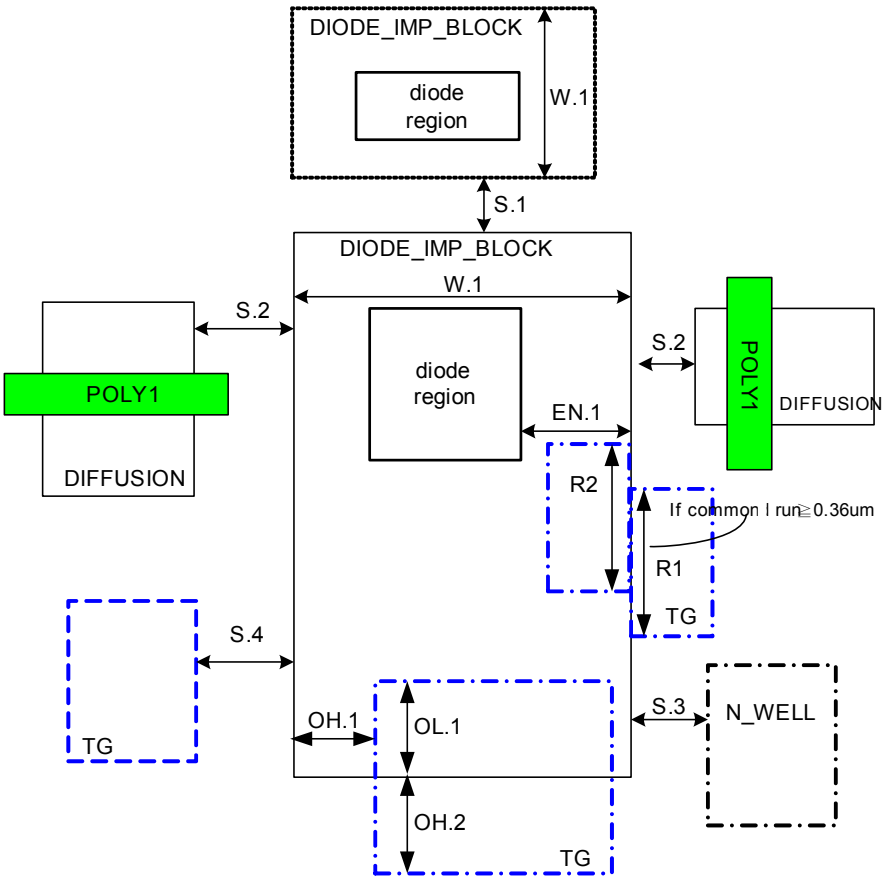
(unit : um)

Rule No.	Description	Label		Rule
NT.W1	NATIVE DIFFUSION width	W.1	≧	0.47
NT.S1	Spacing and notch of NATIVE	S.1	≧	0.47
NT-DF.S2	Spacing of NATIVE to DIFFUSION	S.2	≧	0.25
NT-DF.S2s	Spacing of NATIVE to DIFFUSION (L55SP Shrinkage capable)	S.2	≧	0.28
NT-NW.S3	Spacing of NATIVE to N_WELL	S.3	≧	0.90
NT-TG.S4	Spacing of NATIVE to TG	S.4	≧	0.36
TG-NT.EN2	TG enclosure of NATIVE	EN.2	≧	0.36
TG-NT.R1	If TG and NATIVE have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run	R.1		Yes
TG-NT.R2	If TG and NATIVE have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run	R.2		Yes
NT-NRS.S5	Spacing of NATIVE to N+/P+ POLY1 non-salicide resistor body	S.5	≧	0.48
NT-DF.EN1	NATIVE enclosure of DIFFUSION (two DIFFUSION inside one NATIVE is not allowed)	EN.1		0.25≦EN 1≦ 0.28
NT-DF.EN1s	Exact NATIVE enclosure of DIFFUSION (L55SP Shrinkage capable)		=	0.28
PLY_NT.W2	POLY1 width for NATIVE device over NATIVE but not over TG	W.2	≧	0.20
PLY_NT.W2s	POLY1 width for NATIVE device over NATIVE but not over TG (L55SP Shrinkage capable)		≧	0.22
PLY_NT.W3.TG18	POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device		≧	1.0
PLY_NT.W3s.TG18	POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device(L55SP Shrinkage capable)		≧	1.1
PLY_NT.W3.TG25	POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device		≧	1.2
PLY_NT.W3s.TG25	POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device(L55SP Shrinkage capable)		≧	1.33
PLY_NT.W4.TG25_OD 33	POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS Note: This rule excludes cases over DEEP_N_WELL		≧	1.4
PLY_NT.W4s.TG25_OD 33	POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS (L55SP Shrinkage capable) Note: This rule excludes cases over DEEP_N_WELL		≧	1.55
PLY_NT.W3.TG33	POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device		≧	1.2
PLY_NT.W3s.TG33	POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device(L55SP Shrinkage capable)		≧	1.33
NT.R	NATIVE shapes must be orthogonal			Yes
NT.R1	NATIVE over P+ DIFFUSION is not allowed			Yes


POLY1
N+ DIFFUSION
S.2
W.1
EN.1
S.3
P+ DIFFUSION
N_WELL
NATIVE
W.2
S.1
N+ DIFFUSION
R2
If commond run ≥ 0.36um
NATIVE
NATIVE
EN.2
TG
R1
If commond run ≥ 0.36um
NATIVE
S.4
S.5
SAB
POLY1

4A.7 DIODE_IMP_BLOCK (DIB) Layer Layout Rules (unit : um)

Rule No.	Description	Label		Rule
DIB.W1	DIODE_IMP_BLOCK width	W.1	≧	0.36
DIB.S1	Spacing and notch of DIODE_IMP_BLOCK	S.1	≧	0.36
DIB-DF.S2	Spacing of DIODE_IMP_BLOCK to DIFFUSION which is not in diode region	S.2	≧	0.18
DIB-NW.S3	Spacing of DIODE_IMP_BLOCK to N_WELL	S.3	≧	0.36
DIB-TG.S4	Spacing of DIODE_IMP_BLOCK to TG	S.4	≧	0.36
DIB-DIODE.EN1	DIODE_IMP_BLOCK enclosure of diode region	EN.1	≧	0.12
DIB-TG.OH1	DIODE_IMP_BLOCK overhang of TG	OH.1	≧	0.36
TG-DIB.OH2	TG overhang of DIODE_IMP_BLOCK	OH.2	≧	0.36
DIB-TG.OL1	DIODE_IMP_BLOCK overlap of TG	OL.1	≧	0.36
DIB-TG.R1	If DIODE_IMP_BLOCK and TG have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run	R1		Yes
DIB-TG.R2	If DIODE_IMP_BLOCK and TG have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run	R2		Yes
DIB.R	DIODE_IMP_BLOCK shapes must be orthogonal			Yes

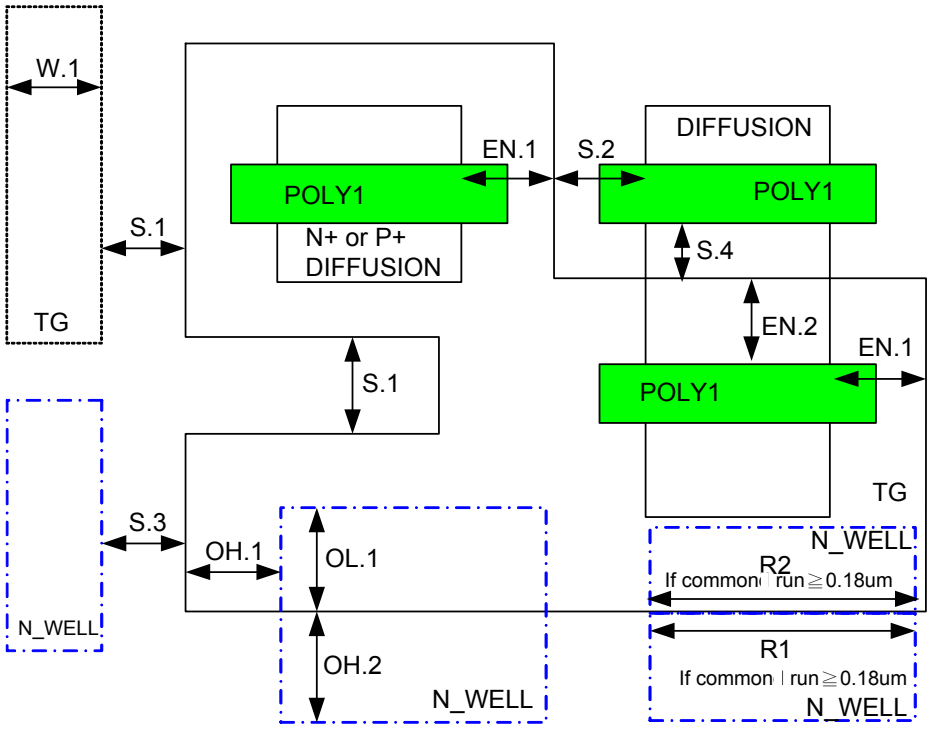


4A.8 TG Layer Layout Rules

This layer defines thick gate oxide devices.

(unit : um)

Rule No.	Description	Label		Rule
TG.W1	TG width	W.1	≧	0.44
TG.S1	Spacing and notch of TG	S.1	≧	0.44
TG-PLY_G.S2	Spacing of TG to unrelated Gate in the direction parallel to Gate width.	S.2	≧	0.30
TG-PLY_G.S4	Spacing of TG to unrelated Gate in the direction parallel to Gate length.	S.4	≧	0.34
TG-NW.S3	Spacing of TG to N_WELL	S.3	≧	0.36
TG-NW.OH1	TG overhang of N_WELL	OH.1	≧	0.36
NW-TG.OH2	N_WELL overhang of TG	OH.2	≧	0.36
TG-NW.OL1	TG overlap of N_WELL	OL.1	≧	0.36
TG-NW.R1	If TG and N_WELL have a common run ≧0.18um, then a spacing of zero is allowed along the common run	R.1		Yes
TG-NW.R2	If TG and N_WELL have a common run ≧0.18um, then a overhang of zero is allowed along the common run	R.2		Yes
TG-LLH.R3	If TG and LL_HVT have a common run ≧ 0.36, then a spacing of zero is allowed along the common run			Yes
TG-LLL.R4	If TG and LL_LVT have a common run≧ 0.36, then a spacing of zero is allowed along the common run			Yes
TG-PLY_G.EN1	TG enclosure of Gate in the direction parallel to Gate width.	EN.1	≧	0.27
TG-PLY_G.EN2	TG enclosure of Gate in the direction parallel to Gate length.	EN.2	≧	0.34
TG.R	TG shapes must be orthogonal			Yes

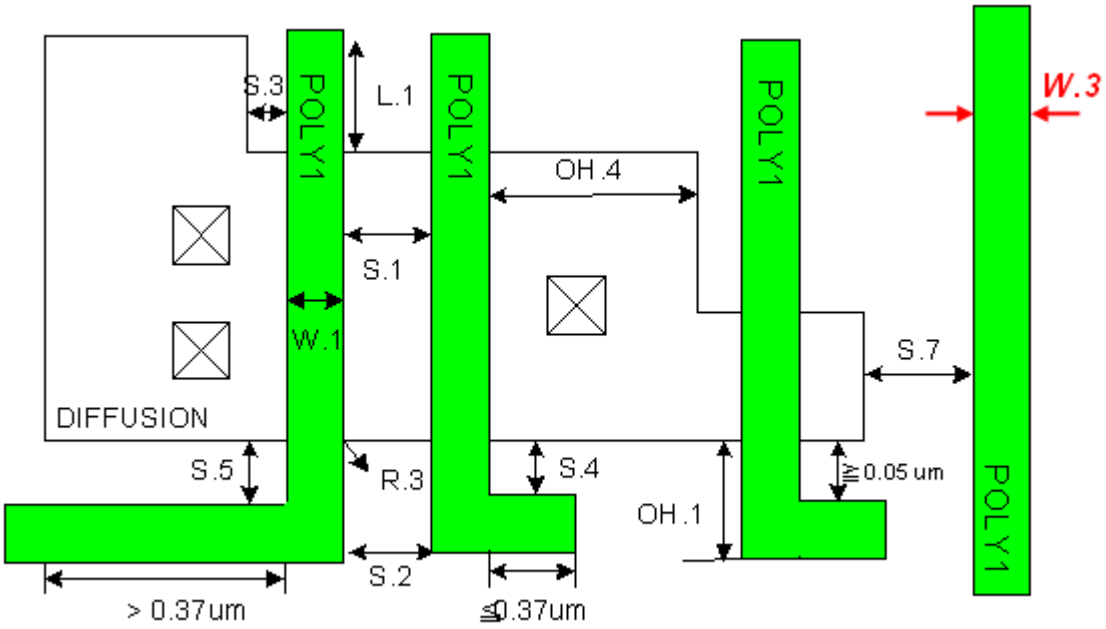


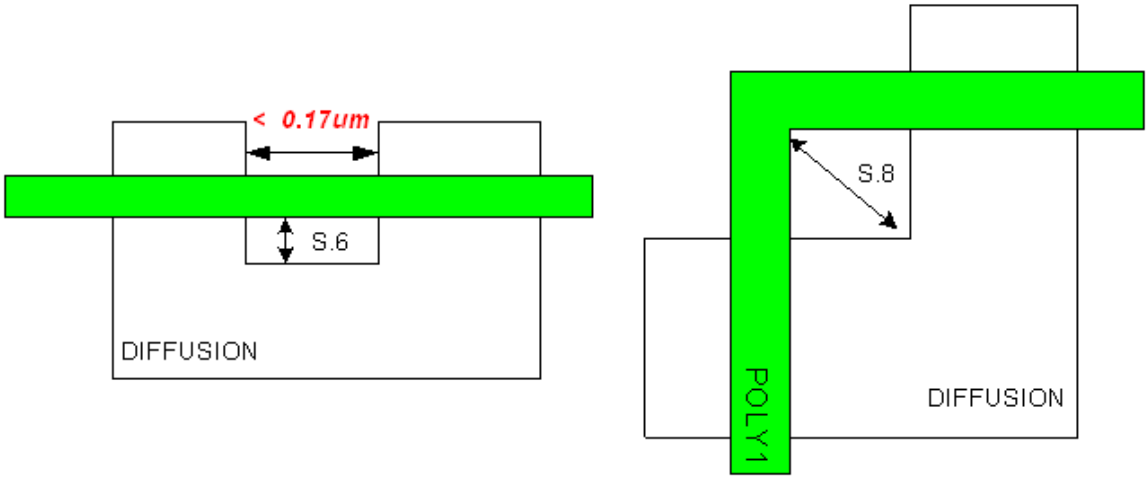
4A.9 POLY1 (PLY) Layer Layout Rules

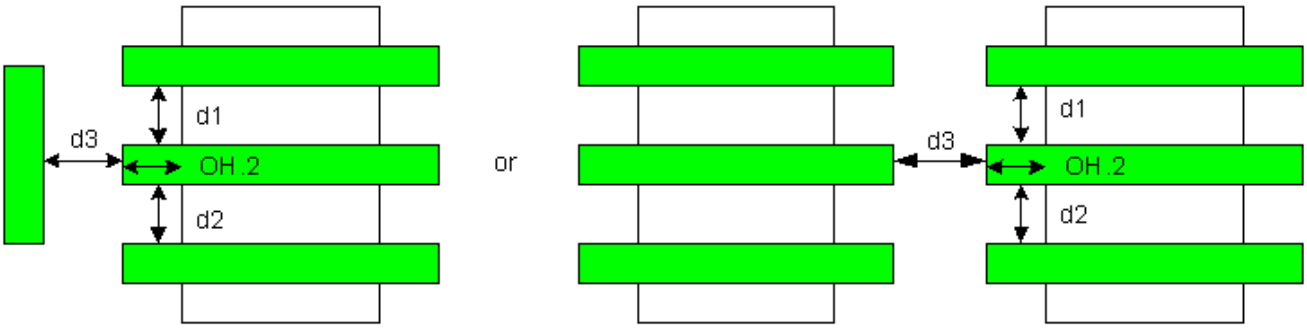
(unit : um)

Rule No.	Description	Label		Rule
PLY_NG.W1	POLY1 Width for NMOS	W.1	≧	0.06
PLY_PG.W2	POLY1 Width for PMOS		≧	0.06
PLY_ICN.W3	POLY1 Width	W.3	≧	0.06
PLY.W.TG18	POLY1 width over TG of 1.8V device (for 1.8V+/-10% voltage tolerance)		≧	0.18
PLY.W.TG18s	POLY1 width over TG of 1.8V device (for 1.8V+/-10% voltage tolerance) (L55SP shrinkage capable)		≧	0.20
PLY.W.TG25	POLY1 width over TG of 2.5V device (for 2.5V+/-10% voltage tolerance)		≧	0.24
PLY.W.TG25s	POLY1 width over TG of 2.5V device (for 2.5V+/-10% voltage tolerance) (L55SP shrinkage capable)		≧	0.26
PLY.W.TG25_UD18	POLY1 width over TG and CAD_UD_MARK of 2.5V underdrive 1.8V device (for 1.8V+/-10% voltage tolerance)		≧	0.22
PLY_NG.W.TG25_OD33	POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS		≧	0.5
PLY_NG.W.TG25_OD33s	POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS(L55SP shrinkage capable)		≧	0.5
PLY_PG.W.TG25_OD33	POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS		≧	0.4
PLY_PG.W.TG25_OD33s	POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS(L55SP shrinkage capable)		≧	0.42
PLY.W.TG33	POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance)		≧	0.37
PLY.W.TG33s	POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance) (L55SP shrinkage capable)		≧	0.41

Rule No.	Description	Labe		Rule
PLY_G.S1	Spacing of parallel POLY1 gates	S.1	≧	0.13
PLY_G.S1s	Spacing of parallel POLY1 gates(L55SP shrinkage capable)	S.1	≧	0.15
PLY_G.S.TG	Spacing of parallel POLY1 gates over TG		≧	0.18
PLY_G.S	Spacing of parallel POLY1 gates if at least one POLY1 width ≧ 0.30um		≧	0.15
PLY_F.S2	Spacing and notch of POLY1 on field	S.2	≧	0.12
PLY_F.S.TG	Spacing and notch of POLY1 on field over TG		≧	0.18
PLY-DF.S3	Spacing of POLY1 end cap to related DIFFUSION	S.3	≧	0.05
PLY-DF.S4	Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION ≤0.37um	S.4	≧	0.05
PLY-DF.S5	Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION >0.37um	S.5	≧	0.07
PLY_F-DF.S6	Spacing of POLY1 on field to DIFFUSION when POLY1 across [DIFFUSION notch with spacing < 0.17um]	S.6	≧	0.12
PLY_F-DF.S7	Spacing of POLY1 on field to DIFFUSION	S.7	≧	0.05
PLY-DF.S8	Spacing of 90° POLY1 corner to 90° DIFFUSION corner	S.8	≧	0.14
PLY-DF.L1	POLY1 endcap length	L.1	≧	0.12
PLY-DF.OH1	POLY1 overhang of DIFFUSION	OH.1	≧	0.11
PLY-DF.OH2	POLY1 overhang of DIFFUSION if spacing of POLY1 to three adjacent POLY1 < 0.13um (i.e. d1, d2 and d3 < 0.13um)	OH.2	≧	0.14
DF-PLY_G.OH4	DIFFUSION overhang of POLY1 Gate	OH.4	≧	0.115
DF-PLY_G.OH.TG	DIFFUSION overhang of POLY1 Gate over TG		≧	0.115
PLY_G.AX	POLY1 overlap DIFFUSION Maximum area		≦	6400
PLY.A	POLY1 area		≧	0.0375
PLY.EA	POLY1 enclosed area		≧	0.077
PLY.D	POLY1 density over 1mm x 1mm area (stepped in 500um increments across the chip) (exclude CAD_TESTKEY_MARK)		≧	15%
PLY.DX	POLY1 density over 1mm x 1mm area (stepped in 500um increments across the chip)		≦	75%
PLY_G.R1	POLY1 bent gate is not allowed			Yes
PLY_G.R2	POLY1 over field region may only turn at 90°			Yes
PLY.R3	POLY1 may only intersect DIFFUSION at 90°	R.3		Yes


S.3
POLY1
L.1
POLY1
OH .4
POLY1
W.3
S.1
W.1
S.7
DIFFUSION
S.5
R.3
S.4
OH .1
≤0.05 um
POLY1
S.2
> 0.37um
≤0.37um


< 0.17um
S.6
DIFFUSION
S.8
POLY1
DIFFUSION


d3
d1
OH .2
d2
or
d3
d1
OH .2
d2

The following two layers are customer poly1 dummy, POLY1_CUSTOMER_DUMMY (GDS no: 71(8))

(unit : um)

Rule No.	Description	Label		Rule
PLYDM.W4	POLY1_CUSTOMER_DUMMY width		≧	1.1
PLYDM.S9	Spacing and notch of POLY1_CUSTOMER_DUMMY		≧	0.9
PLYDM-NW.S10	Spacing of POLY1_CUSTOMER_DUMMY to N_WELL		≧	0.6
PLYDM-NW.EN1	N_WELL enclosure of POLY1_CUSTOMER_DUMMY		≧	0.6
PLYDM-AW.S11	Spacing of POLY1_CUSTOMER_DUMMY to AW		≧	0.6
PLYDM-AW.EN2	AW enclosure of POLY1_CUSTOMER_DUMMY		≧	0.6
PLYDM-DF.S13	Spacing of POLY1_CUSTOMER_DUMMY to DIFFUSION		≧	1.2
PLYDM-PLY.S14	Spacing of POLY1_CUSTOMER_DUMMY to POLY1		≧	1.2
PLYDM-NWR.S15	Spacing of POLY1_CUSTOMER_DUMMY to N_WELL_RESISTOR		≧	1.2
PLYDM- PLYDM.S16	Spacing of POLY1_CUSTOMER_DUMMY to POLY1_DUMMY_BLOCK		≧	1.2
PLYDM-FM.S17	Spacing of POLY1_CUSTOMER_DUMMY to FUSE_MARK		≧	1.2

4A.10 N+ IMPLANT (NSD) Layer Layout Rules

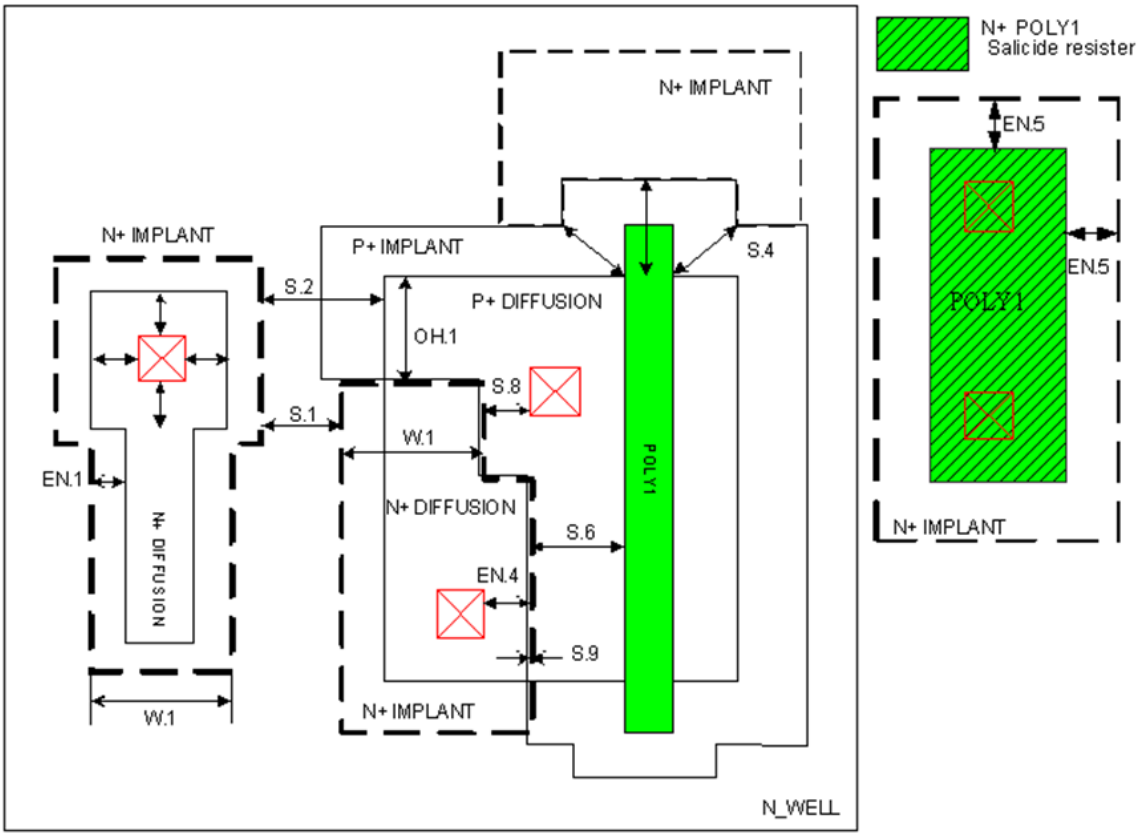
(unit : um)

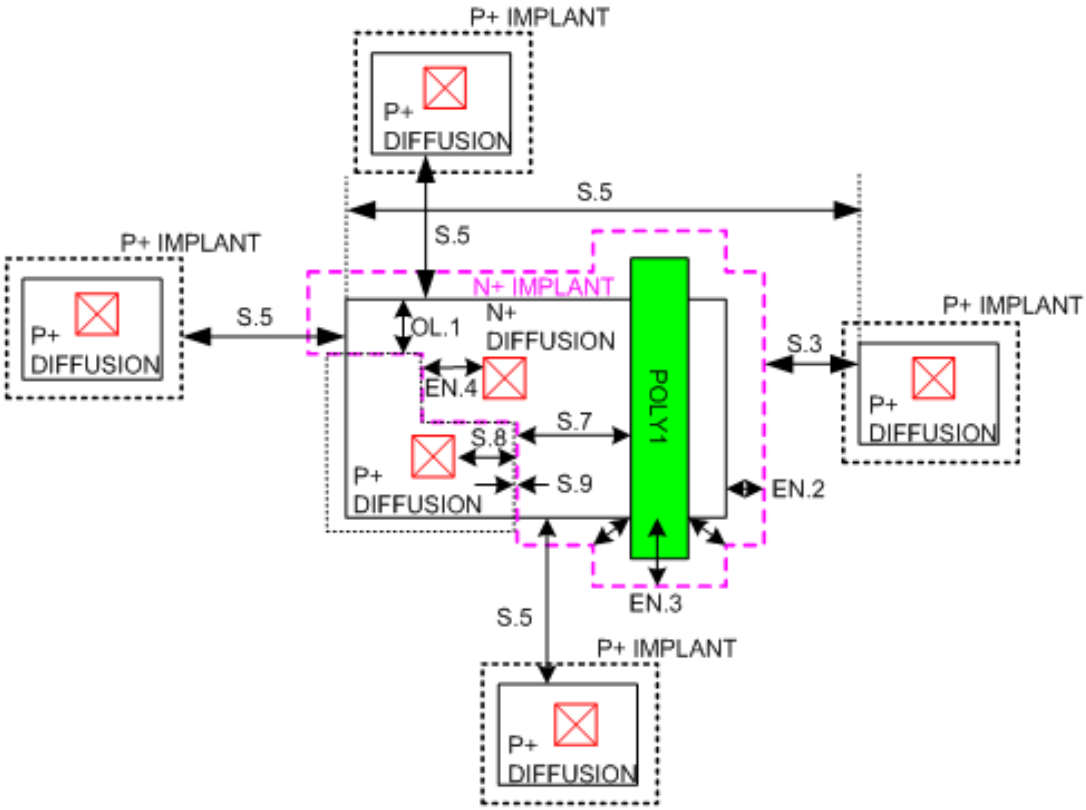
Rule No.	Description	Label		Rule
NSD.W1	N+ IMPLANT width	W.1	≧	0.18
NSD.S1	Spacing and notch of N+ IMPLANT	S.1	≧	0.18
NSD-P_DF.S2.NW	Spacing of N+ IMPLANT to [P+ DIFFUSION over N_WELL]	S.2	≧	0.09
NSD-P_DF.S3.PW	Spacing of N+ IMPLANT to [P+ DIFFUSION over P_WELL]	S.3	≧	0.02
NSD-PLY_PG.S4	Spacing of N+ IMPLANT to PMOS gate	S.4	≧	0.15
NSD-N_DF.EN1.NW	N+ IMPLANT enclosure of [N+ DIFFUSION over N_WELL]	EN.1	≧	0.02
NSD-N_DF.EN2.PW	N+ IMPLANT enclosure of [N+ DIFFUSION over P _WELL]	EN.2	≧	0.09
NSD-PLY_NG.EN3	N+ IMPLANT enclosure of NMOS gate	EN.3	≧	0.15
NSD-NPRS.EN5	N+ IMPLANT enclosure of N+ POLY1 salicide resistor	EN.5	≧	0.15
NSD.A	N+ IMPLANT area		≧	0.122
NSD.EA	N+ IMPLANT enclosed area		≧	0.122

4A.10.1 N+/P+ Butting Rules

(unit : um)

Rule No.	Description	Label		Rule
N_DF-P_PU.S5.PW	Spacing of N+ DIFFUSION to the nearest [P+ DIFFUSION pick-up within P_WELL] - I/O, RAM, ROM, capacitor and diode are excepted	S.5	≦	30
NPBJ-PLY_PG.S6	Spacing of N+/P+ butted junction edge to PMOS gate	S.6	≧	0.22
NPBJ-PLY_PG.S.TG	Spacing of N+/P+ butted junction edge to [PMOS gate over TG]		≧	0.30
NPBJ-PLY_NG.S7	Spacing of N+/P+ butted junction edge to NMOS gate	S.7	≧	0.22
NPBJ-PLY_NG.S.TG	Spacing of N+/P+ butted junction edge to [NMOS gate over TG]		≧	0.30
NSD-CT_P_DF.S8	Spacing of N+ IMPLANT to CONTACT over P+ DIFFUSION	S.8	≧	0.06
N_DF-P_DF.S9	Spacing of N+ DIFFUSION to P+ DIFFUSION in the same potential, while N+ IMPLANT overlap of P+ DIFFUSION is not allowed	S.9	≧	0
NSD-CT_N_DF.EN4	N+ IMPLANT enclosure of CONTACT over N+ DIFFUSION	EN.4	≧	0.06
P_DF-NSD.OH1	P+ DIFFUSION overhang of N+ IMPLANT	OH.1	≧	0.13
NSD-DF.OL1	N+ IMPLANT overlap of DIFFUSION to form N+ region	OL.1	≧	0.13
NSD.R	Soft CONTACTs are prohibited			Yes


N+ POLY1
Salicide resister
N+ IMPLANT
EN.5
EN.5
POLY1
N+ IMPLANT
N+ IMPLANT
P+ IMPLANT
S.4
S.2
P+ DIFFUSION
OH.1
S.8
S.1
W.1
EN.1
N+ DIFFUSION
POLY1
S.6
EN.4
S.9
N+ IMPLANT
W.1
N_WELL


P+ IMPLANT
P+ DIFFUSION
S.5
S.5
P+ IMPLANT
P+ DIFFUSION
S.5
N+ IMPLANT
OL.1
N+ DIFFUSION
EN.4
S.8
P+ DIFFUSION
S.7
S.9
POLY1
S.3
P+ IMPLANT
P+ DIFFUSION
EN.2
EN.3
S.5
P+ IMPLANT
P+ DIFFUSION

4A.11 P+ IMPLANT (PSD) Layer Layout Rules

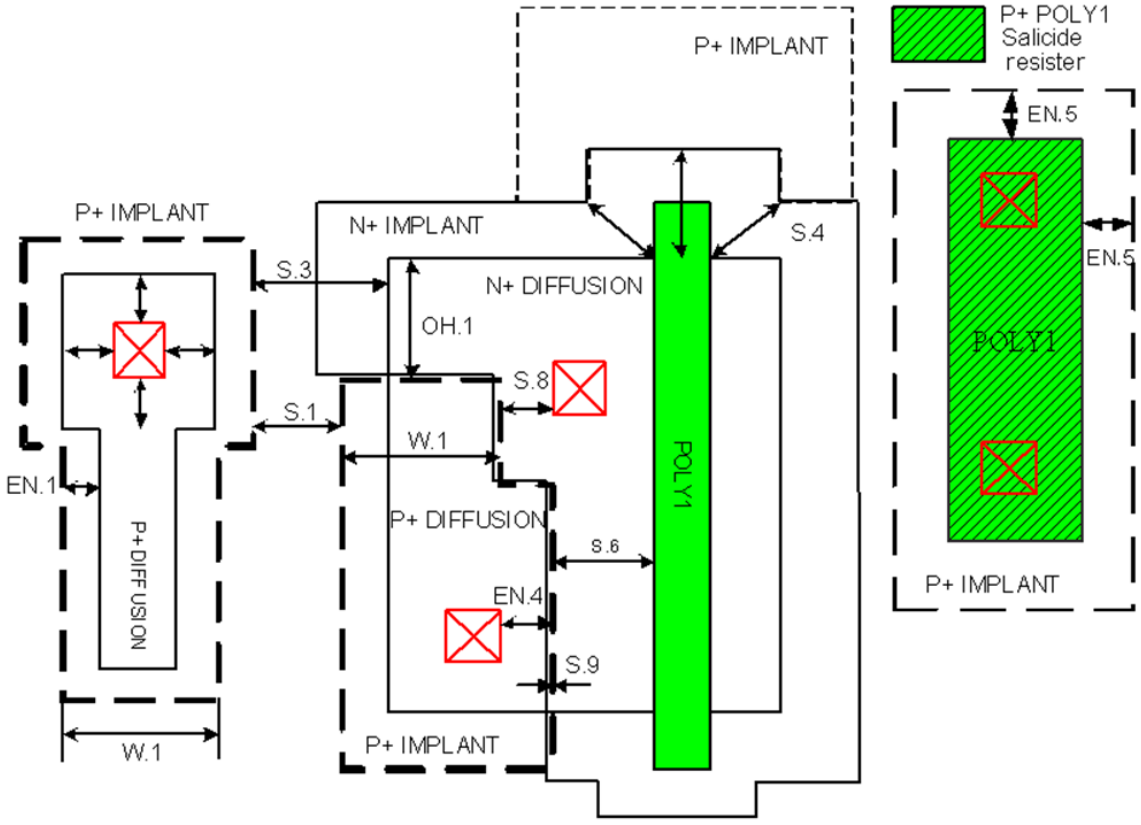
(unit : um)

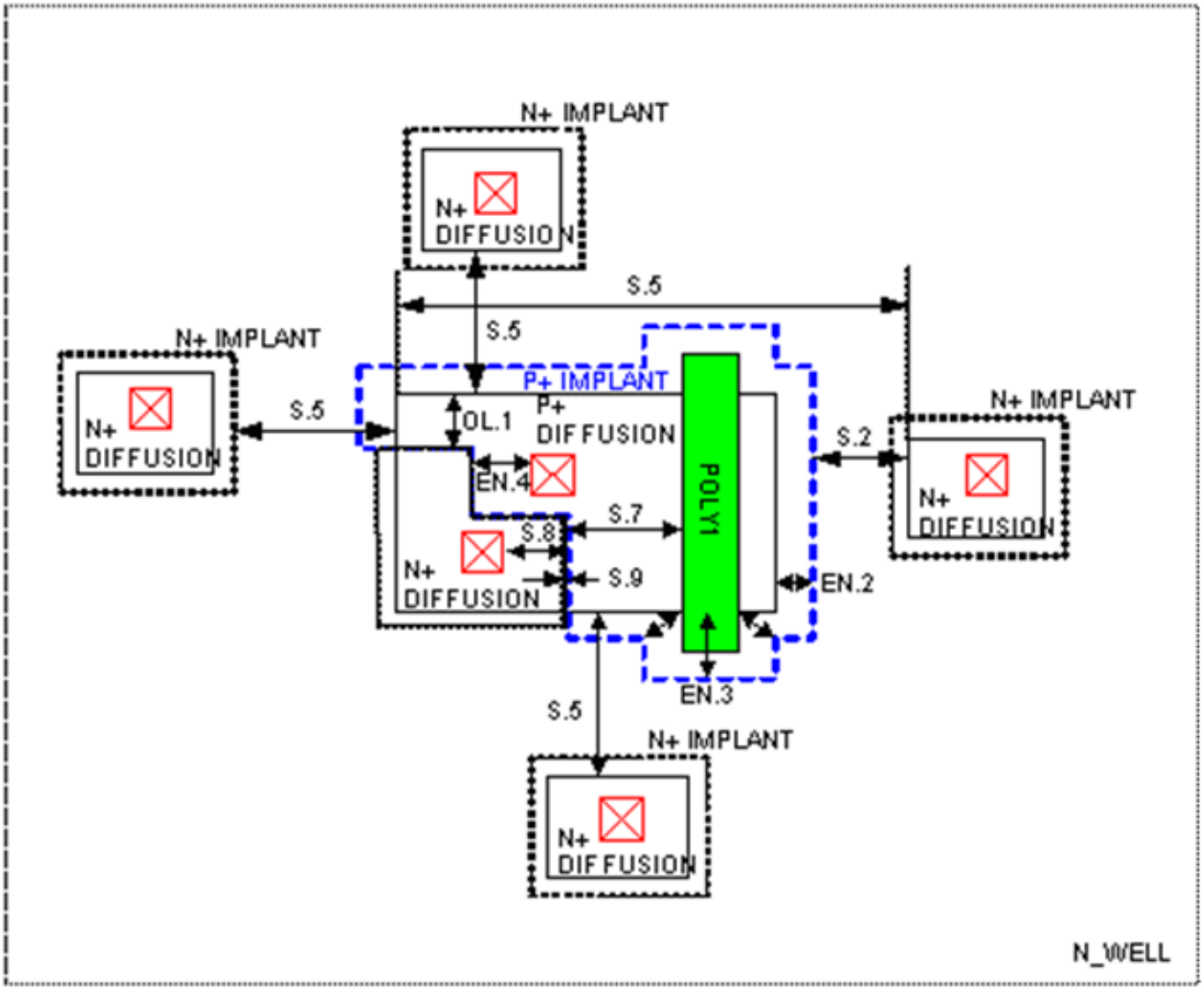
Rule No.	Description	Label		Rule
PSD.W1	P+ IMPLANT width	W.1	≧	0.18
PSD.S1	Spacing and notch of P+ IMPLANT	S.1	≧	0.18
PSD-N_DF.S2.NW	Spacing of P+ IMPLANT to [N+ DIFFUSION over N_WELL]	S.2	≧	0.02
PSD-N_DF.S3.PW	Spacing of P+ IMPLANT to [N+ DIFFUSION over P_WELL]	S.3	≧	0.09
PSD-PLY_NG.S4	Spacing of P+ IMPLANT to NMOS gate	S.4	≧	0.15
PSD-P_DF.EN1.PW	P+ IMPLANT enclosure of [P+ DIFFUSION over P_WELL]	EN.1	≧	0.02
PSD-P_DF.EN2.NW	P+ IMPLANT enclosure of [P+ DIFFUSION over N _WELL]	EN.2	≧	0.09
PSD-PLY_PG.EN3	P+ IMPLANT enclosure of PMOS gate	EN.3	≧	0.15
PSD-PPRS.EN5	P+ IMPLANT enclosure of P+ POLY1 salicide resistor	EN.5	≧	0.15
PSD.A	P+ IMPLANT area		≧	0.122
PSD.EA	P+ IMPLANT Enclosed area		≧	0.122

4A.11.1 N+/P+ Butting Rules

(unit : um)

Rule No.	Description	Label		Rule
P_DF-N_PU.S5.NW	Spacing of P+ DIFFUSION to the nearest [N+ DIFFUSION pick-up within N_WELL] - I/O, RAM, ROM, capacitor and diode are excepted	S.5	≦	30
NPBJ-PLY_NG.S6	Spacing of N+/P+ butted junction edge to NMOS gate	S.6	≧	0.22
NPBJ-PLY_NG.S.TG	Spacing of N+/P+ butted junction edge to [NMOS gate over TG]		≧	0.30
NPBJ-PLY_PG.S7	Spacing of N+/P+ butted junction edge PMOS gate	S.7	≧	0.22
NPBJ-PLY_PG.S.TG	Spacing of N+/P+ butted junction edge [PMOS gate over TG]		≧	0.30
PSD-CT_N_DF.S8	Spacing of P+ IMPLANT to [CONTACT over N+ DIFFUSION]	S.8	≧	0.06
P_DF-N_DF.S9	Spacing of P+ DIFFUSION to N+ DIFFUSION in the same potential, while P+ IMPLANT overlap of N+ DIFFUSION is not allowed	S.9	≧	0
PSD-CT_P_DF.EN4	P+ IMPLANT enclosure of CONTACT over P+ DIFFUSION	EN.4	≧	0.06
N_DF-PSD.OH1	N+ DIFFUSION overhang of P+ IMPLANT	OH.1	≧	0.13
PSD-DF.OL1	P+ IMPLANT overlap of DIFFUSION to form P+ region	OL.1	≧	0.13




N+ IMPLANT
N+ DIFFUSION
S.5
S.5
N+ IMPLANT
N+ DIFFUSION
S.5
P+ IMPLANT
P+ DIFFUSION
OL.1
EN.4
S.7
S.8
S.9
N+ DIFFUSION
POLY1
S.2
N+ IMPLANT
N+ DIFFUSION
EN.2
EN.3
S.5
N+ IMPLANT
N+ DIFFUSION
N_WELL

4A.12 Salicide-Block Layers Layout Rules

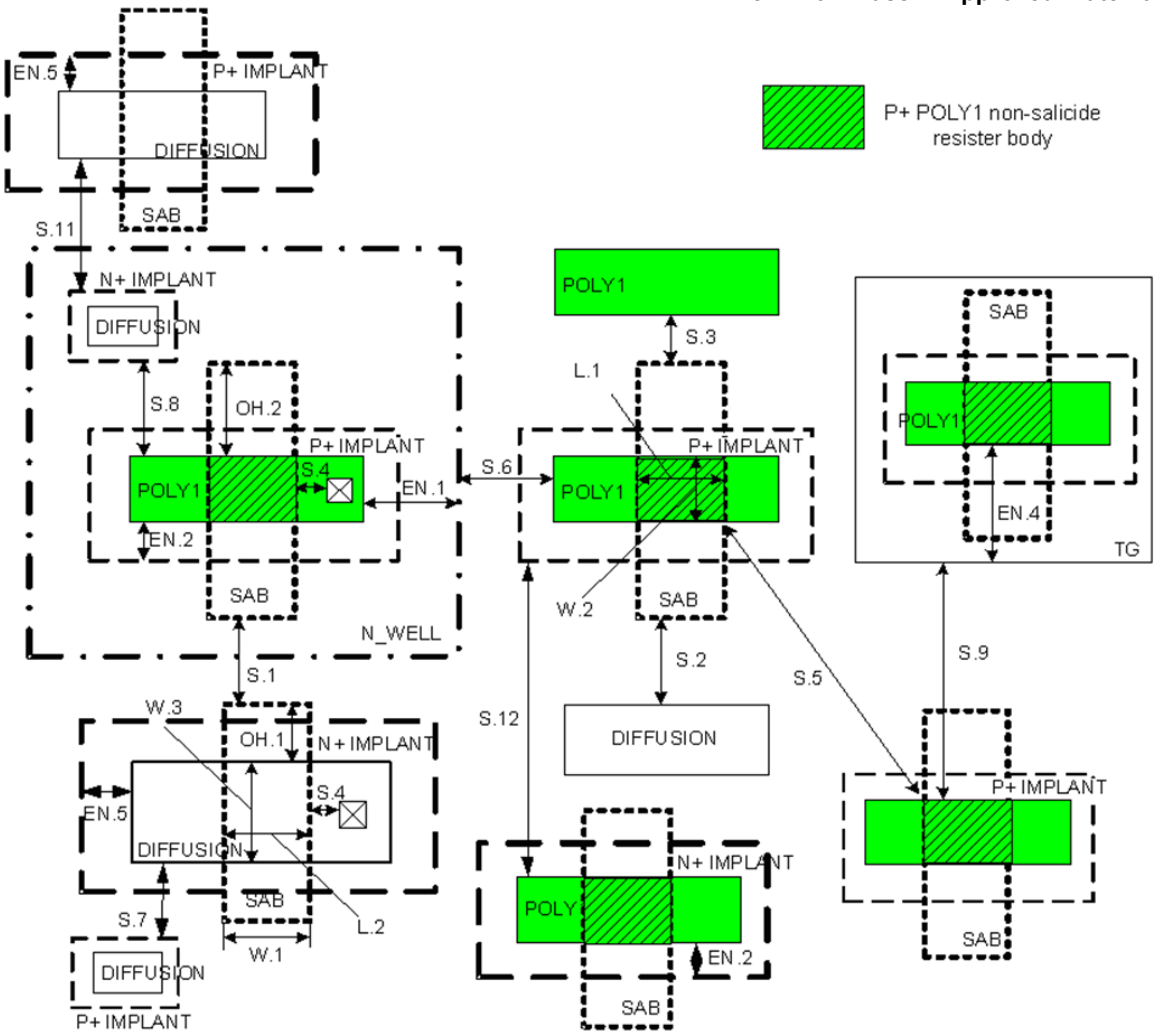
SAB layer defines non-salicided resistors, while SBLK layer is created to eliminate ESD degradation due to salicide formation. SBLK prohibits salicide formation at S/D diffusion area of ESD device. SAB layer is also used to block Vt/LDD implant but SBLK area still receives Vt/LDD implant for device performance.

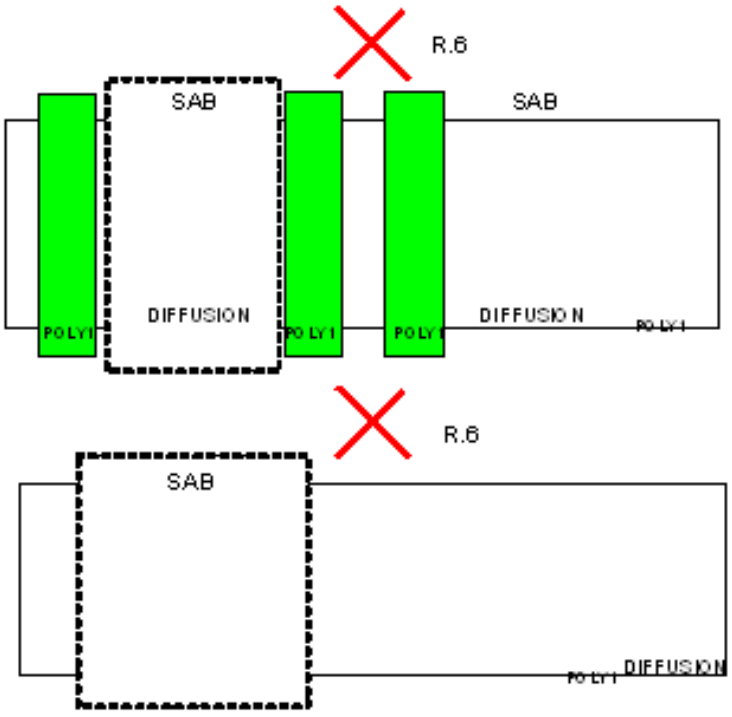
4A.12.1 SAB Layer (SAB) Layout Rules For Non-Salicide Resistor

The SAB mask is used to block the formation of silicide on either selected N+/P+ DIFFUSION or N+/P+ POLY1 resistor regions.

(unit : um)

Rule No.	Description	Label		Rule
SAB.W1	SAB width	W.1	≧	0.36
SAB.S1	Spacing and notch of SAB	S.1	≧	0.36
SAB-DF.S2	Spacing of SAB to DIFFUSION	S.2	≧	0.15
SAB-PLY.S3	Spacing of SAB to POLY1	S.3	≧	0.20
SAB-CT.S4	Spacing of SAB to CONTACT	S.4	≧	0.18
SAB-DNRS.OH1	SAB overhang of N+/P+ DIFFUSION non-salicide resistor	OH.1	≧	0.17
SAB-PNRS.OH2	SAB overhang of N+/P+ POLY1 non-salicide resistor	OH.2	≧	0.17
SAB.A	SAB area		≧	0.30
SAB.EA	SAB enclosed area		≧	0.30
SAB.R1	CONTACT over SAB is not allowed			Yes
PNRS.W2	Width of N+/P+ POLY1 non-salicide resistor	W.2	≧	0.36
PNRS.L1	Length of N+/P+ POLY1 non-salicide resistor	L.1	≧	0.70
PPNRS.S5	Spacing of P+ POLY1 non-salicide resistor body to P+ POLY1 non-salicide resistor body with no common run length	S.5	≧	0.60
NPNRS.S10	Spacing of N+ POLY1 non-salicide resistor body to N+ POLY1 non-salicide resistor body with no common run length		≧	0.60
PPNRS-NW.S6	Spacing of P+ POLY1 non-salicide resistor to N_WELL	S.6	≧	0.20
PSD-NDNRS.S7	Spacing of P+ IMPLANT to N+ DIFFUSION non-salicide resistor	S.7	≧	0.18
NSD-PDNRS.S11	Spacing of N+ IMPLANT to P+ DIFFUSION non-salicide resistor	S.11	≧	0.18
NSD-PPNRS.S8	Spacing of N+ IMPLANT to P+ POLY1 non-salicide resistor	S.8	≧	0.20
PSD-NPNRS.S12	Spacing of P+ IMPLANT to N+ POLY1 non-salicide resistor		≧	0.20
NW-PPNRS.EN1	N_WELL enclosure of P+ POLY1 non-salicide resistor	EN.1	≧	0.20
PSD-PPNRS.EN2	P+ IMPLANT enclosure of P+ POLY1 non-salicide resistor(HR and MR layer are excepted)	EN.2	≧	0.20
NSD-NPNRS.EN3	N+ IMPLANT enclosure of N+ POLY1 non-salicide resistor		≧	0.20
TG-PNRS.EN4	TG enclosure of N+/P+ POLY1 non-salicide resistor body	EN.4	≧	0.48
PSD-DNRS.EN5	P+ IMPLANT enclosure of P+ DIFFUSION non-salicide resistor	EN.5	≧	0.20
NSD-DNRS.EN6	N+ IMPLANT enclosure of N+ DIFFUSION non-salicide resistor		≧	0.20
PNRS-TG.S9	Spacing of N+/P+ POLY1 non-salicide resister body to TG	S.9	≧	0.48
DNRS.W3	Width of N+/P+ DIFFUSION non-salicide resistor	W.3	≧	0.36
DNRS.L2	Length of N+/P+ DIFFUSION non-salicide resistor	L.2	≧	0.70
SAB.R4	Non-salicide POLY1 on DIFFUSION (SAB over gate) is not allowed			Yes
SAB.R5	SAB overlap of SBLK is not allowed			Yes
SAB.R6	(DIFFUSION touching SAB) touching POLY1 is not allowed	R.6		Yes


EN.5
P+ IMPLANT
DIFFUSION
SAB
S.11
N+ IMPLANT
DIFFUSION
S.8
OH.2
P+ IMPLANT
POLY1
S.4
EN.1
EN.2
SAB
N_WELL
S.1
W.3
OH.1
N+ IMPLANT
S.4
EN.5
DIFFUSION
SAB
S.7
L.2
W.1
DIFFUSION
P+ IMPLANT
P+ POLY1 non-salicide resister body
POLY1
S.3
L.1
S.6
P+ IMPLANT
POLY1
W.2
SAB
S.2
DIFFUSION
S.12
N+ IMPLANT
POLY1
EN.2
SAB
SAB
POLY1
EN.4
TG
S.9
S.5
P+ IMPLANT
SAB

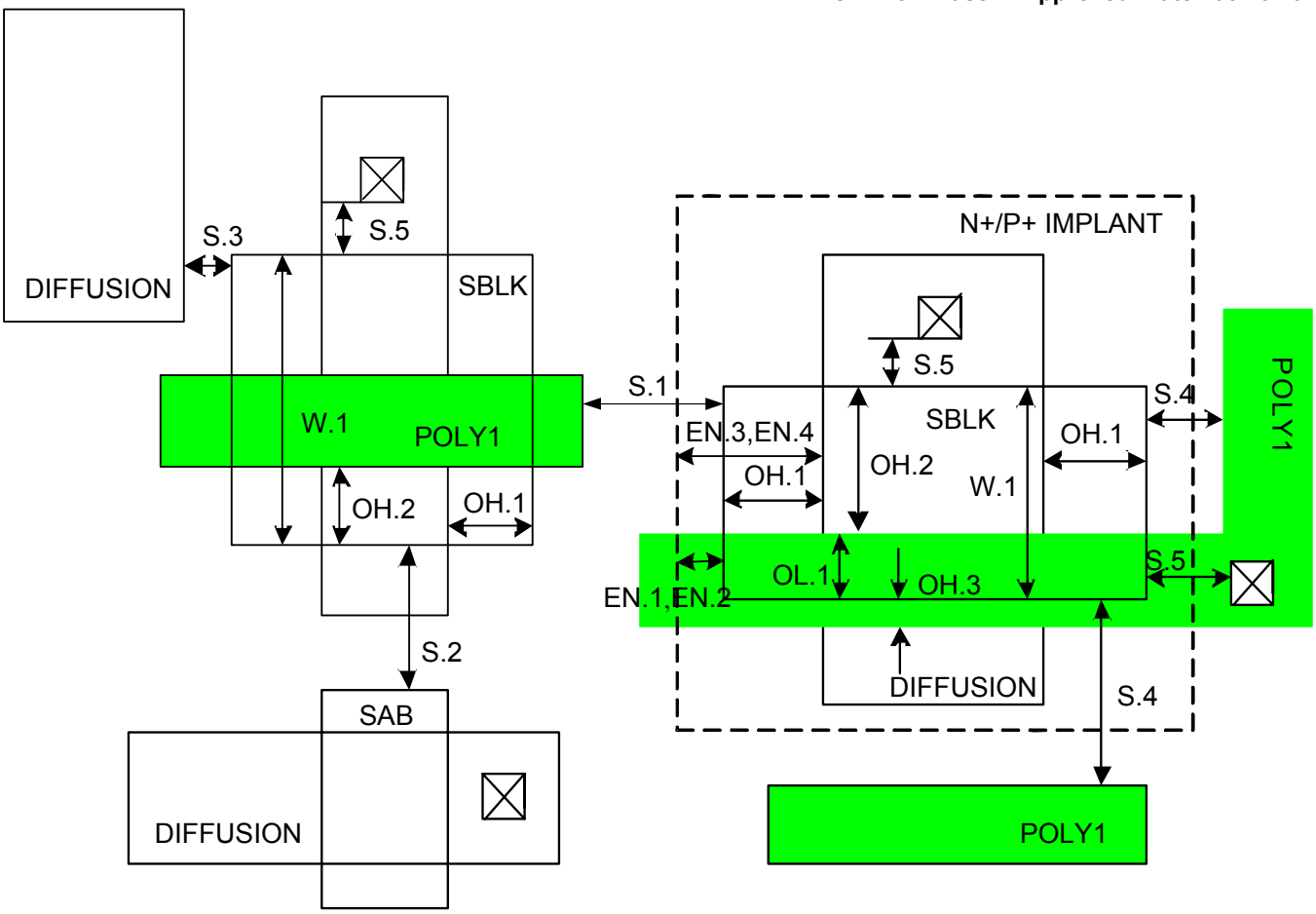

R.6
SAB
SAB
DIFFUSION
DIFFUSION
POLY1
POLY1
POLY1
POLY1
R.6
SAB
DIFFUSION
POLY1

4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling)

The rules defined in this section only describe the process requirements for SBLK layer. It is intended to give the designers rules how to use the SBLK layer to build silicide-blocked devices. It is NOT a description of ESD devices or ESD protection concepts. For detail ESD layout rules, please refer to 65nm ESD Design Rules (Spec. NO.: G-03E-GENERATION65N-TLR/ESD)

(unit: um)

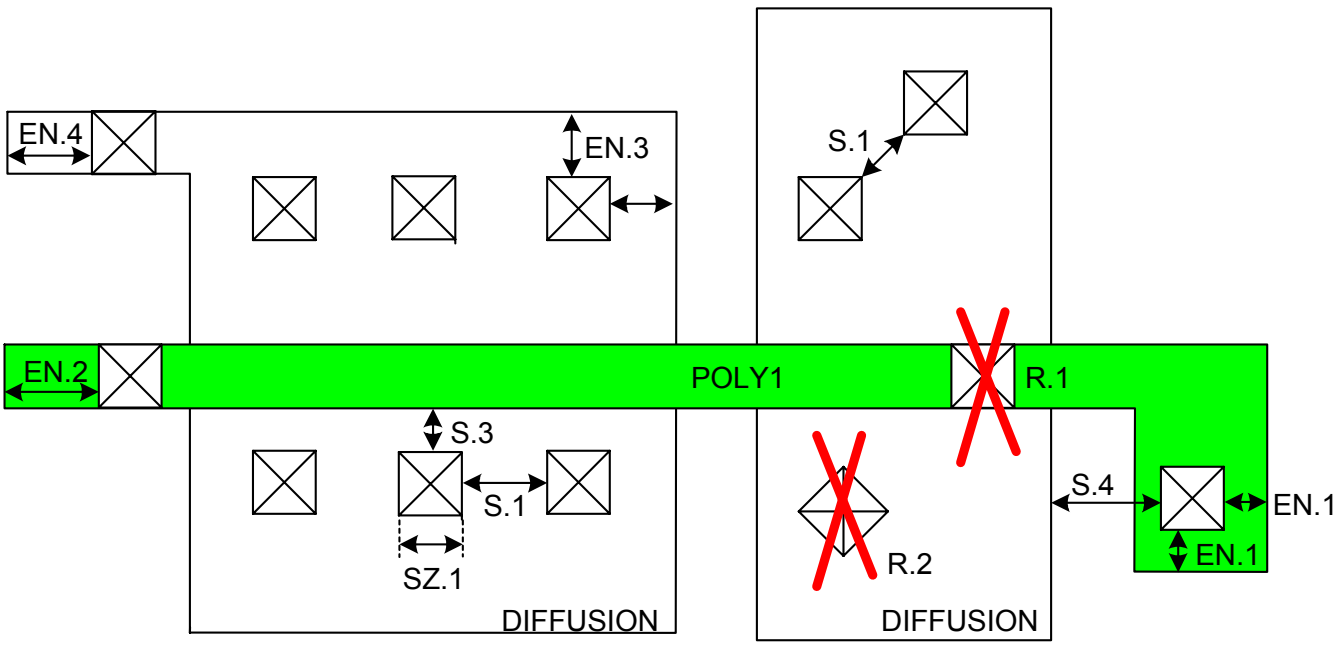
Rule No.	Description	Label		Rule
SBLK.W1	SBLK width	W.1	≧	0.36
SBLK.S1	Spacing and notch of SBLK	S.1	≧	0.36
SBLK-SA B.S2	Spacing of SBLK to SAB	S.2	≧	0.36
SBLK-DF.S3	Spacing of SBLK to DIFFUSION	S.3	≧	0.15
SBLK-PLY.S4	Spacing of SBLK to POLY1 (SBLK overlap POLY1 in the direction parallel to Gate width is not allowed)	S.4	≧	0.20
SBLK-CT.S5	Spacing of SBLK to CONTACT (SBLK overlap CONTACT is not allowed)	S.5	≧	0.18
SBLK-DF.OH1	SBLK overhang of DIFFUSION	OH.1	≧	0.17
SBLK-PLY_G.OH2	SBLK overhang of POLY1 gate	OH.2	≧	0.1
PLY_G-SBLK.OH3	POLY1 gate overhang of SBLK	OH.3	≧	0.15
SBLK-PLY_G.OL1	SBLK overlap of POLY1 gate Note: Zero is allowed if not over TG	OL.1	≧	0.06
PSD-PPSBLK.EN1	P+ IMPLANT enclosure of (P+ POLY over SBLK)	EN.1	≧	0.20
NSD-NPSBLK.EN2	N+ IMPLANT enclosure of (N+ POLY over SBLK)	EN.2	≧	0.20
PSD-PDSBLK.EN3	P+ IMPLANT enclosure of (P+ DIFFUSION over SBLK)	EN.3	≧	0.20
NSD-NDSBLK.EN4	N+ IMPLANT enclosure of (N+ DIFFUSION over SBLK)	EN.4	≧	0.20
SBLK.A	SBLK area		≧	0.30
SBLK.EA	SBLK enclosed area		≧	0.30
SBLK.R	Non-salicide POLY1 on DIFFUSION (SBLK over gate) is not allowed except ESD structure			Yes

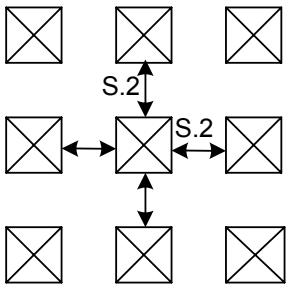

DIFFUSION
S.3
S.5
SBLK
W.1
POLY1
S.1
OH.2
OH.1
S.2
SAB
DIFFUSION
N+/P+ IMPLANT
S.5
S.4
POLY1
EN.3,EN.4
SBLK
OH.1
OH.2
OH.1
W.1
OL.1
OH.3
S.5
EN.1,EN.2
DIFFUSION
S.4
POLY1

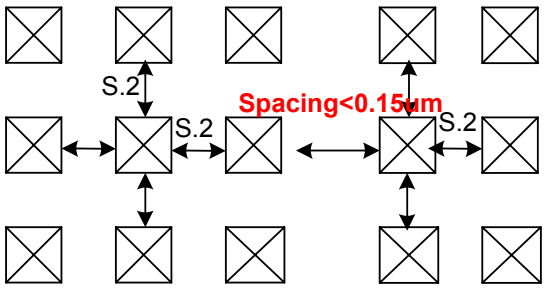
4A.13 CONTACT (CT) Layer Layout Rules

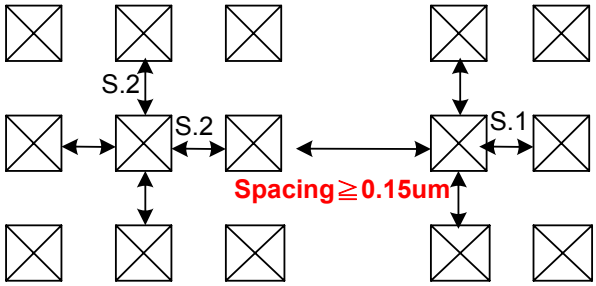
(unit : um)

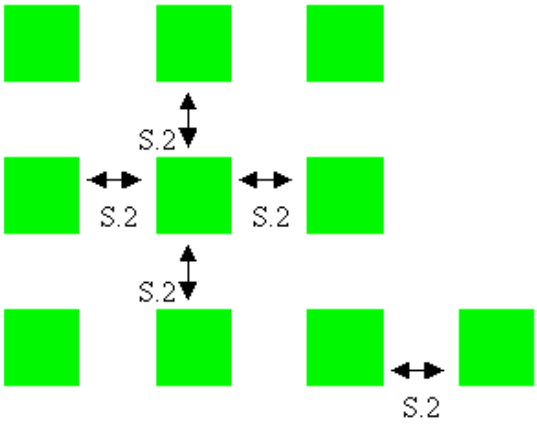
Rule No.	Description	Label		Rule
CT.SZ1	Exact CONTACT size (exclude CAD_CONTACT_EFUSE_BLOCK layer)	SZ.1	=	0.09X0.09
CT.SZ2	Exact CONTACT size inside CAD_CONTACT_EFUSE_BLOCK layer		=	0.12X0.12
CT.S1	Spacing of CONTACT sharing a common Metal shape above or DIFFUSION below (equal-potential)	S.1	≧	0.11
CT.S	Spacing of CONTACT NOT sharing a common Metal shape above or DIFFUSION below (non-equal-potential)		≧	0.12
CT.S2	Spacing of CONTACT for 3x3 array group. An array group is an array where spacing < 0.15um.	S.2	≧	0.14
CT_DF-PLY_G.S3	Spacing of DIFFUSION_CONTACT to POLY1 Gate	S.3	≧	0.055
CT_DF-PLY_G.S.TG	Spacing of DIFFUSION_CONTACT to [POLY1 Gate over TG]		≧	0.07
CT_PLY-DF.S4	Spacing of POLY1_CONTACT to DIFFUSION	S.4	≧	0.07
PLY-CT.EN1	POLY1 enclosure of CONTACT	EN.1	≧	0.02
PLY-CT.EN2	POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero if PLY-CT.EN1 is not fulfilled	EN.2	≧	0.04
DF-CT.EN3	DIFFUSION enclosure of CONTACT	EN.3	≧	0.015
DF-CT.EN4	DIFFUSION enclosure of two opposite sides of CONTACT when other sides have enclosure of zero if DF-CT.EN3 is not fulfilled	EN.4	≧	0.04
CT.R1	CONTACT must be within [POLY1 or DIFFUSION] and not over Gate area	R.1		Yes
CT.R2	ALL CONTACT shapes must be orthogonal except LOGO area. CONTACT_BAR is only allowed in die seal ring area.	R.2		Yes




S.2
S.2


S.2
S.2
Spacing<0.15um
S.2


S.2
S.2
S.1
Spacing≧0.15um


S.2
S.2
S.2
S.2
S.2

4A.14 BIPOLAR (BP) Layer Layout Rules (Non-tooling)

PNP (P+/N_WELL/P_WELL) type and NPN (N+/P_WELL/DEEP_N_WELL) of vertical Bipolar transistors are offered. The Bipolar marking layer is drawn over the emitter which excludes/blocks the extension implant from the DIFFUSION area (emitter). If customer would like to use BIPOLAR, please exactly follow UMC's GDS provided in model.

(unit : um)

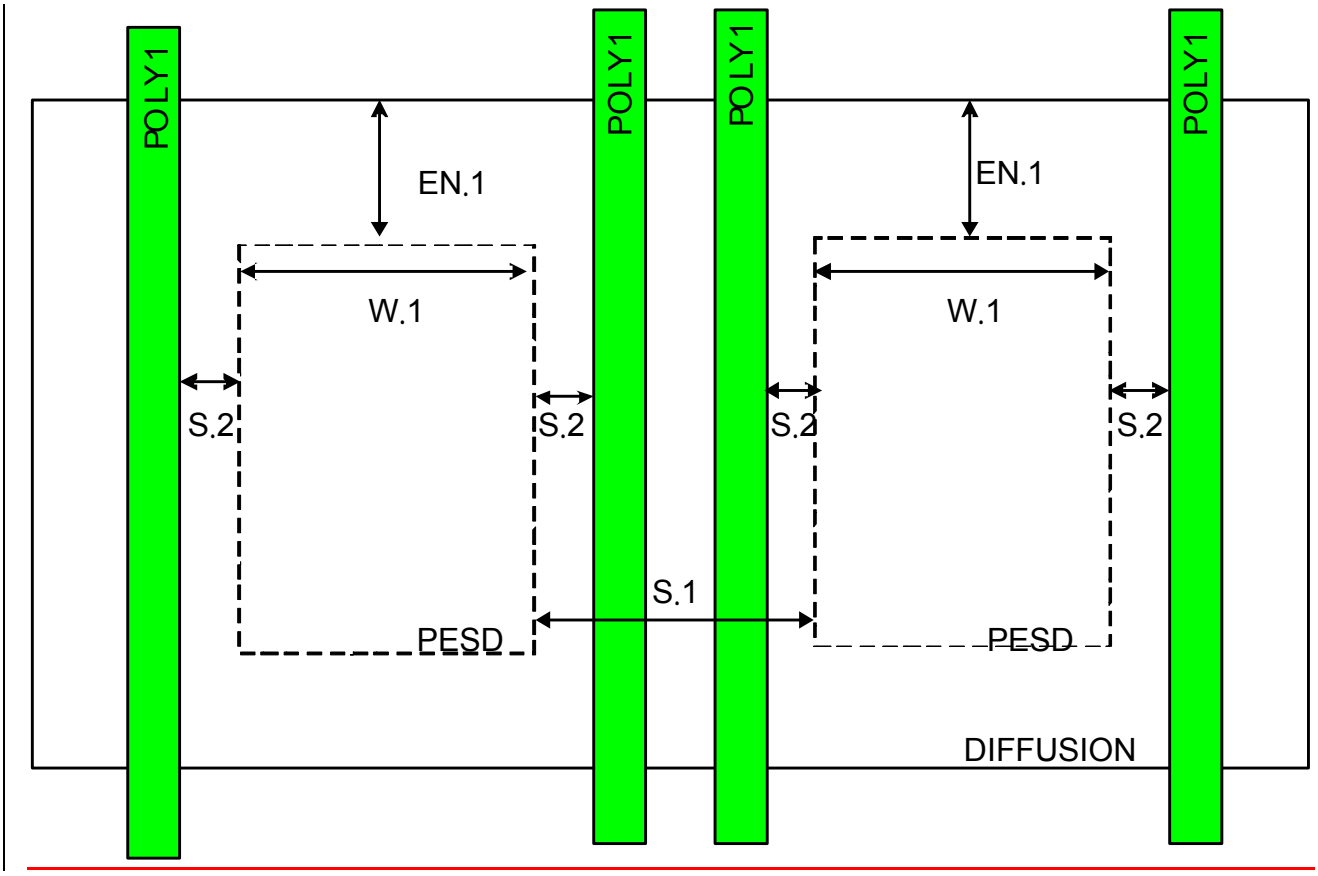
Rule No.	Description	Label		Rule
BP.W	BIPOLAR width		≧	0.36
BP.S	Spacing and notch of BIPOLAR		≧	0.36
BP.R	POLY1 and TG are not allowed over BIPOLAR			Yes

4A.15 PESD Layer Layout Rules

PESD is only allowed for ESD structures. The rules defined here are only for process requirements. For ESD immunity related PESD rules, please refer to the 65nm ESD Design Rule (Spec No.:G-03E-GENERATION65N-TLR/ESD)

(unit : um)

Rule No.	Description	Label		Rule
PESD.W1	PESD width	W.1	≧	0.54
PESD.S1	Spacing and notch of PESD	S.1	≧	0.54
PESD-PLY_G.S2	Spacing of PESD to POLY1 gate	S.2	≧	0.20
DF-PESD_N.EN1	DIFFUSION enclosure of PESD in NMOS	EN.1	≧	0.40
PESD.A	PESD area		≧	0.60
PESD.EA	PESD enclosed area		≧	0.60
PESD.R	PESD in (P+ DIFFUSION within N_WELL) is not allowed (exclude CAD_PESD_DRC_BLOCK layer(GDS No: 32(1))		≧	Yes

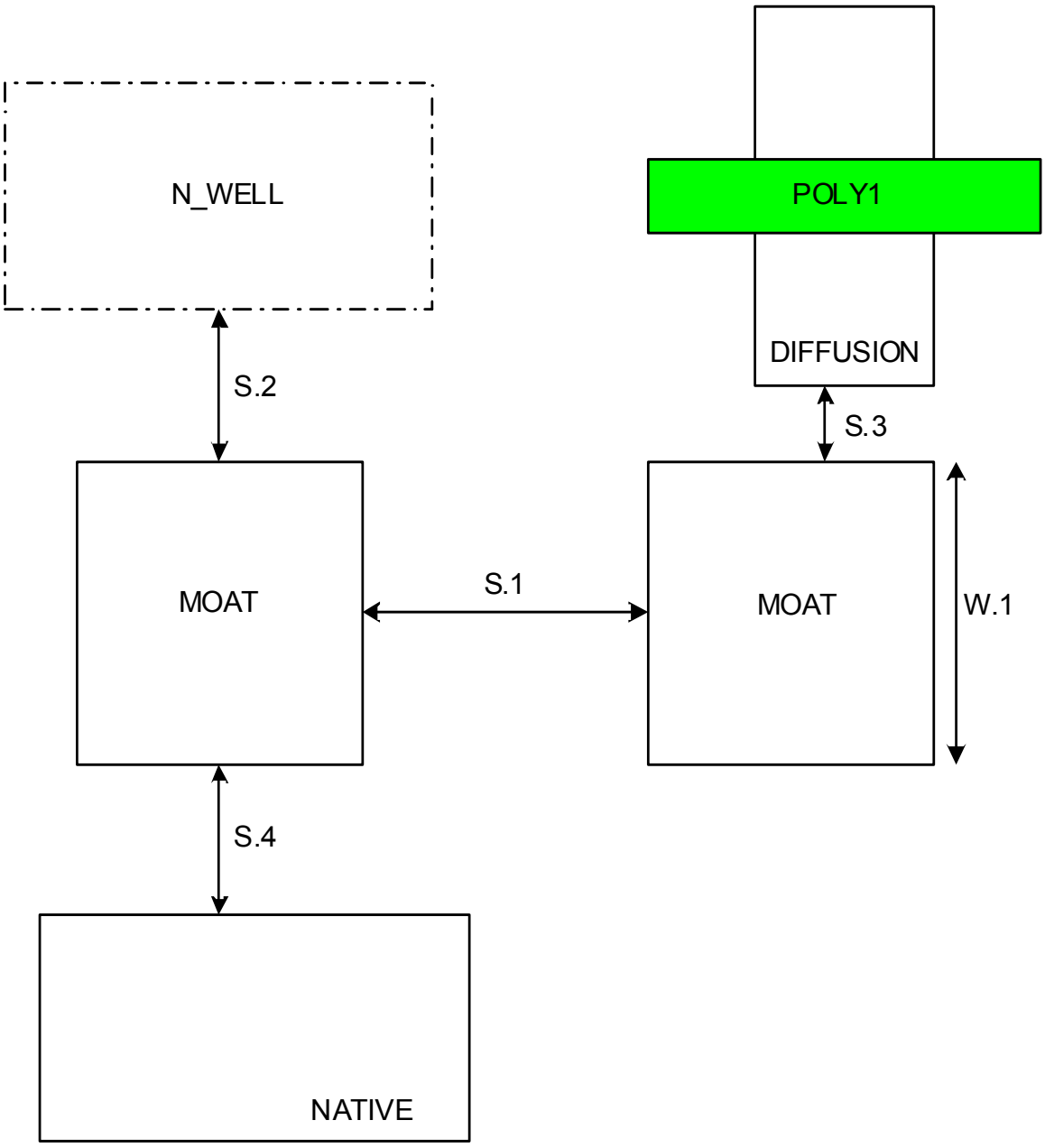


4A.16 MOAT Layer Layout Rules (Non-tooling)

MOAT layer defines resistive substrate area to reduce the coupling of substrate noise between proximity active regions on the same chip.

(unit : um)

Rule No.	Description	Label		Rule
MOAT.W1	MOAT width	W.1	≧	10
MOAT.S1	Spacing and notch of MOAT	S.1	≧	10
MOAT-NW.S2	Spacing of MOAT to N_WELL	S.2	≧	2
MOAT-DF.S3	Spacing of MOAT to DIFFUSION	S.3	≧	1
MOAT-NT.S4	Spacing of MOAT to NATIVE	S.4	≧	2
MOAT.R1	MOAT overlap N_WELL ,NATIVE, and DIFFUSION is not allowed			Yes
MOAT.R2	DIFFUSION dummy is allowed over MOAT			Yes

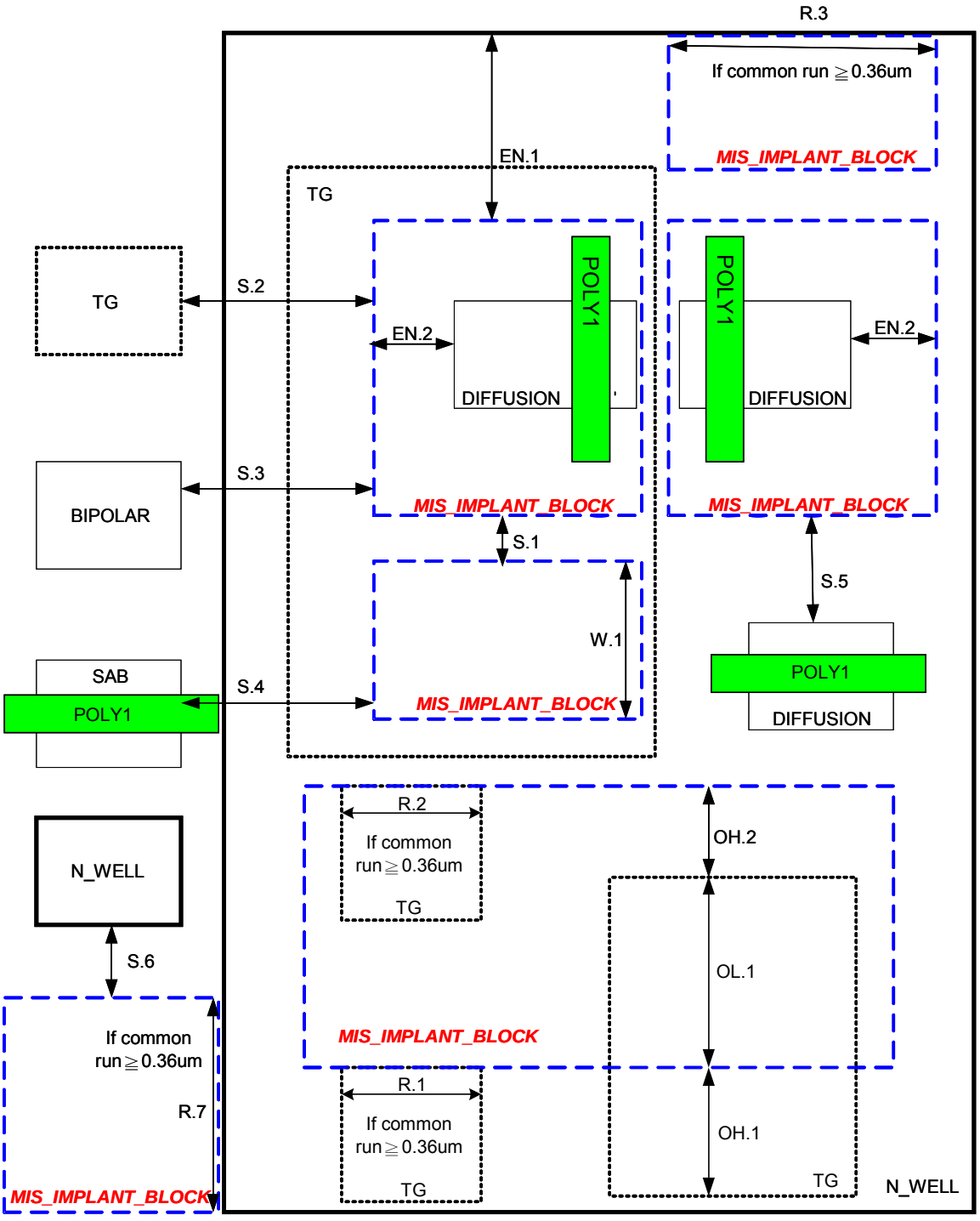


4A.17 MIS_IMPLANT_BLOCK Layer (Non-tooling)

This layer defines as the block layer of VT and LDD implant.

(unit : um)

Rule No.	Description	Label		Rule
MIS.W1	MIS_IMPLANT_BLOCK width	W.1	≧	0.36
MIS.S1	MIS_IMPLANT_BLOCK spacing and notch	S.1	≧	0.36
NW-MIS.EN1	N_WELL enclosure of MIS_IMPLANT_BLOCK	EN.1	≧	0.36
MIS-DF.EN2	MIS_IMPLANT_BLOCK enclosure of DIFFUSION	EN.2	≧	0.16
MIS-TG.S2	Spacing of MIS_IMPLANT_BLOCK to TG	S.2	≧	0.36
MIS-BP.S3	Spacing of MIS_IMPLANT_BLOCK to BIPOLAR (MIS_IMPLANT_BLOCK overlap BIPOLAR is not allowed)	S.3	≧	0.36
MIS-SAB.S4	Spacing of MIS_IMPLANT_BLOCK to N+/P+ non-salicide resistor body (MIS_IMPLANT_BLOCK overlap N+/P+ non-salicide resistor body is not allowed)	S.4	≧	0.48
MIS-DF.S5	Spacing of MIS_IMPLANT_BLOCK to DIFFUSION	S.5	≧	0.13
MIS-NW.S6	Spacing of MIS_IMPLANT_BLOCK to N_WELL	S.6	≧	0.36
TG-MIS.OH1	TG overhang of MIS_IMPLANT_BLOCK	OH.1	≧	0.36
MIS-TG.OH2	MIS_IMPLANT_BLOCK overhang of TG	OH.2	≧	0.36
TG-MIS.OL1	TG overlap of MIS_IMPLANT_BLOCK	OL.1	≧	0.36
TG-MIS.R1	If TG and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run	R.1		Yes
TG-MIS.R2	If TG and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run	R.2		Yes
NW-MIS.R3	If N_WELL and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run	R.3		Yes
NW-MIS.R7	If N_WELL and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run	R.7		Yes
MIS.R4	MIS_IMPLANT_BLOCK is not allowed over SAB, NATIVE, BIPOLAR, N+/P+ non-salicide resistor body			Yes
MIS.R6	MIS_IMPLANT_BLOCK shapes must be orthogonal			Yes

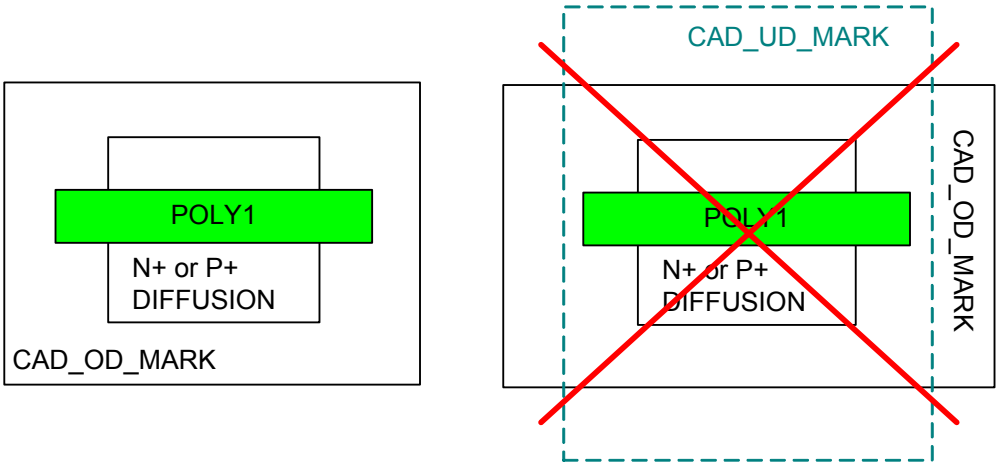

R.3
If common run ≧0.36um
MIS_IMPLANT_BLOCK
EN.1
TG
TG
S.2
EN.2
POLY1
DIFFUSION
POLY1
EN.2
DIFFUSION
BIPOLAR
S.3
MIS_IMPLANT_BLOCK
MIS_IMPLANT_BLOCK
S.1
S.5
W.1
SAB
POLY1
S.4
MIS_IMPLANT_BLOCK
POLY1
DIFFUSION
R.2
If common run ≧0.36um
TG
OH.2
N_WELL
OL.1
S.6
MIS_IMPLANT_BLOCK
If common run ≧0.36um
R.7
R.1
If common run ≧0.36um
TG
OH.1
TG
N_WELL
MIS_IMPLANT_BLOCK

4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Non-tooling)

This layer defines overdrive device for DRC/LVS operation only.

(unit : um)

Rule No.	Description	Label		Rule
OD.R1	Gate of overdrive device must be fully covered by CAD_OD_MARK			Yes
OD.R2	Gate of overdrive device over CAD_UD_MARK is not allowed			Yes

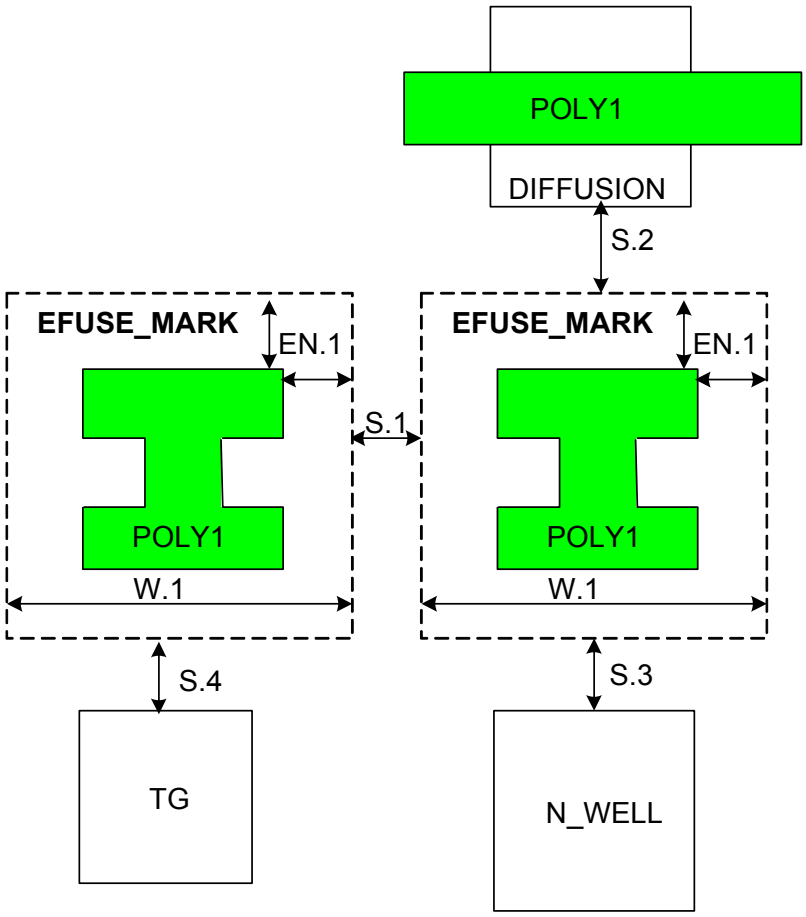


4A.19 EFUSE_MARK Layer Layout Rules

The layer is only allowed for UMC EFUSE team to create UMC EFUSE IP. If customers want to create their own EFUSE macro IP, please contact UMC/IPDS/DSCE for the details. It is not allowed for customers to use this layer to create their EFUSE IP due to the special Boolean operations associated with this mark layer.

(unit : um)

Rule No.	Description	Label		Rule
EFM.W1	EFUSE_MARK width	W.1	≧	0.36
EFM.S1	Spacing and notch of EFUSE_MARK	S.1	≧	0.36
EFM-DF.S2	Spacing of EFUSE_MARK to DIFFUSION	S.2	≧	0.18
EFM-NW.S3	Spacing of EFUSE_MARK to N_WELL	S.3	≧	0.18
EFM-TG.S4	Spacing of EFUSE_MARK to TG	S.4	≧	0.18
EFM-PLY.EN1	EFUSE_MARK enclosure of POLY1	EN.1	≧	0
NW-EFM.EN2	N_WELL enclosure of EFUSE_MARK		≧	0
TG-EFM.EN3	TG enclosure of EFUSE_MARK		≧	0
EFM.R1	DIFFUSION over EFUSE_MARK is not allowed			Yes
EFM.R2	EFUSE_MARK shapes must be orthogonal			Yes

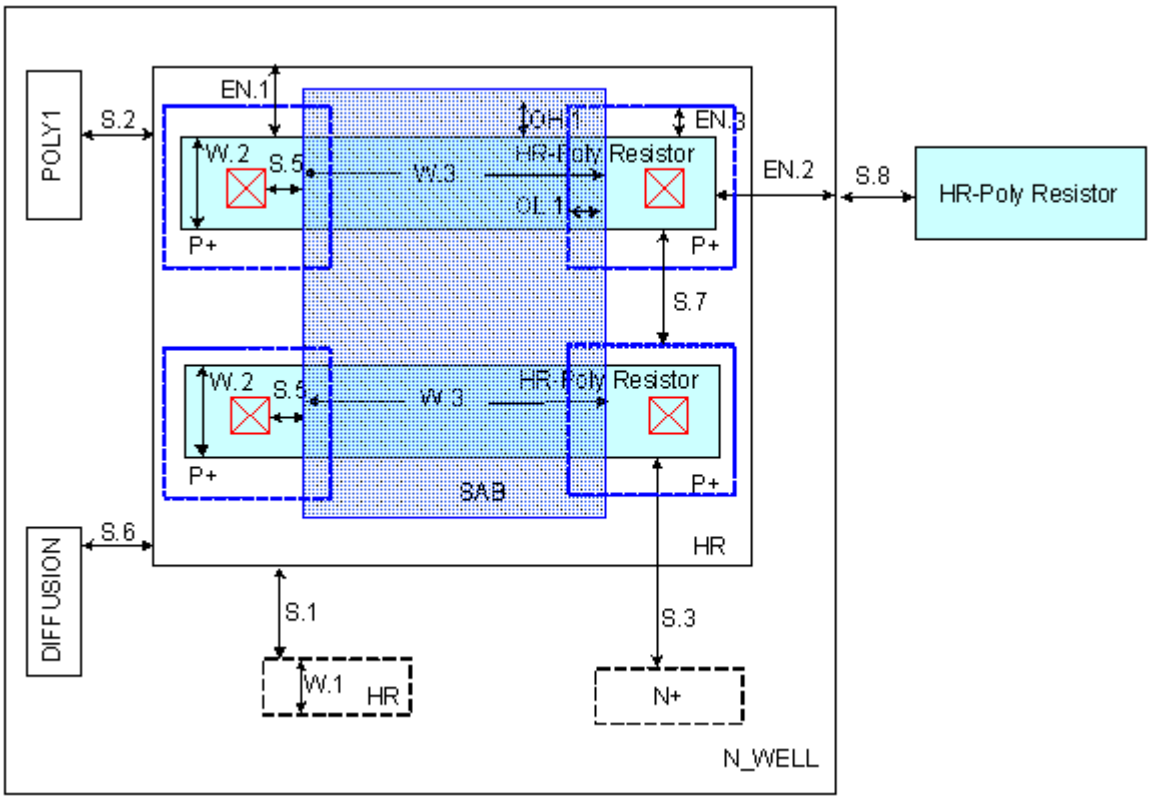


4A.20 HR Layer

HR layer is created for implantation of high resistance Poly resistors (HR-Poly resistor).

(unit : um)

Rule No.	Description	Label		Rule
HR.W1	HR width	W.1	≧	0.40
HR.S1	Spacing and notch of HR	S.1	≧	0.40
HRP_PLY.W2	POLY1 width of HR-Poly resistor	W.2	≧	0.44
HRP_SAB.W3	SAB width for HR-Poly resistor (Define HR-Poly resistor length)	W.3	≧	1.00
HR-HRP.EN1	HR enclosure of HR-Poly resistor	EN.1	≧	0.20
HR-PLY.S2	Spacing of HR to unrelated POLY1	S.2	≧	0.20
NSD-HRP.S3	Spacing of N+ IMPLANT to HR-Poly resistor	S.3	≧	0.20
SAB-HRP.OH1	SAB overhang of HR-Poly resistor	OH.1	≧	0.17
HRP_CT-SAB.S5	Spacing of HR-Poly CONTACT to SAB	S.5	≧	0.18
HR-DF.S6	Spacing of HR to unrelated DIFFUSION	S.6	≧	0.18
NW-HRP.EN2	N_WELL enclosure of HR-Poly resistor	EN.2	≧	0.20
HRP-NW.S8	Spacing of HR-Poly resistor to N_WELL	S.8	≧	0.20
HR_PSD- HRP.EN3	HR P+ IMPLANT enclosure of HR-Poly resistor edge where edge is not covered by SAB	EN.3	≧	0.20
HR_PSD-SAB.OL1	Exact HR P+ IMPLANT overlap of SAB	OL.1	=	0.20
PSD-HRP.S7	Spacing of P+ IMPLANT to unrelated HR-Poly resistor	S.7	≧	0.20



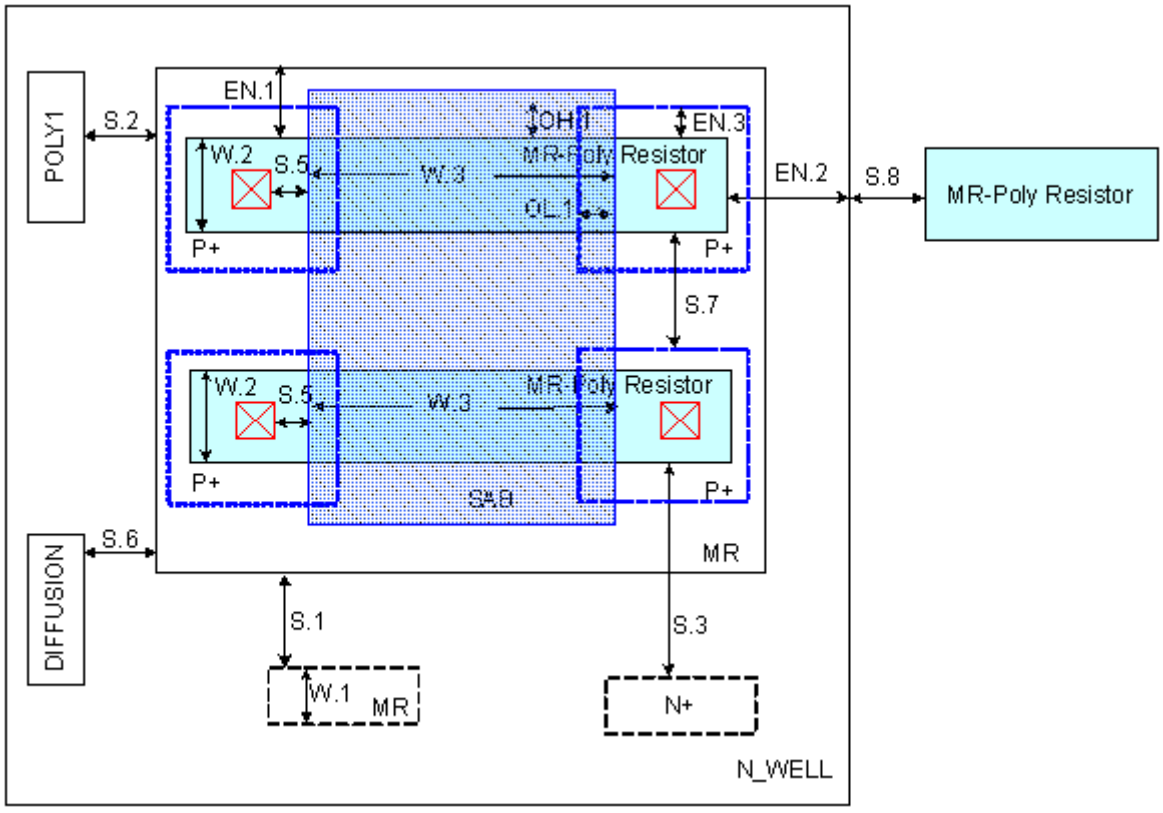
4A.21 MR Layer

MR layer is created for implantation of medium resistance Poly resistors (MR-Poly resistor).

The following rules are reserved for future customized medium resistance Poly resistors (MR-Poly resistor). To determine the suitable resistance, customers will need to discuss with UMC's CE and integration team based on their design specs.

(unit : um)

Rule No.	Description	Label		Rule
MR.W1	MR width	W.1	≧	0.40
MR.S1	Spacing and notch of MR	S.1	≧	0.40
MRP_PLY.W2	POLY1 width of MR-Poly resistor	W.2	≧	0.44
MRP_SAB.W3	SAB width for MR-Poly resistor (Define MR-Poly resistor length)	W.3	≧	1.00
MR-MRP.EN1	MR enclosure of MR-Poly resistor	EN.1	≧	0.20
MR-PLY.S2	Spacing of MR to unrelated POLY1	S.2	≧	0.20
NSD-MRP.S3	Spacing of N+ IMPLANT to MR-Poly resistor	S.3	≧	0.20
SAB-MRP.OH1	SAB overhang of MR-Poly resistor	OH.1	≧	0.17
MRP_CT-SAB.S5	Spacing of MR-Poly CONTACT to SAB	S.5	≧	0.18
MR-DF.S6	Spacing of MR to unrelated DIFFUSION	S.6	≧	0.18
NW-MRP.EN2	N_WELL layer enclosure of MR-Poly resistor	EN.2	≧	0.20
MRP-NW.S8	Spacing of MR-Poly resistor to N_WELL	S.8	≧	0.20
MR_PSD-MRP.EN3	MR P+ IMPLANT enclosure of MR-Poly resistor edge where edge is not covered by SAB	EN.3	≧	0.20
MR_PSD-SAB.OL1	Exact MR P+ IMPLANT overlap of SAB	OL.1	=	0.20
PSD-MRP.S7	Spacing of P+ IMPLANT to unrelated MR-Poly resistor	S.7	≧	0.20



4B BEOL Layout Rules

4B.a UMC platform offering: 1P10M (1X, 2X, 4X Metal, Top 32.5KA Metal)

Auto-metal slot generation will not be provided for L65 process. Customers should follow metal maximum width and density criteria during layout. If customers would like to create slots in metals, please use normal metal layer to layout holes or slots in metal and do not use METALn_CUSTOMER_SLOT layers. METALn_CUSTOMER_SLOT layers are not allowed except CAD_WAT_PAD_MARK area.

4B.a.1 1X pitch Metal Layers: (Maximum 6 levels of thin 1X pitch metal)

For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=1,2,3,4,5,6). For the definition of MnDMBK, please consult UMC representatives for more details about 65nm Logic Dummy Rules for Metal Layers.

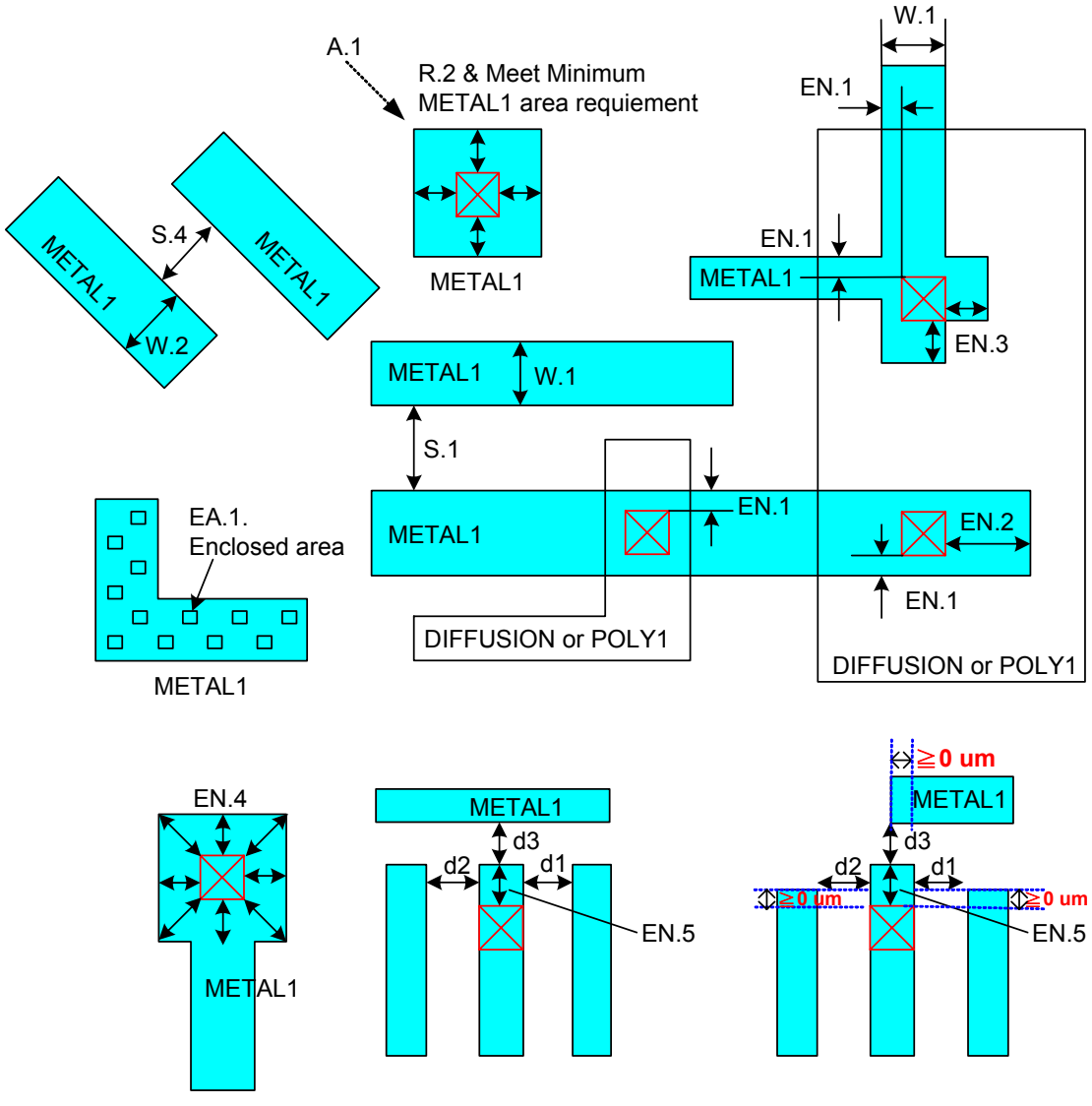
4B.a.1.1 METAL1 (M1) Layer Layout Rules

(unit : um)

Rule No.	Description	Label		Rule
M1.W1	METAL1 width	W.1	≧	0.09
M1.WX	METAL1 maximum width (NOTE1)		≦	12.00
M1.S1	Spacing and notch of METAL1	S.1	≧	0.09
M1.S2	Spacing and notch of METAL1 to [METAL1 with width > 0.5um] for common run length >0.5um		≧	0.16
M1.S3	Spacing and notch of METAL1 to [METAL1 with width > 2.80um] for common run length >2.8um		≧	0.30
M1-CT.EN1	METAL1 enclosure of CONTACT	EN.1	≧	0
M1-CT.EN2	METAL1 line end enclosure of CONTACT	EN.2	≧	0.03
M1-CT.EN3	METAL1 line end enclosure of CONTACT at METAL1 outer corner (for two adjacent sides, one side should be treated as metal line end)	EN.3	≧	0.03
M1-CT.EN4	METAL1 line end enclosure of CONTACT, including diagonal enclosure, for four sides if M1-CT.EN2 is not fulfilled	EN.4	≧	0.02
M1-CT.EN5	METAL1 line end enclosure of CONTACT if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e.. d1, d2, d3≦ 0.12um) Note: This rule excludes the case d3+EN.5≧0.16um.	EN.5	≧	0.04
M1.A1	METAL1 area	A.1	≧	0.042
M1.EA1	METAL1 enclosed area	EA.1	≧	0.2
M1.D	METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7)		≧	15%
M1.D1	METAL1 density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments (Note 2, 4, 7, ***8***)		≦	80%
M1.R2	CONTACT must be within METAL1	R.2		Yes
M1.W2	Width of 45 degree METAL1	W.2	≧	0.19
M1.S4	Spacing of 45 degree METAL1	S.4	≧	0.19
M1.R3	METAL1_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.
8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.



Below rule is for customer metal1 Dummy, METAL1_CUSTOMER_DUMMY (GDS no: 72(8))

Rule No.	Description	Label		Rule
M1DM.L1	METAL1_CUSTOMER_DUMMY length		=	0.6~12
M1DM.W3	METAL1_CUSTOMER_DUMMY width		=	0.6~12
M1DM.S5	Spacing of METAL1_CUSTOMER_DUMMY		≧	0.3
M1DM-Mn.S6	Spacing of METAL1_CUSTOMER_DUMMY to METAL1		≧	0.3
M1DM-M1DMBK.S7	Spacing of METAL1_CUSTOMER_DUMMY to METAL1_DUMMY_BLOCK		≧	0.8
M1DM-IND.S8	Spacing of METAL1_CUSTOMER_DUMMY to IND		≧	0.8
M1DM-FM.S9	Spacing of METAL1_CUSTOMER_DUMMY to FUSE_MARK		≧	0.8
M1DM-PM.S10	Spacing of METAL1_CUSTOMER_DUMMY to PAD_MARK		≧	0.8
M1DM-SRM.S11	Spacing of METAL1_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	0.8

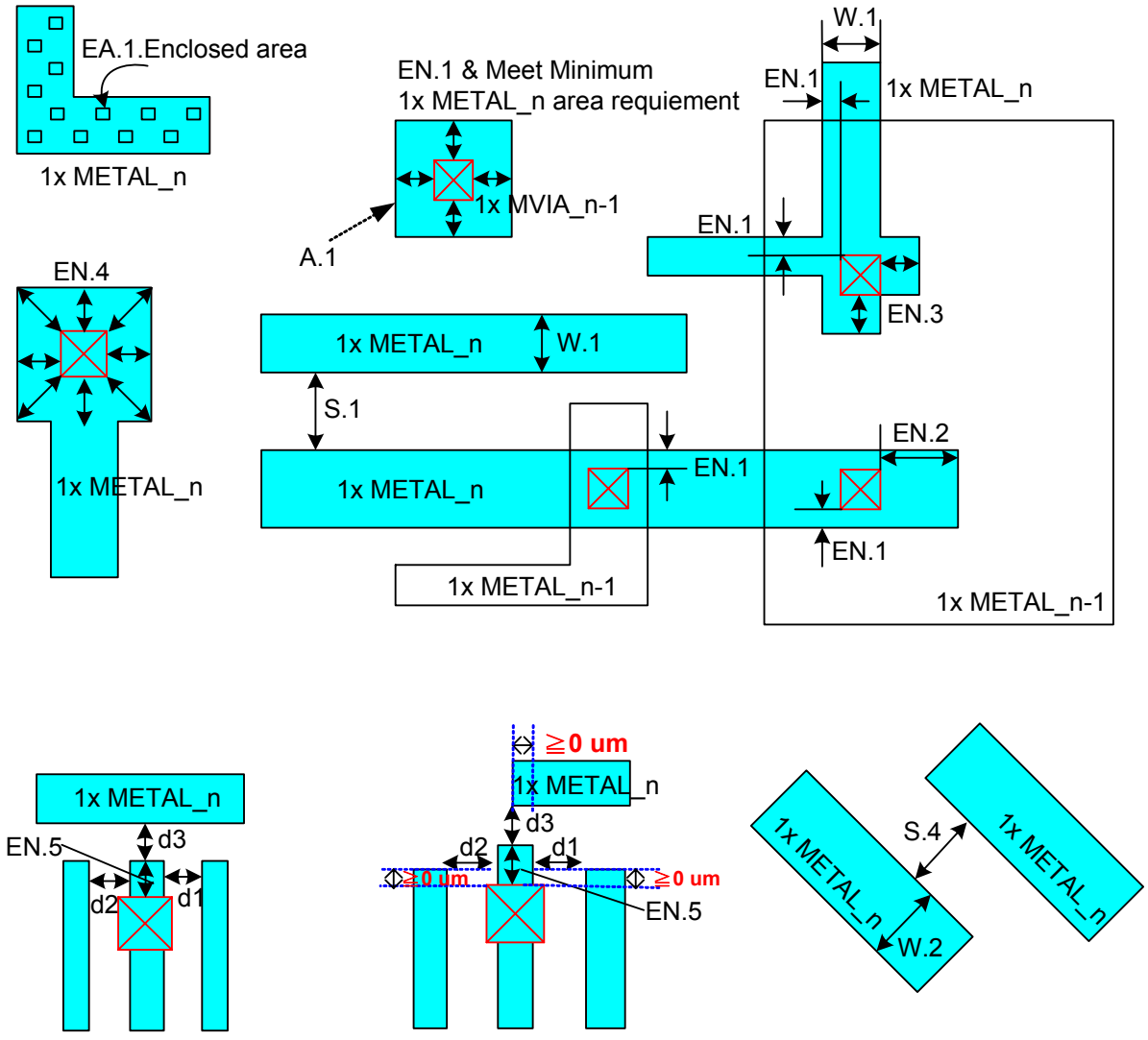
4B.a.1.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6)

(unit : um)

Rule No.	Description	Label		Rule
1XMn.W1	METAL_n width (n=2,3,4,5,6)	W.1	≧	0.10
1XMn.WX	METAL_n maximum width (n=2,3,4,5,6) (NOTE1)		≦	12.00
1XMn.S1	Spacing and notch of METAL_n to METAL_n (n=2,3,4,5,6)	S.1	≧	0.10
1XMn.S2	Spacing and notch of METAL_n to [METAL_n with width > 0.50um] for common run length >0.5um (n=2,3,4,5,6)		≧	0.16
1XMn.S3	Spacing and notch of METAL_n to [METAL_n with width > 2.80um] for common run length >1.5um (n=2,3,4,5,6)		≧	0.30
1XMn-1XVm.EN1	METAL_n enclosure of MVIA_n-1(n=2,3,4,5,6)	EN.1	≧	0
1XMn-1XVm.EN2	METAL_n line end enclosure of MVIA_n-1	EN.2	≧	0.03
1XMn-1XVm.EN3	METAL_n line end enclosure of MVIA_n-1 at METAL_n outer corner (for two adjacent sides, one side should be treated as metal line end)	EN.3	≧	0.03
1XMn-1XVm.EN4	METAL_n line end enclosure of MVIA_n-1, including diagonal enclosure, for four sides if 1XMn-1XVm.EN2 is not fulfilled	EN.4	≧	0.02
1XMn-1XVm.EN5	METAL_n line end enclosure of MVIA_n-1 if METAL_n width ≦ 0.11um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.12um (i.e. d1, d2 and d3 ≦ 0.12um) Note: This rule excludes the case d3+EN.5≧0.16um.	EN.5	≧	0.04
1XMn.A1	METAL_n area (n=2,3,4,5,6) (Non-shrinkable)	A.1	≧	0.046um^2
1XMn.A1s	METAL_n area (n=2,3,4,5,6) (Shrinkable)	A.1		0.052um^2
1XMn.EA1	METAL_n enclosed area (n=2,3,4,5,6)	EA.1	≧	0.11um^2
1XMn.D	METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 6, 7, 8, 9)		≧	15%
1XMn.D1	METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 5, 8)		≦	80%
1XMn.W2	Width of 45 degree METAL (NOTE4)	W.2	≧	0.20
1XMn.S4	Spacing of 45 degree METAL (NOTE4)	S.4	≧	0.20
1XMn. R	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B.a.1.3.
5) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
6) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
7) Skip rule check if violate area include top copper metal over FUSE_MARK
8) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.
9) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.

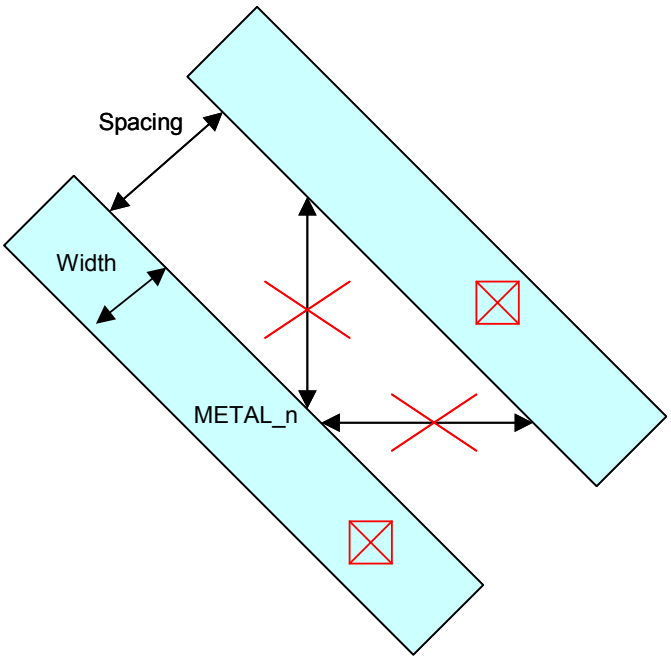

EA.1.Enclosed area
1x METAL_n
EN.1 & Meet Minimum
1x METAL_n area requiement
1x MVIA_n-1
A.1
W.1
EN.1
1x METAL_n
EN.1
EN.3
EN.4
1x METAL_n
1x METAL_n
W.1
S.1
1x METAL_n
EN.1
EN.2
EN.1
1x METAL_n-1
1x METAL_n-1
1x METAL_n
EN.5
d3
d2
d1
≧0 um
1x METAL_n
d3
d2
d1
≧0 um
≧0 um
EN.5
1x METAL_n
1x METAL_n
S.4
W.2

4B.a.1.3 X-Architecture of 1 x pitch Metal Layer

For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard METAL process.

For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "BLOCK" on the design levels of MnDMBK (n=1,2,3,4,5,6), respectively. For the definition of MnDMBK, please refer to the individual Mask Tooling Information (i.e. G-06 document listed in the individual DSM).

Width and Spacing are defined as distances along 45 or 135 degree direction.



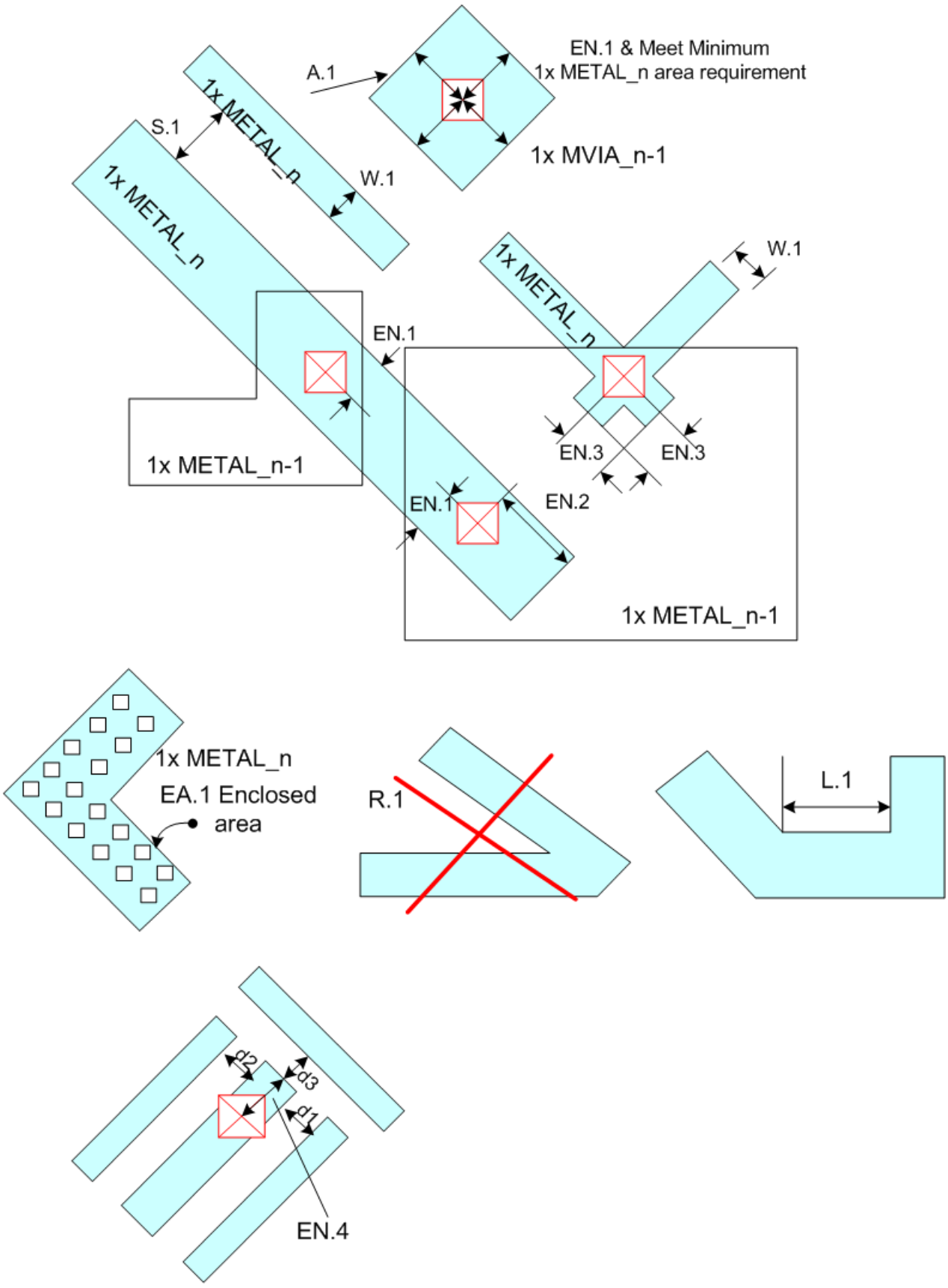
METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6) :

(unit : um)

Rule No.	Description	Label		Rule
1XMn.X.W1	METAL_n width (n=2,3,4,5,6)	W.1	≧	0.11
1XMn.X.WX1	METAL_n maximum width (n=2,3,4,5,6) (NOTE1)		≦	12.00
1XMn.X.S1	Spacing and notch of METAL_n to METAL_n (n=2,3,4,5,6)	S.1	≧	0.11
1XMn.X.S2	Spacing and notch of METAL_n to [METAL_n with width > 0.50um](n=2,3,4,5,6)		≧	0.16
1XMn.X.S3	Spacing and notch of METAL_n to [METAL_n with width > 2.80um](n=2,3,4,5,6)		≧	0.30
1XMn-1XVm.X.EN1	METAL_n enclosure of MVIA_n-1 center (n=2,3,4,5,6)	EN.1	≧	0.055
1XMn-1XVm.X.EN2	METAL_n line end enclosure of MVIA_n-1 center (n=2,3,4,5,6)	EN.2	≧	0.08
1XMn-1XVm.X.EN3	METAL_n line end enclosure of MVIA_n-1 center at METAL_n outer corner (for two adjacent sides, at least one side should be treated as metal line end) (n=2,3,4,5,6)	EN.3	≧	0.08
1XMn-1XVm.X.EN4	METAL_n line end enclosure of MVIA_n-1 center if METAL_n width ≦ 0.12um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.16um (i.e. d1, d2 and d3 ≦ 0.16um)	EN.4	≧	0.11
1XMn.X.A1	METAL_n area (n=2,3,4,5,6)	A.1	≧	$0.046um^2$
1XMn.X.EA1	METAL_n enclosure area (n=2,3,4,5,6)	EA.1	≧	$0.11um^2$
1XMn.X.D	METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7)		≧	15%
1XMn.X.D1	METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)		≦	80%
1XMn.X.R1	Angle of routing wires when changing direction should be greater or equal to 90 degree	R.1		Yes
1XMn.X.L1	Metal length between two connected metal corners	L.1	≧	0.2
1XMn.X. R2	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC DRC can check METAL_n density over the whole chip.


A.1
EN.1 & Meet Minimum
1x METAL_n area requirement
1x MVIA_n-1
S.1
1x METAL_n
W.1
1x METAL_n
W.1
EN.1
1x METAL_n-1
EN.3
EN.3
EN.2
EN.1
1x METAL_n-1
1x METAL_n
EA.1 Enclosed
area
R.1
L.1
d2
d3
d1
EN.4

The following layers are for customer 1x pitch metal Dummy (n=2~6), METALn_CUSTOMER_DUMMY (GDS no: 73(8), 74(8), 75(8), 76(8), 77(8))

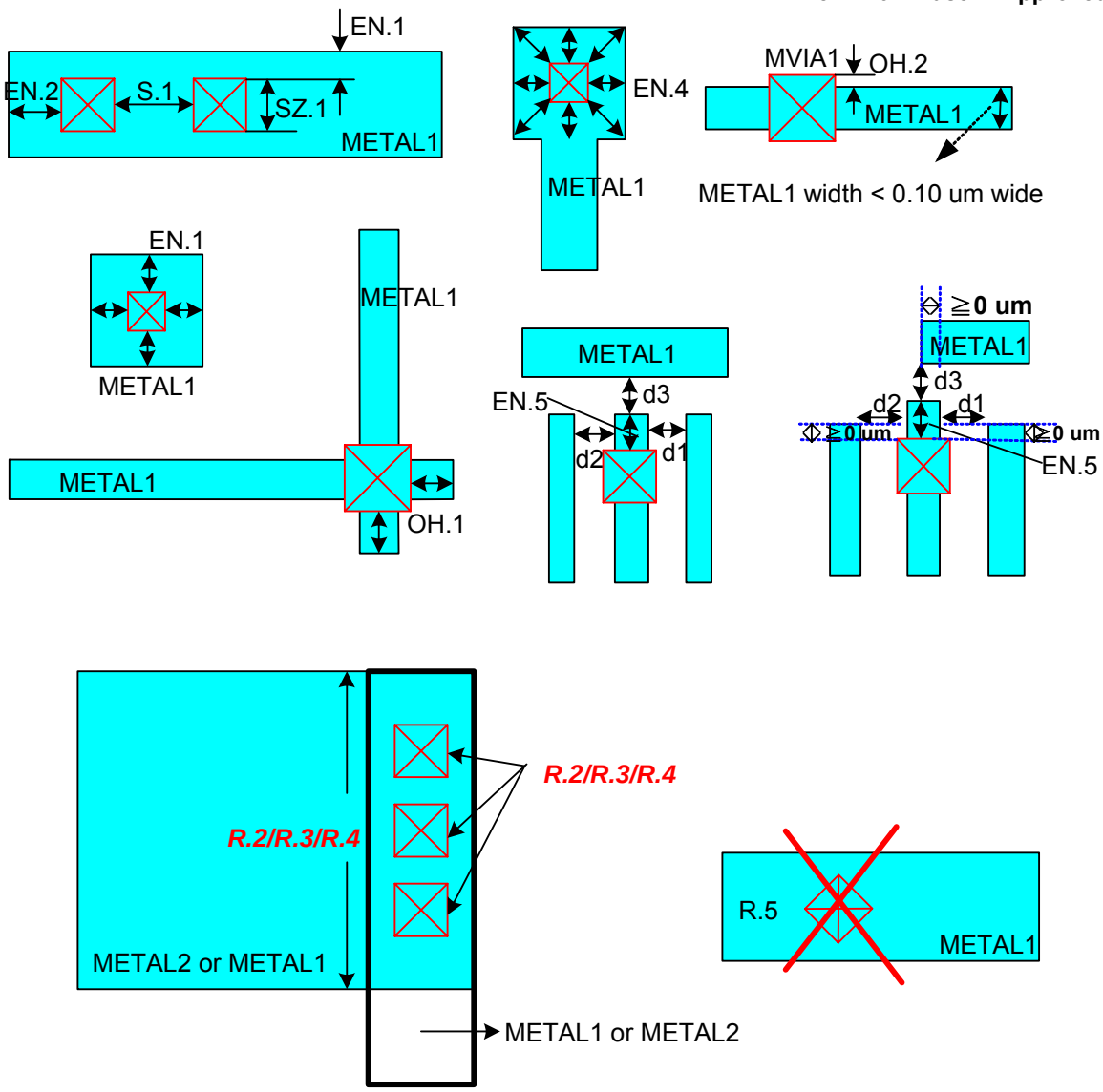
Rule No.	Description	Label		Rule
1XMnDM.L1	METALn_CUSTOMER_DUMMY length		=	0.6~12
1XMnDM.W3	METALn_CUSTOMER_DUMMY width		=	0.6~12
1XMnDM.S5	Spacing of METALn_CUSTOMER_DUMMY		≧	0.3
1XMnDM-Mn.S6	Spacing of METALn_CUSTOMER_DUMMY to METAL_n		≧	0.3
1XMnDM-MnDMBK.S7	Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY_BLOCK		≧	0.8
1XMnDM-IND.S8	Spacing of METALn_CUSTOMER_DUMMY to IND		≧	0.8
1XMnDM-FM.S9	Spacing of METALn_CUSTOMER_DUMMY to FUSE_MARK		≧	0.8
1XMnDM-PM.S10	Spacing of METALn_CUSTOMER_DUMMY to PAD_MARK		≧	0.8
1XMnDM-SRM.S11	Spacing of METALn_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	0.8

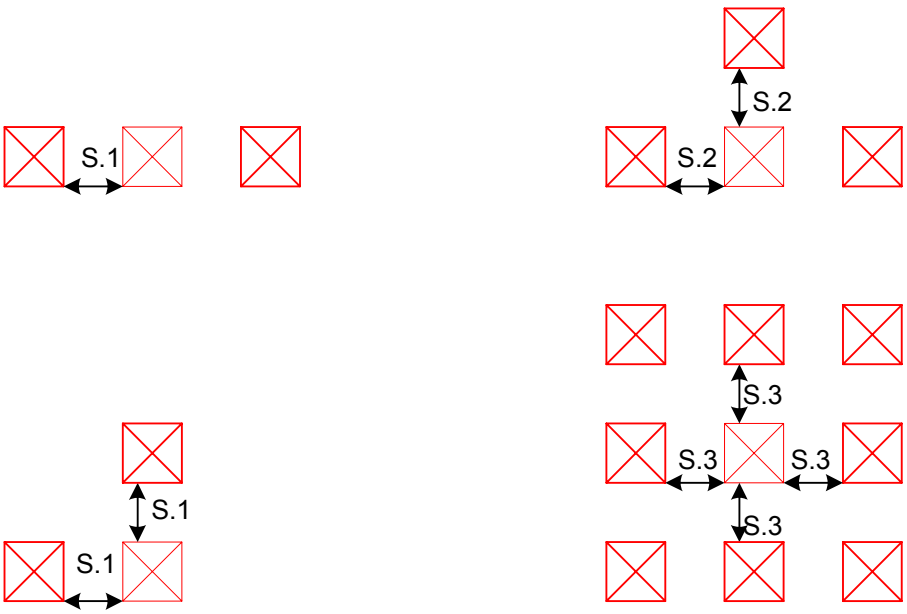
4B.a.2 1X pitch MVIA Layers : (Maximum 5 levels of thin 1X pitch MVIA)

4B.a.2.1 MVIA1 (V1) Layer Layout Rules

(unit : um)

Rule No.	Description	Label		Rule
V1.SZ1	Exact MVIA1 size	SZ.1	=	0.10X0.10
V1.S1	Spacing of MVIA1	S.1	≧	0.10
V1.S2	Spacing of MVIA1 with 3 or more neighboring MVIA1 ("Neighboring" is defined as having spacing of < 0.14um.)	S.2	≧	0.11
V1.S3	Spacing of MVIA1 for ≧ 3X3 array group (An "array group" is defined as an array where spacing <0.14um.)	S.3	≧	0.13
M1-V1.EN1	[METAL1 width ≧ 0.1 um] enclosure of MVIA1	EN.1	≧	0
M1-V1.EN2	METAL1 line end enclosure of MVIA1	EN.2	≧	0.03
M1-V1.OH1	METAL1 line end overhang of MVIA1 at METAL1 outer corner (for two adjacent sides, at least one side should be treated as metal line end)	OH.1	≧	0.03
M1-V1.EN4	METAL1 line end enclosure of MVIA1, including diagonal enclosure, for four sides if M1-V1.EN2 is not fulfilled	EN.4	≧	0.02
M1-V1.EN5	METAL1 line end enclosure of MVIA1 if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) Note: This rule excludes the case d3+EN.5≧0.16um.	EN.5	≧	0.04
V1-M1.OH2	MVIA1 overhang of [METAL1 with width < 0.10 um]	OH.2	<	0.005
V1.R1	MVIA1 must be within METAL1 when METAL1 width ≧ 0.10 um	R.1		Yes
V1.R2	A minimum of 2 MVIA1 at a spacing ≦ 0.3um must connect METAL1 and METAL2 when METAL1 or METAL2 ≧ 0.5um wide	R.2		Yes
V1.R3	A minimum of 3 MVIA1 at a spacing ≦ 0.3um must connect METAL1 and METAL2 when METAL1 or METAL2 > 0.7um wide	R.3		Yes
V1.R4	A minimum of 4 MVIA1 at a spacing ≦ 0.3um must connect METAL1 and METAL2 when METAL1 or METAL2 ≧ 1.5um wide	R.4		Yes
V1.R5	All MVIA1 shapes must be orthogonal except LOGO area. MVIA1_BAR is only allowed in die seal ring and fuse area.	R.5		Yes
V1.R6	MVIA1 can be fully or partially stacked on CONTACT			Yes

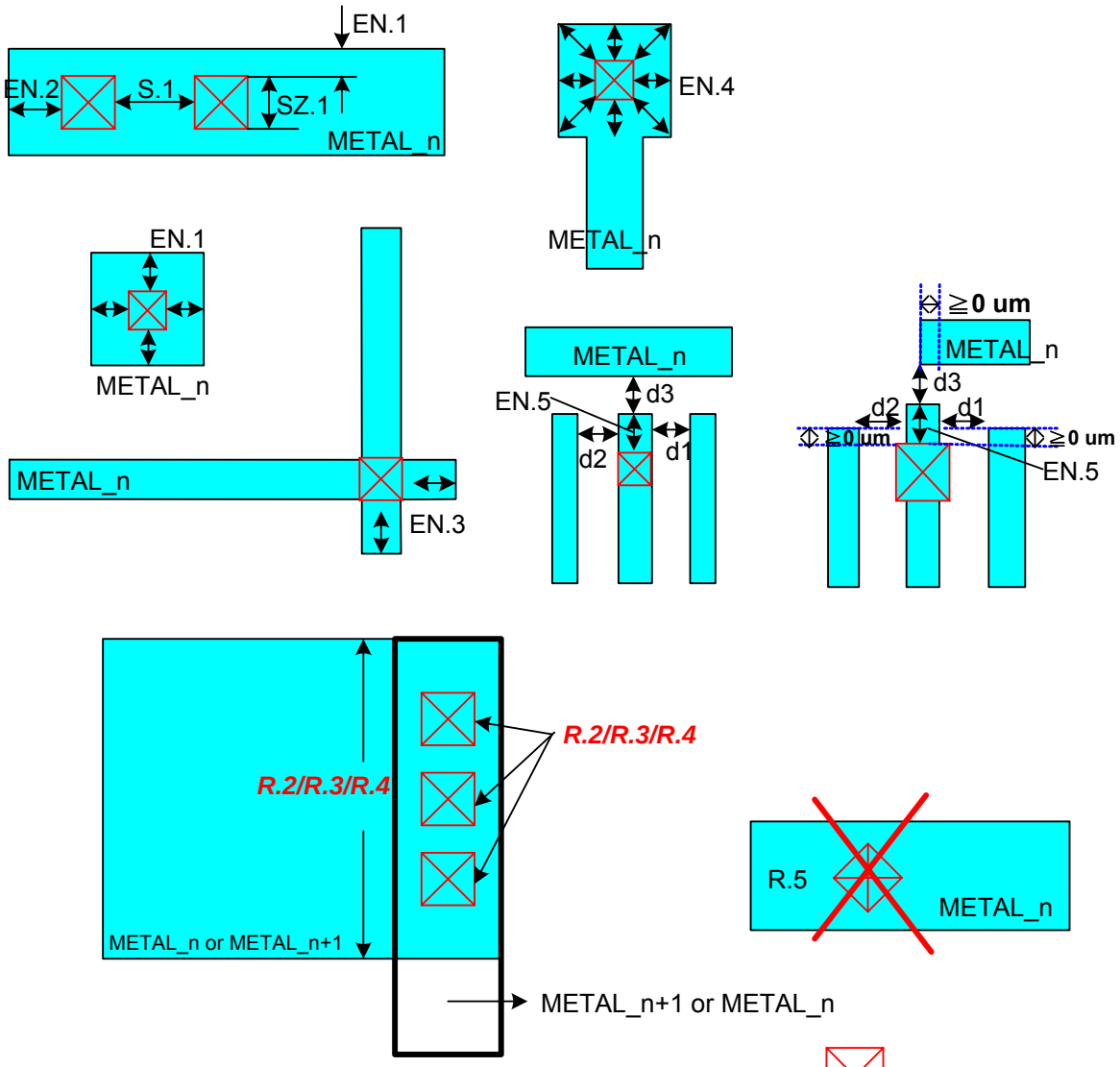

EN.1
EN.2
S.1
SZ.1
METAL1
EN.4
METAL1
MVIA1
OH.2
METAL1
METAL1 width < 0.10 um wide
EN.1
METAL1
METAL1
METAL1
OH.1
METAL1
EN.5
d3
d2
d1
≧0 um
METAL1
d3
d2
d1
≧0 um
≧0 um
EN.5
R.2/R.3/R.4
R.2/R.3/R.4
METAL2 or METAL1
METAL1 or METAL2
R.5
METAL1

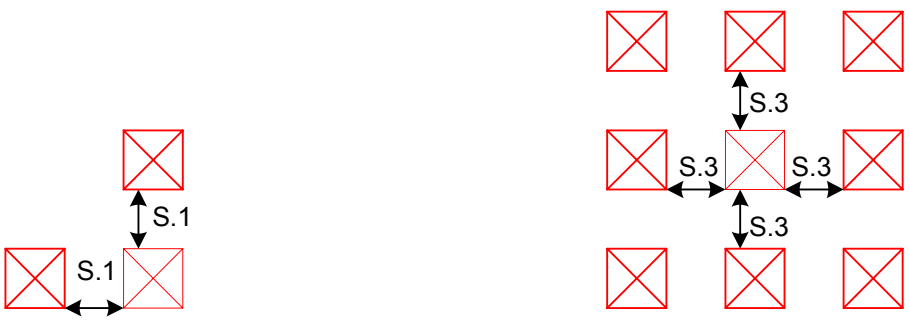

S.1
S.2
S.2
S.1
S.1
MVIA1 within<0.14um
S.3
S.3
S.3
S.3
MVIA1 within<0.14um

4B.a.2.2 MVIA2 and above (1XVn) – 1X pitch MVIA_n Layer (n=2,3,4,5)

(unit : um)

Rule No.	Description	Label		Rule
1XVn.SZ1	Exact MVIA_n size (n=2,3,4,5)	SZ.1	=	0.10 x 0.10
1XVn.S1	Spacing of MVIA_n	S.1	≧	0.10
1XVn.S2	Spacing of MVIA_n with 3 or more neighboring MVIA_n ("Neighboring" is defined as having spacing of < 0.14um.)	S.2	≧	0.11
1XVn.S3	Spacing of MVIA_n for ≧ 3X3 array group (An "array group" is defined as an array where spacing <0.14um.)	S.3	≧	0.13
1XMn-1XVn.EN1	METAL_n enclosure of MVIA_n (n=2,3,4,5)	EN.1	≧	0
1XMn-1XVn.EN2	METAL_n line end enclosure of MVIA_n (n=2,3,4,5)	EN.2	≧	0.03
1XMn-1XVn.EN3	METAL_n line end enclosure of MVIA_n at METAL_n outer corner (for two adjacent sides, at least one side should be treated as metal line end) (n=2,3,4,5)	EN.3	≧	0.03
1XMn-1XVn.EN4	METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides if 1XMn-1XVn.EN2 is not fulfilled (n=2,3,4,5)	EN.4	≧	0.02
1XMn-1XVn.EN5	METAL_n line end enclosure of MVIA_n if METAL_n width ≦ 0.11um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) Note: This rule excludes the case d3+EN.5≧0.16um.	EN.5	≧	0.04
1XVn.R1	MVIA_n must within METAL_n (n=2,3,4,5)	R.1		Yes
1XVn.R2	A minimum of 2 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide	R.2		Yes
1XVn.R3	A minimum of 3 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 > 0.7um wide	R.3		Yes
1XVn.R4	A minimum of 4 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide	R.4		Yes
1XVn.R5	All MVIA_n (n=2,3,4,5) shapes must be orthogonal except LOGO area. MVIA_n_BAR (n=2,3,4,5) is only allowed in die seal ring and fuse area.	R.5		Yes
1XVn.R6	MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…, n-1 and CONTACT			Yes
1XVn.R7	Layers of stacked via including MVIA1,1X,2X,4XVn and 32.5KA MVIA(exclude all layers with stacked redundant via)		≦	4





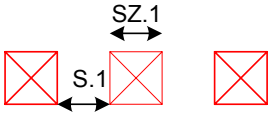
MVIA_n within<0.14um

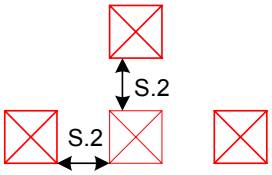
MVIA_n within<0.14um

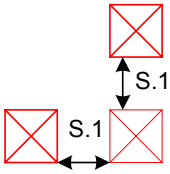
4B.a.2.3 X-Architecture of MVIA2 and above 1X pitch MVIA -- MVIA_n (n=2,3,4,5)

(unit : um)

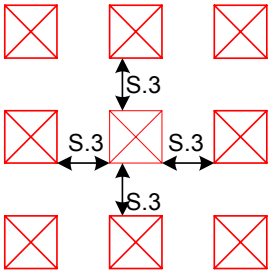
Rule No.	Description	Label		Rule
1XVn.X.SZ1	Exact MVIA_n size (n=2,3,4,5)	SZ.1	=	0.10 x 0.10
1XVn.S1	Spacing of MVIA_n	S.1	≧	0.10
1XVn.S2	Spacing of MVIA_n with 3 or more neighboring MVIA_n ("Neighboring" is defined as having spacing of < 0.14um.	S.2	≧	0.11
1XVn.S3	Spacing of MVIA_n for ≧ 3X3 array group (An "array group" is defined as an array where spacing <0.14um.)	S.3	≧	0.13
1XMn-1XVn.X.EN1	METAL_n enclosure of MVIA_n center (n=2,3,4,5)	EN.1	≧	0.055
1XMn-1XVn.X.EN2	METAL_n line end enclosure of MVIA_n (n=2,3,4,5)	EN.2	≧	0.08
1XMn-1XVn.X.EN3	METAL_n line end enclosure of MVIA_n at METAL_n outer corner (for two adjacent sides, at least one side should be treated as metal line end) (n=2,3,4,5)	EN.3	≧	0.08
1XMn-1XVn.X.EN4	METAL_n line end enclosure of MVIA_n center for four sides (n=2,3,4,5)	EN.4	≧	0.07
1XMn-1XVn.X.EN5	METAL_n line end enclosure of MVIA_n if METAL_n width ≦ 0.12um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.16um (i.e. d1, d2 and d3 ≦ 0.16um)	EN.5	≧	0.11
1XVn.X.R2	A minimum of 2 MVIA_n at a spacing ≦*0.35*um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide	R.2		Yes
1XVn.X.R3	A minimum of 3 MVIA_n at a spacing ≦ *0.35*um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 > 0.7um wide	R.3		Yes
1XVn.X.R4	A minimum of 4 MVIA_n at a spacing ≦ *0.35*um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide	R.4		Yes
1XVn.X.R5	All MVIA_n (n=2,3,4,5) shapes must be orthogonal except LOGO area. MVIA_n_BAR (n=2,3,4,5) is only allowed in die seal ring and fuse area.	R.5		Yes
1XVn.X.R6	MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…, n-1 and CONTACT			Yes
1XVn.X.R7	Layers of stacked via including MVIA1,1X,2X,4XVn and 32.5KA MVIA(exclude all layers with stacked redundant via)		≦	4



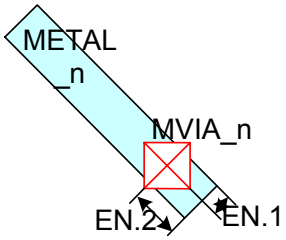


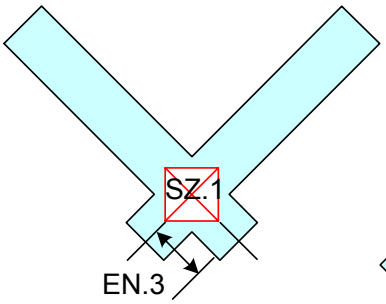


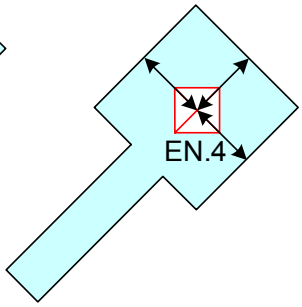
MVIA_n within<0.14um

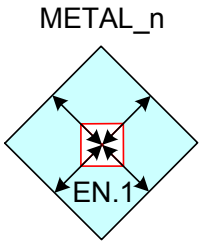


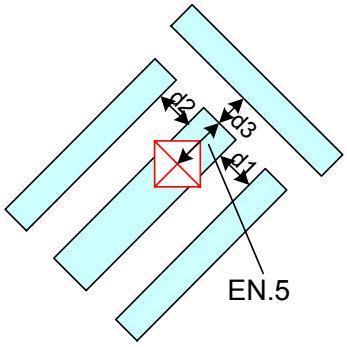
MVIA_n within<0.14um

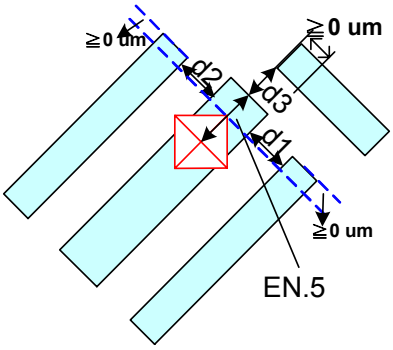


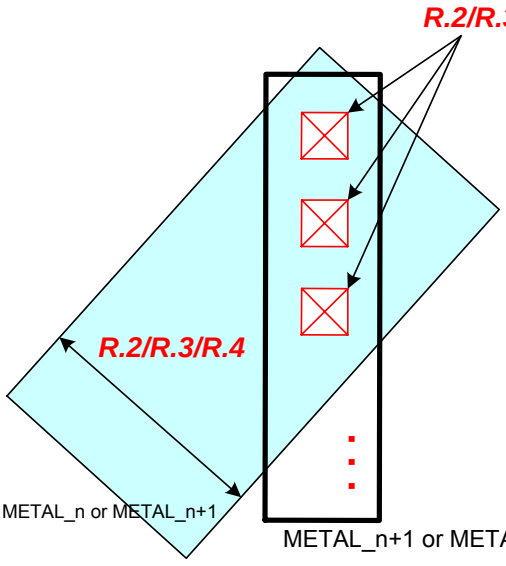


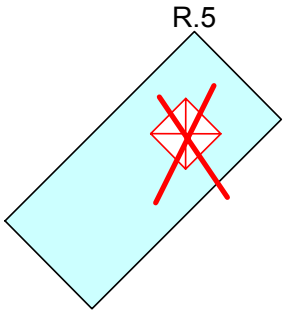












4B.a.3 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) (Maximum 2 levels of 2x pitch metal)

For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=7,8). For the definition of MnDMBK, please consult UMC representatives for more details about 65nm Logic Dummy for Metal Layers.

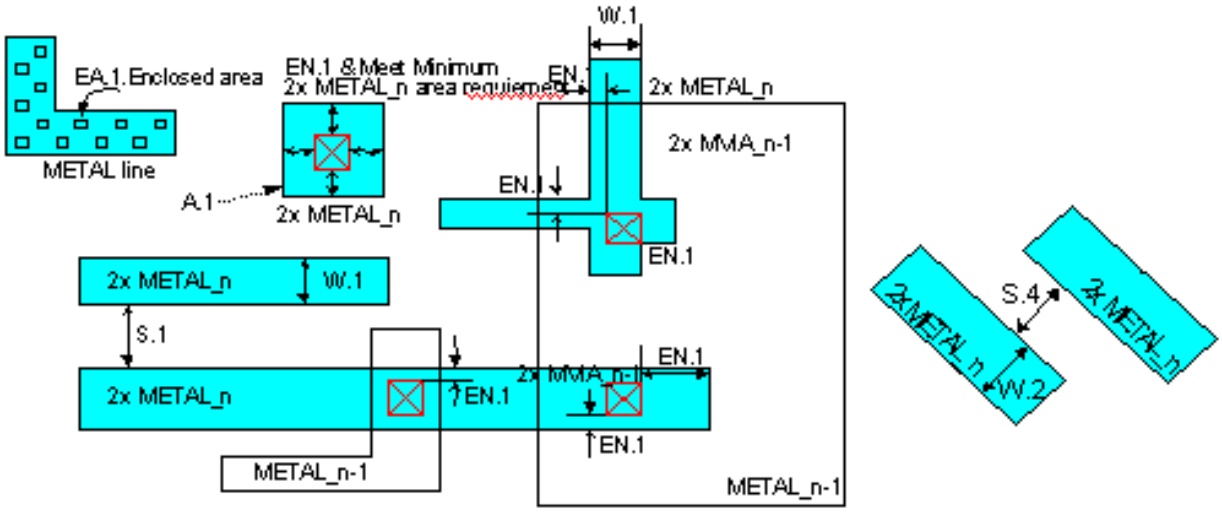
(unit : um)

Rule No.	Description	Label		Rule
2XMn.W1	METAL_n width (n=7,8)	W.1	≧	0.20
2XMn.WX	METAL_n maximum width (n=7,8) (Note1)		≦	12.00
2XMn.S1	Spacing and notch of METAL_n (n=7,8)	S.1	≧	0.20
2XMn.S2	Spacing and notch of METAL_n to [METAL_n with width > 2um] for common run length >1.5um		≧	0.35
2XMn.S3	Spacing and notch of METAL_n to [METAL_n with width > 8 um] for common run length >4.5um		≧	0.84
2XMn-2XVm.EN1	METAL_n enclosure of MVIA_n-1 (n=7,8)	EN.1	≧	0
2XMn.A1	METAL_n area (n=7,8)	A.1	≧	0.10
2XMn.EA1	METAL_n enclosed area (n=7,8)	EA.1	≧	0.31
2XMn.D	METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7, ***8***)		≧	15%
2XMn.D1	METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)		≦	80%
2XMn.W2	Width of 45 degree METAL	W.2	≧	0.40
2XMn.S4	Spacing of 45 degree METAL	S.4	≧	0.40
2XMn. R1	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area ,CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area ,CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.

8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.



The following layers are for customer 2x pitch metal Dummy (n=3~8), METALn_CUSTOMER_DUMMY (GDS no: 74(8), 75(8), 76(8), 77(8), 78(8), 79(8))

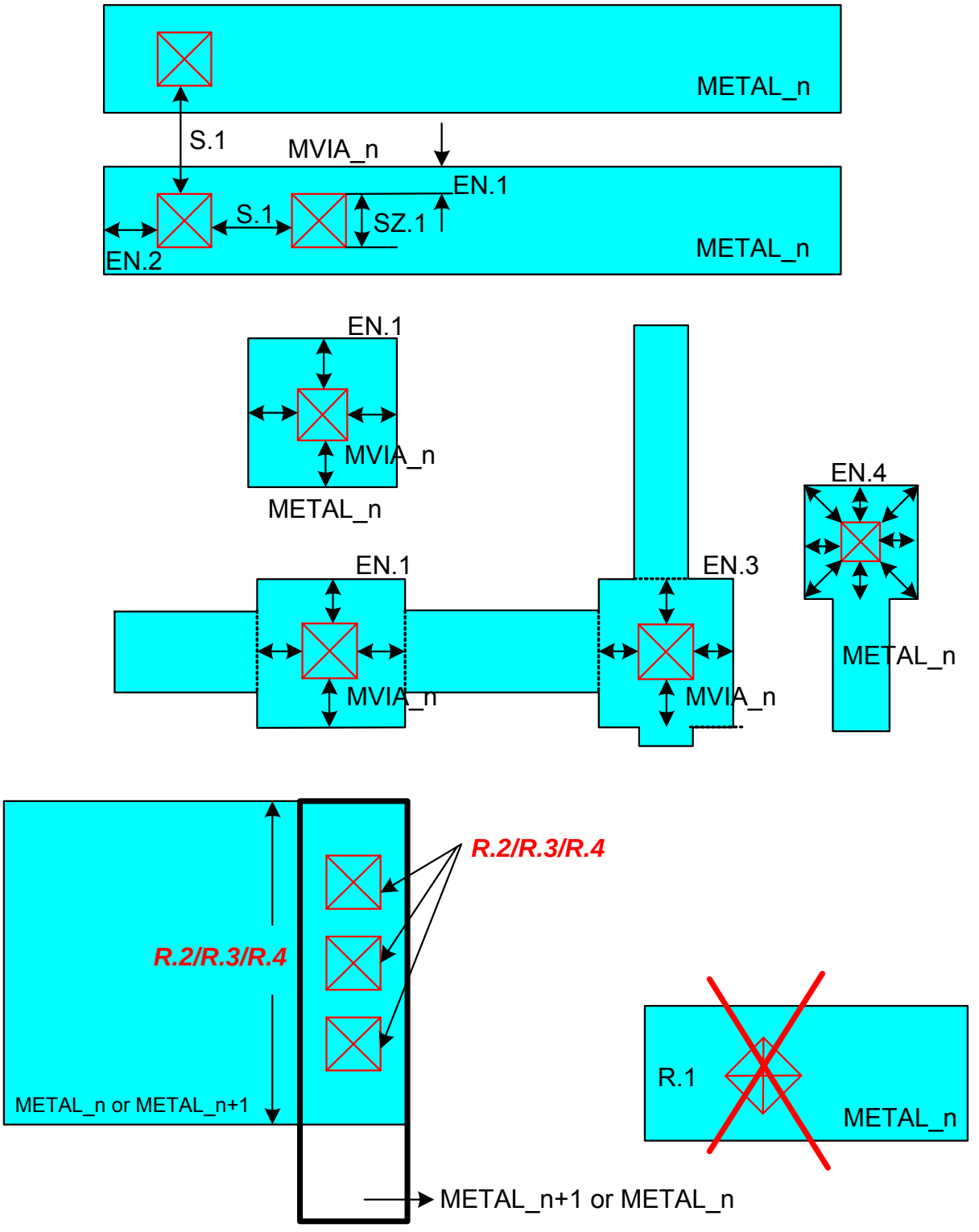
Rule No.	Description	Label		Rule
2XMnDM.L1	METALn_CUSTOMER_DUMMY length		=	1.2~12
2XMnDM.W2	METALn_CUSTOMER_DUMMY width		=	1.2~12
2XMnDM.S5	Spacing of METALn_CUSTOMER_DUMMY		≧	0.6
2XMnDM-Mn.S6	Spacing of METALn_CUSTOMER_DUMMY to METAL_n		≧	0.6
2XMnDM-MnDMBK.S7	Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY_BLOCK		≧	0.8
2XMnDM-IND.S8	Spacing of METALn_CUSTOMER_DUMMY to IND		≧	0.8
2XMnDM-FM.S9	Spacing of METALn_CUSTOMER_DUMMY to FUSE_MARK		≧	0.8
2XMnDM-PM.S10	Spacing of METALn_CUSTOMER_DUMMY to PAD_MARK		≧	0.8
2XMnDM-SRM.S11	Spacing of METALn_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	0.8

4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6,7)

(Maximum 2 levels of 2X pitch MVIA)

(unit : um)

Rule No.	Description	Label		Rule
2XVn.SZ1	Exact MVIA_n size (n=6,7)	SZ.1	=	0.20X0.20
2XVn.S1	Spacing of MVIA_n (n=6,7)	S.1	≧	0.20
Mn-2XVn.EN1	1X METAL_n or 2X METAL_n enclosure of MVIA_n(n=6,7) (excluding MIMBP layer)	EN.1	≧	0
Mn -2XVn.EN2	1X METAL_n or 2X METAL_n line end enclosure of MVIA_n	EN.2	≧	0.03
Mn -2XVn.EN3	1X METAL_n or 2X METAL_n line end enclosure of MVIA_n (for two adjacent sides, at least one side should be treated as metal line end)	EN.3	≧	0.03
Mn -2XVn.EN4	1X METAL_n or 2X METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides, if Mn-2XVn.EN2 is not fulfilled	EN.4	≧	0.02
2XVn.R1	All 2XMVIA_n shapes must be orthogonal except LOGO area. 2XMVIA_n_BAR is only allowed in die seal ring and fuse area.	R.1		Yes
2XVn.R2	A minimum of 2 MVIA_n at a spacing ≦ 0.6um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.0um wide (excluding SEAL_RING_MARK layer)	R.2		Yes
2XVn.R3	A minimum of 3 MVIA_n at a spacing ≦ 0.6um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.4um wide	R.3		Yes
2XVn.R4	A minimum of 4 MVIA_n at a spacing ≦ 0.6um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 3.0um wide	R.4		Yes
2XVn.R5	MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…n-1 and CONTACT			Yes


METAL_n
S.1
MVIA_n
EN.1
S.1
SZ.1
EN.2
METAL_n
EN.1
MVIA_n
METAL_n
EN.1
EN.3
MVIA_n
MVIA_n
EN.4
METAL_n
R.2/R.3/R.4
R.2/R.3/R.4
METAL_n or METAL_n+1
R.1
METAL_n
METAL_n+1 or METAL_n

4B.a.5 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules

4B.a.5.1 4X pitch METAL_n (4XMn) Layer Layout Rules: (n=9, 10) (Maximum 2 levels of 4X pitch metal)

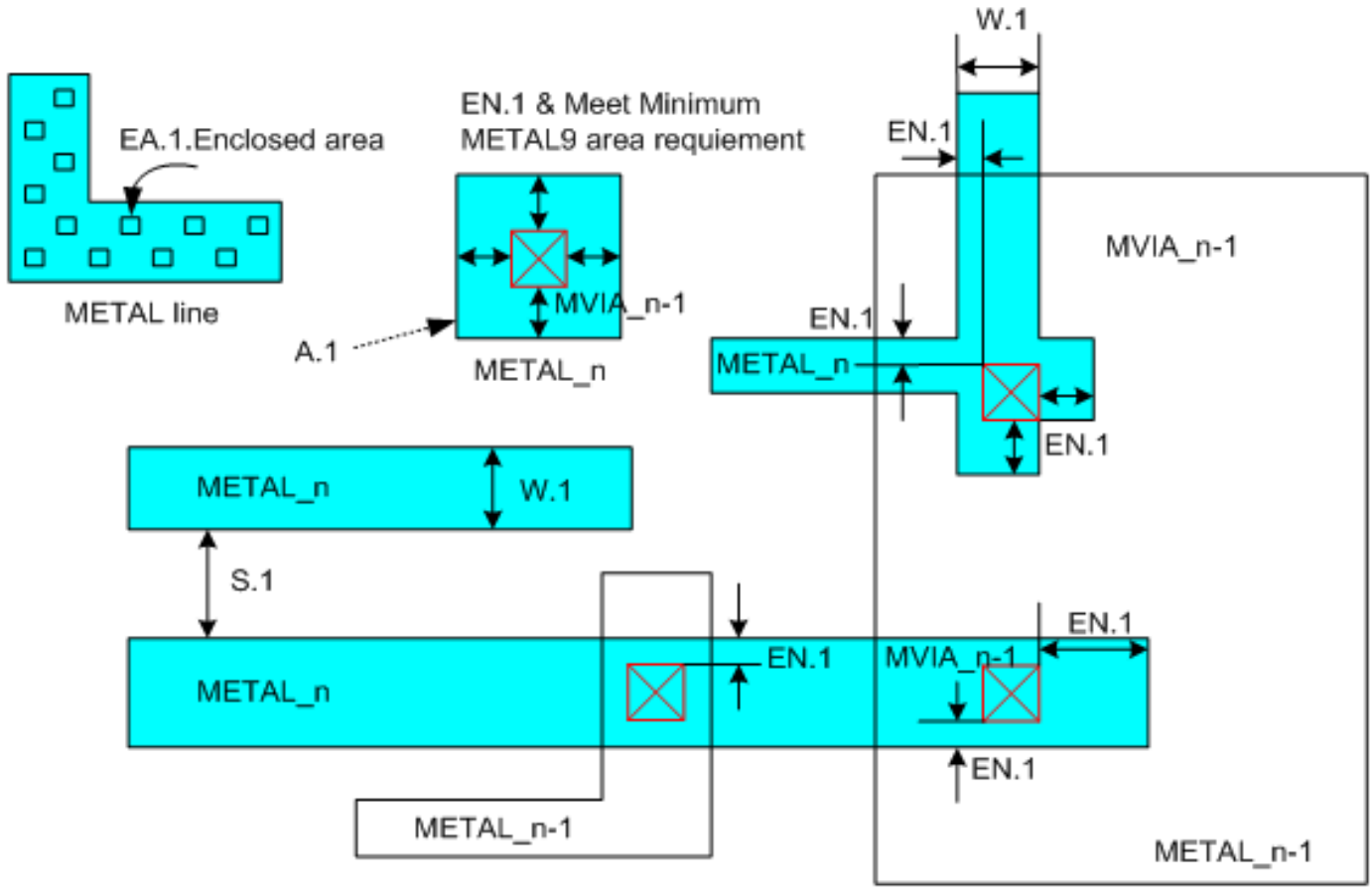
For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=9,10). For the definition of MnDMBK, please consult UMC representatives for more details about 65nm Logic Dummy for Metal Layers.

(unit : um)

Rule No.	Description	Label		Rule
4XMn.W1	METAL_n width (n=9,10)	W.1	≧	0.40
4XMn.WX	METAL_n maximum width (n=9,10) (NOTE1)		≦	12.00
4XMn.S1	Spacing and notch of METAL_n (n=9,10)	S.1	≧	0.40
4XMn.S2	Spacing and notch of METAL_n to [METAL_n with width > 4.60um] (n=9,10)		≧	0.92
4XMn-4XVm.EN1	METAL_n enclosure of MVIA_n-1 (n=9,10)	EN.1	≧	0
4XMn.A1	METAL_n area (n=9,10)	A.1	≧	0.33
4XMn.EA1	METAL_n enclosed area (n=9,10)	EA.1	≧	0.87
4XMn.D	METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7, 8)		≧	15%
4XMn.D1	METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)		≦	80%
4XMn.R1	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area, CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area ,CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.
8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.



The following layers are for customer 4x pitch metal Dummy (n=4~10), METALn_CUSTOMER_DUMMY (GDS no: 75(8), 76(8), 77(8), 78(8), 79(8), 80(8), 84(8))

Rule No.	Description	Label		Rule
4XMnDM.L1	METALn_CUSTOMER_DUMMY length		=	1.2~12
4XMnDM.W2	METALn_CUSTOMER_DUMMY width		=	1.2~12
4XMnDM.S3	Spacing of METALn_CUSTOMER_DUMMY		≧	0.6
4XMnDM-Mn.S4	Spacing of METALn_CUSTOMER_DUMMY to METAL_n		≧	0.6
4XMnDM-MnDMBK.S5	Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY_BLOCK		≧	0.8
4XMnDM-IND.S6	Spacing of METALn_CUSTOMER_DUMMY to IND		≧	0.8
4XMnDM-FM.S7	Spacing of METALn_CUSTOMER_DUMMY to FUSE_MARK		≧	0.8
4XMnDM-PM.S8	Spacing of METALn_CUSTOMER_DUMMY to PAD_MARK		≧	0.8
4XMnDM-SRM.S9	Spacing of METALn_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	0.8

4B.a.5.2 32.5KA thickness Metal Layer (Maximum 1 level of 32.5K thickness Metal)

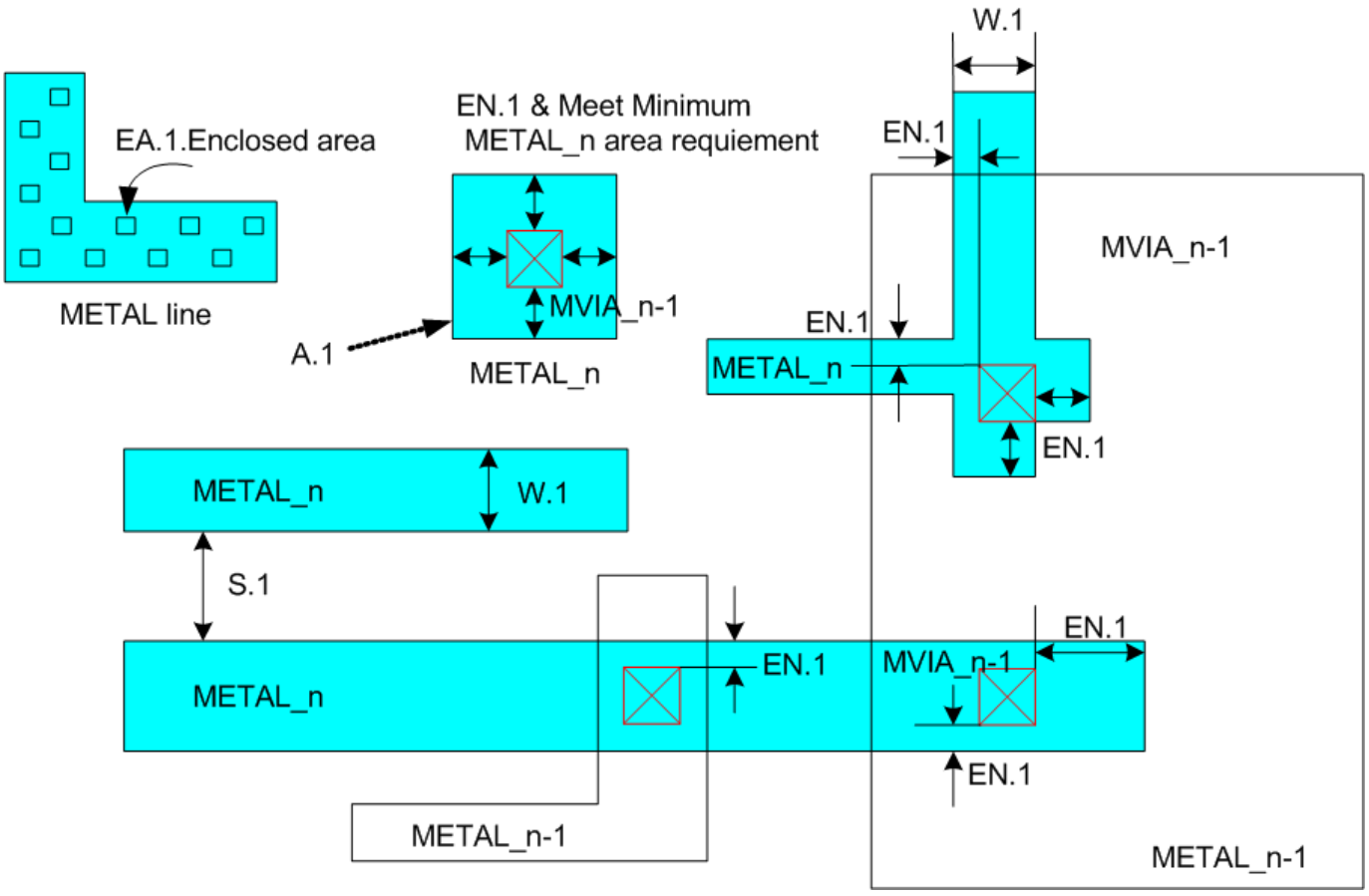
For the top metal, there are two thickness options: 8KA and 32.5KA Cu process. Inductor also can be designed by using 32.5KA top metal to improve the Q factor. The layout example will be provided with UMC 65nm design kit or 65nm UMC Cadence MM/RF FDK. For the product with thickness of 32.5KA top metal, please refer to the mask tooling information for details.

(unit: um)

Rule No.	Description	Label		Rule
325KA Mn.W1	32.5KA METAL_n width (n= for all applicable n)	W.1	≧	2
325KA Mn.WX	32.5KA METAL_n maximum width (n= for all applicable n) (NOTE1)		≦	12.00
325KA Mn.S1	Spacing and notch of 32.5KA METAL_n (n= for all applicable n)	S.1	≧	2
325KA Mn-325KA Vm.EN1	32.5KA METAL_n enclosure of 32.5KA MVIA_n-1(n= for all applicable n)	EN.1	≧	0.5
325KA Mn.A1	32.5KA METAL_n area (n= for all applicable n)	A.1	≧	9
325KA Mn.EA1	32.5KA METAL_n enclosed area (n= for all applicable n)	EA.1	≧	9
325KA Mn.D	32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7, 8)		≧	15%
325KA Mn.D1	32.5KA METAL_n (n= for all applicable n) density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 7)		≦	80%
325KAMn.R1	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.
8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.



The following layers are for customer 32.5KA Thickness pitch metal Dummy (n=4~10),

METALn_CUSTOMER_DUMMY (GDS no: 75(8), 76(8), 77(8), 78(8), 79(8), 80(8), 84(8))

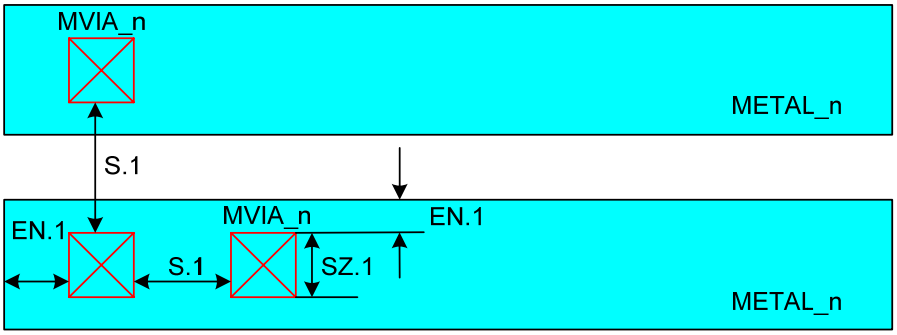
Rule No.	Description	Label		Rule
32.5KAMnDM.L1	METALn_CUSTOMER_DUMMY length		=	3.6~12
32.5KAMnDM.W2	METALn_CUSTOMER_DUMMY width		=	3.6~12
32.5KAMnDM.S2	Spacing of METALn_CUSTOMER_DUMMY		≧	2
32.5KAMnDM-Mn.S3	Spacing of METALn_CUSTOMER_DUMMY to METALn		≧	2.4
32.5KAMnDM-MnDMBK.S4	Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY_BLOCK		≧	2.4
32.5KAMnDM-IND.S5	Spacing of METALn_CUSTOMER_DUMMY to IND		≧	2.4
32.5KAMnDM-FM.S6	Spacing of METALn_CUSTOMER_DUMMY to FUSE_MARK		≧	2.4
32.5KAMnDM-PM.S7	Spacing of METALn_CUSTOMER_DUMMY to PAD_MARK		≧	2.4
32.5KAMnDM-SRM.S8	Spacing of METALn_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	2.4

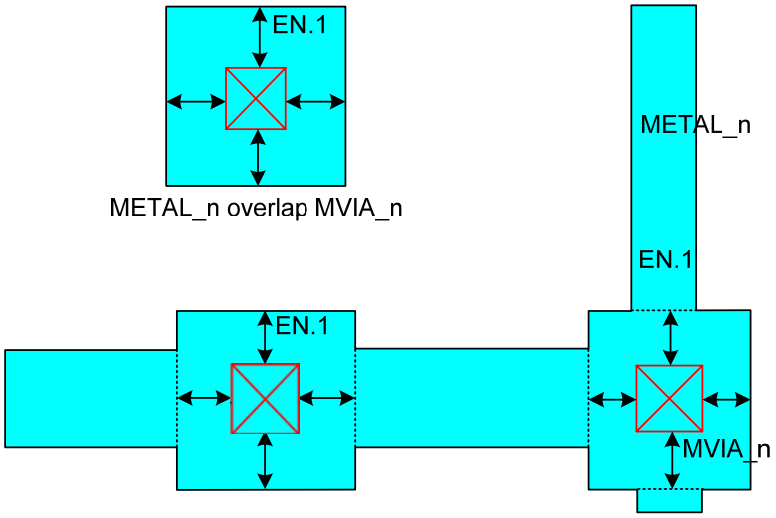
4B.a.6 4X pitch MVIA_n (4XVn)/ 32.5KA MVIA Layer Layout Rules

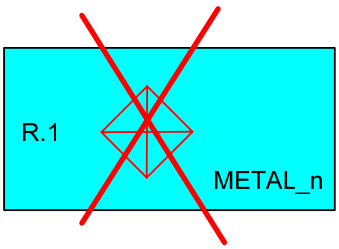
4B.a.6.1 4X pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9) (Maximum 2 levels of 4X pitch MVIA)

(unit: um)

Rule No.	Description	Label		Rule
4XVn.SZ1	Exact MVIA_n size (n=8,9)	SZ.1	=	0.4X0.4
4XVn.S1	Spacing of MVIA_n(n=8,9)	S.1	≧	0.4
Mn-4XVn.EN1	1X METAL_n or 2X METAL_n or 4X METAL_n enclosure of MVIA_n (n=8,9)	EN.1	≧	0
4XVn.R1	All 4XMVIA_n shapes must be orthogonal except LOGO area. 4xMVIA_n_BAR is only allowed in die seal ring and fuse area.	R.1		Yes
4XVn.R2	MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…n-1 and CONTACT			Yes





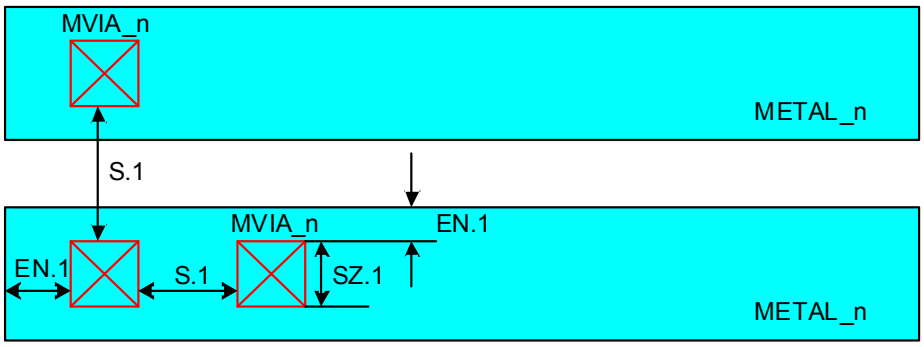


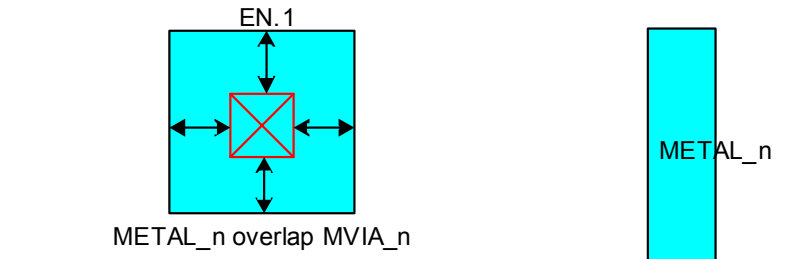
4B.a.6.2 32.5KA MVIA Layer (Maximum 1 level of 32.5KA MVIA)

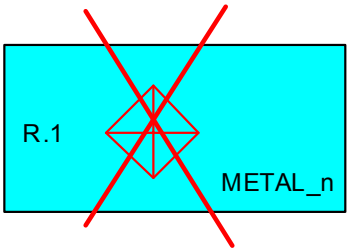
When using the 32.5KA thickness Metal, it must use specified 32.5KA MVIA for process stability.

(unit: um)

Rule No.	Description	Label		Rule
325KA Vn.SZ1	Exact 32.5KA MVIA_n size (n= for all applicable n)	SZ.1	=	0.6X0.6
325KA Vn.S1	Spacing of 32.5KA MVIA_n (n= for all applicable n)	S.1	≧	0.75
Mn_325KA Vn.EN1	METAL_n enclosure of 32.5KA MVIA_n(n= for all applicable n)	EN.1	≧	0.2
325KA Vn.R1	All 32.5KA MVIA_n shapes must be orthogonal except LOGO area. 32.5KA MVIA_n_BAR is only allowed in die seal ring.	R.1		Yes
325KA Vn.R2	32.5KA MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…n-1 and CONTACT(n= for all applicable n)			Yes







4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure

This spec establishes the PAD layout guidelines for wire bonding ONLY. Because packaging requirements vary widely across the industry, the rules defined here are applicable only to UMC's package subcontractors – ASE & SPIL . If customers want to use other assembly houses, UMC strongly suggest that they should get sufficient information from their designated assembly houses and probing subcontractors.

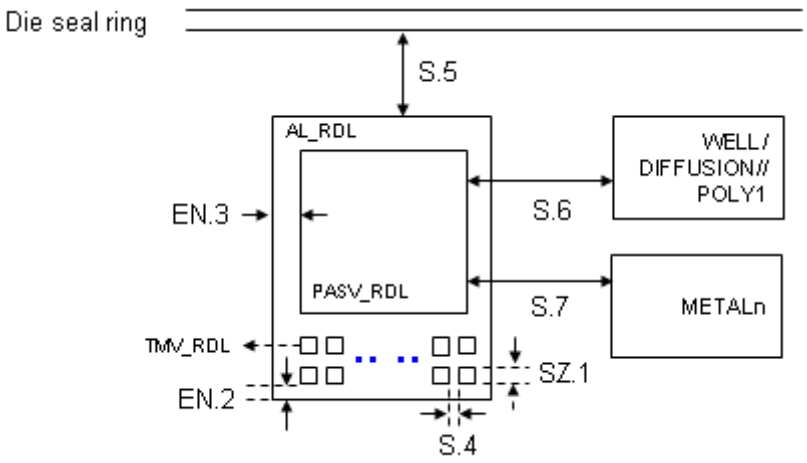
These rules are applicable for BGA- & QFP-type packaging. If customers need to apply it to thin profile packaging or other packaging types, they should confirm with their designated assembly houses and probing subcontractors in advance.

4B.a.7.1 Generic Wirebond Pad Layout Rules

UMC offers BOAC (Bonding Over Active Circuit) for wire bonding structure. Refer to Spec. No.: "G-03B-GENERATION65N-TLR/BOAC".
UMC defines Generic Wirebond Pad Layout Rules by rules including all in Section “Bond Pad Layout Rules” of Spec. No.: "G-03B-GENERATION65N-TLR/BOAC" and the following rules associating pad components and environment.

If Customers design wirebond in CLVS (Copper Line and Via Support Structure) structure instead, refer to “4B.a.7.2 Copper Line and Via Support Structure (CLVS) Layout Rules”. Generic Wirebond Pad Layout Rules must be followed for this structure.

Rule No.	Description	Label		Rule
L1.SZ1	Exact TMV_RDL size	SZ.1	=	4x4
L1.S4	Spacing of TMV_RDL	S.4	≧	2
L2-DSR.S5	Spacing of AL_RDL to die seal ring	S.5	≧	3
L3-WELL.S6	Spacing of PASV_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule)	S.6	≧	12
L3-Mn.S7	Spacing of PASV_RDL to unrelated METALn (n=1~10) (BOAC and die seal ring are excluded from this rule)	S.7	≧	5
L2-L1.EN2	AL_RDL enclosure of terminal TMV_RDL	EN.2	≧	0.5
L2-L3.EN3	AL_RDL enclosure of PASV_RDL	EN.3	≧	2
AC.S	Spacing of active circuit (DIFFUSION, POLY1, METALn, n= 1,2,3,4,5,6,7,8,9,10) to die seal ring		≧	3
L2.S8	Spacing of corner pad center to center when one side pad to die seal ring corner ≦ 150um	S.8	≧	100

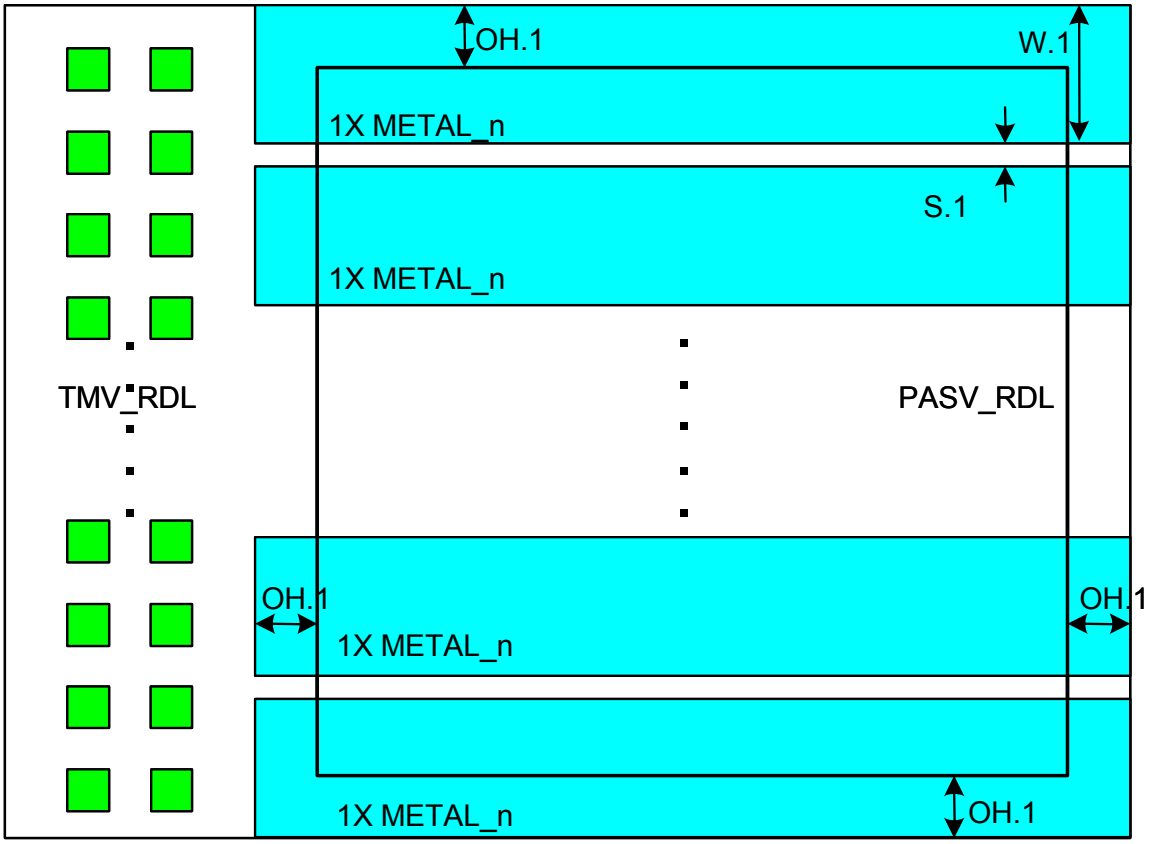


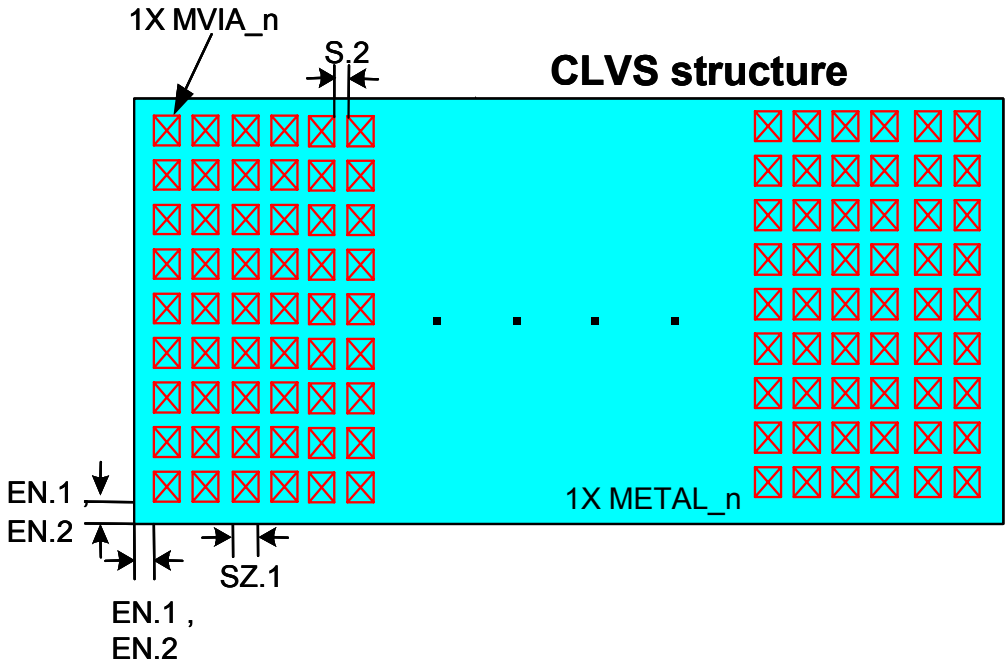
4B.a.7.2 Copper Line and Via Support Structure (CLVS) Layout Rules

The CLVS structure is used only for the mechanical support of the wirebond pad. DRC check will exclude “CAD_BOAC_MARK” with the GDS number 90(1).Thus, no interconnection using CLVS is allowed. The CLVS structure is required in all low-k dielectric levels. No CLVS structure is allowed in the oxide dielectric levels. As Metal Dummy (MnDummy) is required for every design in 65nm generation, one must add metal dummy block (MnDMBK) to the bond pads at all metal layers used. Please refer to the 65nm MASK TOOLING INFORMATION for details. 65nm bond pad structure consists of both transfer pad (L1/L2/L3) and metal pad (M1 and 1x Metal in low-k).A "Pad area mark layer", with the GDS number 90(0), also needs to be drawn on each pad for DRC check will exclude metal density check within bonding pad area. This mark layer size is the same as the Al pad size.

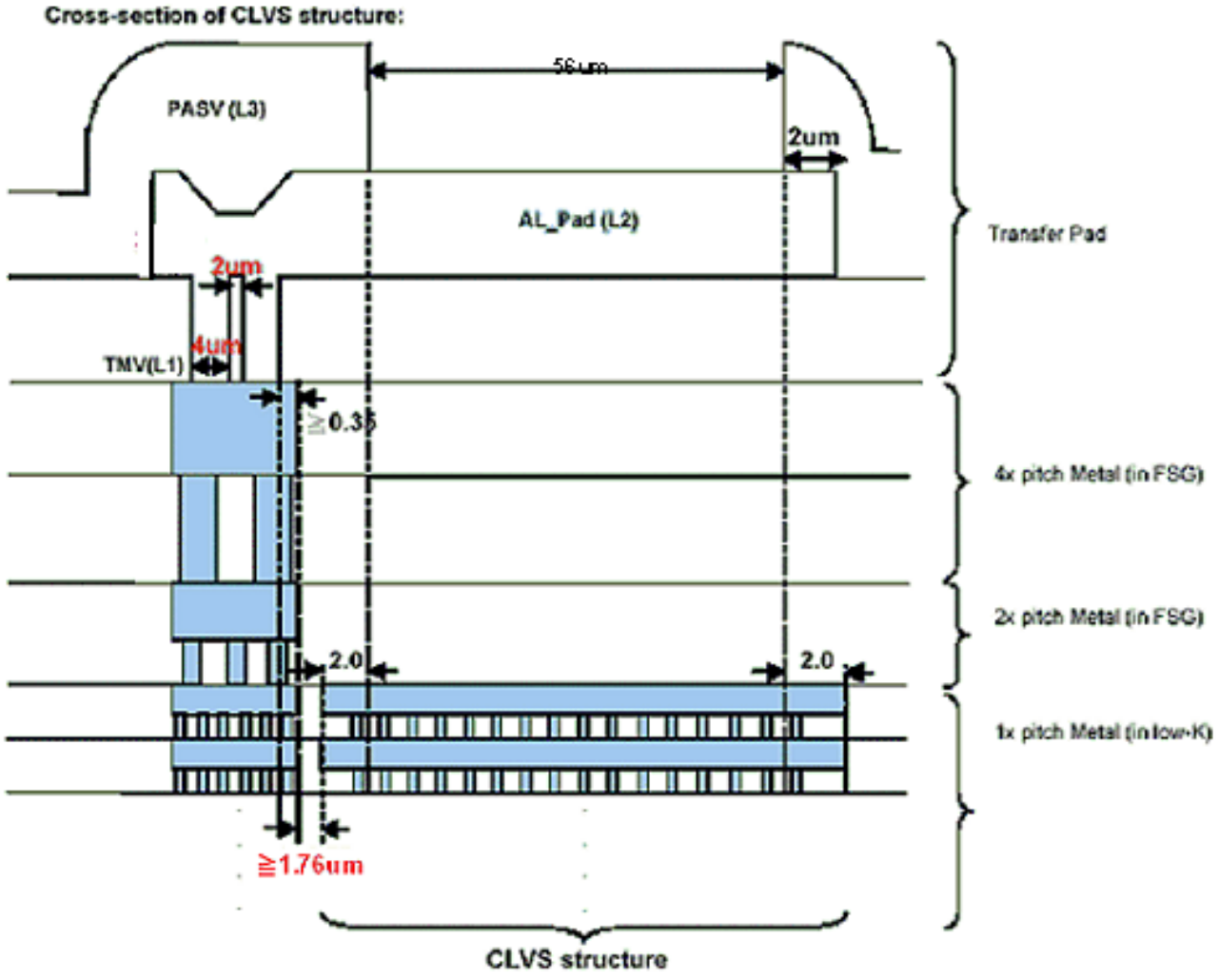
(unit: um)

Rule No.	Description	Label		Rule
1XMn.W1.CLVS	Exact 1x pitch METAL width under PASV_RDL at least in one direction	W.1	=	2.42
1XMn.S1.CLVS	1x pitch METAL spacing under PASV_RDL	S.1	≧	0.35
1XMn.SX.CLVS	1x pitch METAL spacing under PASV_RDL		≦	0.96
1XMn-L3.OH1.CLVS	Exact 1x pitch METAL overhang PASV_RDL	OH.1	=	2.00
1XMn-1XVm.EN1.CLVS	1x pitch METAL_n enclosure of MVIA_n-1 in CLVS structure	EN.1	≧	0.02
1XMn-1XVn.EN2.CLVS	1x pitch METAL_n enclosure of MVIA_n in CLVS structure	EN.2	≧	0.02
1XVn.SZ1.CLVS	Exact 1x pitch MVIA size in CLVS structure	SZ.1	=	0.10x0.10
1XVn.S2.CLVS	1x pitch MVIA spacing in CLVS structure	S.2	≧	0.14
Mn.D.CLVS	MVIA_n density under pad open area		≧	12%
CLVS.R	2x, 4x pitch METAL & MVIA in oxide under PASV_RDL of wirebond pad are not allowed to contain CLVS structures			Yes


OH.1
W.1
1X METAL_n
S.1
1X METAL_n
TMV_RDL
PASV_RDL
OH.1
OH.1
1X METAL_n
1X METAL_n
OH.1


1X MVIA_n
S.2
CLVS structure
EN.1
EN.2
SZ.1
EN.1 ,
EN.2
1X METAL_n

Cross-section of CLVS structure :



4B.a.8 Flip Chip Layout Rules

Flip Chip Layout Design Guideline please refer to "G-03FC-GENERATION65N-TLR/FLIP_CHIP"

4B.a.9 BEOL METAL/MVIA Layer Options

To restrict the number of possible BEOL schemes, the following BEOL options are the only ones allowed for usage. Any deviations must be approved by the Design Manual owner and the manufacturing fab. Customers should contact UMC to confirm if the packaging options for the intended BEOL stack have been qualified. For products without metal fuses, L3 layer (PASV_RDL layer) is used for the last mask to define Al-pad window for wirebond wafer. For products with metal (Cu) fuses, one additional mask is required for better process margin.

Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	
1	4	1	2		1		0		M1, V1, M2, V2, M3, V3, M4
46	4	1	1		1		1		M1, V1, M2, V2, M3, V3, M4
47	4	1	2		0		1		M1, V1, M2, V2, M3, V3, M4
2	5	1	3		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5
48	5	1	2		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5
49	5	1	2		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5
50	5	1	2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
51	5	1	3		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
3	6	1	4		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
4	6	1	3		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
5	6	1	3		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
6	6	1	4		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
52	6	1	2		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
53	6	1	2		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
54	6	1	3		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
7	7	1	5		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
8	7	1	4		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
9	7	1	4		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
10	7	1	3		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
11	7	1	4		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
12	7	1	5		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
55	7	1	2		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
56	7	1	3		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
13	8	1	5		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
14	8	1	5		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
15	8	1	4		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
16	8	1	3		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
17	8	1	5		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
57	8	1	4		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
18	9	1	5		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
58	9	1	4		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
59	9	1	5		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9

Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options (continued)

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	
19	10	1	5		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9, V9, M10

Table2: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with 32.5KA top metal

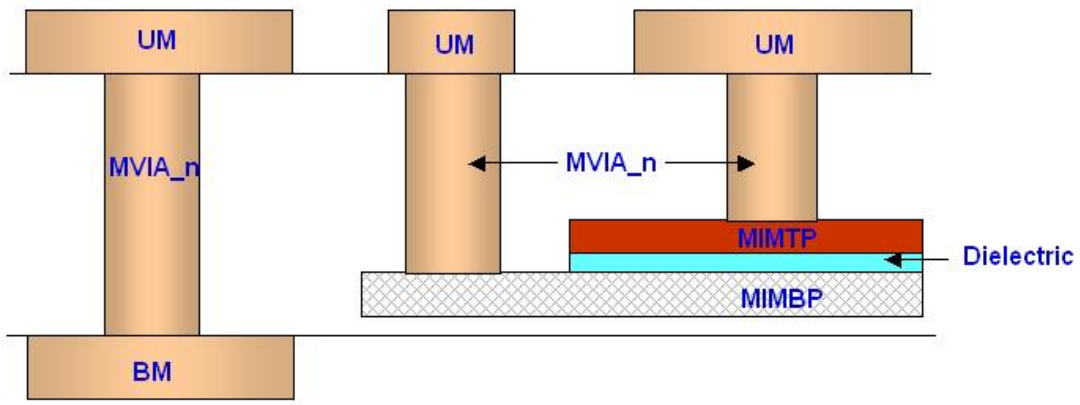
Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Ultra Thick Metal (32.5K)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	2um	0.6um	
60	4	1	2		0		0		1		M1, V1, M2, V2, M3, V3, M4
61	5	1	2		0		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
62	5	1	2		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
63	5	1	3		0		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
20	6	1	3		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
21	6	1	4		0		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
64	6	1	2		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
65	6	1	2		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
66	6	1	3		0		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
22	7	1	4		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
23	7	1	3		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
24	7	1	4		0		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
25	7	1	5		0		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
67	7	1	2		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
68	7	1	3		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
26	8	1	5		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
27	8	1	4		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
28	8	1	3		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
29	8	1	5		0		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
69	8	1	4		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
30	9	1	5		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
70	9	1	4		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
71	9	1	5		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
31	10	1	5		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9, V9, M10

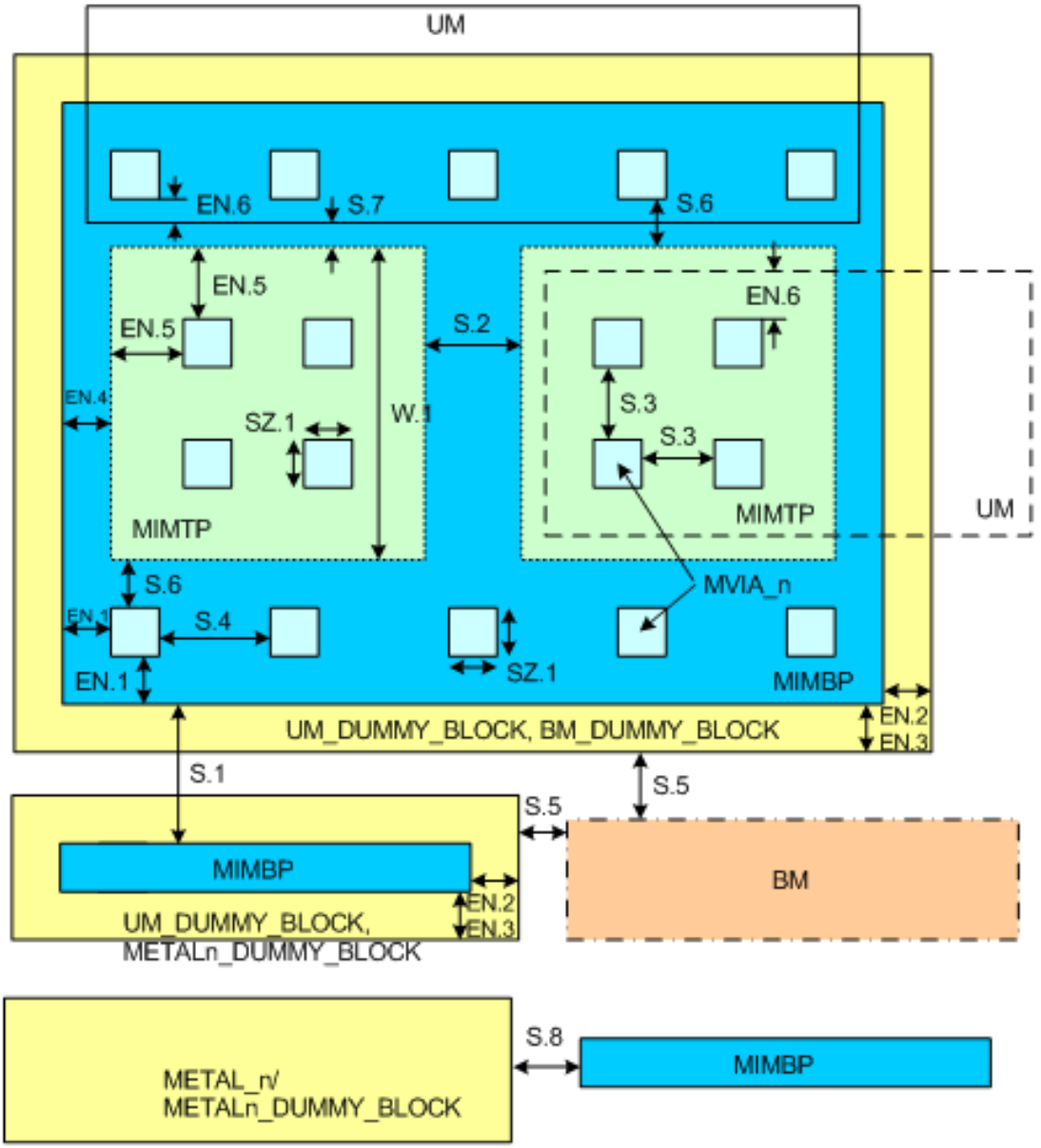
4B.a.10 BEOL Layout Rules of Mixed-Mode Specific Devices

4B.a.10.1 MIM capacitor

Metal-Insulator-Metal (MIM) capacitor is defined between Upper Metal (UM) layer and Bottom Metal (BM) layer. 2X pitch MVIA_n are needed. Three mask layers are necessary to form MIM Capacitors: One layer is an alignment mark opening (MIMAM). The other two are bottom plate (MIMBP) and top plate (MIMTP). Both plates of the capacitor are wired to UM through MVIA_n. (unit : um)

Rule No.	Description	Label		Non-strinkable	Shrinkable
MIMTP.W1	MIMTP width	W.1	≧	2.00	2.2
MIMTP.WX	MIMTP width		≦	100.00	110.00
MIMBP.S1	MIMBP spacing	S.1	≧	2.00	2.2
MIMTP.S2	MIMTP spacing	S.2	≧	0.80	0.88
2XVn-MIMTP.S3	spacing of MVIA_n over MIMTP	S.3	≧	0.88	0.96
2XVn-MIMBP.S4	spacing of MVIA_n over MIMBP	S.4	≧	0.28	0.3
BDBK-BM.S5	spacing of BM_DUMMY_BLOCK (under MIMBP) to BM	S.5	≧	0.40	0.44
2XVn-MIMTP.S6	spacing of MIMTP to MVIA_n	S.6	≧	0.30	0.33
MIMTP-UM.S7	spacing of MIMTP to UM	S.7	≧	0.30	0.33
MIMBP-UM.S8	Spacing of METAL DUMMY/METAL_n (all below MIM) to MIMBP	S.8	≧	0.40	0.44
MIMBP-2XVn.EN1	MIMBP enclosure of MVIA_n	EN.1	≧	0.30	0.33
UDBK-MIMBP.EN2	UM_DUMMY_BLOCK enclosure of MIMBP	EN.2	≧	0.40	0.44
MnBK-MIMBP.EN3	METALn_DUMMY_BLOCK (all below MIM) enclosure of MIMBP	EN.3	≧	0.40	0.44
MIMBP-MIMTP.EN4	MIMBP enclosure of MIMTP	EN.4	≧	0.40	0.44
MIMTP-2XVn.EN5	MIMTP enclosure of MVIA_n	EN.5	≧	0.28	0.3
UM-2XVn.EN6	UM (over MIMBP) enclosure of MVIA_n	EN.6	≧	0.50	0.55
MIMTP.AX	MIMTP total area per chip (mm^2)		≦	10.00	11.00
2XVn-MIMBP.SZ1	Exact MVIA_n size over MIMBP	SZ.1	=	0.2 x 0.2	0.22 x 0.22
MIM.R1	MIMBP not over MIMTP is not allowed.			YES	YES
MIM.R2	MIMBP must be within UM_DUMMY_BLOCK and BM_DUMMY_BLOCK			YES	YES
MIM.R3	MIMBP over BM is not allowed.			YES	YES
MIM.R4	All MIMBP shapes must be rectangular and orthogonal.			YES	YES
MIM.R5	All MIMTP shapes must be rectangular and orthogonal.			YES	YES
MIM.R6	MIMTP and MIMBP must touch two or more MVIA_n shapes			YES	YES
MIM.R7	METAL DUMMY /METAL_n (all below MIM) touching MIMBP are not allowed			YES	YES





*Note: Below table shows the metal layer option in which the MIM layer can be put.

Table3: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with MIM

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	
1	4	1	2		1		0		M1, V1, M2, V2, M3, MIM, V3, M4
46	4	1	1		1		1		M1, V1, M2, MIM, V2, M3, V3, M4
47	4	1	2		0		1		not support MIM
2	5	1	3		1		0		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5
48	5	1	2		2		0		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5
49	5	1	2		0		2		not support MIM
50	5	1	2		1		1		M1, V1, M2, V2, M3, MIM, V3, M4, V4, M5
51	5	1	3		0		1		not support MIM
3	6	1	4		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6
4	6	1	3		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6
5	6	1	3		1		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5, V5, M6
6	6	1	4		0		1		not support MIM
52	6	1	2		2		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5,V5, M6
53	6	1	2		1		2		M1, V1, M2, V2, M3, MIM, V3, M4, V4, M5,V5, M6
54	6	1	3		0		2		not support MIM
7	7	1	5		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7
8	7	1	4		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7
9	7	1	4		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7
10	7	1	3		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7
11	7	1	4		0		2		not support MIM
12	7	1	5		0		1		not support MIM
55	7	1	2		2		2		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5, V5, M6, V6, M7
56	7	1	3		1		2		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5, V5, M6, V6, M7
13	8	1	5		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, MIM, V7, M8
14	8	1	5		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8
15	8	1	4		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8
16	8	1	3		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7, V7, M8
17	8	1	5		0		2		not support MIM
57	8	1	4		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7, V7, M8
18	9	1	5		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, MIM, V7, M8, V8, M9
58	9	1	4		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8, V8, M9
59	9	1	5		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8, V8, M9

Table3: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with MIM (continued)

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	
19	10	1	5		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, MIM, V7, M8, V8, M9, V9, M10

Table4: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with 32.5KA top metal and MIM

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Thin Metal (4X)		Ultra Thick Metal (32.5K)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	2um	0.6um	
60	4	1	2		0		0		1		not support MIM
61	5	1	2		0		1		1		not support MIM
62	5	1	2		1		0		1		M1, V1, M2, V2, M3, MIM, V3, M4, V4, M5
63	5	1	3		0		0		1		not support MIM
20	6	1	3		1		0		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5,V5, M6
21	6	1	4		0		0		1		not support MIM
64	6	1	2		2		0		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5,V5, M6
65	6	1	2		1		1		1		M1, V1, M2, V2, M3, MIM, V3, M4, V4, M5,V5, M6
66	6	1	3		0		1		1		not support MIM
22	7	1	4		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7
23	7	1	3		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7
24	7	1	4		0		1		1		not support MIM
25	7	1	5		0		0		1		not support MIM
67	7	1	2		2		1		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5, V5, M6, V6, M7
68	7	1	3		1		1		1		M1, V1, M2, V2, M3, V3, M4, MIM, V4, M5, V5, M6, V6, M7
26	8	1	5		1		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8
27	8	1	4		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8
28	8	1	3		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7, V7, M8
29	8	1	5		0		1		1		not support MIM
69	8	1	4		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, MIM, V5, M6, V6, M7, V7, M8
30	9	1	5		2		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, MIM, V7, M8, V8, M9
70	9	1	4		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8, V8, M9
71	9	1	5		1		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, MIM, V6, M7, V7, M8, V8, M9
31	10	1	5		2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, MIM, V7, M8, V8, M9, V9, M10

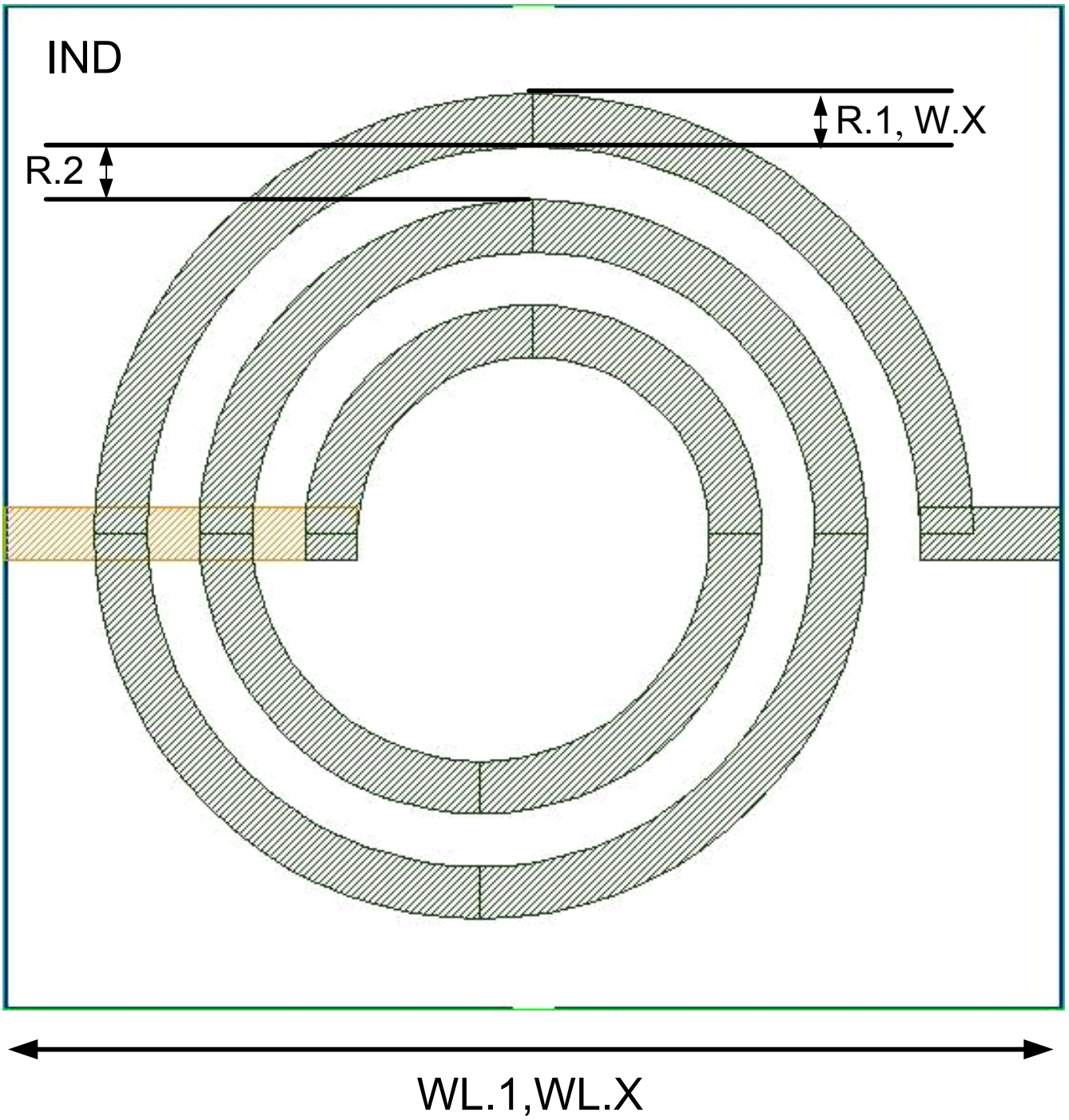
*Note: The MIM is located below the last 2XVia layer.

4B.a.10.2 INDUCTOR (Non-tooling)

For INDUCTOR application, one additional drawing layer, IND, will be necessary for mask generation and DRC check. UMC standard tape out flow will use IND layer to exclude P_WELL implant and POLY1/METAL dummy insertion. If customer's product doesn't follow UMC official IND application, customer must individually handle P_WELL mask, POLY1/METAL dummy generation for their IND design.

(unit : um)

Rule No.	Description	Label		Rule
IND.WX	width of 1x, 2x, 4x, 32.5KA METAL width within IND	W.X	≦	12.00
IND.WL	IND width & length	WL.1	≧	30.00
IND.WLX	IND width & length	WL.X	≦	430.00
IND.R1	width of 1x, 2x, 4x, 32.5KA METAL within IND must refer to BEOL layout rule	R.1		Yes
IND.R2	spacing of 1x, 2x, 4x, 32.5KA METAL within IND must refer to BEOL layout rule	R.2		Yes
IND.R3	1x pitch MVIA Rule within IND must refer to BEOL layout rule			Yes
IND.R4	2x pitch MVIA Rule within IND must refer to BEOL layout rule			Yes
IND.R5	4x pitch/32.5KA MVIA Rule within IND must refer to BEOL layout rule			Yes
IND.R7	Circular metal regions are allowed inside IND.			Yes
IND.R8	Metal edges that intersect at acute angles greater than 80° inside IND (i.e. inductor line begin/end) are excluded from metal width design rule check.			Yes
IND.R9	Gate under IND is not allowed.			Yes
IND.R10	TMV_RDL (L1) within IND must follow the layout rules in Section 7.2			Yes
IND.R11	AL_RDL (L2) within IND must follow the layout rules in Section 7.2			Yes



4B.a.10.3 Mesh MOM Capacitor

There are special 1xpitch METAL_n (n=2,3,4,5,6) rules for mesh MOM capacitor;
please refer to Spec. No.: G-03M-GENERATION65N-TLR/MOM

4B.b Option1: 1P10M2T2H (1x, 2x, 6x Metal)

Auto-metal slot generation will not be provided for L65 process. Customers should follow metal maximum width and density criteria during layout. If customers would like to create slots in metals, please use normal metal layer to layout holes or slots in metal and do not use METALn_CUSTOMER_SLOT layers. METALn_CUSTOMER_SLOT layers are not allowed except CAD_WAT_PAD_MARK area.

4B.b.1 1x pitch METAL Layers: (Maximum 6 levels of thin 1x pitch METAL)

Please refer to section ”4B.a.1 1x pitch METAL Layers”.

4B.b.2 1x pitch MVIA Layers: (Maximum 5 levels of thin 1x pitch MVIA)

Please refer to section ”4B.a.2 1x pitch MVIA Layers”

4B.b.3 2X pitch METAL_n (2XMn) Layer Layout Rules: (n=7, 8)

Please refer to section ”4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules”

4B.b.4 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6, 7)

(Maximum 2 levels of 2X pitch MVIA)

Please refer to section ”4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules”

4B.b.5 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10)

(Maximum 2 levels of 6X pitch metal)

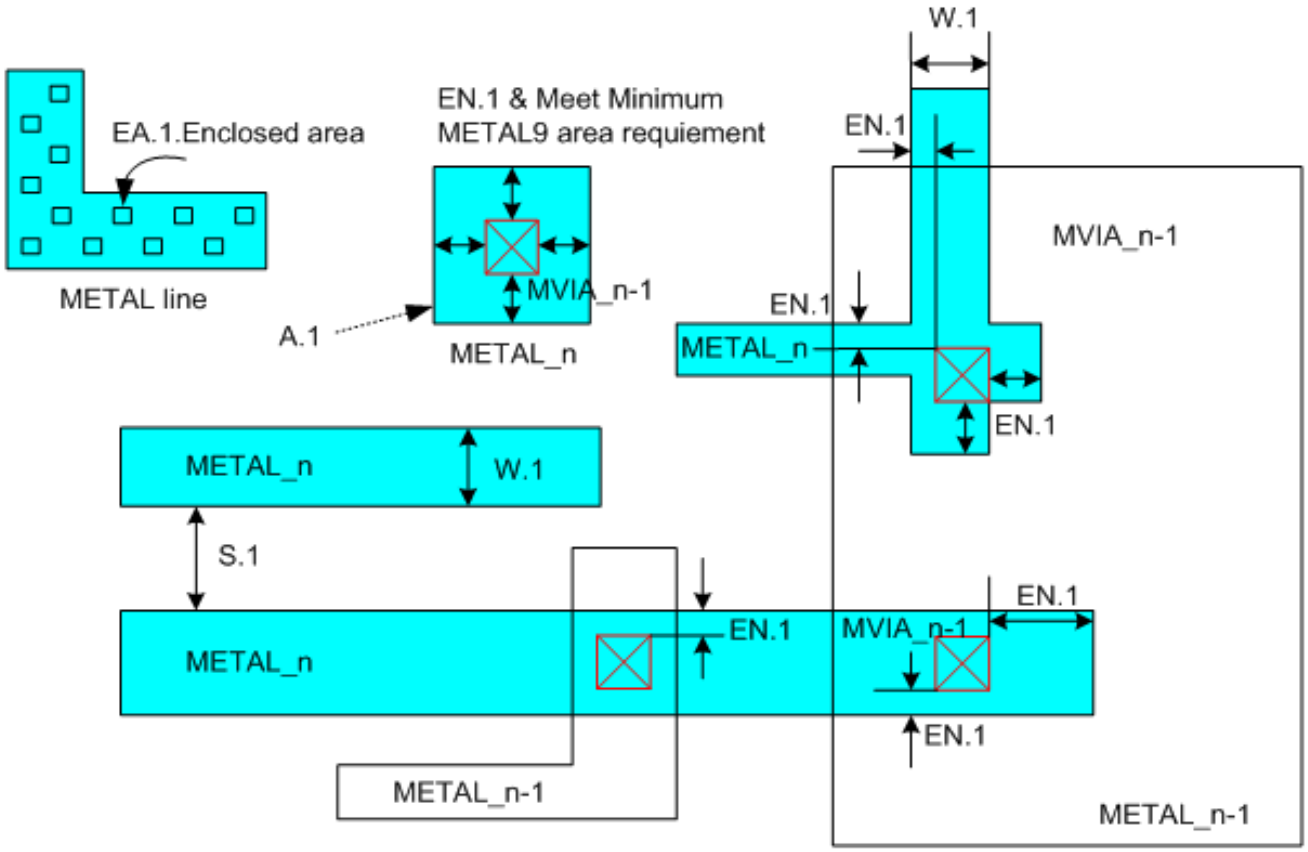
For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=9,10). For the definition of MnDMBK, please consult UMC representatives for more details about 65nm Logic Dummy for Metal Layers.

(unit: um)

Rule No.	Description	Label		Rule
6XMn.W1	METAL_n width (n=9,10)	W.1	≧	0.56
6XMn.WX	METAL_n maximum width (n=9,10) (Note1)		≦	12.00
6XMn.S1	Spacing and notch of METAL_n (n=9,10)	S.1	≧	0.56
6XMn.S2	Spacing and notch of METAL_n to [METAL_n with width > 4.60um] (n=9,10)		≧	0.92
6XMn-4XVm.EN1	METAL_n enclosure of MVIA_n-1 (n=9,10)	EN.1	≧	0.06
6XMn.A1	METAL_n area (n=9,10)	A.1	≧	0.94
6XMn.EA1	METAL_n enclosed area (n=9,10)	EA.1	≧	1.68
6XMn.D	METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (Note 5, 6, 7, 8)		≧	15%
6XMn.D1	METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)		≦	80%
6XMn.R	METALn_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area			Yes

Note

1) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area.
2) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.
3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer.
4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.
5) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, IND area and top copper metal over CAD_RF_PAD_MARK area
6) Skip rule check if violate area include top copper metal over FUSE_MARK
7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip.
8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.



The following layers are for customer 6x pitch metal Dummy (n=4~10), METALn_CUSTOMER_DUMMY (GDS no: 75(8), 76(8), 77(8), 78(8), 79(8), 80(8), 84(8))

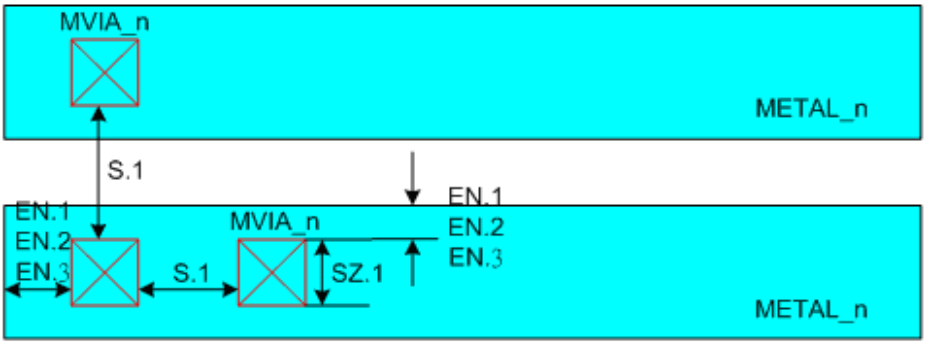
Rule No.	Description	Label		Rule
6XMnDM.L1	METALn_CUSTOMER_DUMMY length		=	1.2~12
6XMnDM.W2	METALn_CUSTOMER_DUMMY width		=	1.2~12
6XMnDM.S3	Spacing of METALn_CUSTOMER_DUMMY		≧	0.6
6XMnDM-Mn.S4	Spacing of METALn_CUSTOMER_DUMMY to METAL_n		≧	0.8
6XMnDM-MnDMBK.S5	Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY_BLOCK		≧	0.8
6XMnDM-IND.S6	Spacing of METALn_CUSTOMER_DUMMY to IND		≧	0.8
6XMnDM-FM.S7	Spacing of METALn_CUSTOMER_DUMMY to FUSE_MARK		≧	0.8
6XMnDM-PM.S8	Spacing of METALn_CUSTOMER_DUMMY to PAD_MARK		≧	0.8
6XMnDM-SRM.S9	Spacing of METALn_CUSTOMER_DUMMY to SEAL_RING_MARK		≧	0.8

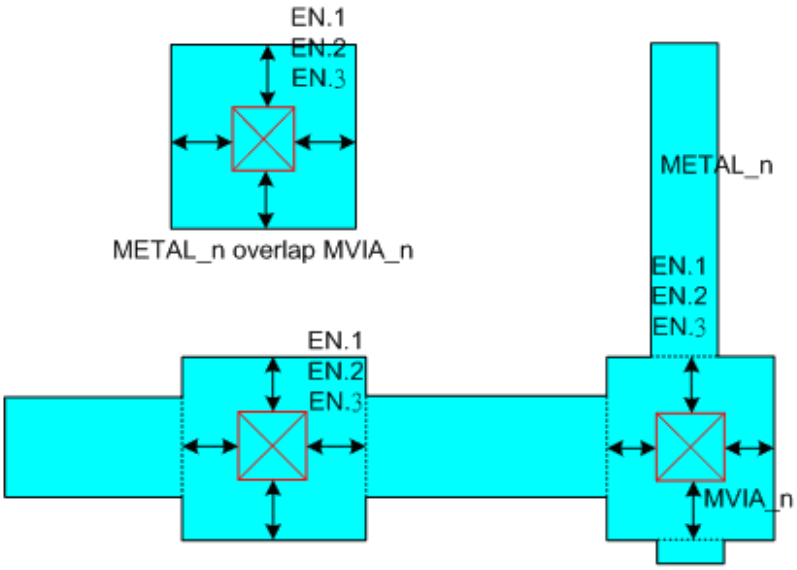
4B.b.6 4x pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9)

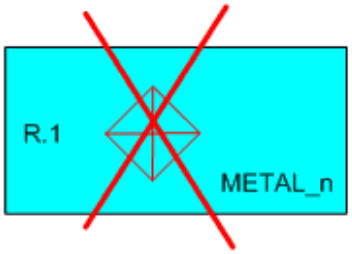
(Maximum 2 levels of 4X pitch MVIA)

(unit: um)

Rule No.	Description	Label		Rule
4XVn.SZ1	Exact MVIA_n size (n=8,9)	SZ.1	=	0.4X0.4
4XVn.S1	Spacing of MVIA_n(n=8,9)	S.1	≧	0.4
6XMn-4XVn.EN1	6x METAL_n enclosure of MVIA_n (n=8,9)	EN.1	≧	0
1XMn-4XVn.EN2	1x METAL enclosure of 4x MVIA directly above 1x METAL	EN.2	≧	0
2XMn-4XVn.EN3	2x METAL enclosure of 4x MVIA directly above 2x METAL	EN.3	≧	0
4XVn.R1	All 4xMVIA_n shapes must be orthogonal except LOGO area. 4xMVIA_n_BAR is only allowed in die seal ring and fuse area.	R.1		Yes
4XVn.R2	MVIA_n can be fully or partially stacked on MVIA_1,2,3,4…n-1 and CONTACT			Yes







4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure

Please refer to section “4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure” for all wirebond pad layout rules.

4B.b.8 Flip Chip Layout Rules

Flip Chip Layout Design Guideline please refer to "G-03FC-GENERATION65N-TLR/FLIP_CHIP"

4B.b.9 BEOL METAL/MVIA Layer Options

To restrict the number of possible BEOL schemes, the following BEOL options are the only ones allowed for usage. Any deviations must be approved by the Design Manual owner and the manufacturing fab. Customers should contact UMC to confirm if the packaging options for the intended BEOL stack have been qualified. For products without metal fuses, L3 layer (PASV_RDL layer) is used for the last mask to define Al-pad window for wirebond wafer. For products with metal (Cu) fuses, one additional mask is required for better process margin.

Table5: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options.

Option	Total Metal Layer	METAL1	Thin Metal (1X)		Thin Metal (2X)		Ultra Thick Metal (6X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.56um	0.4um	
32	4	1	2		0		1		M1, V1, M2, V2, M3, V3, M4
33	5	1	2		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
72	5	1	2		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5
73	5	1	3		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5
34	6	1	3		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
35	6	1	4		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
74	6	1	2		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
75	6	1	2		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
76	6	1	3		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6
36	7	1	4		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
37	7	1	3		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
38	7	1	4		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
39	7	1	5		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
77	7	1	2		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
78	7	1	3		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7
40	8	1	5		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
41	8	1	4		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
42	8	1	3		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
43	8	1	5		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
79	8	1	4		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8
44	9	1	5		2		1		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
80	9	1	4		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
81	9	1	5		1		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9
45	10	1	5		2		2		M1, V1, M2, V2, M3, V3, M4, V4, M5,V5, M6,V6, M7,V7, M8, V8, M9, V9, M10

4B.c Option2: 1P9M (1x, 2x, 6x Metal; with maximum 7 levels of 1x Metal)

Auto-metal slot generation will not be provided for L65 process. Customers should follow metal maximum width and density criteria during layout. If customers would like to create slots in metals, please use normal metal layer to layout holes or slots in metal and do not use METALn_CUSTOMER_SLOT layers. METALn_CUSTOMER_SLOT layers are not allowed except CAD_WAT_PAD_MARK area.

4B.c.1 1x pitch METAL Layers: (Maximum 7 levels of thin 1x pitch METAL)

Refer to section ”4B.a.1 1x pitch METAL Layers” with allowed n=7 for 1XMn.

4B.c.2 1x pitch MVIA Layers: (Maximum 6 levels of thin 1x pitch MVIA)

Refer to section ”4B.a.2 1x pitch MVIA Layers”

4B.c.3 2X pitch METAL_n (2XMn) Layer Layout Rules: (n=8, 9)

Refer to section ”4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules”

4B.c.4 2X pitch MVIA_n (2XVn) Layer Layout Rules: (Maximum 2 levels of 2X pitch MVIA)

Refer to section ”4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules”

4B.c.5 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=8, 9)

Refer to section ”4B.b.5 6x pitch METAL_n (6XMn) Layer Layout Rules”

4B.c.6 4x pitch MVIA_n (4XVn) Layer Layout Rules: (Maximum 2 levels of 4X pitch MVIA)

Refer to section ”4B.b.6 4x pitch MVIA_n (4XVn) Layer Layout Rules”

4B.c.7 Wirebond Pad Layers, Scribe Line and Pad Structure

Refer to section ”4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure”

4B.c.8 Flip Chip Layout Rules

For Flip Chip Layout Design Guideline refer to "G-03FC-GENERATION65N-TLR/FLIP_CHIP".

4B.c.9 BEOL METAL/MVIA Layer Options

To restrict the number of possible BEOL schemes, the following BEOL options are the only ones allowed for usage. Any deviations must be approved by the Design Manual owner and the manufacturing fab. Customers should contact UMC to confirm if the packaging options for the intended BEOL stack have been qualified. For products without metal fuses, L3 layer (PASV_RDL layer) is used for the last mask to define Al-pad window for wirebond wafer. For products with metal (Cu) fuses, one additional mask is required for better process margin.

Table6: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options.

Option	Total Metal Layers	METAL1	METAL (1X)		METAL (2X)		METAL (6X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.56um	0.4um	
82	8	1	6		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8
83	8	1	6		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8
85	9	1	6		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9
86	9	1	6		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9
88	9	1	6		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9

Note: For other METAL/MVIA layer options refer to “4B.b.10 BEOL METAL/MVIA Layer Options” Table5

4B.d Option3: 1P9M (1x, 2x, 4x Metal; with maximum 7 levels of 1x Metal)

Auto-metal slot generation will not be provided for L65 process. Customers should follow metal maximum width and density criteria during layout. If customers would like to create slots in metals, please use normal metal layer to layout holes or slots in metal and do not use METALn_CUSTOMER_SLOT layers. METALn_CUSTOMER_SLOT layers are not allowed except CAD_WAT_PAD_MARK area.

4B.d.1 1x pitch METAL Layers: (Maximum 7 levels of thin 1x pitch METAL)

Refer to section ”4B.a.1 1x pitch METAL Layers” with allowed n=7 for 1XMn.

4B.d.2 1x pitch MVIA Layers: (Maximum 6 levels of thin 1x pitch MVIA)

Refer to section ”4B.a.2 1x pitch MVIA Layers”

4B.d.3 2X pitch METAL_n (2XMn) Layer Layout Rules: (n=8, 9)

Refer to section ”4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules”

4B.d.4 2X pitch MVIA_n (2XVn) Layer Layout Rules: (Maximum 2 levels of 2X pitch MVIA)

Refer to section ”4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules”

4B.d.5 4x pitch METAL_n (4XMn) Layer Layout Rules: (n=8, 9)

Refer to section ”4B.a.5 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules”

4B.d.6 4x pitch MVIA_n (4XVn) Layer Layout Rules: (Maximum 2 levels of 4X pitch MVIA)

Refer to section ”4B.b.6 4x pitch MVIA_n (4XVn) Layer Layout Rules”

4B.d.7 Wirebond Pad Layers, Scribe Line and Pad Structure

Refer to section ”4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure”

4B.d.8 Flip Chip Layout Rules

For Flip Chip Layout Design Guideline refer to "G-03FC-GENERATION65N-TLR/FLIP_CHIP".

4B.d.9 BEOL METAL/MVIA Layer Options

To restrict the number of possible BEOL schemes, the following BEOL options are the only ones allowed for usage. Any deviations must be approved by the Design Manual owner and the manufacturing fab. Customers should contact UMC to confirm if the packaging options for the intended BEOL stack have been qualified. For products without metal fuses, L3 layer (PASV_RDL layer) is used for the last mask to define Al-pad window for wirebond wafer. For products with metal (Cu) fuses, one additional mask is required for better process margin.

Table7: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options.

Option	Total Metal Layers	METAL1	METAL (1X)		METAL (2X)		METAL (4X)		Layers component in layout rules
		Line	Line	Via	Line	Via	Line	Via	
		0.09um	0.1um	0.1um	0.2um	0.2um	0.4um	0.4um	
82	8	1	6		1		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8
84	8	1	6		0		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8
85	9	1	6		2		0		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9
87	9	1	6		1		1		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9
89	9	1	6		0		2		M1, V1, M2, V2, M3, V3, M4, V4, M5, V5, M6, V6, M7, V7, M8, V8, M9

Note: For other METAL/MVIA layer options refer to “4B.a.10 BEOL METAL/MVIA Layer Options” Table1

5. Die Seal Ring Rules

Please refer to the Spec. No. G-03DSR-GENERATION65N-TLR/DIE_SEAL_RING and G-03DSR-GENERATION65N-ADV-TLR/DIE_SEAL_RING.

6. Electromigration Rules

6.A UMC platform: 1P10M2T2F

6.A.1 Electromigration Rules for Cu METAL and Cu MVIA Layers

6.A.1.1 Lifetime Criteria

The Electromigration refers to the gradual degradation of interconnects due to the combined effects of current and temperature. The following rules give designers the information needed to assure that electromigration will have a negligible impact on the product reliability
The rules as listed are based on an assumed cumulative failure rate of 0.1%, an assumed product power on life of 10 years and an assumed junction temperature of 110℃.
The failure criteria is defined as 10% of resistance increase or 1uA of extrusion leakage. Adjustment factors for other lifetime and temperatures are given. When applications are more stringent, the adjustment factor must be applied. When applications are less stringent, adjustment factors should be used only when it is absolutely certain that the designs will never be used at more stringent conditions. Rules are given to protect against two types of current induced failures: standard EM and local-heating enhanced EM.

A. Standard EM

In DC mode, the rules define a maximum DC current per unit width (Imax_dc*). At maximum Irms, the joule heating temperature $\leqq$5°K.
In AC mode, the rules are obtained by replacing the DC maximum current per unit width (Imax_dc) with the average current per unit width value (Iave*), which is obtained by averaging the current over one cycle.

B. Local-heating enhanced EM

The rules defined a maximum root mean square current, Irms*.
* Definition of Iave, Irms and design values are listed in section 8.1.2 and 8.1.3.

6.A.1.2 DC rules

Rule No.	Description	Imax_dc (at 110℃) unit
M1.EM	METAL1	1.89 mA/um
1XMn.EM	METAL2 & above 1x pitch METAL_n	2.31 mA/um
2XMn.EM	2X METAL7 and METAL8(FSG)	4.14 mA/um
4XMn.EM	4X METAL9 and METAL10(FSG)	9.2 mA/um
CT.EM	CONTACT	0.20 mA/cont
1XVn.EM	1x pitch MVIA (MVIA1 & above 1x pitch MVIA_n)	0.25 mA/via
2XVn.EM.I1	2x pitch MVIA_n (1x pitch METAL_n & 2x pitch METAL_n+1)	0.39 mA/via
2XVn.EM.I2	2x pitch MVIA_n (2x pitch METAL_n & 2x pitch METAL_n+1)	0.96 mA/via
4XVn.EM	4x pitch MVIA_n	3.91 mA/via
325KMn.EM	32.5K Top METAL10 (FSG)	30 mA/um
325KVn.EM.I1	32.5K MVIA_n (1x pitch METAL_n& 32.5K METAL_n)	8.63 mA/via
325KVn.EM.I2	32.5K MVIA_n (2x pitch METAL_n& 32.5K METAL_n)	8.63 mA/via
325KVn.EM.I3	32.5K MVIA_n (4x pitch METAL_n& 32.5K METAL_n)	8.63 mA/via

Note:
As many CONTACTs or vias as design allowed are recommended to improve reliability.

6.A.1.3 AC Rules

A. For Standard EM

Maximum allowable average current (Iave_max) per unit width or per via or contact is defined. The Iave is obtained by averaging the current over one cycle.

$$Iave \equiv \left(\int_0^{\tau} I(t)dt \quad / \tau \right)$$

Iave_max is obtained by replacing the Imax_dc defined in previous section. As in DC case, Iave rules apply to METAL, MVIA and CONTACT.

B. For Local-heating Enhanced EM

Maximum allowable root-mean-square current (Irms) through a metal line is defined for each metal layers.

$$Irms \equiv \left\{ \left(\int_0^{\tau} I^2(t)dt \right) \Big/ \tau \right\}^{1/2}$$

Following equations should be used to calculate the maximum Irms for each metal layer:
Irms_max (unit: mA)
This rule is specific for the BEOL metallization stack: 6-1X(Coral), 2-2X(FSG), 2-4X(FSG) and AL_RDL.

Table 6.A.1: for 1P10M2T2F

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
METAL1 (1x)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
METAL2 (1x)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
METAL3 (1x)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
METAL4 (1x)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
METAL5 (1x)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
METAL6 (1x)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
METAL7 (2x)	0.2	$3.250w\sqrt{1+\frac{2.774}{(w+0.0887)}}$	2.117
METAL8 (2x)	0.2	$3.022w\sqrt{1+\frac{3.345}{(w+0.0995)}}$	2.108
METAL9 (4x)	0.4	$4.121w\sqrt{1+\frac{4.155}{(w+0.1428)}}$	4.849
METAL10 (4x)	0.4	$3.708w\sqrt{1+\frac{5.284}{(w+0.1659)}}$	4.769
Al (12KA)	2.7	$3.621w\sqrt{1+\frac{6.918}{(w+0.2070)}}$	17.974

Table 6.A.1: for 1P10M2T2F (continued)

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
Al (25KA)	2.7	$5.227w\sqrt{1+\frac{6.918}{(w+0.2070)}}$	25.945
Al (36KA)	2.7	$6.272w\sqrt{1+\frac{6.918}{(w+0.2070)}}$	31.132

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

Table 6.A.2: for 1P10M2T1F1U

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
METAL1 (1x)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
METAL2 (1x)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
METAL3 (1x)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
METAL4 (1x)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
METAL5 (1x)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
METAL6 (1x)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
METAL7 (2x)	0.2	$3.250w\sqrt{1+\frac{2.774}{(w+0.0887)}}$	2.117
METAL8 (2x)	0.2	$3.022w\sqrt{1+\frac{3.345}{(w+0.0995)}}$	2.108
METAL9 (4x)	0.4	$4.121w\sqrt{1+\frac{4.155}{(w+0.1428)}}$	4.849
METAL10 (UTM)	2	$7.493w\sqrt{1+\frac{5.272}{(w+0.1777)}}$	27.718
Al (12KA)	2.7	$3.249w\sqrt{1+\frac{8.661}{(w+0.2580)}}$	17.386

Table 6.A.2: for 1P10M2T1F1U (continued)

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
AL (25KA)	2.7	$4.690w\sqrt{1+\frac{8.661}{(w+0.2580)}}$	25.097
AL (36KA)	2.7	$5.628w\sqrt{1+\frac{8.661}{(w+0.2580)}}$	30.116

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

6.A.1.4 EM Rule Adjustment for Temperature and product life times

The Idc_max and Iave limits may be adjusted for cases of junction temperature limits different from 110℃ and product life times other than 10 years.

No adjustment for the local-heating EM (Irms) is allowed.

Adjustment for	Multiplier
Temperature	$e^{\left(\frac{9178}{T_{max}(°K)}-23.96\right)}$
Product lifetime	$\left(\frac{10}{EOL_{actual}}\right)^{0.909}$

Note :

1. Using temperature and product life time adjustment factors to justify higher current usage should be contemplated only when the lower temperature or application end of life (EOL) is absolutely certain. Designing with such a derivation in effect inherently limits the application of the product.
2. The valid temperature range is 85~125℃.

6.A.2 Electromigration Rules for AL_RDL and TMV_RDL

6.A.2.1 DC Rules

This design rule sets temperature of 110℃ as circuit operation condition.

Rule No.	Imax_dc (at110℃) unit	Description	Non-shrinkable (for 65nm)	Shrinkable (for 55nm) (*1)
L2.W.EM	mA/um	AL_RDL (Al thickness 12KA, width 3um)	2.09	1.89
L2.W.EM_25K	mA/um	AL_RDL (Al thickness 25KA, width 3um)	4.35	3.92
L2.W.EM_36K	mA/um	AL_RDL (Al thickness 36KA, width 3um)	6.27	5.65
L1.A1.EM	mA/***Via***	TMV_RDL (4um x 4um)	11.64	9.43
L1.A1.EM_3	mA/Via	TMV_RDL (3um x 3um)	6.55	5.31

Note*1 UMC does not offer 90% shrink technology for 65LL. Rules of this column are provided for reference if ever applicable.

6.A.2.2 AL_RDL and TMV_RDL Temperature adjustment and product lifetime

Adjustment for	Multiplier
Temperature	$e^{\left(\frac{3482}{T_{max}(°K)} - 9.09\right)}$
Product lifetime	$\left(\frac{10}{EOL_{actual}}\right)^{0.5}$

6.B Option1: 1P10M2T2H

6.B.1 Electromigration Rules for Cu METAL and Cu MVIA Layers

6.B.1.1 Lifetime Criteria:

Please refer to" 6.A.1.1 Lifetime Criteria"

6.B.1.2 DC rules

Rule No.	Description	Imax_dc (at 110℃) unit
M1.EM	METAL1	1.89 mA/um
1XMn.EM	METAL2 & above 1x pitch METAL_n	2.31 mA/um
2XMn.EM	2X METAL7 and METAL8(FSG)	4.14 mA/um
6XMn.EM	6X METAL9 and METAL10(FSG)	14.83mA/um
CT.EM	CONTACT	0.20 mA/cont
1XVn.EM	1x pitch MVIA (MVIA1 & above 1x pitch MVIA_n)	0.25 mA/via
2XVn.EM.I1	2x pitch MVIA_n (1x pitch METAL_n & 2x pitch METAL_n+1)	0.39 mA/via
2XVn.EM.I2	2x pitch MVIA_n (2x pitch METAL_n & 2x pitch METAL_n+1)	0.96 mA/via
4XVn.EM	4x pitch MVIA_n	3.91 mA/via

Note:
As many CONTACTs or vias as design allowed are recommended to improve reliability.

6.B.1.3 AC Rules

A. For Standard EM

Maximum allowable average current (Iave_max) per unit width or per via or contact is defined. The Iave is obtained by averaging the current over one cycle.

$$Iave \equiv \left(\int_0^{\tau} I(t)dt \quad / \tau \right)$$

Iave_max is obtained by replacing the Imax_dc defined in previous section. As in DC case, Iave rules apply to METAL, MVIA and CONTACT.

B. For Local-heating Enhanced EM

Maximum allowable root-mean-square current (Irms) through a metal line is defined for each metal layers.

$$Irms \equiv \left\{ \left(\int_0^{\tau} I^2(t)dt \right) \Big/ \tau \right\}^{1/2}$$

Following equations should be used to calculate the maximum Irms for each metal layer:
Irms_max (unit: mA)
This rule is specific for the BEOL metallization stack: 6-1X (Coral), 2-2X (FSG), 2-6X (FSG) and AL_RDL.

Table 6.B.1: 1P10M2T2H

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
METAL1 (1x)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
METAL2 (1x)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
METAL3 (1x)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
METAL4 (1x)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
METAL5 (1x)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
METAL6 (1x)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
METAL7 (2x)	0.2	$3.250w\sqrt{1+\frac{2.774}{(w+0.0887)}}$	2.117
METAL8 (2x)	0.2	$3.022w\sqrt{1+\frac{3.345}{(w+0.0995)}}$	2.108
METAL9 (6x)	0.56	$5.142w\sqrt{1+\frac{4.159}{(w+0.1540)}}$	7.523
METAL10 (6x)	0.56	$4.495w\sqrt{1+\frac{5.641}{(w+0.1899)}}$	7.348
Al (12KA)	2.7	$3.460w\sqrt{1+\frac{7.587}{(w+0.2276)}}$	17.704

Table 6.B.1: 1P10M2T2H (continued)

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
Al (25KA)	2.7	$4.994w\sqrt{1+\frac{7.587}{(w+0.2276)}}$	25.554
Al (36KA)	2.7	$5.993w\sqrt{1+\frac{7.587}{(w+0.2276)}}$	30.665

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

6.B.1.4 EM Rule Adjustment for Temperature and product life times

Please refer to "6.A.1.4 EM Rule Adjustment for Temperature and product life times"

6.B.2 Electromigration Rules for AL_RDL and TMV_RDL

Please refer to "6.A.2 Electromigration Rules for AL_RDL and TMV_RDL”

6.C Option2: 1P9M (1x, 2x, 6x Metal; with maximum 7 levels of 1x Metal)

6.C.1 Electromigration Rules for Cu METAL and Cu MVIA Layers

6.C.1.1 Lifetime Criteria:

Refer to" 6.A.1.1 Lifetime Criteria"

6.C.1.2 DC rules

Refer to" 6.A.1.2 DC rules"

6.C.1.3 AC Rules

A. For Standard EM

Maximum allowable average current (Iave_max) per unit width or per via or contact is defined. The Iave is obtained by averaging the current over one cycle.

$$Iave \equiv \left(\int_0^{\tau} I(t)dt \quad / \tau \right)$$

Iave_max is obtained by replacing the Imax_dc defined in previous section. As in DC case, Iave rules apply to METAL, MVIA and CONTACT.

B. For Local-heating Enhanced EM

Maximum allowable root-mean-square current (Irms) through a metal line is defined for each metal layers.

$$Irms \equiv \left\{ \left(\int_0^{\tau} I^2(t)dt \right) \Big/ \tau \right\}^{1/2}$$

Following equations should be used to calculate the maximum Irms for each metal layer:
Irms_max (unit: mA)
This rule is specific for the BEOL metallization stack: maximum 7 layers of 1X (Coral), maximum 2 layers of 2X (FSG), maximum 2 layers of 6X (FSG) and AL_RDL.

Table 6.C.1: 1P9M2H

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
METAL1 (1x)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
METAL2 (1x)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
METAL3 (1x)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
METAL4 (1x)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
METAL5 (1x)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
METAL6 (1x)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
METAL7 (1x)	0.1	$2.552w\sqrt{1+\frac{2.634}{(w+0.0645)}}$	1.053
METAL8 (6x)	0.56	$5.497w\sqrt{1+\frac{3.348}{(w+0.1297)}}$	7.448
METAL9 (6x)	0.56	$4.720w\sqrt{1+\frac{4.873}{(w+0.1724)}}$	7.312
AI (12KA)	2.7	$3.589w\sqrt{1+\frac{6.858}{(w+0.2050)}}$	17.765
AL (25KA)	2.7	$5.181w\sqrt{1+\frac{6.858}{(w+0.2050)}}$	25.645
AL (36KA)	2.7	$6.217w\sqrt{1+\frac{6.858}{(w+0.2050)}}$	30.773

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

Table 6.C.2: 1P9M1T1H

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
Metal-1 (1X)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
Metal-2 (1X)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
Metal-3 (1X)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
Metal-4 (1X)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
Metal-5 (1X)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
Metal-6 (1X)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
Metal-7 (1X)	0.1	$2.552w\sqrt{1+\frac{2.634}{(w+0.0645)}}$	1.053
Metal-8 (2X)	0.2	$3.046w\sqrt{1+\frac{3.094}{(w+0.0950)}}$	2.065
Metal-9 (6X)	0.56	$5.175w\sqrt{1+\frac{3.913}{(w+0.1470)}}$	7.408
AL (12KA)	2.7	$3.837w\sqrt{1+\frac{5.948}{(w+0.1742)}}$	18.150
AL (25KA)	2.7	$5.538w\sqrt{1+\frac{5.948}{(w+0.1742)}}$	26.197
AL (36KA)	2.7	$6.646w\sqrt{1+\frac{5.948}{(w+0.1742)}}$	31.438

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

6.C.1.4 EM Rule Adjustment for Temperature and product life times

Please refer to "6.A.1.4. EM Rule Adjustment for Temperature and product life times"

6.C.2 Electromigration Rules for AL_RDL and TMV_RDL

Please refer to "6.A.2 Electromigration Rules for AL_RDL and TMV_RDL”

6.D Option3: 1P9M (1x, 2x, 4x Metal; with maximum 7 levels of 1x Metal)

6.D.1 Electromigration Rules for Cu METAL and Cu MVIA Layers

6.D.1.1 Lifetime Criteria

Refer to" 6.A.1.1 Lifetime Criteria"

6.D.1.2 DC rules

Refer to" 6.A.1.2 DC rules"

6.D.1.3 AC Rules

A. For Standard EM

Maximum allowable average current (Iave_max) per unit width or per via or contact is defined. The Iave is obtained by averaging the current over one cycle.

$$Iave \equiv \left(\int_0^{\tau} I(t)dt \quad / \tau \right)$$

Iave_max is obtained by replacing the Imax_dc defined in previous section. As in DC case, Iave rules apply to METAL, MVIA and CONTACT.

B. For Local-heating Enhanced EM

Maximum allowable root-mean-square current (Irms) through a metal line is defined for each metal layers.

$$Irms \equiv \left\{ \left(\int_0^{\tau} I^2(t)dt \right) \Big/ \tau \right\}^{1/2}$$

Following equations should be used to calculate the maximum Irms for each metal layer:
Irms_max (unit: mA)
This rule is specific for the BEOL metallization stack: maximum 7 layers of 1X (Coral), maximum 2 layers of 2X (FSG), maximum 2 layers of 4X (FSG) and AL_RDL.

Table 6.D.1: 1P9M2F

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
Metal-1 (1X)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
Metal-2 (1X)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
Metal-3 (1X)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
Metal-4 (1X)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
Metal-5 (1X)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
Metal-6 (1X)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
Metal-7 (1X)	0.1	$2.552w\sqrt{1+\frac{2.634}{(w+0.0645)}}$	1.053
Metal-8 (4X)	0.4	$4.407w\sqrt{1+\frac{3.346}{(w+0.1227)}}$	4.796
Metal-9 (4X)	0.4	$3.909w\sqrt{1+\frac{4.508}{(w+0.1506)}}$	4.739
AL (12KA)	2.7	$3.772w\sqrt{1+\frac{6.170}{(w+0.1820)}}$	18.049
AL (25KA)	2.7	$5.445w\sqrt{1+\frac{6.170}{(w+0.1820)}}$	26.055
AL (36KA)	2.7	$6.534w\sqrt{1+\frac{6.170}{(w+0.1820)}}$	31.266

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

Table 6.D.2: 1P9M1T1F

Layer	Minimum drawn width (μm)	Max Irms (mA) for line width w (μm)*	Max Irms (mA) @ wmin**
Metal-1 (1X)	0.09	$5.629w\sqrt{1+\frac{0.714}{(w+0.0271)}}$	1.350
Metal-2 (1X)	0.1	$4.663w\sqrt{1+\frac{1.004}{(w+0.0356)}}$	1.352
Metal-3 (1X)	0.1	$3.848w\sqrt{1+\frac{1.332}{(w+0.0433)}}$	1.235
Metal-4 (1X)	0.1	$3.351w\sqrt{1+\frac{1.659}{(w+0.0499)}}$	1.164
Metal-5 (1X)	0.1	$3.007w\sqrt{1+\frac{1.986}{(w+0.0555)}}$	1.116
Metal-6 (1X)	0.1	$2.752w\sqrt{1+\frac{2.311}{(w+0.0604)}}$	1.080
Metal-7 (1X)	0.1	$2.552w\sqrt{1+\frac{2.634}{(w+0.0645)}}$	1.053
Metal-8 (2X)	0.2	$3.046w\sqrt{1+\frac{3.094}{(w+0.0950)}}$	2.065
Metal-9 (4X)	0.4	$4.148w\sqrt{1+\frac{3.910}{(w+0.1371)}}$	4.774
AL (12KA)	2.7	$3.946w\sqrt{1+\frac{5.595}{(w+0.1613)}}$	18.316
AL (25KA)	2.7	$5.696w\sqrt{1+\frac{5.595}{(w+0.1613)}}$	26.439
AL (36KA)	2.7	$6.835w\sqrt{1+\frac{5.595}{(w+0.1613)}}$	31.726

Note:

* w denotes drawn width

** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width

6.D.1.4 EM Rule Adjustment for Temperature and product life times

Please refer to "6.A.1.4. EM Rule Adjustment for Temperature and product life times"

6.D.2 Electromigration Rules for AL_RDL and TMV_RDL

Please refer to "6.A.2 Electromigration Rules for AL_RDL and TMV_RDL”

6.E Pulse Rule

Metal Level	*Minimum Metal width (um)*	*Minimum Metal Thickness (um)*	Ipeak (mA)
M1	*0.09*	*0.18*	*40.04 x w*
1X	*0.1*	*0.22*	*23.10 x w*
2X	*0.2*	*0.36*	*41.40 x w*
4X	*0.4*	*0.80*	*64.14 x w*
6X	*0.56*	*1.25*	*94.65 x w*

1. w is drawn metal width in um.
2. ***The design should follow pulse rule if pulse width is smaller than 1 micro second***.

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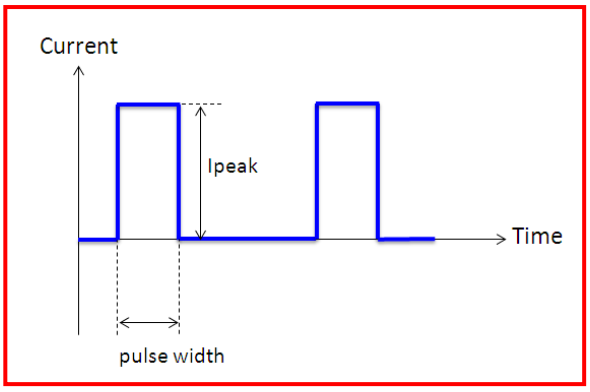
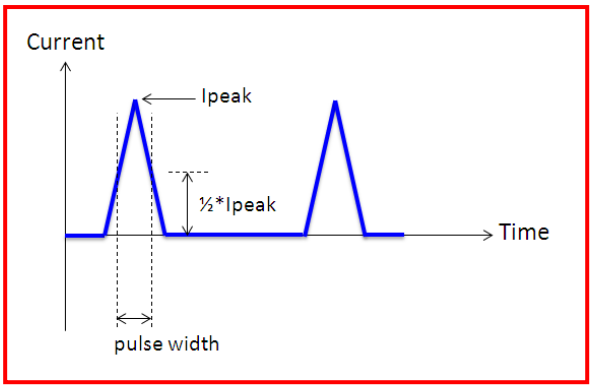




7. Wirebond and Al Re-Distribution Layer (AL_RDL) Rules

7.1 Purpose

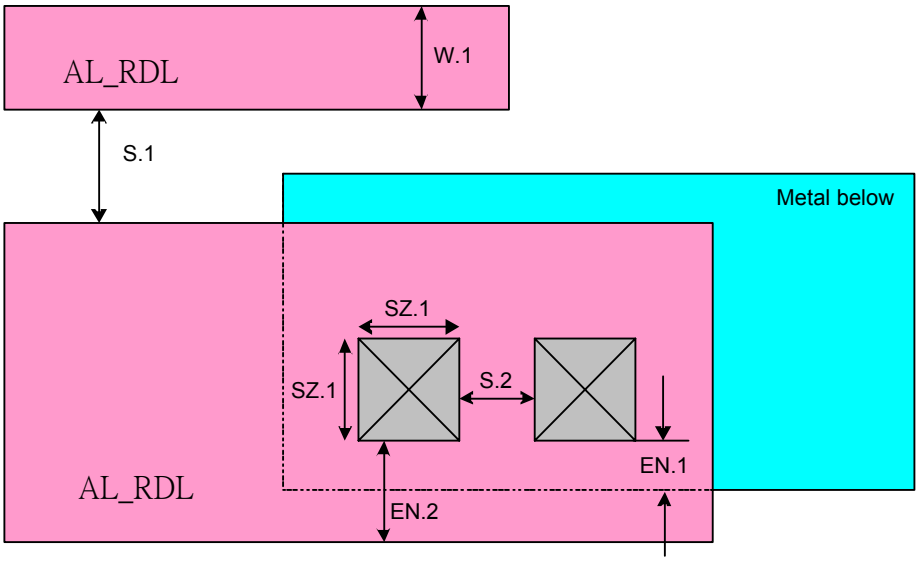
This section defines the layout rules AL_RDL routing for and only for wirebond package types. Refer to Section “4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure” for wirebond packaging information.

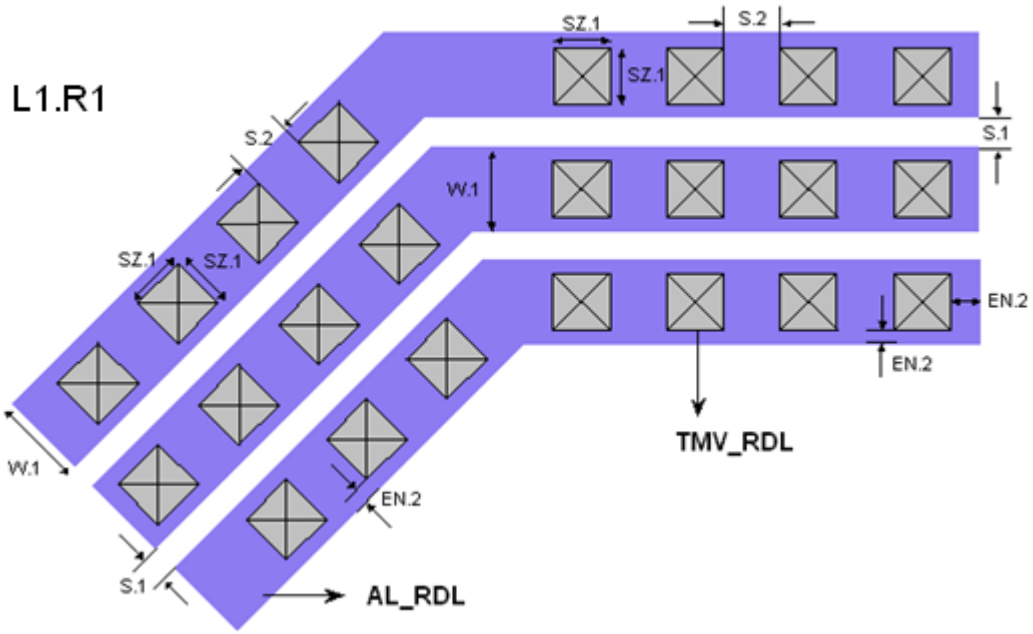
7.2 Layout Rules for AL_RDL Routing

(unit: um)

Rule No.	Description	Label		Rule
L2_L.W1	Width of Al-metal line at AL_RDL layer	W.1	≧	2.7
L2_L.S1	Spacing and notch of AL_RDL (Al thickness 12KA)	S.1	≧	1.6
L2_L.S1_2	Spacing and notch of AL_RDL line (Al thickness 36KA or 25KA)	S.1	≧	1.8
L2_L.S	Spacing and notch of [AL_RDL with width > 35um]		≧	3
L1.SZ1	TMV_RDL size	SZ.1	=	4x4 or 3x3
L1.S2	Spacing of TMV_RDL to TMV_RDL	S.2	≧	2
LM-L1.EN1	Last Copper Metal METAL_n enclosure of TMV_RDL Note: TMV_RDL must be within Last METAL_n	EN.1	≧	0.35
L2_L-L1.EN2	AL_RDL enclosure of TMV_RDL	EN.2	≧	0.5
L1.R1	All TMV_RDL shapes must be orthogonal except in LOGO, IND and die seal ring areas. TMV_RDL_BAR is allowed only in die seal ring area.			Yes
L2.D1	Minimum AL_RDL density cross full chip		≧	10%
L2.D2	Maximum AL_RDL density cross full chip		≦	85%
L2-L3.R1	All PASV_RDL must be within AL_RDL except over FUSE_MARK, CAD_WAT_PAD_MARK, CAD_CU_FLIP_MARK and SEAL_RING_MARK.			Yes

Note: For wide AL_RDL, please refer to Section “7.3 AL_RDL Stress Relief Rules”.




L1.R1
SZ.1
S.2
SZ.1
S.1
W.1
S.2
SZ.1
SZ.1
EN.2
EN.2
TMV_RDL
W.1
EN.2
S.1
AL_RDL

7.3 AL_RDL Stress Relief Rules

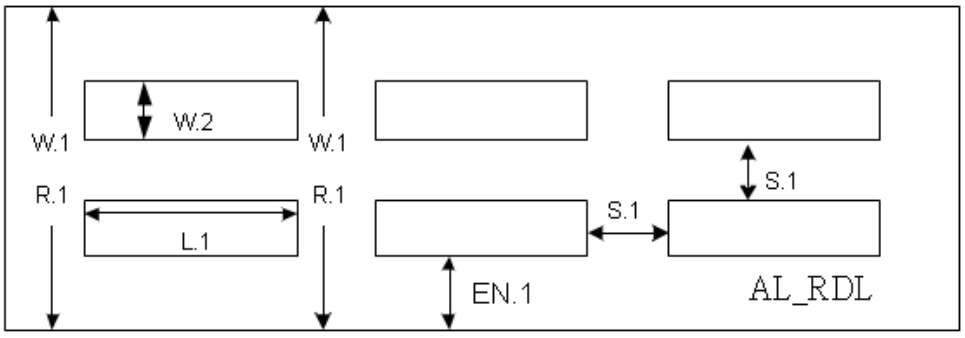
(AL_RDL_CUSTOMER_SLOT)

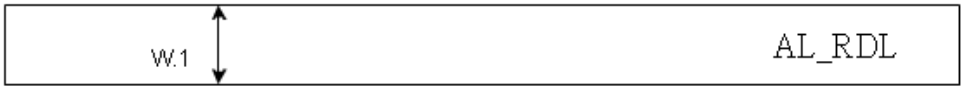
The following rules are applied to AL_RDL to avoid the reliability problem due to thermal stress. Slots in AL_RDL must be drawn at a different GDS layer, AL_RDL_CUSTOMER_SLOT(GDS# 67(9)) for DRC checking and tape out.

Please note that customers are responsible for drawing the slots in AL_RDL.

(unit: um)

Rule No.	Description	Label		Rule
L2.W1.L2SLOT	Width of AL_RDL (L2) EXCEPT bonding pad area	W.1	<	35
L2SLOT.W2	Slot width	W.2	≧	2
L2SLOT.WX	Slot width		≦	5
L2SLOT.L1	Slot length	L.1	≧	10
L2SLOT.LX	Slot length		≦	250
L2SLOT.S1	Spacing of slot	S.1	≧	9
L2SLOT.SX	Spacing of slot		≦	20
L2SLOT-Mn.EN1	AL_RDL enclosure of slot	EN.1	≧	9
L2SLOT-Mn.ENX	AL_RDL enclosure of slot		≦	20
L2SLOT.R1	All slots should be parallel with the direction of current flow on the Metal line	R.1		Yes
L2SLOT.R2	For AL_RDL within die corner area, please follow the "Metal Stress Relief Rules for Die Corner Area" defined in Chapter 5	R.2		Yes





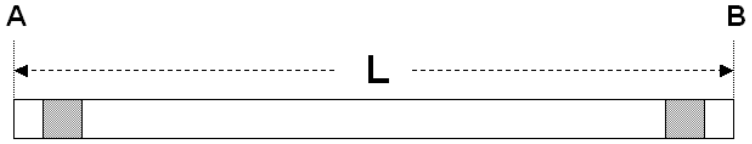
8. Short Length Effect

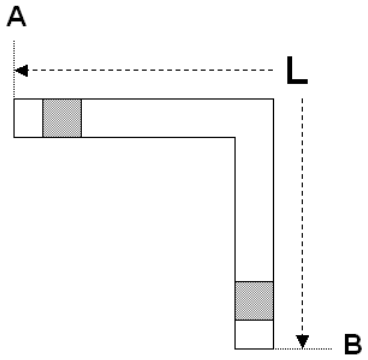
Metal Length (um)	Ratio of Imax_dc
L>20	1X
20≧L>5	2X
L≦5	4X

(1) If metal length is less than 20 um, Imax is allowed relaxation follow the above table.

(2) Metal length definition (L): The metal length is from point-A to point-B.

(3) The table is valid for all metal layers.





9. Cu-Fuse Rules

Please refer to the Spec. No. G-03F-GENERATION65N-CU-TLR/FUSE

10. ESD Rules

Please refer to the Spec. No. G-03E-GENERATION65N-TLR/ESD

11. Latch-up Rules

Please refer to the Spec. No. : G-03L-GENERATION65N-TLR/LATCH_UP

12. Dummy Rules

Please refer to Spec. No.: G-03D-GENERATION65N-METAL-TLR/DUMMY and
G-03D-GENERATION65N/55N-DIFFUSION/POLY1-TLR/DUMMY

13. Logo Rules

Please refer to the Spec. No. : G-03LO-GENERATION25_BEYOND-TLR/LOGO

14. Antenna Rule (ATN)

14.1 Definitions

1. The antenna ratio defined as the plasma receive top area to the poly gate area that is connected directly to it or through contact or via.
2. The antenna rules apply separately to all devices.
3. The protection diode defined as N+ DIFFUSION or P+ DIFFUSION area connected to poly gate through metal 1 (including source or drain diffusion area of MOSFET)
4. The minimum diode area is 0.1 um^2 and could be a summation area of the diodes in the same net.

14.2 Antenna Design Rule Assumptions

The antenna rules are designed under the following assumptions: A device having the allowed antenna ratio will differ from a device without antenna not more than...

* Threshold voltage shift less than 1/2 tolerance offered by current technology (For exact values, please refer to the individual Electrical Design Rule (i.e. G-02 document listed in the individual DSM) .

  Example: 2.5V NMOS Vtsat (W / L= 10 / 0.24): 0.29V (Min), 0.44V (Typ), 0.59V (Max) =>
  0.365V (Min)< Threshold voltage of the device w/ antenna < 0.515V (Max)

* Difference in gate dielectric leakage < 10X

14.3 Rule and Recommendation

Without Diode

Rule No.	Description		Ratio	
			Core	IO
R_PLY-PLY.ANT	Ratio of the poly area to the poly gate area	<	250	250
R_PLY.SW-PLY.ANT	Ratio of the poly sidewall area to the poly gate area	<	500	500
R_CT-PLY.ANT	Ratio of the contact area to the poly gate area	<	10	10
R_Cum.Mn-PLY_ANT.WD	Ratio of cumulative METAL_n area (n=1~10) to the poly gate area	<	5000	5000
R_Cum.Vn-PLY_ANT.WD	Ratio of cumulative MVIA_n area (n=1~9) to the poly gate area	<	180	180
R_L1-PLY.ANT.WD	Ratio of L1 area to the poly gate area	<	80	20
R_L2.SW-PLY.ANT.WD	Ratio of L2 sidewall area to the poly gate area	<	2000	1000

With Diode

With Diode				
Rule No.	Description		Ratio	
			Core	IO
R_Cum.Vn-PLY.ANT	Ratio of cumulative MVIA_n area (n=1~9) to the poly gate area	<	800 + 200 x diode area	
R_Cum.Mn-PLY.ANT	Ratio of cumulative METAL_n area (n=1~10) to the poly gate area	<	45000 + 450 x diode area	
R_L1-PLY.ANT	Ratio of L1 area to the poly gate area	<	400 + 83 x diode area	
R_L2.SW-PLY.ANT	Ratio of L2 sidewall area to the poly gate area	<	30000 + 8000 x diode area	

Note:

1. When P_WELL (not include P_WELL touch DEEP_N_WELL) connects to metal or via, it can be treated as the effective protection diode against plasma charging. This kind of metal or via can be excluded from Antenna Rule.

14.4 Minimum Antenna Protection Diode Area check only for IP vender and U IP

Rule No.	Description		Rule
R_ANT.A	Minimum Antenna Protection Diode area connected to poly gate through metal 1 for IP pin (note1).	≧	0.1 um^2

Note:

1. The additional layer to mark metal with pins are required for DRC.

Metal layer	Layer name	GDS number and data type
METAL1	CAD_METAL1_PORT	72 (11)
METAL2	CAD_METAL2_PORT	73 (11)
METAL3	CAD_METAL3_PORT	74 (11)
METAL4	CAD_METAL4_PORT	75 (11)
METAL5	CAD_METAL5_PORT	76 (11)
METAL6	CAD_METAL6_PORT	77 (11)
METAL7	CAD_METAL7_PORT	78 (11)
METAL8	CAD_METAL8_PORT	79 (11)
METAL9	CAD_METAL9_PORT	80 (11)
METAL10	CAD_METAL10_PORT	81 (11)

2.Flag anonymous p Antenna diodes as error.

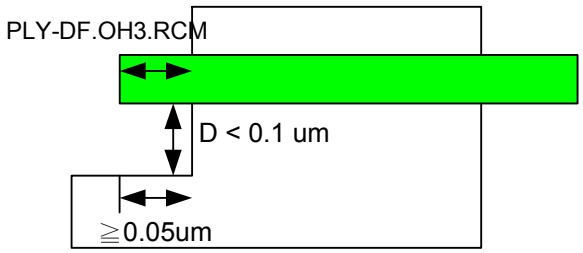
3.The anonymous p Antenna defined as P+/N_WELL diode that is not including source/drain, BIPOLAR, CAD_DIFFUSION_RESISTOR_SYMBOL and DIODE_IMPLANT_BLOCK Layer and P+ DIFFUSION without contact.

15. DFM (Design For Manufacturing)

15.1 Recommended Rules

The recommended rules are suggested to use when the use is not to cause concern of chip area increase and performance degradation. The recommended rules are prioritized. The higher priority recommended rules are strongly suggested for design to use since evidence for yield improvement for these rules is observed, although we understand that the recommended rules are not possible to be implemented in 100%.

Priority	Rule No.	Description		TLR Rule	Recom. Rule
1	V1.R.RCM	Use redundant via for all metal layer interconnection			
2	PLY_G.RCM	Poly gate length≦0.08um not over TG should be aligned in one direction. Horizontal direction is preferred.		YES	
2	DF.W1.RCM	DIFFUSION width for device (not over TG)	≧	0.08	0.12
2	PLY-DF.S3.RCM	Spacing of POLY1 end cap to related DIFFUSION, When the relative transistor width <0.2um	≧	0.05	0.10
2	PLY-DF.S4.RCM	Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS), When the relative transistor width <0.2um	≧	0.05	0.10
2	PLY-DF.OH3.RCM	POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um	≧	NA	0.16
2	PLY-CT.EN1.RCM	POLY1 enclosure of CONTACT	≧	0.02	0.04
2	PLY-CT.EN2.RCM	POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero	≧	0.04	0.06
2	DF.S1.RCM	Spacing and notch of DIFFUSION	≧	0.11	0.13
2	DF.S2.RCM	Spacing and notch of DIFFUSION patterns with width >= 1.5um (at least one side)	≧	0.12	0.15
2	PLY_F.S2.RCM	Spacing and notch of POLY1 on field (not over TG)	≧	0.12	0.14
2	DF-CT.EN3.RCM	DIFFUSION enclosure of CONTACT	≧	0.015	0.03
2	DF-CT.EN4.RCM	DIFFUSION enclosure of two opposite sides of CONTACT when other sides have enclosure of zero	≧	0.04	0.06
2	M1-CT.EN2.RCM	METAL1 line end enclosure of CONTACT	≧	0.03	0.05
2	1XMn-Vn.EN2.RCM	METAL_n line end enclosure of MVIA_n (n=2, 3, 4, 5, 6, 7)	≧	0.03	0.05
2	DF.W2.RCM	DIFFUSION width	≧	0.08	0.10
2	CT.R.RCM	Use redundant CONTACT when layout is allowed		-	YES



15.2 OPC Friendly Design Guidelines

The OPC friendly design guidelines are suggested for reducing OPC/mask generation cycle time and further device performance enhancement with OPC concerns in mind.

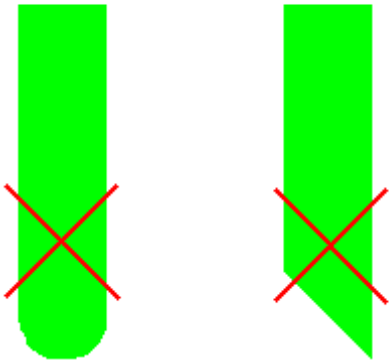
Guideline #	Description of OPC Friendly Design Guideline
OPC.1	OPC recipes capability limitation
OPC.1-A	Provide a DRC clean database and no TLR rule violation
OPC.1-B	Layout line end to be rectangular shape. For X-architecture layout, please refer to X-architecture specific TLR layout for details
OPC.1-C	Avoid using "head-to-head" corners at minimum width or space for DIFFUSION, POLY1, METAL1, 1Xpitch METAL and 2x pitch METAL.
OPC.2	OPC run time, database size and mask-making cycle time reduction
OPC.2-A	Avoid using small jogs. Distance between jogs is recommended to be greater than half pitch(NOTE1,2)
OPC.2-B	Avoid using small zigzags. Distance between zigzags is recommended to be greater than half pitch(NOTE1,2)
OPC.2-C	Recommend that you do not have more than 3 consecutive sides with length < 1/4 pitch of DIFFUSION/POLY1/METAL1/1x pitch Metal/2x pitch Metal. (NOTE1)
OPC.3	Layout rounding effect minimization
OPC.3-A	Minimize H shape DIFFUSION utilization if possible
OPC.3-B	If H shape DIFFUSION is needed, please follow DFM rule with POLY1 to DIFFUSION corner >= 0.10,When the relative transistor width <0.2um
OPC.3-C	Place CONTACT/MVIA at the center of POLY1/ DIFFUSION /METAL lines to minimize the impact of POLY1/METAL shape rounding effect
OPC.3-D	Adopt DFM recommended DIFFUSION /POLY1/METAL enclosure rules if space allowed
OPC.4	Critical CD variation minimization for better device matching
OPC.4-A	Layout all gate POLY1 in same direction
OPC.4-B	Add dummy feature (using same width/space as ending transistor) adjacent to REAL ending transistor, ideally with same pitch as active POLY1 lines

NOTE1: Half and 1/4 pitch table

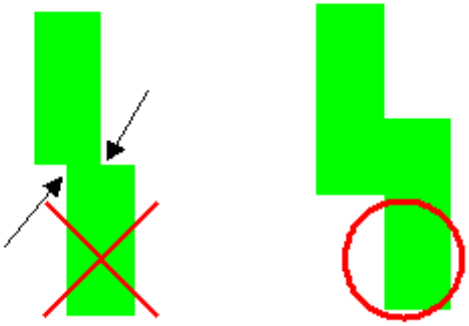
Layer	Pitch (um)	Half pitch (um)	1/4 pitch(um)
DIFFUSION	0.19	0.095	0.048
POLY1	0.19	0.095	0.048
METAL1	0.18	0.09	0.045
1x pitch Metal	0.20	0.10	0.05
2x pitch Metal	0.40	0.20	0.10

NOTE2: This rule must be followed to prevent pattern open or short.

OPC.1-B



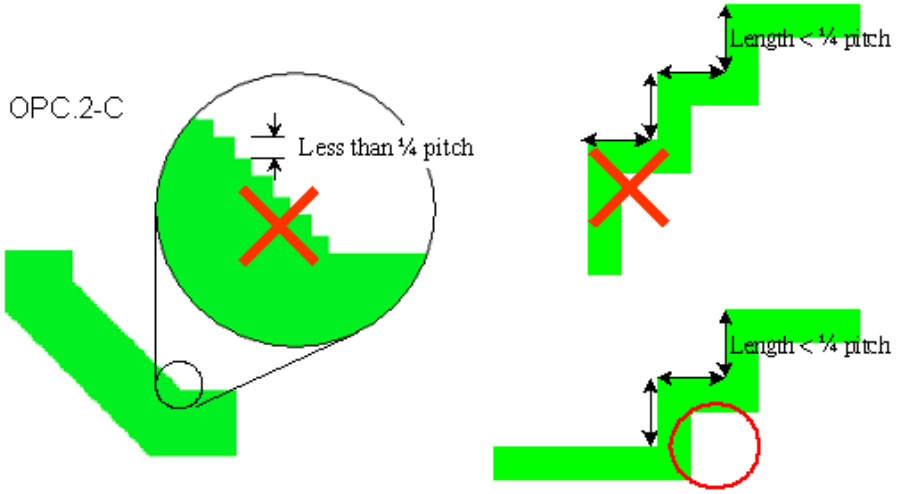
OPC. 1-C

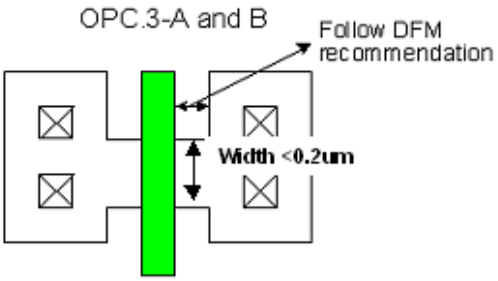


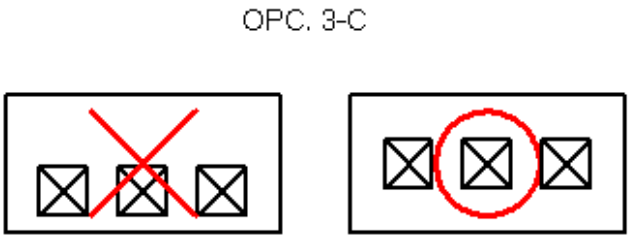
OPC.2-A

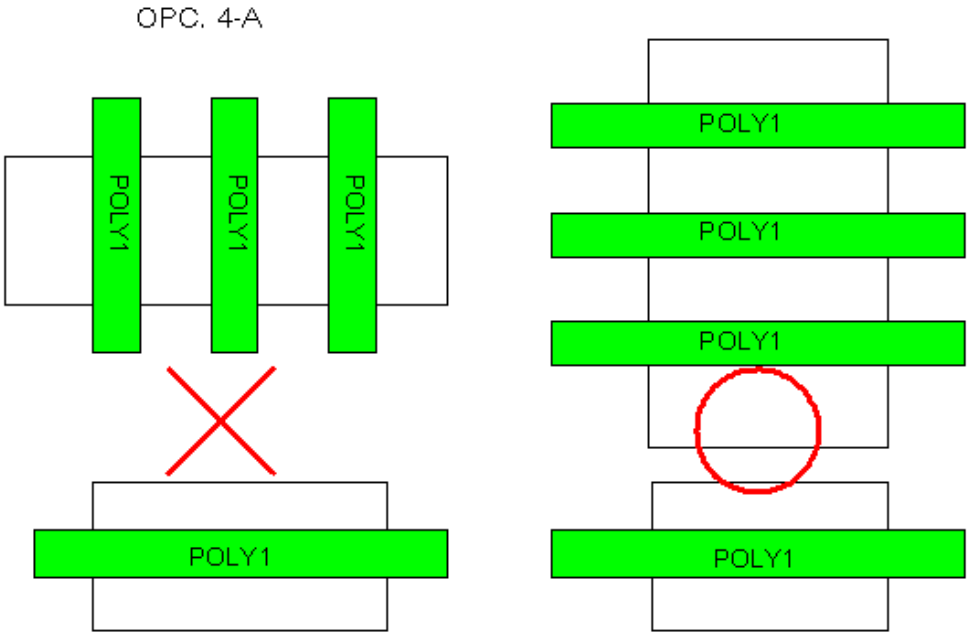
OPC.2-B

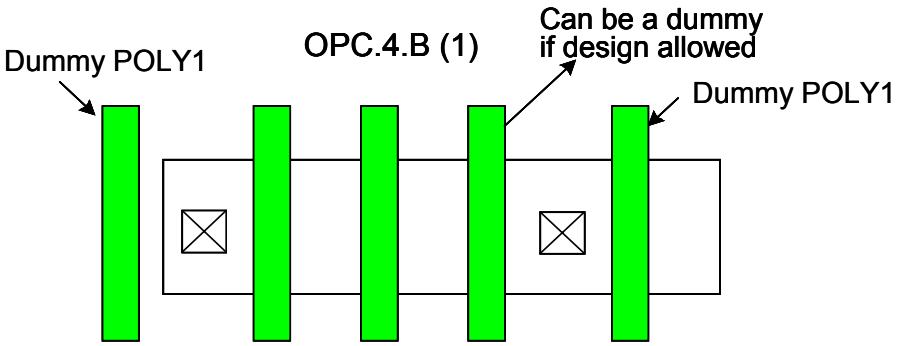
OPC.2-C

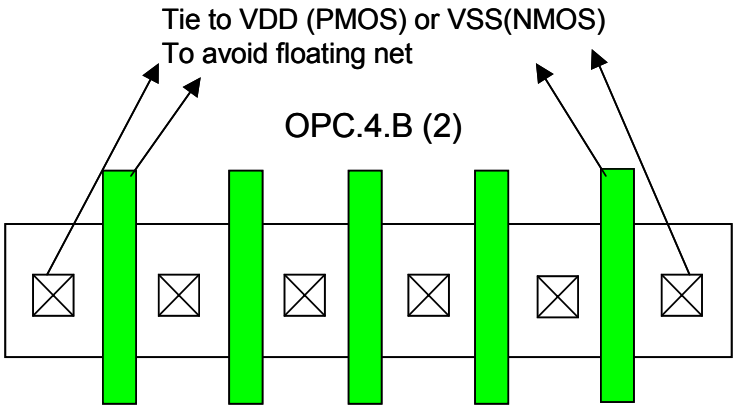



OPC.3-A and B
Follow DFM recommendation
Width <0.2um


OPC. 3-C


OPC. 4-A
POLY1
POLY1
POLY1
POLY1
POLY1
POLY1
POLY1
POLY1


Dummy POLY1
OPC.4.B (1)
Can be a dummy if design allowed
Dummy POLY1


Tie to VDD (PMOS) or VSS(NMOS)
To avoid floating net
OPC.4.B (2)

16. Appendix Revision History

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.0	1	07/12/2005	-	-	Original
T.1	1	11/11/2005	3.Mask Layer: P90 T_WELL Define SP device (P16,P13,P17,P95,PB2,PB3)	UC0 DEEP_N_WELL Delete	
			4.0.3 NA 4A.1 DF.WX: except guard ring DF.A≧0.06 DF.EA≧0.09 4A.2.1 NA 4A.3 T_WELL NA 4A.4 SP_RVT layer 4A.5 LL_RVT (LLR) Layer Layout Rules all LL_RVT LLH-NW.OH:0 or ≧ 0.36 NW-LLH.OH:0 or ≧ 0.36 NW-LLH.OL:0 or ≧ 0.36 NA 4A.8 MG 4A.9 TG.W≧0.4 TG.S≧0.4 TG-NW.S≧0.4 TG-NW.OH: 0 or ≧0.4 NW-TG.OH≧0.4 TG-NW.OL: 0 or ≧0.4 NA 4A.10 PLY-DF.OH1: POLY1 < 0.12um NA PLY-DF.OH2:No PLY.A≧0.044 PLY.EA≧0.068 PLY-DF.S1≦0.2um PLY-DF.S2>0.2um	4.0.3 : For DIFFUSION, POLY1, N+, P+, CONTACT, 1x pitch METAL, 1x pitch MVIA, 2x pitch METAL and 2x pitch MVIA layer, 1nm grid is allowed. 4A.1 DF.WX :Delete DF.A≧0.054 DF.EA≧0.085 4A.2.1 NWR-N_DF.NW Delete 4A.3 DEEP_N_WELL Delete 4A.4 LL_HVT (LLH) Layer Layout Rules all LL_HVT LLH-NW.OH:≧ 0.36 NW-LLH.OH:≧ 0.36 NW-LLH.OL:≧ 0.36 LLH-NW.R Delete 4A.7 TG.W≧0.44 TG.S≧0.44 TG-NW.S≧0.44 TG-NW.OH≧0.44 NW-TG.OH≧0.44 TG-NW.OL≧0.44 TG-NW.R 4A.8 PLY-DF.OH1: POLY1 < 0.13um PLY-DF.S3 PLY-DF.OH2:When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and PLY.A≧0.0375 PLY.EA≧0.077 PLY-DF.S1≦0.3um PLY-DF.S2>0.3um	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	4A.11 NSD.A≧0.15 NSD.EA≧0.15 NSD-P_DF.S.NW : not over T_WELL NSD-P_DF.S.TW NSD-N_DF.EN.TW N_DF-P_PU.SX.TW 4A.12 PSD.A≧0.15 PSD.EA≧0.15 PSD-N_DF.S.TW PSD-P_DF.EN.TW P_DF-N_PU.SX.NW 4A.13 PPNRS.S :NA PPNRS-LLH.S TG-PPNRS.EN:NA SAB-PLY.S:0.22 SBLK-PLY.S:0.22 PPNRS-SPR.S PPNRS-TW.S TW-PPNRS.EN 4A.14 CONTACT CT.S1:S.2 CT.S2:<0.18um , NA DF-CT.EN1:NA 4A.17 MOAT.R:T_WELL 4B.1 For products using copper BEOL process, both Metal Dummy and Oxide Slot generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. Oxide Slots will be inserted into the metal lines automatically for 1x pitch metal with line width ≧ 12um during the Oxide Slot generation. For certain circuit regions where Metal Dummy or Oxide Slot are not allowed, Metal Dummy and Oxide Slot generation can be locally inhibited by using "Block" on the design levels of MnDMBK and MnSLBK (n=1,2,3,4,5,6), respectively. For the definition of MnDMBK and MnSLBK, please consult UMC representatives for more details about 65nm Logic Dummy and Slot Rules for Metal Layers.	4A.9 NSD.A≧0.122 NSD.EA≧0.122 NSD-P_DF.S.NW: Delete Delete Delete Delete 4A.10 PSD.A≧0.122 PSD.EA≧0.122 Delete Delete Delete 4A.11 PPNRS.S : body Delete TG-PPNRS.EN :body SAB-PLY.S:0.20 SBLK-PLY.S :0.2 Delete Delete Delete 4A.12 CONTACT CT.S1:NA CT.S2<0.17um , :S.2 DF-CT.EN1:Add EN.4 plot and symbol 4A.15 MOAT.R:DEEP_N_WELL 4B.1 For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=1,2,3,4,5,6). For the definition of MnDMBK , please consult UMC representatives for more details about 65nm Logic Dummy Rules for Metal Layers	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	4B.1.1 M1.WX≦25um M1-CT.EN5 M1.WX.M1SLBK M1.S.M1SLBK M1.A≧0.038 M1.EA≧0.11 M1.D METAL1 density, d, over 50umx50um area within either MnDMBK or MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. M1.D1 METAL1 density, d, over 50umx50um area without MnDMBK and MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments M1.R M1.R2 4B.1.2 1XMn.WX≦25um 1XMn.WX.MnSLBK 1XMn.S.MnSLBK 1XMn.S1.MnSLBK 1XMn.A≧0.046 1XMn.EA≧0.11	4B.1.1 M1.WX:except PAD area mark layer≦12um M1-CT.EN5:METAL1 line end enclosure of CONTACT can be released when METAL1 has redundant CONTACTs except when d1,d2,d3,d4,d5,d6 ≦ 0.12um. When d1,d2,d3,d4,d5,d6 ≦ 0.12um and one end METAL1 enclosure drawn between 0.03 to 0.06um,the minimum enclosure of the other end METAL1 is 0.06um. Delete Delete M1.A≧0.042 M1.EA≧0.2 M1.D METAL1 density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments M1.D1 METAL1 density, d, over 50umx50um area without MnDMBK.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments M1.R:except Die Seal Ring and Die corner within 150um area. see section 5.1 for details. Delete 4B.1.2 1XMn.WX:except PAD area mark layer and BOAC PAD area metal supporting layer≦12um Delete Delete Delete 1XMn.A≧0.052 1XMn.EA≧0.2	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	1XMn.D METAL_n density, d, over 50umx50um area within either MnDMBK or MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments 1XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK and MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments 1XMn.R1 1XMn.R :NA 4B.2.2 1XVn.R1≦0.42um 1XVn.R2≦0.42um 1XVn.R3≦0.42um 4B.3 For products using copper BEOL process, both Metal Dummy and Oxide Slot generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. Oxide Slots will be inserted into the metal lines automatically for 2x pitch Metal with line width ≧ 5um during the Oxide Slot generation. For certain circuit regions where Metal Dummy or Oxide Slot are not allowed, Metal Dummy and Oxide Slot generation can be locally inhibited by using "Block" on the design levels of MnDMBK and MnSLBK (n=7,8), respectively. For the definition of MnDMBK and MnSLBK, please consult UMC representatives for more details about 65nm Logic Dummy and Slot Rules for Metal Layers.	1XMn.D METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments 1XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments Delete 1XMn.R :except Die Seal Ring and Die corner within 150um area.see section 5.1 for details.(*1) Remark: *1. X-Routing rules are being developed which will update TLR once rules are being verified. 1XVn.R1≦0.3um 1XVn.R2≦0.3um 1XVn.R3≦0.3um 4B.3 For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=7,8). For the definition of MnDMBK , please consult UMC representatives for more details about 65nm Logic Dummy for Metal Layers	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	2XMn.WX≦25um 2XMn.WX.MnSLBK 2XMn.S.MnSLBK 2XMn.S1.MnSLBK 2XMn.S2.MnSLBK 2XMn.S3.MnSLBK 2XMn.D METAL_n density, d, over 50umx50um area within either MnDMBK or MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. 2XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK and MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments 2XMn.R 4B.5 For products using copper BEOL process, both Metal Dummy and Oxide Slot generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. Oxide Slots will be inserted into the metal lines automatically for 2x pitch Metal with line width ≧ 5um during the Oxide Slot generation. For certain circuit regions where Metal Dummy or Oxide Slot are not allowed, Metal Dummy and Oxide Slot generation can be locally inhibited by using "Block" on the design levels of MnDMBK and MnSLBK (n=7,8), respectively. For the definition of MnDMBK and MnSLBK, please consult UMC representatives for more details about 65nm Logic Dummy and Slot Rules for Metal Layers	2XMn.WX:except Pad area mark layer and BOAC PAD area metal supporting layer≦12um Delete Delete Delete Delete Delete 2XMn.D METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. 2XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments Delete 4B.5 For products using copper BEOL process, Metal Dummy generations are needed. This ensures that the metal lines meet the pattern density requirements for standard Metal process. For certain circuit regions where Metal Dummy are not allowed, Metal Dummy generation can be locally inhibited by using "Block" on the design levels of MnDMBK (n=9,10). For the definition of MnDMBK , please consult UMC representatives for more details about 65nm Logic Dummy for Metal Layers	

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T.1	1	11/11/2005	4XMn.WX≦25um 4XMn.WX.MnSLBK 4XMn.S.MnSLBK 4XMn.S1.MnSLBK 4XMn.S2.MnSLBK 4XMn.S3.MnSLBK 4XMn.S2 4XMn.D METAL_n density, d, over 50umx50um area within either MnDMBK or MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. 4XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK and MnSLBK. If "MnDMBK" and "MnSLBK" are overlapped, the "MnDMBK" and "MnSLBK" must be the same size (same X and Y dimensions). In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments 4XMn.R 4B.7.2 L2.S≧14 No No No No L2_L.S1≧4	4XMn.WX:except Pad area mark layer and BOAC PAD area metal supporting layer≦12um Delete Delete Delete Delete Delete Delete 4XMn.D METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. 4XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments Delete L2.S≧3 Add:L2-WELL.S Add:L2-DF.S Add:L2-PLY.S Add:L2-Mn.S L2_L.S1≧3	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	4B.7.4 The CLVS structure is used only for the mechanical support of the wirebond pad. Thus, no interconnection using CLVS is allowed. The CLVS structure is required in all low-k dielectric levels. No CLVS structure is allowed in the oxide dielectric levels. As Metal Dummy (MnDummy) and Oxide Slot (MnSLOT) are required for every design in 65nm generation, one must add both metal dummy block (MnDMBK) and oxide slot block (MnSLBK) to the bond pads at all metal layers used. Customer has to draw the slot patterns in the MnSLOT layer with data type (9), and not directly at the Mn layer. Please refer to the 65nm MASK TOOLING INFORMATION for details. 65nm bond pad structure consists of both transfer pad (L1/L2/L3) and metal pad (M1 and 1x Metal in low-k). 1XMn.W.CLVS : over 1XMn.S.CLVS : over 1XMn.SX.CLVS : over CLVS.R : over 4B.9 VIAFARM (VF) Rules No 7.2 L2_L.S1≧4 5.Die Seal Ring Rules Due to the reliability concern, main chips must be surrounded by two seal rings. Each ring consists of metal tracks connected to power line and the substrate (this rule is for P-sub which has the same potential as the power line). A “SEAL RING MARK” layer, with the GDS number 86(36),also needs to be drawn on die seal rings for DRC check (it is a non-mask-tooling layer, only used for DRC check)	4B.7.4 The CLVS structure is used only for the mechanical support of the wirebond pad. Thus, no interconnection using CLVS is allowed. The CLVS structure is required in all low-k dielectric levels. No CLVS structure is allowed in the oxide dielectric levels. As Metal Dummy (MnDummy) are required for every design in 65nm generation, one must add both metal dummy block (MnDMBK) to the bond pads at all metal layers used. Please refer to the 65nm MASK TOOLING INFORMATION for details. 65nm bond pad structure consists of both transfer pad (L1/L2/L3) and metal pad (M1 and 1x Metal in low-k).A "Pad area mark layer", with the GDS number 90(0), also needs to be drawn on each pad for DRC check . The DRC check will exclude metal density check within bonding pad area. This mark layer size is the same as the Al pad size. under under under under Delete 13 Antenna Rule(ATN) ≧3 5.Die Seal Ring Rules Due to the reliability concern, main chips must be surrounded by two seal rings A “SEAL_RING_MARK” layer, with the GDS number 86(36),also needs to be drawn on die seal rings and corner filler area for DRC check (it is a non-mask-tooling layer, only used for DRC check)	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.1	1	11/11/2005	5.1 1A NA DSR.W≧4.5(M1) DSR.S≧2 DSR.R NA DF.W.DSR≧4.5 CTB.S.DSR≧1.5 Mn.W.DSR=4.5 Mn-1XVBn.EN.DSR(n=1,2,3,4,5) Mn-VBm.EN.DSR(n=1~9) 2XMn.W.DSR Mn-2XVBn.EN.DSR(n=6,7)≧0.32 W7 4XMn.W.DSR(n=9,10) Mn-4XVBn.EN.DSR(n=8,9)≧0.32 W.9 NA W.10 L2-SLE.S.DSR S.8 S.10≧0.75 14.1 DFM PLY_G.P.RCM≦ 370 mm PLY-DF.S1.RCM PLY-DF.S.RCM 14.2 Design Guidelines:#9	5.1 Excluding corner fillers. 1B. Within 150um square area, fillers are unnecessary to rotate 45 o. Note: Filler is within SEALRMARK (Seal Ring Mark Layer) layer. DSR.W≧5(METAL1) DSR.S≧1 n=7,8,9 DSR.R3 DF.W.DSR≧5 CTB.S.DSR≧1.3 Mn.W.DSR=5.0 1XMn-VBn.EN.DSR(n=1,2,3,4,5,6) Mn-VBm.EN.DSR(n=6,7,8,9) Delete 2XMn-VBn.EN.DSR(n=7,8)≧0.4 W6 TMn.W.DSR(n=10) 4XMn-4XVBn.EN.DSR(n=9)≧0.6 W.8 Vn-Vm.S.DSR W.9 Delete S.9 S.10≧1.0 14.1 DFM PLY_G.P.RCM≦ 0.34 um PLY-DF.S1.RCM:When the relative transistor width <0.2um PLY-DF.S.RCM: When the relative transistor width <0.2um Delete	

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T.2	1	12/09/2005	4A.3 DNW-PW.EN : DEEP_N_WELL overlap of N_WELL 4A.11 Revision history : PPNRS-LLH.S PPNRS-LLH.S:NA 5.2 1XMn-VBn.EN.DSR: METAL_n enclosure of 1x MVIAn_BAR (n=1,2,3,4,5,6) DSR.R2 : NA 2XVBn.S.DSR : 1.5 4XMn-4XVBn.EN.DSR :4x METAL_n enclosure of 4x MVIAn_BAR (n=9)	4A.3 DNW-PW.EN : DEEP_N_WELL enclosure of P_WELL 4A.11 Revision history : Delete 5.2 1XMn-VBn.EN.DSR: 1x METAL_n enclosure of MVIAn_BAR (n=1,2,3,4,5,6) DSR.R2 : ring 2XVBn.S.DSR : 1.3 4XMn-VBn.EN.DSR :4x METAL_n enclosure of MVIAn_BAR (n=9)	
T.3	1	03/16/2006	3.Mask Layer Definitions : Digitized Pattern Diffusion Poly Contact Metal1 Mvia1 Metal2 Mvia2 Metal3 Mvia3 Metal4 Mvia4 Metal5 Mvia5 Metal6 Mvia6 Metal7 Mvia7 Metal8 Mvia8 Metal9 Mvia9 Metal10 TMV-RDL AL-RDL PASV-RDL CU-FUSE-PAD 4B.7.2 L2-WELL.S6 exclude of L2-DF.S9 exclude of L2-PLY.S8 exclude of L2-Mn.S7 exclude of	3.Mask Layer Definitions : Digitized Pattern DIFFUSION POLY1 CONTACT METAL1 MVIA1 METAL2 MVIA2 METAL3 MVIA3 METAL4 MVIA4 METAL5 MVIA5 METAL6 MVIA6 METAL7 MVIA7 METAL8 MVIA8 METAL9 MVIA9 METAL10 TMV_RDL AL_RDL PASV_RDL CU_FUSE_PAD 4B.7.2 L2-WELL.S6 excluded from L2-DF.S9 excluded from L2-PLY.S8 excluded from L2-Mn.S7 excluded from	Just align ! TYPO !

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.3	1	03/16/2006	4 Rule No Label DF.W DF.WX W.1 DF.W1 DF.S DF.S1 NW.W NW.S NW.S1 NW-N_DF.S NW-P_DF.S NW-N_DF.S.TG NW-N_DF.EN NW-P_DF.EN NW-P_DF.EN.TG NWR.W NWR.WX W.1 NWR.S NWR-NW.S DNW.W DNW.S DNW-N_DF.S PW.S PW.S.TG DNW-PG.S DNW-PG.EN NW-DNW.EN DNW-PW.EN LLH.W LLH.S LLH-PLY_G.S LLH-PLY_G.EN LLH-NW.S LLH-TG.S LLH-NW.OH NW-LLH.OH NW-LLH.OL NT.W NT.S NT-DF.S NT-NW.S NT-DF.EN PLY.W.NT DIB.W DIB.S DIB-DF.S DIB-NW.S DIB-TG.S DIB-DIODE.EN TG.W TG.S TG-PLY_G.S TG-NW.S TG-NW.OH NW-TG.OH TG-NW.OL TG-PLY_G.EN	4 Rule No Label DF.W1 DF.WX Delete DF.W2 DF.S1 DF.S2 NW.W1 NW.S1 NW.S2 NW-N_DF.S3 NW-P_DF.S4 NW-N_DF.S5.TG NW-N_DF.EN1 NW-P_DF.EN2 NW-P_DF.EN3.TG NWR.W1 NWR.WX Delete NWR.S1 NWR-NW.S2 DNW.W1 DNW.S1 DNW-N_DF.S2 PW.S3 PW.S4.TG DNW-PG.S5 DNW-PG.EN1 NW-DNW.EN2 DNW-PW.EN3 LLH.W1 LLH.S1 LLH-PLY_G.S2 LLH-PLY_G.EN1 LLH-NW.S3 LLH-TG.S4 LLH-NW.OH1 NW-LLH.OH2 NW-LLH.OL1 NT.W1 NT.S1 NT-DF.S2 NT-NW.S3 NT-DF.EN1 PLY.W2.NT DIB.W1 DIB.S1 DIB-DF.S2 DIB-NW.S3 DIB-TG.S4 DIB-DIODE.EN1 TG.W1 TG.S1 TG-PLY_G.S2 TG-NW.S3 TG-NW.OH1 NW-TG.OH2 TG-NW.OL1 TG-PLY_G.EN1	Just align Rule No & Label !

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
T.3	1	03/16/2006	PLY_NG.W PLY_PG.W PLY_ICN.W W.1 PLY_G.S PLY_G.S1 PLY_F.S PLY_F.S.TG PLY-DF.S PLY-DF.S1 PLY-DF.S2 PLY-DF.S3 PLY_F-DF.S PLY_F-DF.S1 PLY-DF.OH PLY-DF.OH1 PLY-DF.OH2 DF-PLY_G.OH OH.3 PLY_G.R PLY_G.R1 PLY.R1 R.1 NSD.W NSD.S NSD-P_DF.S.NW NSD-P_DF.S.PW NSD-PLY_PG.S NSD-N_DF.EN.NW NSD-N_DF.EN.PW NSD-PLY_NG.EN N_DF-P_PU.SX.PW NPBJ-PLY_PG.S NPBJ-PLY_NG.S NSD-CT_P_DF.S N_DF-P_DF.S NSD-CT_N_DF.EN P_DF-NSD.OH NSD-DF.OL PSD.W PSD.S PSD-N_DF.S.NW PSD-N_DF.S.PW PSD-PLY_NG.S PSD-P_DF.EN.PW PSD-P_DF.EN.NW PSD-PLY_PG.EN P_DF-N_PU.SX.NW NPBJ-PLY_NG.S NPBJ-PLY_PG.S PSD-CT_N_DF.S P_DF-N_DF.S PSD-CT_P_DF.EN N_DF-PSD.OH PSD-DF.OL	PLY_NG.W1 PLY_PG.W2 PLY_ICN.W3 W.3 PLY_G.S1 PLY_G.S PLY_F.S2 PLY_F.S.TG PLY-DF.S3 PLY-DF.S4 PLY-DF.S5 PLY-DF.S8 PLY_F-DF.S6 PLY_F-DF.S7 PLY-DF.OH1 PLY-DF.OH2 PLY-DF.OH3 DF-PLY_G.OH4 OH.4 PLY_G.R1 PLY_G.R2 PLY.R3 R.3 NSD.W1 NSD.S1 NSD-P_DF.S2.NW NSD-P_DF.S3.PW NSD-PLY_PG.S4 NSD-N_DF.EN1.NW NSD-N_DF.EN2.PW NSD-PLY_NG.EN3 N_DF-P_PU.S5.PW NPBJ-PLY_PG.S6 NPBJ-PLY_NG.S7 NSD-CT_P_DF.S8 N_DF-P_DF.S9 NSD-CT_N_DF.EN4 P_DF-NSD.OH1 NSD-DF.OL1 PSD.W1 PSD.S1 PSD-N_DF.S2.NW PSD-N_DF.S3.PW PSD-PLY_NG.S4 PSD-P_DF.EN1.PW PSD-P_DF.EN2.NW PSD-PLY_PG.EN3 P_DF-N_PU.S5.NW NPBJ-PLY_NG.S6 NPBJ-PLY_PG.S7 PSD-CT_N_DF.S8 P_DF-N_DF.S9 PSD-CT_P_DF.EN4 N_DF-PSD.OH1 PSD-DF.OL1	

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T.3	1	03/16/2006	SAB.W	SAB.W1	
			SAB.S	SAB.S1	
			SAB-DF.S	SAB-DF.S2	
			SAB-PLY.S	SAB-PLY.S3	
			SAB-CT.S	SAB-CT.S4	
			SAB-NDNRS.OH	SAB-NDNRS.OH1	
			SAB-PPNRS.OH	SAB-PPNRS.OH2	
			SAB.R	SAB.R1	
			SAB.R1	SAB.R2	
			SAB.R2	SAB.R3	
			PPNRS.W	PPNRS.W2	
			PPNRS.L	PPNRS.L1	
			PPNRS.S	PPNRS.S5	
			PPNRS-NW.S	PPNRS-NW.S6	
			PSD-NDNRS.S	PSD-NDNRS.S7	
			NSD-PPNRS.S	NSD-PPNRS.S8	
			NW-PPNRS.EN	NW-PPNRS.EN1	
			PSD-PPNRS.EN	PSD-PPNRS.EN2	
			TG-PPNRS.EN	TG-PPNRS.EN3	
			PPNRS-TG.S	PPNRS-TG.S9	
			NDNRS.W	NDNRS.W3	
			NDNRS.L	NDNRS.L2	
			SBLK.W	SBLK.W1	
			SBLK.S	SBLK.S1	
			SBLK-SA B.S	SBLK-SA B.S2	
			SBLK-DF.S	SBLK-DF.S3	
			SBLK-PLY.S	SBLK-PLY.S4	
			SBLK-CT.S	SBLK-CT.S5	
			SBLK-DF.OH	SBLK-DF.OH1	
			SBLK-PLY.OH	SBLK-PLY.OH2	
			PLY-SBLK.OH	PLY-SBLK.OH3	
			SBLK-PLY.OL	SBLK-PLY.OL1	
			CT.SZ	CT.SZ1	
			CT.S	CT.S1	
			CT.S1	CT.S	
			CT.S2	CT.S2	
			CT_DF-PLY.S	CT_DF-PLY.S3	
			CT_PLY-DF.S	CT_PLY-DF.S4	
			PLY-CT.EN	PLY-CT.EN1	
			PLY-CT.EN1	PLY-CT.EN2	
			DF-CT.EN	DF-CT.EN3	
			DF-CT.EN1	DF-CT.EN4	
			CT.R	CT.R1	
			CT.R1	CT.R2	
			CT.R.RCM	CT.R3.RCM	
			PESD.W	PESD.W1	
			PESD.S	PESD.S1	
			MOAT.W	MOAT.W1	
			MOAT.S	MOAT.S1	
			MOAT-NW.S	MOAT-NW.S2	
			MOAT-DF.S	MOAT-DF.S3	
			MOAT-NT.S	MOAT-NT.S4	
			M1.W	M1.W1	
			M1.WX W.1	M1.WX Delete	
			M1.S	M1.S1	
			M1.S1	M1.S2	
			M1.S2	M1.S3	
			M1-CT.EN	M1-CT.EN1	
			M1-CT.EN1	M1-CT.EN2	
			M1-CT.EN2	M1-CT.EN3	
			M1-CT.EN3	M1-CT.EN4	
			M1-CT.EN4	M1-CT.EN5	
			M1-CT.EN5	M1-CT.EN6	
			M1.A	M1.A1	
			M1.EA	M1.EA1	
			M1.R	M1.R1	
			M1.R1	M1.R2	

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T.3	1	03/16/2006	1XMn.W 1XMn.WX W.1 1XMn.S 1XMn.S1 1XMn.S2 1XMn-1XVm.EN 1XMn-1XVm.EN1 1XMn-1XVm.EN2 1XMn-1XVm.EN3 1XMn.A 1XMn.EA 1XMn.R V1.SZ V1.S V1.S1 V1.S2 M1-V1.EN M1-V1.EN1 M1-V1.EN2 Enclosure EN.3 M1-V1.EN3 M1-V1.EN4 M1-V1.EN5 V1-M1.OH OH.1 V1.R V1.R1 V1.R2 R.2 V1.R3 R.2 V1.R4 R.3 V1.R5 1XVn.SZ 1XVn.S 1XVn.S1 1XVn.S2 1XMn-1XVn.EN 1XMn-1XVn.EN1 1XMn-1XVn.EN2 enclosure EN.1 1XMn-1XVn.EN3 1XMn-1XVn.EN4 1XMn-1XVn.EN5 1XVn.R 1XVn.R1 1XVn.R2 R.2 1XVn.R3 R.2 1XVn.R4 R.3 1XVn.R5 2XMn.W 2XMn.WX W.1 2XMn.S 2XMn.S1 2XMn.S2 2XMn-2XVm.EN 2XMn.A 2XMn.EA 2XVn.SZ 2XVn.S 2XMn-2XVn.EN 2XMn-2XVn.EN1 2XMn-2XVn.EN2 2XMn-2XVn.EN3 2XVn.R 2XVn.R1 2XVn.R2 R.2 2XVn.R3 R.2 2XVn.R4	1XMn.W1 1XMn.WX Delete 1XMn.S1 1XMn.S2 1XMn.S3 1XMn-1XVm.EN1 1XMn-1XVm.EN2 1XMn-1XVm.EN3 1XMn-1XVm.EN4 1XMn.A1 1XMn.EA1 1XMn.R1 V1.SZ1 V1.S1 V1.S2 V1.S3 M1-V1.EN1 M1-V1.EN2 M1-V1.OH1 overhang OH.1 M1-V1.EN4 M1-V1.EN5 M1-V1.EN6 V1-M1.OH2 OH.2 V1.R1 V1.R2 V1.R3 R.3 V1.R4 R.4 V1.R5 R.5 V1.R6 1XVn.SZ1 1XVn.S1 1XVn.S2 1XVn.S3 1XMn-1XVn.EN1 1XMn-1XVn.EN2 1XMn-1XVn.OH1 overhang OH.1 1XMn-1XVn.EN4 1XMn-1XVn.EN5 1XMn-1XVn.EN6 1XVn.R1 1XVn.R2 1XVn.R3 R.3 1XVn.R4 R.4 1XVn.R5 R.5 1XVn.R6 2XMn.W1 2XMn.WX Delete 2XMn.S1 2XMn.S2 2XMn.S3 2XMn-2XVm.EN1 2XMn.A1 2XMn.EA1 2XVn.SZ1 2XVn.S1 2XMn-2XVn.EN1 2XMn-2XVn.EN2 2XMn-2XVn.EN3 2XMn-2XVn.EN4 2XVn.R1 2XVn.R2 2XVn.R3 R.3 2XVn.R4 R.4 2XVn.R5	

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T.3	1	03/16/2006	4XMn.W	4XMn.W1	
			4XMn.WX W.1	4XMn.WX Delete	
			4XMn.S	4XMn.S1	
			4XMn.S1	4XMn.S2	
			4XMn-4XVm.EN	4XMn-4XVm.EN1	
			4XMn.A	4XMn.A1	
			4XMn.EA	4XMn.EA1	
			4XVn.SZ	4XVn.SZ1	
			4XVn.S	4XVn.S1	
			4XMn-4XVn.EN	4XMn-4XVn.EN1	
			4XVn.R	4XVn.R1	
			4XVn.R1	4XVn.R2	
			L3.W	L3.W1	
			L3.L	L3.L1	
			L3.P	L3.P1	
			L3.S	L3.S1	
			L1.SZ	L1.SZ1	
			L2.S	L2.S2	
			L3-L1.S	L3-L1.S3	
			L1.S	L1.S4	
			L2-DSR.S	L2-DSR.S5	
			L2-WELL.S	L2-WELL.S6	
			L2-DF.S S.6	L2-DF.S9 S.9	
			L2-PLY.S S.6	L2-PLY.S8 S.8	
			L2-Mn.S	L2-Mn.S7	
			SL-SLP.EN	SL-SLP.EN1	
			SL.W	SL.W2	
			L2-L1.EN	L2-L1.EN2	
			L2-L3.EN	L2-L3.EN3	
			1XMn.W.CLVS	1XMn.W1.CLVS	
			1XMn.S.CLVS	1XMn.S1.CLVS	
			1XMn-L3.OH.CLVS	1XMn-L3.OH1.CLVS	
			1XMn-1XVm.EN.CLVS	1XMn-1XVm.EN1.CLVS	
			1XMn-1XVn.EN.CLVS	1XMn-1XVn.EN2.CLVS	
			EN.1	EN.2	
			1XVn.SZ.CLVS	1XVn.SZ1.CLVS	
			1XVn.S.CLVS	1XVn.S2.CLVS	
			DSR.W	DSR.W1	
			DSR.S	DSR.S1	
			DSR-AC.S	DSR-AC.S2	
			DSR.R	DSR.R1	
			DSR.R1	DSR.R2	
			DSR.R2	DSR.R3	
			DSR.R3	DSR.R4	
			DF.W.DSR	DF.W2.DSR	
			DF.WX.DSR	DF.WX.DSR Delete	
			W.2	DF-CTB.EN1.DSR	
			DF-CTB.EN.DSR	CTB.W3.DSR	
			CTB.W.DSR	CTB.S3.DSR	
			CTB.S.DSR	M1.W4.DSR	
			M1.W.DSR	M1-CTB.EN2.DSR	
			M1-CTB.EN.DSR	1XMn-VBn.EN3.DSR	
			1XMn-VBn.EN.DSR	Mn-VBm.EN4.DSR	
			Mn-VBm.EN.DSR	1XVBn.W5.DSR	
			1XVBn.W.DSR	1XVBn.S4.DSR	
			1XVBn.S.DSR	1XVn-1XVm.S5.DSR	
			1XVn-1XVm.S.DSR	2XMn-VBn.EN5.DSR	
			2XMn-VBn.EN.DSR	2XVBn.W6.DSR	
			2XVBn.W.DSR	2XVBn.S6.DSR	
			2XVBn.S.DSR	TMn.W7.DSR	
			TMn.W.DSR	4XMn-VBn.EN6.DSR	
			4XMn-VBn.EN.DSR	4XVBn.W11.DSR	
			4XVBn.W.DSR	W.11	
			W.8	4XVBn.S7.DSR	
			4XVBn.S.DSR	Vn-Vm.S10.DSR	
			Vn-Vm.S.DSR		

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T.3	1	03/16/2006	S.8 L1B.W.DSR W.9 LM-L1B.EN.DSR EN.7 L2.W.DSR W10. L2-L1B.EN.DSR EN.8 Mn-SLE.S.DSR S.9 L3-L2.S.DSR S.10 L3.W.DSR W.11 DCA.L L2_L.W L2_L.S L2_L.S1 L1.SZ L1.S LM-L1.EN L2_L-L1.EN L2.W.L2SLOT L2SLOT.W L2SLOT.WX W.2 L2SLOT.L L2SLOT.LX L.1 L2SLOT.S L2SLOT.SX S.1 L2SLOT-Mn.S L2SLOT-Mn.SX S.2 L2SLOT.R L2SLOT.R1	S.10 L1B.W8.DSR W.8 LM-L1B.EN6.DSR EN.6 L2.W9.DSR W.9 L2-L1B.EN7.DSR EN.7 Mn-SLE.S8.DSR S.8 L3-L2.S9.DSR S.9 L3.W10.DSR W.10 DCA.L1 L2_L.W1 L2_L.S1 L2_L.S L1.SZ1 L1.S2 LM-L1.EN1 L2_L-L1.EN2 L2.W1.L2SLOT L2SLOT.W2 L2SLOT.WX Delete L2SLOT.L1 L2SLOT.LX Delete L2SLOT.S1 L2SLOT.SX Delete L2SLOT-Mn.S2 L2SLOT-Mn.SX Delete L2SLOT.R1 L2SLOT.R2	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	3. Mask Layer Definitions: LV_NLDD Define SP family NMOS devices and 1.0V/1.8V Native NMOS devices HV_NLDD Define 1.8V/2.5V/3P3V_GOX52 NMOS and 1.8V Native NMOS devices TMV_RDL Define 11th Metal and Al-Pad Contacts N+ Diffusion (Diffusion not over P+) not over Poly none	3. Mask Layer Definitions: LV_NLDD Define SP family NMOS devices and 1.0VNative NMOS devices HV_NLDD Define 1.8V/2.5V NMOS and 1.8V Native NMOS devices TMV_RDL Define 10th Metal and Al-Pad Contacts N+ Diffusion (Diffusion over N+) not over Poly N+ Diffusion non-salicide resistor (Diffusion over SAB) over N+ P+ Diffusion non-salicide resistor (Diffusion over SAB) over P+ N+ POLY1 non-salicide resistor (POLY1 over SAB) over N+ P+ POLY1 non-salicide resistor (POLY1 over SAB) over P+ N+ POLY1 non-salicide resistor body N+ POLY1 non-salicide resistor AND SAB P+ POLY1 non-salicide resistor body P+ POLY1 non-salicide resistor AND SAB MOS Transistor structure consists drain/source/gate/substrate	typo
			4.0.2 Abbreviations NCAP/VARACTOR Device	4.0.2 Abbreviations NCAP/ MIS_VAR Device	typo

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	4A.1 DIFFUSION (DF) Layer DF.W.TG DIFFUSION width [for device over TG]≧0.32 Spacing and notch of DIFFUSION to [DIFFUSION touch TG] None none	4A.1 DIFFUSION (DF) Layer DIFFUSION width [over TG of 1.8V device] DIFFUSION width [over TG of 2.5V device] Spacing and notch of DIFFUSION to [DIFFUSION touching TG] DF.W.TG33GOX52 DIFFUSION width [over TG and 3P3V_GOX52_IMPLANT_MARK of 3.3V device]≧0.32 DIFFUSION width [over TG of 3.3V device] ≧ 0.32	
			4A.4 LL_HVT (LLH) Layer NONE	4A.4 LL_HVT (LLH) Layer If LL_HVT and N_WELL have a common run >= 0.36, then a overhang of zero is allowed along the common run Plot modify	
			NONE	4A.5 LL_LVT (LLL) Layer	
			4A.6 NATIVE DEVICE (NT) Layer NT.S1 Spacing of NATIVE S.1≧TBD NONE NONE PLY.W2.NT POLY1 width for 1.0V/1.2V/1.8V/2.5V NATIVE device W.2≧TBD	4A.6 NATIVE DEVICE (NT) Layer NT.S1 Spacing and notch of NATIVE S.1≧TBD NT-TG.S4 Spacing of NATIVE to TG S.4≧TBD NT-NRS.S5 Spacing of NATIVE to N+/P+ POLY1 non-salicide resistor body S.5≧TBD PLY_NT.W2 POLY1 width for NATIVE device over NATIVE but not over TG W.2≧TBD	
			4A.7 DIODE_IMP_BLOCK (DIB) DIB.W1 DIODE_IMP_BLOCK width W.1≧ 0.40 DIB.S1 Spacing and notch of DIODE_IMP_BLOCK S.1≧0.40 DIB-NW.S3 Spacing of DIODE_IMP_BLOCK to N_WELL S.3≧0.40 DIB-TG.S4 Spacing of DIODE_IMP_BLOCK to TG S.4≧0.40	4A.7 DIODE_IMP_BLOCK (DIB) DIB.W1 DIODE_IMP_BLOCK width W.1≧0.36 DIB.S1 Spacing and notch of DIODE_IMP_BLOCK S.1≧0.36 DIB-NW.S3 Spacing of DIODE_IMP_BLOCK to N_WELL S.3≧0.36 DIB-TG.S4 Spacing of DIODE_IMP_BLOCK to TG S.4≧0.36	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	4A.8 TG Layer TG.W1 TG width W.1≧0.44 TG.S1 Spacing and notch of TG S.1≧0.44 TG-NW.S3 Spacing of TG to N_WELL S.3≧0.44 TG-NW.OH1 TG overhang of N_WELL OH.1≧0.44 NW-TG.OH2 N_WELL overhang of TG OH.2≧ 0.44 TG-NW.OL1 TG overlap of N_WELL OL.1 ≧ 0.44 TG-NW.R If TG and N_WELL have a common run >= 0.44, then a spacing of zero is allowed along the common run R Yes NONE NONE NONE	4A.8 TG Layer TG.W1 TG width W.1≧0.40 TG.S1 Spacing and notch of TG S.1≧0.40 TG-NW.S3 Spacing of TG to N_WELL S.3≧0.36 TG-NW.OH1 TG overhang of N_WELL OH.1≧0.36 NW-TG.OH2 N_WELL overhang of TG OH.2≧0.36 TG-NW.OL1 TG overlap of N_WELL OL.1 ≧0.36 TG-NW.R1 If TG and N_WELL have a common run >= 0.36, then a spacing of zero is allowed along the common run R1 Yes TG-NW.R2 If TG and N_WELL have a common run >= 0.36, then a overhang of zero is allowed along the common run R2 Yes TG-NW.R3 If TG and LL_HVT have a common run >= 0.36, then a overhang of zero is allowed along the common run Yes TG-NW.R4 If TG and LL_LVT have a common run >= 0.36, then a overhang of zero is allowed along the common run Yes Plot modify	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	4A.9 POLY1 (PLY) Layer none	4A.9 POLY1 (PLY) Layer PLY.W.TG18 POLY1 width over [TG (for 1.8V device)]≧0.18 PLY.W.TG33 POLY1 width over TG of 3.3V device (for 3.3V+/-10% voltage tolerance) ≧0.37	
			none	PLY_G.R4 Spacing of parallel POLY1 gates when POLY1 gates width=0.06 um and POLY1 gate pitch < 0.34um (This is recommended rule, customer can select if DRC check applies) =0.16 or 0.20	
			PLY-DF.S3 Spacing of POLY1 end cap to related DIFFUSION S.3≧0.055 PLY-DF.S4 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION ≦ 0.3um S.4≧0.055 PLY-DF.S5 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION > 0.3um S.5≧0.075 PLY_F-DF.S7 Spacing of POLY1 on field to DIFFUSION S.7≧0.055 PLY-DF.OH1 POLY1 overhang of DIFFUSION OH.1≧ 0.12 None PLY-DF.OH3 POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧0.05um≧ 0.16 DF-PLY_G.OH4 DIFFUSION overhang of POLY1 Gate OH.4 ≧0.14 DF-PLY_G.OH.TG DIFFUSION overhang of POLY1 Gate over TG ≧ 0.20 None	PLY-DF.S3 Spacing of POLY1 end cap to related DIFFUSION S.3≧ 0.05 PLY-DF.S4 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION ≦ 0.3umS.4≧0.05 PLY-DF.S5 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION > 0.3um S.5≧0.07 PLY_F-DF.S7 Spacing of POLY1 on field to DIFFUSION S.7≧0.05 PLY-DF.OH1 POLY1 endcap OH.1 ≧0.12 PLY-DF.OH5 POLY1 overhang of DIFFUSION OH.5 ≧0.11 PLY-DF.OH3 POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um OH.3 ≧0.16 DF-PLY_G.OH4 DIFFUSION overhang of POLY1 Gate OH.4 ≧0.135 DF-PLY_G.OH.TG DIFFUSION overhang of POLY1 Gate over TG≧0.175	

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0.1	1	08/21/2006	4A.10 N+ implant (NSD) Layer 4A.10.1 N+/P+ Butting Rules NSD-P_DF.S3.PW Spacing of N+ IMPLANT to [P+ DIFFUSION over P_WELL] S.3≧ 0.03 NSD-N_DF.EN1.NW N+IMPLANT enclosure of [N+ DIFFUSION over N_WELL] EN.1 ≧ 0.03 N_DF-P_PU.S5.PWSpacing of N+ DIFFUSION to the nearest [P+ pick-up within P_WELL] - I/O, RAM, ROM, capacitor and diode are excepted S.5 ≦ 20	4A.10 N+ implant (NSD) Layer 4A.10.1 N+/P+ Butting Rules NSD-P_DF.S3.PW Spacing of N+ IMPLANT to [P+DIFFUSION over P_WELL] S.3≧ 0.02 NSD-N_DF.EN1.NW N+ IMPLANT enclosure of [N+ DIFFUSION over N_WELL] EN.1 ≧0.02 N_DF-P_PU.S5.PW Spacing of N+ DIFFUSION to the nearest [P+ pick-up within P_WELL] - I/O, RAM, ROM, capacitor and diode are excepted S.5≦30	
			4A.11 P+ implant (PSD) Layer 4A.11.1 N+/P+ Butting Rules PSD-N_DF.S2.NW Spacing of P+ IMPLANT to [N+ DIFFUSION over N_WELL] S.2≧0.03 PSD-P_DF.EN1.PW P+ IMPLANT enclosure of [P+ DIFFUSION over P_WELL] EN.1≧0.03 P_DF-N_PU.S5.NWSpacing of P+ DIFFUSION to the nearest [N+ pick-up within N_WELL] - I/O, RAM, ROM, capacitor and diode are excepted S.5≦20	4A.11 P+ implant (PSD) Layer 4A.11.1 N+/P+ Butting Rules PSD-N_DF.S2.NW Spacing of P+ IMPLANT to [N+ IFFUSION over N_WELL] S.2≧0.02 PSD-P_DF.EN1.PW P+ IMPLANT enclosure of [P+ DIFFUSION over P_WELL] EN.1≧0.02 P_DF-N_PU.S5.NW Spacing of P+ DIFFUSION to the nearest [N+ pick-up within N_WELL] - I/O, RAM, ROM, capacitor and diode are excepted S.5≦30	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	4A.12.1 SAB Layer (SAB) layout Rules For Non-Salicide Resistor PPNRS.W2 Width of P+_POLY1 non-salicide resistor W.2≧0.44 PPNRS.L1 Length of P+_POLY1 non-salicide resistor L.1 ≧0.88 none TG-PPNRS.EN3 TG enclosure of P+_POLY1 non-salicide resistor body≧0.48 PPNRS-TG.S9 Spacing of P+ POLY1 non-salicide resister body toTG≧0.48 NDNRS.W3 Width of N+_DIFFUSION non-salicide resistor W.3≧ 0.48 NDNRS.L2 Length of N+_DIFFUSION non-salicide resistor L.2≧0.96	4A.12.1 SAB Layer (SAB) layout Rules For Non-Salicide Resistor PPNRS.W2 Width of P+_POLY1 non-salicide resistorW.2≧0.36 PPNRS.L1 Length of P+_POLY1 non-salicide resistor L.1≧0.70 NSD-NPNRS.EN3 N+ implant enclosure of P+_POLY1 non-salicide resistor EN.3 ≧0.22 TG-PNRS.EN4 TG enclosure of N+/P+_POLY1 non-salicide resistor body ≧0.48 PNRS-TG.S9 Spacing of N+/P+ POLY1 non-salicide resister body toTG ≧0.48 DNRS.W3 Width of N+/P+_DIFFUSION non-salicide resistor W.3≧0.36 DNRS.L2 Length of N+/P+_DIFFUSION non-salicide resistor L.2≧0.70 Plot modify	
			4A.13 CONTACT (CT) Layer CT_PLY-DF.S4 Spacing of POLY1_CONTACT to DIFFUSION S.4≧0.075	4A.13 CONTACT (CT) Layer CT_PLY-DF.S4 Spacing of POLY1_CONTACT to DIFFUSION S.4≧0.07	
			4A.14 BIPOLAR (BP) Layer BP.W BIPOLAR width ≧0.40 BP.S Spacing and notch of BIPOLAR ≧0.40	4A.14 BIPOLAR (BP) Layer BP.W BIPOLAR width ≧0.36 BP.S Spacing and notch of BIPOLAR ≧0.36	
			NONE	4A.17 MIS_IMPLANT_BLOCK Layer	
			NONE	4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Not tooling) :	
			NONE	4A.19 CAD_UD_MARK (UD) Layer Layout Rules (Not tooling) :	
			NONE	4A.21 EFUSE_MARK Layer	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.1	1	08/21/2006	4B.1 METAL1 (M1) Layer M1-CT.EN5 METAL1 line end enclosure of CONTACT if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e.. d1, d2, d3≦ 0.12um) EN.5 ≧0.06 M1-CT.EN6 METAL1 line end enclosure of CONTACT can be released when METAL1 has redundant CONTACTs except when d1,d2,d3,d4,d5,d6 ≦0.12um. When d1,d2,d3,d4,d5,d6 ≦ 0.12um and one end METAL1 enclosure drawn between 0.03 to 0.06um,the minimum enclosure of the other end METAL1 is 0.06um. EN.6 ≧0.03	4B.1 METAL1 (M1) Layer M1-CT.EN5 METAL1 line end enclosure of CONTACT if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e.. d1, d2, d3≦ 0.12um) EN.5 ≧0.04 delete	
			4B.1.2 METAL2 and above (1XMn) -- 1x pitch METAL_n : (n=2,3,4,5,6) 1XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 0.50um](n=2,3,4,5,6)≧0.18 none 1XMn.R1 45 degrees METAL_n is not allowed (n=2, 3, 4, 5, 6) except Die Seal Ring and Die corner within 150um area.See section 5.1 for details.(*1) R.1 Yes	4B.1.2 METAL2 and above (1XMn) -- 1x pitch METAL_n : (n=2,3,4,5,6) 1XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 0.50um](n=2,3,4,5,6)≧0.16 1XMn-1XVm.EN5 METAL_n line end enclosure of MVIA_n-1 if METAL_n width ≦ 0.11um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.12um (i.e. d1, d2 and d3 ≦ 0.12um)EN.5≧0.04 1XMn.R In manhattan routing, 45 degrees METAL_n is not allowed (n=2,3,4,5,6,7) except Die Seal Ring and Die corner within 150um area. Please refer to section 5.1 for details. R.1 Yes plot modify	
			none	4B.2.1 X-Architecture of 1 x pitch Metal	

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0.1	1	08/21/2006	4B.3 MVIA1 (V1) Layer V1.S1 Spacing of MVIA1 to MVIA1when MVIA1 sharing a common Metal shape above or below (equal-potential) S.1 ≧0.10 V1.S2 Spacing of MVIA1 when MVIA1 NOT sharing a common Metal shape above or below (non-equal-potential) ≧0.11 V1.S3 Spacing of MVIA1 to MVIA1 spacing for ≧ 3X3 MVIA1 array group. An array group is an array where spacing < 0.18um. ≧0.14 M1-V1.EN5 METAL1 line end enclosure of MVIA1 if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) EN.5 ≧0.06 M1-V1.EN6 METAL1 line end enclosure of MVIA1 can be released when METAL1 has redundant MVIA1 except when d1,d2,d3,d4,d5,d6 ≦ 0.12um. When d1,d2,d3,d4,d5,d6 ≦ 0.12um and one end METAL1 enclosure drawn between 0.03 to 0.06um, the other end METAL1 enclosure has to be larger than 0.06um. EN.6 ≧ 0.03 V1-M1.OH2 MVIA1 overhang of [METAL1 with width < 0.10 um] OH.2 ≧ 0.005 V1.R1 MVIA1 must touch METAL1 R.1 Yes	4B.3 MVIA1 (V1) Layer V1.S1 Spacing of MVIA1 S.1≧0.10 V1.S2 Spacing of MVIA1 with 3 or more neighboring MVIA1 ("Neighboring" is defined as having spacing of < 0.14um.)S.2≧0.11 V1.S3 Spacing of MVIA1 for ≧ 3X3 array group (An "array group" is defined as an array where spacing <0.14um.) S.3≧0.13 M1-V1.EN5 METAL1 line end enclosure of MVIA1 if METAL1 width ≦ 0.11um and the spacing of METAL1 line to three adjacent METAL1 patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) EN.5 ≧0.04 Delete V1-M1.OH2 MVIA1 overhang of [METAL1 with width < 0.10 um] OH.2 <0.005 V1.R1 MVIA1 must be within METAL1 when METAL1 width ≧ 0.10 um R.1 Yes Plot modify	

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0.1	1	08/21/2006	4B.3.2 MVIA2 and above (1XVn) -- 1x pitch MVIA_n Layer (n=2,3,4,5) 1XVn.S1 Spacing of MVIA_n when MVIA_n sharing a common Metal shape above or below (equal-potential) S.1≧0.10 1XVn.S2 Spacing of MVIA_n when MVIA_n NOT sharing a common Metal shape above or below (non-equal-potential)≧0.11 1XVn.S3 Spacing of MVIA_n for ≧ 3X3 1xMVIA_n array group. An array group is an array where spacing < 0.18um. ≧0.14 1XMn-1XVn.EN5 METAL_n line end enclosure of MVIA_n if METAL_n width ≦ 0.11um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) EN.5 ≧0.06 1XMn-1XVn.EN6 METAL_n line end enclosure of MVIA_n can be released when METAL_n has redundant MVIA_n except when d1,d2,d3,d4,d5,d6 ≦0.12um. When d1,d2,d3,d4,d5,d6 ≦ 0.12um and one end METAL_n enclosure drawn between 0.03 to 0.06um, the other end METAL_n enclosure has to be larger than 0.06um. EN.6 ≧0.03	4B.3.2 MVIA2 and above (1XVn) -- 1x pitch MVIA_n Layer (n=2,3,4,5) 1XVn.S1 Spacing of MVIA_n S.1≧0.10 1XVn.S2 Spacing of MVIA_n with 3 or more neighboring MVIA_n ("Neighboring" is defined as having spacing of < 0.14um.)S.2≧0.11 1XVn.S3 Spacing of MVIA_n for ≧ 3X3 array group (An "array group" is defined as an array where spacing <0.14um.) S.3≧0.13 1XMn-1XVn.EN5 METAL_n line end enclosure of MVIA_n if METAL_n width ≦ 0.11um and the spacing of METAL_n line to three adjacent METAL_n patterns ≦ 0.12um (i.e. d1, d2, d3 ≦ 0.12um) EN.5 ≧ 0.04 delete Plot modify	
			NONE	4B.3.3 X-Architecture of MVIA2 and above 1x pitch MVIA -- MVIA_n (n=2,3,4,5):	
			NONE	4B.7 4x pitch MVIA_n (4XVn) Layer Layout Rules: (n=8,9) 1XMn-4XVn.EN2 1x METAL enclosure of 4x MVIA directly above 1x METAL EN.2 ≧0	
			4B.8.2 Generic Pad Related Layout Guidelines : L2-DF.S9 Spacing of AL_RDL to DIFFISIUN(BOAC is excluded from this rule) S.9≧ 10 10 L2-PLY.S8 Spacing of AL_RDL to Poly1 (BOAC is excluded from this rule) S.8≧10 10	4B.8.2 Generic Pad Related Layout Guidelines : delete	

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0.1	1	08/21/2006	5. Die Seal Ring Rules 5.1 The die seal ring pattern window size is defined as the area between scribe line edge and active circuit (including the pad metal) edge. Two die seal rings are required.	5. Die Seal Ring Rules delete	
			5.1 Metal Stress Relief Rules for Die Corner Area (DCA)	5.1 Metal Stress Relief Rules for Die Corner Area (DCA) make-up arrangement	
			5.2 Schematic cross sectional view and related M1.W4.DSR METAL_n width, n=1,2,3,4,5,6 W.4 = 5.0 NONE Mn-VBm.EN4.DSR METAL_n+1 enclosure of MVIAn_BAR (n=6,7,8,9) EN.4 ≧0.1 L3-L2.S9.DSR Spacing of AL_RDL to PASV_RDL ring S.9≧1.0 NONE NONE	5.2 Schematic cross sectional view and related M1.W11.DSR METAL1 width, W.11 =5.0 1XMn.W4.DSR 1x METAL_n width W.4=5.0 delete L3-L2.S9.DSR Spacing of AL_RDL to PASV_RDL ring S.9≧0.5 Plot modify 5.3 Die Seal Ring added by customer 5.4 Die Seal Ring added by UMC	
			13.3 OPC Friendly Design Guidelines: none	13.3 OPC Friendly Design Guidelines: add half pitch table plot modify	
			none	Add L55SP shrinkable rules	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.2	1	12/12/2006	3. Mask Layer Definitions : P92 N_WELL Define N-Well implant region (*1) C UC0 DEEP_N_WELL Define DEEP N-WELL region (*1) C None P21 TG Define thick gate oxide formation (*1) D None	3. Mask Layer Definitions : P92 N_WELL Define N-Well implant region N_WELL C UC0 DEEP_N_WELL Define DEEP N-WELL region DEEP_N_WELL C PHF CELL_VTN Define SRAM NMOS device (*1) C P21 TG Define thick gate oxide formation TG D P31 HR Define high resistance Poly resistors HR C P3M MR Define medium resistance Poly resistors MR C	Define new mask layers and typo
			4. Topological Layout Rules: NT-DF.S2 Spacing of NATIVE to unrelated DIFFUSION≧TBD NT-DF.EN1 Exact NATIVE enclosure of DIFFUSION=TBD PLY_NT.W2 POLY1 width for NATIVE device over NATIVE but not over TG≧TBD None	4. Topological Layout Rules: NT-DF.S2 Spacing of NATIVE to unrelated DIFFUSION≧0.25 NT-DF.EN1 Exact NATIVE enclosure of DIFFUSION=0.25 PLY_NT.W2 POLY1 width for NATIVE device over NATIVE but not over TG≧0.2 PLY_NT.W3.TG18 POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device ≧ 1.0 1.1 PLY_NT.W3.TG25 POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device ≧1.2 1.33	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.2	1	12/12/2006	PLY_PG.W.TG33GOX52_2POLY1 width over TG and 3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V +-10% voltage tolerance) for PMOS ≧ 0.28 0.31 4A.2.1 N_WELL_RESISTOR(NWR) Layer NWR.S1 Spacing and notch of N_WELL_RESISTOR S.1≧2.20 NWR-NW.S2 Spacing of N_WELL_RESISTOR to N_WELL S.2≧2.20 NWR-N_DF.NW Exact spacing of N_WELL RESISTOR to N+ DIFFUSION within the same N_WELL (for N_WELL tap) = 0 None NWR.R N_WELL_RESISTOR must be within N_WELL Yes 4A.6 NATIVE DEVICE (NT) Layer NT.W1 NATIVE width W.1≧TBD NT.S1 Spacing and notch of NATIVE S.1≧ TBD NT-DF.S2 Spacing of NATIVE to DIFFUSION S.2≧TBD	PLY_PG.W.TG33GOX52_2POLY1 width over TG and 3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V +-10% voltage tolerance) for PMOS ≧0.32 0.35 4A.2.1 N_WELL_RESISTOR(NWR) Layer Modify plot NWR.S1 Spacing and notch of N_WELL_RESISTOR S.1≧0.9 N_WELL_RESISTOR to N_WELL S.2≧0.9 NWR-N_DF.NW.S3 Exact spacing of N_WELL RESISTOR to N+ DIFFUSION within the same N_WELL (for N_WELL tap) S.3 = 0 NW-NWR.EN1 Exact N_WELL enclosure of length of N_WELL RESISTOR EN.1=0 Delete NWR.R 4A.6 NATIVE DEVICE (NT) Modify plot NT.W1 NATIVE width W.1≧0.47 NT.S1 Spacing and notch of NATIVE S.1≧0.47 NT-DF.S2 Spacing of NATIVE to DIFFUSION S.2≧0.25	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.2	1	12/12/2006	NT-NW.S3 ≧TBD NT-TG.S4 ≧TBD None NT-NRS.S5 ≧ TBD NT-DF.EN1 = TBD PLY_NT.W2 ≧ TBD None NT.R1 NATIVE must be within N+ Yes	NT-NW.S3 ≧0.90 NT-TG.S4 ≧0.36 TG-NT.EN2 TG enclosure of NATIVE EN.2≧0.36 TG-NT.R1 If TG and NATIVE have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run R1 Yes TG-NT.R2 If TG and NATIVE have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run R2 Yes NT-NRS.S5 ≧ 0.48 NT-DF.EN1 = 0.25 PLY_NT.W2 ≧ 0.20 PLY_NT.W3.TG18 POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device ≧ 1.0 PLY_NT.W3s.TG18 POLY1 width for NATIVE device over NATIVE and over TG of 1.8V device(L55SP Shrinkage capable) ≧ 1.1 PLY_NT.W3.TG25 POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device ≧ 1.2 PLY_NT.W3s.TG25 POLY1 width for NATIVE device over NATIVE and over TG of 2.5V device(L55SP Shrinkage capable) ≧ 1.33 NT.R1 NATIVE over P+ DIFFUSION is not allowed Yes	

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0.2	1	12/12/2006	4A.7 DIODE_IMP_BLOCK (DIB) Layer none	4A.7 DIODE_IMP_BLOCK (DIB) Layer Modify plot DIB-TG.OH1 ≧ 0.36 TG-DIB.OH2 ≧ 0.36 DIB-TG.OL1 ≧ 0.36 DIB-TG.R1 If DIODE_IMP_BLOCK and TG have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run R1 Yes DIB-TG.R2 If DIODE_IMP_BLOCK and TG have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run R2 Yes	
			4A.8 TG Layer Layout Rules: TG-PLY_G.S2 Spacing of TG to unrelated Gate S.2 ≧ 0.45 TG-PLY_G.EN1 TG enclosure of Gate EN.1 ≧ 0.45	4A.8 TG Layer Layout Rules: Modify plot TG-PLY_G.S2 Spacing of TG to unrelated Gate in the direction parallel to Gate width. S.2 ≧ 0.30 TG-PLY_G.S4 Spacing of TG to unrelated Gate in the direction parallel to Gate length. S.4 ≧ 0.40 TG-PLY_G.EN1 TG enclosure of Gate in the direction parallel to Gate width. EN.1 ≧ 0.30 TG-PLY_G.EN2 TG enclosure of Gate in the direction parallel to Gate length.EN.2 ≧ 0.40	

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0.2	1	12/12/2006	4A.9 POLY1 (PLY) Layer PLY_PG.W.TG33GOX52_2 POLY1 width over TG & 3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V+-10% voltage tolerance) for PMOS ≧0.28 PLY_PG.W.TG33GOX52_2s POLY1 width over TG &3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V+-10% voltage tolerance) for PMOS (L55SP shrinkage capable)≧0.31	4A.9 POLY1 (PLY) Layer PLY_PG.W.TG33GOX52_2 POLY1 width over TG & 3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V+-10% voltage tolerance) for PMOS ≧0.32 PLY_PG.W.TG33GOX52_2s POLY1 width over TG & 3P3V_GOX52_IMPLANT_MARK of 3.3V device (for 3.3V+-10% voltage tolerance) for PMOS (L55SP shrinkage capable)≧0.35	
			4A.12.1 SAB Layer PSD-PPNRS.EN2 P+ implant enclosure of P+_POLY1 non-salicide resistor PNRS-TG.S9 Spacing of N+/P+ POLY1 non-salicide resister body to TG ≧ 0.48 4A.11.2 4A.17 MIS_IMPLANT_BLOCK MIS-BP.S3 Spacing of MIS_IMPLANT_BLOCK to BIPOLAR MIS-SAB.S4 Spacing of MIS_IMPLANT_BLOCK to N+/P+ non-salicide resistor body	4A.12.1 SAB Layer PSD-PPNRS.EN2 P+ implant enclosure of P+_POLY1 non-salicide resistor(HR and MR layer are excepted) Modify plot PNRS-TG.S9 Spacing of N+/P+ POLY1 non-salicide resister body to TG S.9 ≧ 0.48 4A.12.2 4A.17 MIS_IMPLANT_BLOCK Modify plot MIS-BP.S3 Spacing of MIS_IMPLANT_BLOCK to BIPOLAR (MIS_IMPLANT_BLOCK overlap BIPOLAR is not allowed)	typo

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
0.2	1	12/12/2006	None MIS.R3 MIS.R4 MIS.R5	NW-MIS.R3 If N_WELL and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run R.3 Yes MIS.R4 MIS.R5 MIS.R6	
			None	4A.22 HR Layer	Define HR Layer
			None 4B.1 METAL1 (M1) Layer Layout Rules: None	4A.23 MR Layer 4B.1 METAL1 (M1) Layer Layout Rules: M1.W2 Width of 45 degree Metal W.2 ≧ 0.40 M1.S4 Spacing of 45 degree Metal S.4 ≧ 0.40 M1.L1 Length of 45 degree Metal L.1 ≧ 1.0	Define MR Layer
			4B.2 METAL2 and above 1XMn.R1 In manhattan routing, 45 degrees METAL_n is not allowed (n=2,3,4,5,6) except Die Seal Ring and Die corner within 150um area. Please refer to section 5.1 for details. R.1 Yes None	4B.2 METAL2 and above Delete 1XMn.W2 Width of 45 degree Metal(*) W.2 ≧0.40 1XMn.S4 Spacing of 45 degree Metal(*) S.4 ≧0.40 1XMn.L1 Length of 45 degree Metal(*) L.1 ≧1.0 Note(*) : UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B.2.1.	

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0.2	1	12/12/2006	4B.4 2x pitch METAL_n (2XMn) Layer Layout Rules None 4B.5 2XMn-2XVn.EN1 METAL_n enclosure of MVIA_n(n=6,7) EN.1 ≧ 0 2XVn.R2 A minimum of 2 MVIA_n at a spacing ≦ 0.6um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.0um wide 4B.6 4x pitch METAL_n (4XMn) Layer Layout Rules: (n=9,10) None 4B.7 4x pitch MVIA_n (4XVn) Layer Layout Rules: (n=8,9) None	4B.4 2XMn.W2 Width of 45 degree Metal W.2 ≧ 0.40 2XMn.S4 Spacing of 45 degree Metal S.4 ≧ 0.40 2XMn.L1 Length of 45 degree Metal L.1 ≧ 1.0 4B.5 2XMn-2XVn.EN1 METAL_n enclosure of MVIA_n(n=6,7) (excluding MIMBP layer) EN.1 ≧ 0 2XVn.R2 A minimum of 2 MVIA_n at a spacing ≦ 0.6um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.0um wide (excluding SEAL_RING_MARK layer) 4B.6 4x pitch METAL_n (4XMn)/30KA thickness Metal Layer Layout Rules 4B.6.1 4B.6.2 30KA thickness Metal Layer : (Maximum 1 level of 30KA thickness Metal) 4B.7 4x pitch MVIA_n (4XVn)/ 30KA MVIA Layer Layout Rules 4B.7.1 4B.7.2 30KA MVIA Layer : (Maximum 1 level of 30KA MVIA)	Define 30KA Metal Layer Define 30KA MVIA Layer

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0.2	1	12/12/2006	4B.10 BEOL Metal/Mvia Layer Options None	4B.10 Add options for 30KMetal and 30Kvia 4B.11 BEOL Layout Rules of Mixed-Mode Specific Devices 4B.11.1 MIM capacitor 4B.11.2 INDUCTOR (Not tooling)	Define MIM and IND
			5. Die Seal Ring Rules 5.1 Metal Stress Relief Rules for Die Corner Area (DCA) 5.2 Schematic cross sectional view and related layout rule: TMn.W7.DSR Top METAL_n width Vn-Vm.S10.DSR Spacing of MVIAn_BAR to MVIA(n+1)_BAR (MVIAn+1 for non-1x pitch Mvia) L3-L2.S9.DSR Spacing of AL_RDL to PASV_RDL ring S.9 ≧ 0.5 None	5. Die Seal Ring Rules 5.1 Metal Stress Relief Rules for Die Corner Area (DCA) plot modify Delete R2,R3 DSR.R5 CU_FUSE_PAD (L6) are not allowed over die seal ring region Yes TMn.W7.DSR Top METAL_n width (n= for all applicable n , for 2x, 4x and 30KA METAL_n) W.7 = 3.0 Vn-Vm.S10.DSR Spacing of MVIAn_BAR to MVIA(n+1)_BAR (n= for all applicable n , for not 1x pitch) S.10 ≧ 0.1 L3-L2.EN9.DSR AL_RDL enclosure of PASV_RDL ring EN.9 ≧ 0.5	Add 30K DSR rule

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0.2	1	12/12/2006	5.2.A L55SP Shrinkage Capable L3-L2.S9s.DSR Spacing of AL_RDL to PASV_RDL ring S.9 ≧ 0.5 DSR.R2 Al_Pad window (L3) and Al_Fuse window (L4) are not allowed over die seal ring region Yes DSR.R3 The outer die seal ring must be surrounded with a PASV_RDL ring Yes None	Mn-VBm.EN4.DSR METALn+1 enclosure of MVIAn_BAR ((n= for all applicable n, for not 1x pitch) L3-L2.EN9s.DSR AL_RDL enclosure of PASV_RDL ring EN.9 ≧ 0.50 30KVBn.W12.DSR 30KA MVIAn_BAR width (n=for all applicable n) = 0.6 30KMn-VBm.EN10.DSR 30KA METAL_n enclosure of MVIAn-1_BAR (n= for all applicable n) ≧ 0.5 30KVBn.S11.DSR Spacing of 30KA MVIAn_BAR to 30KA MVIAn_BAR (n=for all applicable n) ≧ 0.755.2.A L55SP Shrinkage Capable Delete R2,R3 DSR.R5 CU_FUSE_PAD (L6) are not allowed over die seal ring region Yes	
			6. Electromigration Rules 6.1.2 DC rules: none 6.2.1 DC Rules : B.b TMV_RDL (2.3um x 2.3um)	6. Electromigration Rules J. 30K Top METAL10 (FSG) 30mA/um K. 30K MVIA_n (4x pitch METAL_n& 30K METAL_n) 5.44 mA/via L. 30K MVIA_n (2x pitch METAL_n& 30K METAL_n) 5.44 mA/via M. 30K MVIA_n (1x pitch METAL_n& 30K METAL_n) 5.44 mA/via 6.2.1 DC Rules : Delete	Add 30K rule for EM

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0.2	1	12/12/2006	7.3 Metal Stress Relief Rules for Al-metal lines at AL_RDL Layer L2.W1.L2SLOT W.1 < 20 L2SLOT.R2 For Al-metal lines within die corner area, please follow the "Metal Stress Relief Rules for Die Corner Area" defined in Chapter 6	7.3 Metal Stress Relief Rules for Al-metal lines at AL_RDL Layer L2.W1.L2SLOT W.1 < 35 L2SLOT.R2 For Al-metal lines within die corner area, please follow the "Metal Stress Relief Rules for Die Corner Area" defined in Chapter 5.1	typo
			14.1 Recommended Rules: 1XVn.R5.RCM Layers of stacked via≦4	14.1 Recommended Rules: 1XVn.R5.RCM Layers of stacked via(exclude all layers with stacked redundant via)≦4	typo
			14.3 OPC Friendly Design Guidelines: OPC.2-A Avoid using small jogs. Distance between jogs is recommended to be greater than half pitch* OPC.2-B Avoid using small zigzags. Distance between zigzags is recommended to be greater than half pitch* None	14.3 OPC.2-A Avoid using small jogs. Distance between jogs is recommended to be greater than half pitch(NOTE1) OPC.2-B Avoid using small zigzags. Distance between zigzags is recommended to be greater than half pitch(NOTE1) OPC.2-C Distance (D) between corners of zigzags and jogs along region boundary is recommended to be greater than 1/4 pitch of DIFFUSION/POLY1/METAL1/1x pitch Metal/2x pitch Metal. This applies only to zigzags consisting of at least three convex corners.NOTE1: delete 4x pitch Metal NOTE2: This rule must be followed to prevent pattern open or short	

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0.3	1	04/18/2007	4. Topological Layout Rules: NONE 4.0.2 Abbreviations N+ Diffusion (Diffusion over N+) not over Poly P+ Diffusion (Diffusion over P+) not over Poly N-Well pick up N+ Diffusion over N-Well P-Well pick up P+ Diffusion over P-Well N+ Diffusion non-salicide resistor N+ Diffusion touching SAB P+ Diffusion non-salicide resistor P+ Diffusion touching SAB N+ POLY1 (POLY1 over N+) not over Diffusion P+ POLY1 (POLY1 over P+) not over Diffusion N+ POLY1 non-salicide resistor N+ POLY1 touching SAB P+ POLY1 non-salicide resistor P+ POLY1 touching SAB N+ POLY1 non-salicide resistor body N+ POLY1 over SAB P+ POLY1 non-salicide resistor body P+ POLY1 over SAB	3. define MIMAM,MIMTP,MIMBP 4. Topological Layout Rules: PLY.W.TG33 POLY1 width for 3.3V device over TG and not over 3P3V_GOX52_IMPLANT_MARK (for 3.3V+/-10% voltage tolerance) ≧0.37 0.41 4A.1 DIFFUSION (DF) Layer Layout Add DF.W3 Width of 45 degree DIFFUSION W.3 ≧ 0.40 DF.S3 Spacing of 45 degree DIFFUSION S.3 ≧ 0.40 DF.L1 Length of 45 degree DIFFUSION L.1 ≧ 1.0 4.0.2 Abbreviations N+ Diffusion Diffusion over N+ P+ Diffusion Diffusion over P+ N-Well pick up (N+ Diffusion not touching Poly) over N-Well P-Well pick up (P+ Diffusion not touching Poly) over P-Well N+ Diffusion non-salicide resistor (N+ Diffusion touching SAB) not touching Poly P+ Diffusion non-salicide resistor (P+ Diffusion touching SAB) not touching Poly N+ POLY1 POLY1 over N+ P+ POLY1 POLY1 over P+	Add 3.3V IO related rule

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0.3	1	04/18/2007	4A.6 NATIVE DEVICE (NT) Layer NONE 4A.3 DNW-N_DF.S2 Spacing of DEEP_N_WELL to N+ DIFFUSION outside DEEP_N_WELL	N+ POLY1 non-salicide resistor (N+ POLY1 not touching Diffusion) touching SAB P+ POLY1 non-salicide resistor (P+ POLY1 not touching Diffusion) touching SAB N+ POLY1 non-salicide resistor body (N+ POLY1 not touching Diffusion) over SAB P+ POLY1 non-salicide resistor body (P+ POLY1 not touching Diffusion) over SAB N+ POLY1 salicide resistor (N+ POLY1 over PSYMBOL) not touching SAB P+_POLY1 salicide resistor (P+ POLY1 over PSYMBOL) not touching SAB 4A.3 DNW-N_DF.S2 Spacing of DEEP_N_WELL to N+ DIFFUSION outside N_WELL 4A.6 NATIVE DEVICE (NT) Layer PLY_NT.W3.TG33 POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device ≧ 1.2 PLY_NT.W3s.TG33 POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device(L55SP Shrinkage capable) ≧ 1.33	Add 3.3V device related rule

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0.3	1	04/18/2007	4A.9 POLY1 (PLY) Layer NONE PLY-DF.S4 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION ≦ 0.3um PLY-DF.S5 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION > 0.3um DF-PLY_G.OH4 DIFFUSION overhang of POLY1 Gate OH.4 ≧ 0.135	4A.9 POLY1 (PLY) Layer PLY.W.TG33s POLY1 width for 3.3V device over TG and not over 3P3V_GOX52_IMPLANT_MARK (for 3.3V+/-10% voltage tolerance) (L55SP shrinkage capable) ≧ 0.41 PLY-DF.S4 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION ≦ 0.37um PLY-DF.S5 Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS) if POLY1 common run length with adjacent, parallel DIFFUSION > 0.37um DF-PLY_G.OH4 DIFFUSION overhang of POLY1 Gate OH.4 ≧0.115	
			4A.10 N+ implant (NSD) Layer Layout Rules: None 4A.11 P+ IMPLANT (PSD) Layer Layout Rules: None PSD.R Soft CONTACTs are prohibited Yes	4A.10 N+ implant (NSD) Layer NSD-NPRS.EN5 N+ IMPLANT enclosure of N+_POLY1 salicide resistor EN.5 ≧ 0.15 4A.11 P+ IMPLANT (PSD) Layer Layout Rules: PSD-PPRS.EN6 P+ IMPLANT enclosure of P+_POLY1 salicide resistor EN.5 ≧ 0.15 Delete PSD.R	

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0.3	1	04/18/2007	4A.12 Salicide-Block Layers Layout Rules: PPNRS-NW.S6 Spacing of P+_POLY1 non-salicide resistor to N_WELL S.6 ≧ 0.22 PSD-NDNRS.S7 Spacing of P+ implant to N+_DIFFUSION non-salicide resistor S.7 ≧ 0.18 NSD-PPNRS.S8 Spacing of N+ implant to P+_POLY1 non-salicide resistor S.8 ≧ 0.22 NW-PPNRS.EN1 N_WELL enclosure of P+_POLY1 non-salicide resistor EN.1 ≧ 0.22 PSD-PPNRS.EN2 P+ implant enclosure of P+_POLY1 non-salicide resistor(HR and MR layer are excepted) EN.2 ≧ 0.22	4A.12 Salicide-Block Layers Layout Rules: Delete SAB.R2,SAB.R3,delete NSD-NPNRS.EN3 PPNRS-NW.S6 Spacing of P+_POLY1 non-salicide resistor to N_WELL S.6 ≧ 0.20 PSD-NDNRS.S7 Spacing of P+ implant to N+_DIFFUSION non-salicide resistor S.7 ≧ 0.18 NSD-PDNRS.S10 Spacing of N+ implant to P+_DIFFUSION non-salicide resistor S.10 ≧ 0.18 NSD-PPNRS.S8 Spacing of N+ implant to P+_POLY1 non-salicide resistor S.8 ≧ 0.20 PSD-NPNRS.S11 Spacing of P+ implant to N+_POLY1 non-salicide resistor S.11 ≧ 0.20	

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0.3	1	04/18/2007	NSD-NPNRS.EN3 N+ implant enclosure of P+_POLY1 non-salicide resistor ≧ 0.22 4A.12 .2 SBLK Layer (SBLK) Layout Rules For ESD (not tooling) None	NW-PPNRS.EN1 N_WELL enclosure of P+_POLY1 non-salicide resistor EN.1 ≧ 0.20 PSD-PPNRS.EN2 P+ implant enclosure of P+_POLY1 non-salicide resistor(HR and MR layer are excepted) EN.2 ≧ 0.20 NSD-NPNRS.EN3 N+ implant enclosure of N+_POLY1 non-salicide resistor ≧ 0.20 PSD-DNRS.EN5 P+ implant enclosure of P+_DIFFUSION non-salicide resistor EN.5 ≧ 0.20 NSD-DNRS.EN6 N+ implant enclosure of N+_DIFFUSION non-salicide resistor ≧ 0.20 4A.12 .2 SBLK Layer (SBLK) Layout Rules For ESD (not tooling) Add PSD-PPSBLK.EN1 NSD-NPSBLK.EN2 PSD-PDSBLK.EN3 NSD-NDSBLK.EN4 TG-PNRS.EN4 TG enclosure of N+/P+_POLY1 non-salicide resistor body EN.4 ≧ 0.48	

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0.3	1	04/18/2007	4A.16 MOAT Layer Layout Rules (Not tooling): MOAT.R1 MOAT overlap N_WELL ,NATIVE,is not allowed 4B.1 M1.WX METAL1 maximum width except Pad area mark layer 4B.1 to 4B.11 4B.11.2 INDUCTOR (Not tooling) : For INDUCTOR (IND) application in top METAL, one additional drawing layer, IND, can be used for data processing. IND defines inductor region for, P_WELL_BLOCK, DIFFUSION_DUMMY_BLOCK, POLY1_DUMMY_BLOCK, METAL_DUMMY_BLOCK and DRC check. Therefore, IND regions are recommended to exclude from diffusion dummy, POLY dummy ,Metal dummy generation, DIFFUSION of active device, and Metal routing.	NPSD-DNRS.EN5 N+/P+ implant enclosure of N+/P+_DIFFUSION non-salicide resistor EN.5 ≧ 0.20 4A.16 MOAT Layer Layout Rules MOAT.R1 MOAT overlap N_WELL ,NATIVE, and DIFFUSION is not allowed 4B.a.1 to 4B. a.6.2 METAL_n maximum width and METAL_n density add NOTE1 *Note1.(a) Rule check excludes copper metal over Pad area mark layer, top copper metal over BOAC PAD area, IND area and top copper metal over CAD_RF_PAD_MARK area. (b). Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer. 4B.a.a1 to 4B.a.11 Renaming: 30KA to 32.5KA 4B.a.11.2 INDUCTOR (Not tooling) : For INDUCTOR (IND) application in top METAL, one additional drawing layer, IND, will be necessary for mask generation and DRC check. UMC standard tape out flow will use IND layer to exclude P_WELL implant and POLY1/METAL dummy insertion. If customer's product doesn't follow UMC official IND application, customer must individually handle P_WELL mask , POLY1/METAL dummy generation for their IND design.	

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0.3	1	04/18/2007		Delete IND.EN1 IND.R7 Circular metal regions are allowed inside IND. Yes IND.R8 Metal edges that intersect at acute angles greater than 800 inside IND (i.e. inductor line begin/end) are excluded from metal width design rule check. add 4B.b Option1: 1P10M2T2H (1x, 2x, 6x Metal):	
			5. Die Seal Ring Rules	Please refer to the SPEC. No. G-03DSR-GENERATION65N-TLR/DIE_SEAL_RING	
			6. Electromigration Rules 6. .1.2 DC rules: A.METAL1 1.89mA/um B.METAL2 & above 1x pitch METAL_n 2.31mA/um C.2X METAL7 and METAL8 (FSG) 4.14mA/um D.4X METAL9 and METAL10 (FSG) 9.2mA/um E.CONTACT 0.20mA/cont F.1x pitch MVIA (MVIA1 & above 1x pitch MVIA_n) 0.25mA/via G.2x pitch MVIA_n (1x pitch METAL_n & 2x pitch METAL_n+1) 0.39 mA/via H.2x pitch MVIA_n (2x pitch METAL_n & 2x pitch METAL_n+1) 0.96 mA/via I.4x pitch MVIA_n (2x pitch METAL_n & 4x pitch METAL_n+1) 2.42 mA/via	6. Electromigration Rules 6. a.1.2 DC rules: M1.EM METAL1 1.89 mA/um 1XMn.EM METAL2 & above 1x pitch METAL_n 2.31 mA/um 2XMn.EM 2X METAL7 and METAL8(FSG) 4.14 mA/um 4XMn.EM 4X METAL9 and METAL10(FSG) 9.2 mA/um CT.EM CONTACT 0.20 mA/cont 1XVn.EM 1x pitch MVIA (MVIA1 & above 1x pitch MVIA_n) 0.25 mA/via 2XVn.EM.I1 2x pitch MVIA_n (1x pitch METAL_n & 2x pitch METAL_n+1) 0.39 mA/via 2XVn.EM.I2 2x pitch MVIA_n (2x pitch METAL_n & 2x pitch METAL_n+1) 0.96 mA/via	

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0.3	1	04/18/2007	J.30K Top METAL10 (FSG) 30mA/um K.30K MVIA_n (4x pitch METAL_n& 30K METAL_n) 5.44 mA/via L.30K MVIA_n (2x pitch METAL_n& 30K METAL_n) 5.44 mA/via M. 30K MVIA_n (1x pitch METAL_n& 30K METAL_n) 5.44 mA/via	4XVn.EM 4x pitch MVIA_n 2.42 mA/via 325KMn.EM 32.5K Top METAL10 (FSG) 30 mA/um 325KVn.EM.I1 32.5K MVIA_n (1x pitch METAL_n& 32.5K METAL_n) 5.44 mA/via 325KVn.EM.I2 32.5K MVIA_n (2x pitch METAL_n& 30K METAL_n) 5.44 mA/via 325KVn.EM.I3 32.5K MVIA_n (4x pitch METAL_n& 32.5K METAL_n) 5.44 mA/via	
			6.1.3. AC Rules : 6.2.1 DC Rules : Imax_dc (at 110oC) A.a AL_RDL Metal (10um > width ≧ 3um) 1.16mA/um A.b AL_RDL Metal (width > 10um) 2.09mA/um B.a TMV_RDL (4um x 4um) 11.64mA/Via 7.3 Metal Stress Relief Rules for Al-metal lines at AL_RDL Layer (L2SLOT) L2.W1.L2SLOT Width when the length of Al-metal without slotting is greater than 30um EXCEPT bonding pad areas and the width of the metal portion between metal edge and slots (R.1) or between slots (R.2) W.1 < 35 L2SLOT.S1 Spacing of lots L2SLOT.SXSpacing of lots	6. a.1.3. AC Rules : same as L65SP TLR AC Rules 6. a.2.1 DC Rules : L2.W1.EM AL_RDL Metal (10um > width ≧ 3um) 1.16mA/um L2.W2.EM AL_RDL Metal (width > 10um) 2.09mA/um L1.A1.EM TMV_RDL (4um x 4um) 11.64mA/Via add 6.b option1:1P10M2T2H 7.2 Layout Rules for Al-Metal Routing : modify plot 7.3 Metal Stress Relief Rules for Al-metal lines at AL_RDL Layer (AL_RDL_CUSTOMER_SLOT) L2.W1.L2SLOT Width of Al-RDL(L2) EXCEPT bonding pad area W.1 < 35 L2SLOT.S1Spacing of Slot L2SLOT.SXSpacing of Slot	
			L2SLOT-Mn.S2 Spacing of lot to METAL edge L2SLOT-Mn.SX Spacing of lot to METAL edge L2SLOT.R2 For Al-metal lines within die corner area, please follow the "Metal Stress Relief Rules for Die Corner Area" defined in Chapter5.1 14.1 Recommended Rules: PLY_G.RCM POLY1 gates with width ≦0.08um not over TG should be ...	L2SLOT-Mn.S2 Spacing of Slot to METAL edge L2SLOT-Mn.SX Spacing of Slot to METAL edge L2SLOT.R2 For Al-metal lines within die corner area, please follow the "Metal Stress Relief Rules for Die Corner Area" defined in Chapter 5 Modify plot 14.1 Recommended Rules: PLY_G.RCM Poly gate length≦0.08um not over TG should be ...	

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0.4	1	07/09/2007	4. Topological Layout Rules: NONE	4.0.2 Abbreviations Add MOM 4. Topological Layout Rules: add PLY_NT.W3.TG33 POLY1 width for NATIVE device over NATIVE and over TG of 3.3V device ≧ 1.2 1.33	
			4A.4 LL_HVT (LLH) Layer LLH.S1 Spacing and notch of LL_HVT S.1 ≧ 0.36 LLH-NW.S3 Spacing of LL_HVT to N_WELL S.3≧0.36 LLH-TG.S4 Spacing of LL_HVT to TG S.4 ≧0.36 LLH-NW.OH1 LL_HVT overhang of N_WELL OH.1 ≧0.36 NW-LLH.OH2 N_WELL overhang of LL_HVT OH.2 ≧0.36 NW-LLH.OL1 N_WELL overlap of LL_HVT OL.1 ≧0.36 LLH-NW.R1 If LL_HVT and N_WELL have a common run ≧0.36um, then a spacing of zero is allowed along the common run R.1 Yes LLH-NW.R2 If LL_HVT and N_WELL have a common run ≧0.36 um, then a overhang of zero is allowed along the common run R.2 Yes 4B. Table1-Table5 : BEOL METAL/MVIA layer options 4A.1 DIFFUSION (DF) Layer Layout Rules: DF.D DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip) ≧ 25% 4A.9 POLY1 (PLY) Layer Layout Rules: PLY.D POLY1 density over 1mm x 1mm area (stepped in 500um increments across the chip) ≧ 15%	4A.4 LL_HVT (LLH) Layer LLH.S1 Spacing and notch of LL_HVT S.1 ≧ 0.20 LLH-NW.S3 Spacing of LL_HVT to N_WELL S.3 ≧0.18 LLH-TG.S4 Spacing of LL_HVT to TG S.4 ≧ 0.18 LLH-NW.OH1 LL_HVT overhang of N_WELL OH.1 ≧ 0.18 NW-LLH.OH2 N_WELL overhang of LL_HVT OH.2 ≧ 0.18 NW-LLH.OL1 N_WELL overlap of LL_HVT OL.1 ≧ 0.18 LLH-NW.R1 If LL_HVT and N_WELL have a common run ≧0.18 um, then a spacing of zero is allowed along the common run R.1 Yes LLH-NW.R2 If LL_HVT and N_WELL have a common run ≧0.18 um, then a overhang of zero is allowed along the common run R.2 Yes Plot modify 4B. Table1-Table5: BEOL METAL_n(Mn)/MVIA_n(Vn) layer options 4A.1 DIFFUSION (DF) Layer Layout Rules: DF.D DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)(exclude CAD_TESTKEY_MARK)≧25% 4A.9 POLY1 (PLY) Layer Layout Rules: PLY.D POLY1 density over 1mm x 1mm area (stepped in 500um increments across the chip) (exclude CAD_TESTKEY_MARK)≧15%	

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0.4	1	07/09/2007	4A.5 LL_LVT (LLL) Layer LLL.S1 Spacing and notch of LL_LVT S.1 ≧ 0.36 LLL-NW.S3 Spacing of LL_LVT to N_WELL S.3 ≧ 0.36 LLL-TG.S4 Spacing of LL_LVT to TG S.4 ≧ 0.36 LLL-NW.OH1 LL_LVT overhang of N_WELL OH.1 ≧ 0.36 NW-LLL.OH2 N_WELL overhang of LL_LVT OH.2 ≧ 0.36 NW-LLL.OL1 N_WELL overlap of LL_LVT OL.1 ≧ 0.36 LLL-NW.R1 If LL_LVT and N_WELL have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run R.1 Yes LLL-NW.R2 If LL_LVT and N_WELL have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run R.2 Yes	4A.5 LL_LVT (LLL) Layer LLL.S1 Spacing and notch of LL_LVT S.1 ≧ 0.20 LLL-NW.S3Spacing of LL_LVT to N_WELLS.3 ≧ 0.18 LLL-TG.S4 Spacing of LL_LVT to TGS.4 ≧ 0.18 LLL-NW.OH1 LL_LVT overhang of N_WELL OH.1 ≧ 0.18 NW-LLL.OH2 N_WELL overhang of LL_LVT OH.2 ≧ 0.18 NW-LLL.OL1 N_WELL overlap of LL_LVT OL.1 ≧ 0.18 LLL-NW.R1 If LL_LVT and N_WELL have a common run ≧0.18 um, then a spacing of zero is allowed along the common run R.1 Yes LLL-NW.R2 If LL_LVT and N_WELL have a common run ≧0.18 um, then a overhang of zero is allowed along the common run R.2 Yes Plot modify	
			4A.6 NATIVE DEVICE (NT) Layer Layout Rules (not tooling) NT.W1 NATIVE width W.1 ≧ 0.47 4A.8 TG Layer TG-NW.R1 If TG and N_WELL have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run R1 Yes TG-NW.R2 If TG and N_WELL have a common run ≧ 0.36 um, then a overhang of zero is allowed along the common run R2 Yes 4B.a.11.1 Table3 Option1 support MIM	4A.6 NATIVE DEVICE (NT) Layer Layout Rules (Non-tooling): NT.W1 NATIVE DIFFUSION width W.1 ≧ 0.47 4A.8 TG Layer TG-NW.R1 If TG and N_WELL have a common run ≧ 0.18um, then a spacing of zero is allowed along the common run R1 Yes TG-NW.R2 If TG and N_WELL have a common run ≧0.18um, then a overhang of zero is allowed along the common run R2 Yes Plot modify 4A.9 POLY1 (PLY) Layer Layout Rules: Delete PLY_NG.W.G_OD* POLY1 width for overdrive LL_RVT, LL_HVT and LL_LVT NMOS device ≧ * Delete PLY_PG.W.G_OD* POLY1 width for overdrive LL_RVT, LL_HVT and LL_LVT PMOS device ≧ * 4B.a.11.1 Table3 Option1 not support MIM	

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0.4	1	07/09/2007	4A.12.1 SAB Layer (SAB)Layout Rules For Non-Salicide Resistor NSD-PDNRS.S10 Spacing of N+ implant to P+_DIFFUSION non-salicide resistor S.10 ≧ 0.18 PSD-NPNRS.S11 Spacing of P+ implant to N+_POLY1 non-salicide resistor SAB.R1 Non-salicide POLY1 on DIFFUSION is not allowed except ESD structure Yes SAB.R2 SAB overlap of SBLK is not allowed Yes 4A.14 BIPOLAR (BP) Layer Layout Rules (Not tooling) : PNP (P+/N-WellL/P-Well) type of vertical Bipolar transistors is offered.	4A.12.1 SAB Layer (SAB)Layout Rules For Non-Salicide Resistor NSD-PDNRS.S11 Spacing of N+ implant to P+_DIFFUSION non-salicide resistor S.11 ≧ 0.18 PSD-NPNRS.S12 Spacing of P+ implant to N+_POLY1 non-salicide resistor SAB.R4 Non-salicide POLY1 on DIFFUSION is not allowed except ESD structure Yes SAB.R5 SAB overlap of SBLK is not allowed Yes Plot modify 4A.14 BIPOLAR (BP) Layer Layout Rules (Non-tooling): PNP (P+/N_WELL/P_WELL) type and NPN (N+/P_WELL/DEEP_NWELL) of vertical Bipolar transistors are offered.	
			4B.a UMC platform offering: 1P10M (1x, 2x, 4x Metal,32.5KA Metal): Note1. a.)Rule check excludes copper metal over PAD_MARK area, top copper metal over BOAC PAD area, IND area and top copper metal over CAD_RF_PAD_MARK area. b.) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer. 4B. a. 1 METAL1 (M1) Layer Layout Rules: M1.S2 Spacing and notch of METAL1 to [METAL1 with width > 0.5um] ≧ 0.16 M1.S3 Spacing and notch of METAL1 to [METAL1 with width > 2.80um] ≧ 0.30 M1.D (NOTE1) M1.D1(NOTE1)	4B.a UMC platform offering: 1P10M (1x, 2x, 4x Metal, Top 32.5KA Metal): Note 1)Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area. 2)Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area. 3)Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer. 4B. a. 1 METAL1 (M1) Layer Layout Rules: M1.S2 Spacing and notch of METAL1 to [METAL1 with width > 0.5um] for common run length >0.5um ≧ 0.16 M1.S3 Spacing and notch of METAL1 to [METAL1 with width > 2.80um] for common run length >2.8um ≧ 0.30 M1.D (NOTE2) M1.D1(NOTE2) 4B. a.2 METAL2 and above (1XMn) 1XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 0.50um] for common run length >0.5um (n=2,3,4,5,6)	

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0.4	1	07/09/2007	4B. a.2 METAL2 and above (1XMn) 1XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 0.50um](n=2,3,4,5,6) 1XMn.S3 Spacing and notch of METAL_n to [METAL_n with width > 2.80um](n=2,3,4,5,6) 1XMn.D METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE1) 1XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments(NOTE1) 1XMn.W2 Width of 45 degree Metal(Note2) 1XMn.S4 Spacing of 45 degree Metal(Note2) 1XMn.L1 Length of 45 degree Metal(Note2) Note1. a.)Rule check excludes copper metal over PAD_MARK area, top copper metal over BOAC PAD area, IND area and top copper metal over CAD_RF_PAD_MARK area. b.) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer. Note2 : UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B. a.2.1.	1XMn.S3 Spacing and notch of METAL_n to [METAL_n with width > 2.80um] for common run length >1.5um (n=2,3,4,5,6) 1XMn.D METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2) 1XMn.D1 METAL_n density, d, over 50umx50um area without MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) 1XMn.W2 Width of 45 degree METAL (NOTE4) 1XMn.S4 Spacing of 45 degree METAL(NOTE4) 1XMn.L1 Length of 45 degree METAL (NOTE4) Note 1) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area. 2) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area. 3) Metal line is forbidden in CAD_RF_PAD_MARK area except for the top copper metal layer. 4) UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B. a.2.1.	
			4B.a.2.1 X-Architecture of 1 x pitch Metal Layer 1XMn.X.D METAL_n …… in 50um increments. (NOTE1) 1XMn.X.D1 METAL_n ……in 50um increments(NOTE1) 4B. a.3.3 X-Architecture of MVIA2 and above 1X pitch MVIA NONE	4B.a.2.1 X-Architecture of 1 x pitch Metal Layer 1XMn.X.D METAL_n ……in 25um increments.(NOTE2) 1XMn.X.D1 METAL_n……in 25um increments(NOTE2) 4B. a.3.3 X-Architecture of MVIA2 and above 1X pitch MVIA 1XVn.X.R7 Layers of stacked via including MVIA1,1X,2X,4XVn and 32.5KA MVIA(exclude all layers with stacked redundant via) $\leqq$ 4	

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0.4	1	07/09/2007	4B. a.3.1 MVIA1 (V1) V1.R3 A minimum of 3 MVIA1 at a spacing ≦ 0.3um must connect METAL1 and METAL2 when METAL1 or METAL2 ≧0.7um wide	4B. a.3.1 MVIA1 (V1) V1.R3 A minimum of 3 MVIA1 at a spacing ≦ 0.3um must connect METAL1 and METAL2 when METAL1 or METAL2 >0.7um wide Plot modify	
			4B. a.3.2 MVIA2 and above (1XVn) 1XVn.R2 A minimum of 2 MVIA_n at a spacing ≦ 0.3um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide 1XVn.R3 A minimum of 3 MVIA_n at a spacing ≦ 0.3um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧0.7um wide 1XVn.R4 A minimum of 4 MVIA_n at a spacing ≦ 0.3 0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide	4B. a.3.2 MVIA2 and above (1XVn) 1XVn.R2 A minimum of 2 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide 1XVn.R3 A minimum of 3 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 > 0.7um wide 1XVn.R4 A minimum of 4 MVIA_n at a spacing ≦0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide Plot modify	
			4B. a.3.3 X-Architecture of MVIA2 and above 1x pitch MVIA -- MVIA_n (n=2,3,4,5): 1XVn.X.R2 A minimum of 2 MVIA_n at a spacing ≦ 0.30um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide 1XVn.X.R3 A minimum of 3 MVIA_n at a spacing ≦ 0.30um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.7um wide 1XVn.X.R4 A minimum of 4 MVIA_n at a spacing ≦ 0.30um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide B. a.4 2x pitch METAL_n 2XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 2um] 2XMn.S3 Spacing and notch of METAL_n to [METAL_n with width > 8 um]	4B. a.3.3 X-Architecture of MVIA2 and above 1x pitch MVIA -- MVIA_n (n=2,3,4,5): 1XVn.X.R2 A minimum of 2 MVIA_n at a spacing ≦ 0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 0.5um wide 1XVn.X.R3 A minimum of 3 MVIA_n at a spacing ≦ 0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 > 0.7um wide 1XVn.X.R4 A minimum of 4 MVIA_n at a spacing ≦ 0.35um must connect METAL_n and METAL_n+1 when METAL_n or METAL_n+1 ≧ 1.5um wide Plot modify 4B. a.4 2x pitch METAL_n 2XMn.S2 Spacing and notch of METAL_n to [METAL_n with width > 2um] for common run length >1.5um 2XMn.S3 Spacing and notch of METAL_n to [METAL_n with width > 8 um] for common run length >4.5um Deleted 4A.19 CAD_UD_MARK (UD) Layer Layout Rules (Not tooling) : 4A.20 3P3V_GOX52_IMPLANT_MARK Layer	

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0.4	1	07/09/2007	4B. a.8 Wirebond Pad Layers, Scribe Line and Pad Structure (No.PL1, PL2, PL3) : 4B. a.8.1 Wirebond Layout Rules ..... in Section 4B.10 "BEOL Metal/Mvia Layer Options") have been qualified. 4B. b.6 6x pitch METAL_n (6XMn) 6XMn.D (Note1) 6XMn.D1(Note1) 4B. b.8 Wirebond Pad Layers, Scribe Line and Pad Structure (No. PL1, PL2, PL3) : Please refer to section" 4B.a.8 Wirebond Pad Layers, Scribe Line and Pad Structure" 4B. b.8.1 Wirebond Layout Rules Please refer to section" 4B.a.8.1 Wirebond Layout Rule" 3 Antenna Rule (ATN) 13.1 Definitions: 3. The protection diode defined as N+/P-sub or P+/N-Well area connected to poly gate through metal 1.	4B. a.8 Wirebond Pad Layers, Scribe Line and Pad Structure (No. Mask ID PL1, PL2, PL3) : 4B. a.8.1 Wirebond Layout Rules .....in Section 4B.a.10 "BEOL Metal/Mvia Layer Options") have been qualified. 4B. a.8.3 Bonding Pad Layout b. Bonding Pad Size : Plot modify B. b.6 6x pitch METAL_n (6XMn) 6XMn.D (Note2) 6XMn.D1(Note2) 4B. b.8 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3) : TMV_RDL (L1, Terminal Al Via), AL_RDL (L2, Al-Pad) and PASV_RDL (L3, Al-Pad Window) layers define the wirebond pad layers for packaging. Please specially note the section 4B.b.8.4 "Copper Line & Via Support Structure (CLVS) Layout Rules". 4B. b.8.1 Wirebond Layout Rules This spec establishes the PAD layout guidelines for wire bonding ONLY. .....Customers should contact UMC representative to confirm if the packaging options for each BEOL stack (as shown in Section 4B.b.10 "BEOL Metal/Mvia Layer Options") have been qualified. 4B. b.10 BEOL Metal/Mvia Layer Options: Some options which are without 6X metal are deleted. 13 Antenna Rule (ATN) 13.1 Definitions: 3. The protection diode defined as N+/P-sub or P+/N-Well area connected to poly gate through metal 1, and the minimum diode area is 0.1 um^2. The diode area is a summation area of the diodes in the same net.	
			14.1 Recommended Rules: 1XVn.R5.RCM Layers of stacked via(exclude all layers with stacked redundant via) ≦ 4 14.3 OPC Friendly Design Guidelines: OPC.2-C Distance (D) between corners of zigzags and jogs along region boundary is recommended to be greater than 1/4 pitch of DIFFUSION/POLY1/METAL1/1x pitch Metal/2x pitch Metal. This applies only to zigzags consisting of at least three convex corners.	14.1 Recommended Rules: Deleted 1XVn.R5.RCM 14.3 OPC Friendly Design Guidelines: OPC.2-C Recommend that you do not have more than 3 consecutive sides with length < 1/4 pitch of DIFFUSION/POLY1/METAL1/1x pitch Metal/2x pitch Metal. (NOTE1) plot modify add 6.a.2.2 AL_RDL and TMV_RDL Temperature adjustment and product lifetime	

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0.4	1	07/09/2007	4. Topological Layout Rules: PLY.W.TG33 POLY1 width for 3.3V device over TG and not over 3P3V_GOX52_IMPLANT_MARK (for 3.3V+/-10% voltage tolerance) 4A.9 POLY1 (PLY) Layer Layout Rules: PLY.W.TG33 POLY1 width for 3.3V device over TG and not over 3P3V_GOX52_IMPLANT_MARK (for 3.3V+/-10% voltage tolerance) PLY.W.TG33s POLY1 width for 3.3V device over TG and not over 3P3V_GOX52_IMPLANT_MARK (for 3.3V+/-10% voltage tolerance) (L55SP shrinkage capable)	4. Topological Layout Rules: delete PLY_NG.W.TG33GOX52_1 PLY_PG.W.TG33GOX52_1 PLY_NG.W.TG33GOX52_2 PLY_PG.W.TG33GOX52_2 PLY.W.TG33 POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance) 4A.1 DIFFUSION (DF) Layer Layout Rules: deleted DF.W.TG33GOX52 4A.9 POLY1 (PLY) Layer Layout Rules: deleted PLY_NG.W.TG33GOX52_1 PLY_PG.W.TG33GOX52_1 PLY_NG.W.TG33GOX52_1s PLY_PG.W.TG33GOX52_1s PLY_NG.W.TG33GOX52_2 PLY_PG.W.TG33GOX52_2 PLY_NG.W.TG33GOX52_2s PLY_PG.W.TG33GOX52_2s PLY.W.TG33 POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance) PLY.W.TG33s POLY1 width for 3.3V device over TG (for 3.3V+/-10% voltage tolerance) (L55SP shrinkage capable) deleted 4A.20 3P3V_GOX52_IMPLANT_MARK Layer	

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0.4	1	07/09/2007	14.1 Recommended Rules: PLY-CT.EN1.RCM PLY-CT.EN2.RCM DF.S1.RCM DF.S2.RCM PLY_F.S2.RCM DF-CT.EN3.RCM DF-CT.EN4.RCM CT.R.RCM M1-CT.EN2.RCM M1-V1.EN2.RCM 1XMn-1XVn.EN1.RCM DF.W2.RCM	14.1 Recommended Rules: DELETED PLY_G.R4.RCM Spacing of parallel POLY1 gates when POLY1 gates width=0.06 um and POLY1 gate pitch < 0.34 um = 0.16 or 0.20 PLY_G.P.RCM Recommended POLY1 gate pitch when POLY1 gate pitch < 0.34 um =0.22 or 0.26 4A.9 POLY1 (PLY) Layer Layout Rules: DELETED PLY_G.R4 Spacing of parallel POLY1 gates when POLY1 gates width=0.06 um and POLY1 gate pitch < 0.34um (This is recommended rule, customer can select if DRC check applies) = 0.16 or 0.20 priority to 2	
			None	add 4B.a.11.3 Mesh MOM capacitor 4B.a.3.2 MVIA2 and above (1XVn) 1XVn.R7 Layers of stacked via including MVIA1,1X,2X,4XVn and 32.5KA MVIA(exclude all layers with stacked redundant via) ≦ 4	

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1.0	1	09/28/2007	4. Topological Layout Rules:	4. Topological Layout Rules: ADD PLY_NT.W4.TG25_OD33 POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS ≧ 1.4 1.55 PLY_NG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS ≧ 0.5 0.55 PLY_PG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS ≧ 0.4 0.77	
			4A.6 NATIVE DEVICE (NT) Layer Layout Rules	4A.6 NATIVE DEVICE (NT) Layer Layout Rules ADD PLY_NT.W4.TG25_OD33 POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS ≧ 1.4 PLY_NT.W4s.TG25_OD33 POLY1 width for NATIVE device over NATIVE and over TG and over CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS(L55SP Shrinkage capable) ≧ 1.55	
			4A.9 POLY1 (PLY) Layer Layout Rules:	4A.9 POLY1 (PLY) Layer Layout Rules: ADD PLY_NG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS≧ 0.5 PLY_NG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS(L55SP shrinkage capable) ≧ 0.55	

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1.0	1	09/28/2007		PLY_PG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS ≧ 0.4 PLY_PG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS(L55SP shrinkage capable) ≧ 0.77 DELETE The following rules are reserved for future customized overdrive specs. To determine the right channel length, customers will need to discuss with UMC's reliability team based on their design specs. An asterisk mark * was put in the following table for reminding purpose and proper number will be assigned based on customers' design need. PLY_NG.W.TG_OD* POLY1 width over TG for overdrive NMOS device ≧ * PLY_PG.W.TG_OD* POLY1 width over TG for overdrive PMOS device ≧ *	
			6. a.1.3. AC Rules Layer Min width wmin max IRMS (mA)@ wmin (μm) POLY1 0.04 0.08 METAL8(2x) 0.2 1.97 AL_RDL 6. a.2.1 DC Rules: 6. b.1.3 AC Rules POLY1 0.04 0.08 METAL8(2x) 0.2 1.97 METAL9(6x) 0.56 5.21 METAL10(6x) 0.56 4.53 AL_RDL	6. a.1.3. AC Rules Modified AC equations Weff changed to Wmin Layer Min width wmin max IRMS (mA)@ wmin (μm) POLY1 0.06 0.12 METAL8(2x) 0.2 2.18 AL_RDL(12KA) 6. a.2.1 DC Rules: DELETE L2.W1.EM AL_RDL Metal (10um > width ≧ 3um) 1.16 mA/um L2.W2.EM--->RENAMING TO L2.W.EM 6. b.1.3 AC Rules POLY1 0.06 0.12 METAL8(2x) 0.2 2.18 METAL9(6x) 0.56 5.77 METAL10(6x) 0.56 5.04 AL_RDL(12KA)	

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1.0	1	09/28/2007	6. a.1.2 DC rules: 6.b.1.2 DC rules:	6. a.1.2 DC rules: delete note1 1. Effective metal line width (Weff) should be used to calculate the allowable current per unit width limit. Please refer to the individual Electrical Design Rule for Weff. No width tolerance nor other systematic offset/bias included yet, need to be defined. add Table2: for 1P10M2T1F1U 6.b.1.2 DC rules: delete note1 1. Effective metal line width (Weff) should be used to calculate the allowable current per unit width limit. Please refer to the individual Electrical Design Rule for Weff . No width tolerance nor other systematic offset/bias included yet, need to be defined.	

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1.0	1	09/28/2007	13. Antenna Rule (ATN)	13. Antenna Rule (ATN) Modify 13.1 definition 3&4 Add 13.3 note. Add 13.4 section	
			4A.11 P+ IMPLANT (PSD) Layer Layout Rules: PSD.W1 Width	4A.11 P+ IMPLANT (PSD) Layer Layout Rules: PSD.W1 P+ IMPLANT width	
			4A.21 MR Layer: MRP_SAB.W3 R-Poly resistor (Define MR-Poly resistor length)	4A.21 MR Layer: MRP_SAB.W3 SAB width for MR-Poly resistor (Define MR-Poly resistor length)	
			4B. a.4 2x pitch METAL_n (2XMn) Layer 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA 4B. b.6 6x pitch METAL_n (6XMn) Layer Note 1) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area. 2) Rule check excludes copper metal over PAD_MARK area and CAD_WAT_PAD_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.	4B. a.4 2x pitch METAL_n (2XMn) Layer 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA 4B. b.6 6x pitch METAL_n (6XMn) Layer Note 1) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area and top copper metal over CAD_RF_PAD_MARK area. 2) Rule check excludes copper metal over PAD_MARK area , CAD_WAT_PAD_MARK and CAD_CU_FLIP_MARK, top copper metal over CAD_BOAC_MARK area, IND area and top copper metal over CAD_RF_PAD_MARK area.	
1.0	2	10/22/2007	4A.13 CONTACT(CT)Layer Layout Rules: CT_DF-PLY.S3 Spacing of DIFFUSION_CONTACT to POLY1 CT_DF-PLY.S.TG Spacing of DIFFUSION_CONTACT to [POLY1 over TG]	4A.13 CONTACT (CT) Layer Layout Rules: CT_DF-PLY_G.S3 Spacing of DIFFUSION_CONTACT to POLY1 Gate CT_DF-PLY_G.S.TG Spacing of DIFFUSION_CONTACT to [POLY1 Gate over TG]	Define more clear

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1.1	1	11/29/2007	4. Topological Layout Rules: NT-DF.EN1 Exact NATIVE enclosure of DIFFUSION =0.25 0.28 Die Seal Ring Rules Please refer to chapter 5. Die Seal Ring Rules	4. Topological Layout Rules: NT-DF.EN1 NATIVE enclosure of DIFFUSION = 0.25≦EN1≦ 0.28 0.28 Die Seal Ring Rules Please refer to the Spec. No. G-03DSR-GENERATION65N-TLR/ DIE_SEAL_RING	
			4A.13 CONTACT (CT) Layer Layout Rules: CT.SZ1 Exact CONTACT size SZ.1 = 0.09X0.09 4A.18 CAD_OD_MARK OD.S1Spacing and notch of CAD_OD_MARK S.1 ≧0.36	4A.13 CONTACT (CT) Layer Layout Rules: CT.SZ1 Exact CONTACT size(exclude CAD_CONTACT_EFUSE_BLOCK Layer) SZ.1 = 0.09X0.09 add CT.SZ2 Exact CONTACT size inside CAD_CONTACT_EFUSE_BLOCK Layer = 0.12X0.12 4A.18 CAD_OD_MARK (OD) OD.S1Spacing and notch of CAD_OD_MARK S.1 ≧ 0.2	
			4B. b.8.4 Copper Line and Via Support Structure (CLVS) Layout Rules:The CLVS structure is used only for the mechanical support of the wirebond pad.Thus, no interconnection...	4B. b.8.4 Copper Line and Via Support Structure (CLVS) Layout Rules:The CLVS structure is used only for the mechanical support of the wirebond pad. DRC check will exclude “CAD_BOAC_MARK” with the GDS number 90(1).Thus, no interconnection...	
			4B.a.2.1 X-Architecture of 1 x pitch Metal Layer The subsequent rules are recommended for designers to follow, and these rules can prevent extreme density violation through proper space control during design phase. 13.4 Minimum Antenna Protection Diode Area check only for IP vender and U IP (IP area: BOUNDMK with the GDS number 121(2) or PRBNDMK(CAD_PRBOUNDARY_MARK) with the GDS number 121(3))	4B.a.2.1 X-Architecture of 1 x pitch Metal Layer deleted wordings 13.4 Minimum Antenna Protection Diode Area check only for IP vender and U IP Modify RSYMBOL to CAD_DIFFUSION_RESISTOR_SYMBOL	

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1.1	1	11/29/2007	4A.6 NATIVE DEVICE (NT) Layer Layout Rules (Non-tooling): NT-DF.EN1 Exact NATIVE enclosure of DIFFUSION (two DIFFUSION inside one NATIVE is not allowed) EN.1 = 0.25	4A.6 NATIVE DEVICE (NT) Layer Layout Rules (Non-tooling): NT-DF.EN1 NATIVE enclosure of DIFFUSION (two DIFFUSION inside one NATIVE is not allowed) EN.1 0.25≦EN1≦ 0.28	
			4A.1 DIFFUSION (DF) Layer Layout Rules: DF.D DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)(exclude CAD_TESTKEY_MARK)≧25% DF.DXDIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)≦ 75%	4A.1 DIFFUSION (DF) Layer Layout Rules: DF.D DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)(exclude CAD_TESTKEY_MARK)≧20% DF.DXDIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)≦ 80%	
			METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2)20%≦d≦ 80% METAL_n density, d, over 50umx50um area without MnDMBK.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) d≦ 80%	Modify ALL METAL(Metal1, X-Architecture of 1 x pitch Metal,2xMetal,4xMetal,6xMetal,and 32.5KMetal) density rule as below: METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) ≧ 15% METAL_n density over 50umx50um area across whole chip.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2,4) ≦80% Add Note 4) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.	

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1.1	1	11/29/2007	METAL_n density, d, over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2)20%≦d≦ 80% METAL_n density, d, over 50umx50um area without MnDMBK.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) d≦ 80%	Modify 1XMETAL density rule as below: METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) ≧ 15% METAL_n density over 50umx50um area across whole chip.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2,5) ≦80% Add Note 5) This rule is not applied when the width of (checking window NOT excluded area) is smaller than 10um.	
1.2	1	01/24/2008	4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) SBLK-PLY.S4 Spacing of SBLK to POLY1 S.4 ≧ 0.20 SBLK-PLY.OH2 SBLK overhang of POLY1 PLY-SBLK.OH3 POLY1 overhang of SBLK SBLK-PLY.OL1 SBLK overlap of POLY1 4A.13 CONTACT (CT) Layer Layout Rules: CT.R2 ALL CONTACT shapes must be orthogonal. 4B. a.3.1 MVIA1 (V1) Layer Layout Rules: V1.R5 All MVIA1 shapes must be square or rectangular and not at 45° Rectangular MVIA_n (include MVIA_n bar) is only allowed in Die Seal Ring/Fuse/Inductor structure 4B. a.3.2 MVIA2 and above (1XVn) – 1X pitch MVIA_n Layer (n=2,3,4,5) 1XVn.R5 All MVIA_n (n=2,3,4,5) shapes must be square or rectangular and not at 45° Rectangular MVIA_n (include MVIA_n bar) is only allowed in Die Seal Ring/Fuse/Inductor structure	4A.9 POLY1 (PLY) Layer Layout Rules: modify fig. 4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) SBLK-PLY.S4 Spacing of SBLK to POLY1 (SBLK overlap POLY1 in the direction parallel to Gate width is not allowed) S.4 ≧ 0.20 SBLK-PLY_G.OH2 SBLK overhang of POLY1 gate PLY_G-SBLK.OH3 POLY1 gate overhang of SBLK SBLK-PLY_G.OL1 SBLK overlap of POLY1 gate 4A.13 CONTACT (CT) Layer Layout Rules: CT.R2 ALL CONTACT shapes must be orthogonal except LOGO area. CONTACT_BAR is only allowed in die seal ring area. 4B. a.3.1 MVIA1 (V1) Layer Layout Rules: V1.R5 All MVIA1 shapes must be orthogonal except LOGO area. MVIA1_BAR is only allowed in die seal ring and fuse area. 4B. a.3.2 MVIA2 and above (1XVn) – 1X pitch MVIA_n Layer (n=2,3,4,5) 1XVn.R5 All MVIA_n (n=2,3,4,5) shapes must be orthogonal except LOGO area. MVIA_n_BAR (n=2,3,4,5) is only allowed in die seal ring and fuse area.	

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1.2	1	01/24/2008	4B. a.3.3 X-Architecture of MVIA2 and above 1X pitch MVIA -- MVIA_n (n=2,3,4,5): 1XVn.X.R5 All MVIA_n (n=2,3,4,5) shapes must be square or rectangular and not at 45° Rectangular MVIA_n (including MVIAn_BAR) is only allowed in Die Seal Ring/Fuse/Inductor structure 4B. a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6,7) 2XVn.R1 All MVIA_n (n=6,7)shapes must be square or rectangular and not at 45° Rectangular MVIA_n (include MVIA_n bar) is only allowed in Die Seal Ring/Fuse/Inductor structure 4B. a.7.1 4X pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9) 4XVn.R1 All MVIA_n (n=8,9) shapes must be square or rectangular and not at 45°. Rectangular MVIA_n (include MVIA_n bar) is only allowed in Die Seal Ring/Fuse/Inductor structure 4B. a.7.2 32.5KA MVIA Layer: (Maximum 1 level of 32.5KA MVIA) 325KA Vn.R1 All 32.5KA MVIA_n shapes must be square or rectangular and not at 45°. Rectangular 32.5KA MVIA_n (including 32.5KA MVIAn_BAR) is only allowed in Die Seal Ring/Fuse/Inductor structure(n= for all applicable n) 4B. a.10 BEOL METAL/MVIA Layer Options : Option1: not support MIM	4B. a.3.3 X-Architecture of MVIA2 and above 1X pitch MVIA -- MVIA_n (n=2,3,4,5): 1XVn.X.R5 All MVIA_n (n=2,3,4,5) shapes must be orthogonal except LOGO area. MVIA_n_BAR (n=2,3,4,5) is only allowed in die seal ring and fuse area. 4B. a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6,7) 2XVn.R1 All 2XMVIA_n shapes must be orthogonal except LOGO area. 2XMVIA_n_BAR is only allowed in die seal ring and fuse area. 4B. a.7.1 4X pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9) 4XVn.R1 All 4XMVIA_n shapes must be orthogonal except LOGO area. 4xMVIA_n_BAR is only allowed in die seal ring and fuse area. 4B. a.7.2 32.5KA MVIA Layer: (Maximum 1 level of 32.5KA MVIA) 325KA Vn.R1 All 32.5KA MVIA_n shapes must be orthogonal except LOGO area. 32.5KA MVIA_n_BAR is only allowed in die seal ring. 4B. a.10 BEOL METAL/MVIA Layer Options : Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options. add options:46-59 Table2: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with 32.5KA top metal. add options:60-71 Table3: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with MIM. Option1: support MIM add options:46-59 Table4: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options with 32.5KA top metal and MIM. add options:60-71 Table5: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options. add options:72-81	

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1.2	1	01/24/2008	4B. b.7 4x pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9) 4XVn.R1 All MVIA_n (n=8,9) shapes must be square or rectangular and not at 45°. Rectangular MVIA_n (include MVIA_n bar) is only allowed in Die Seal Ring/Fuse/Inductor structure 13.3 Rule and Recommendation: R_Vn-PLY.ANT Ratio of each MVIA_n area(n=1~9) to the poly gate area < 20 R_Mn-PLY.ANT Ratio of each METAL_n area(n=1~10) to the poly gate area < 500 13.4 Minimum Antenna Protection Diode Area check only for IP vender and U IP 3. The anonymous p Antenna defined as P+/N_WELL diode that is not including source/drain, BIPOLAR, CAD_DIFFUSION_RESISTOR_SYMBOL and DIODE_IMPLANT_BLOCK Layer	4B. b.7 4x pitch MVIA_n (4XVn) Layer Layout Rules: (n=8, 9) 4XVn.R1 All 4xMVIA_n shapes must be orthogonal except LOGO area. 4xMVIA_n_BAR is only allowed in die seal ring and fuse area. 7.2 Layout Rules for Al-Metal Routing: add L1.R1 All TMV_RDL shapes must be orthogonal except LOGO area. TMV_RDL_BAR is only allowed in die seal ring and Inductor area Yes 13.3 Rule and Recommendation: R_Cum.Vn-PLY_ANT.WD Ratio of cumulative MVIA_n area(n=1~9) to the poly gate area < 180 R_Cum.Mn-PLY_ANT.WD Ratio of cumulative METAL_n area(n=1~10) to the poly gate area < 5000 13.4 Minimum Antenna Protection Diode Area check only for IP vender and U IP 3. The anonymous p Antenna defined as P+/N_WELL diode that is not including source/drain, BIPOLAR, CAD_DIFFUSION_RESISTOR_SYMBOL and DIODE_IMPLANT_BLOCK Layer and P+ diffusion without contact.	
1.3	1	04/15/2008	4. Topological Layout Rules: PLY_NG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS ≧ 0.5 0.55 PLY_PG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS ≧ 0.4 0.77	4. Topological Layout Rules: Deleted PLY_NG.W.TG25_OD33 PLY_PG.W.TG25_OD33 POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS ≧ 0.4 0.42	Modify rule

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1.3	1	04/15/2008	4A.9 POLY1 (PLY) Layer Layout Rules: PLY_NG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS(L55SP shrinkage capable) ≧ 0.55 PLY_PG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS(L55SP shrinkage capable) ≧ 0.77	4A.9 POLY1 (PLY) Layer Layout Rules: PLY_NG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for NMOS(L55SP shrinkage capable) ≧ 0.5 PLY_PG.W.TG25_OD33s POLY1 width over TG and CAD_OD_MARK of 2.5V overdrive 3.3V device (for 3.3V+/-10% voltage tolerance) for PMOS(L55SP shrinkage capable) ≧ 0.42	Modify rule
			4A.17 MIS_IMPLANT_BLOCK Layer NW-MIS.EN1N_WELL enclosure of MIS_IMPLANT_BLOCK (MIS_IMPLANT_BLOCK outside N_WELL is not allowed) EN.1≧0.36 None MIS.R5 (Gate within MIS_IMPLANT_BLOCK) is not allowed over P+ Yes 4B. a.8.2 Generic Pad Related Layout Guidelines: L2-WELL.S6 Spacing of AL_RDL to (WELL/DIFFUSION/POLY1) (BOAC is excluded from this rule)	4A.17 MIS_IMPLANT_BLOCK Layer NW-MIS.EN1N_WELL enclosure of MIS_IMPLANT_BLOCKEN.1 ≧0.36 Add MIS-NW.S6Spacing of MIS_IMPLANT_BLOCK to N_WELLS.6≧0.36 NW-MIS.R7If N_WELL and MIS_IMPLANT_BLOCK have a common run ≧ 0.36 um, then a spacing of zero is allowed along the common run R.7 Yes DELETE MIS.R5 4B. a.8.2 Generic Pad Related Layout Guidelines: L2-WELL.S6 Spacing of AL_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule)	For PCAP
1.4	1	06/19/2008	4A.9 POLY1 (PLY) Layer Layout Rules: PLY-DF.OH3 POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um OH3 ≧0.16 4A.21 MR Layer: SAB-MRP.OH1 SAB overhang of MR-Poly resistor OH.1 ≧ 0.24	4A.9 POLY1 (PLY) Layer Layout Rules: MODIFY 4A.9 FIG DELETE PLY-DF.OH3 POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um OH3 ≧0.16 4A.21 MR Layer: SAB-MRP.OH1 SAB overhang of MR-Poly resistor OH.1 ≧ 0.17	Move to DFM Align to SAB rule

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1.4	1	06/19/2008	4A.17 MIS_IMPLANT_BLOCK Layer (Non-tooling): MIS-DF.S5 Spacing of MIS_IMPLANT_BLOCK to DIFFUSION S.5 ≧ 0.45	4A.17 MIS_IMPLANT_BLOCK Layer (Non-tooling): MIS-DF.S5 Spacing of MIS_IMPLANT_BLOCK to DIFFUSION S.5 ≧ 0.15	
			14.1 Recommended Rules: NONE PLY-DF.S4.RCM Spacing of end cap POLY1 to related DIFFUSION, When the relative transistor width <0.2um ≧ 0.05 0.10 PLY-DF.S3.RCM Spacing of POLY1 corner to DIFFUSION, When the relative transistor width <0.2um ≧ 0.05 0.10	14.1 Recommended Rules: ADD PLY-DF.OH3.RCM POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um ≧NA 0.16 ADD FIG 4B. a. and 4B.b ADD DESCRIPTION:Auto-metal slot generation will not be provided for L65 process. Customers should follow metal maximum width and density criteria during layout. If customers would like to create slots in metals, please use normal metal layer to layout holes or slots in metal and do not use METALn_CUSTOMER_SLOT layers. METALn_CUSTOMER_SLOT layers are not allowed except CAD_WAT_PAD_MARK area. All metal layers add: METAL1_CUSTOMER_SLOT is not allowed except CAD_WAT_PAD_MARK (GDS No: 90(5)) area Yes PLY-DF.S3.RCM Spacing of POLY1 end cap to related DIFFUSION, When the relative transistor width <0.2um ≧ 0.05 0.10 PLY-DF.S4.RCM Spacing of POLY1 corner to DIFFUSION (POLY1 and DIFFUSION on the same MOS), When the relative transistor width <0.2um ≧ 0.05 0.10	**Add rule**
			4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Non-tooling): This layer defines overdrive device for Boolean operation only.	4B. a.3.1 MVIA1 (V1) Layer Layout Rules: modify fig. to follow R1,R2,R3 4B. a.3.2 MVIA2 and above (1XVn) 4B. a.5 2X pitch MVIA_n 4B. a.3.3 X-Architecture of MVIA2 and above 1X pitch MVIA 4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Non-tooling): This layer defines overdrive device fo DRC/LVS operation only.	

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1.4	1	06/19/2008	4B. a.8.2 Generic Pad Related Layout Guidelines: L2-WELL.S6 Spacing of AL_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule) S.6 ≧ 10 10 L2-Mn.S7 Spacing of Al pad to unrelated METAL_n(n=1~10) (BOAC is excluded from this rule) S.7 ≧ 3 3	4B. a.8.2 Generic Pad Related Layout Guidelines: L3-WELL.S6 Spacing of PASV_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule) S.6 ≧ 12 12 L3-Mn.S7 Spacing of PASV_RDL to unrelated METALn(n=1~10) (BOAC is excluded from this rule) S.7 ≧ 5 5	
			4A.20 HR Layer: SAB-HRP.OH1 SAB overhang of HR-Poly resistor OH.1 ≧ 0.24	4A.20 HR Layer: SAB-HRP.OH1 SAB overhang of HR-Poly resistor OH.1 ≧ 0.17	to align SAB resistor
			4A.12 Salicide-Block Layers Layout Rules: SAB layer defines non-salicided resistors, while SBLK layer is created to eliminate I/O degradation due to salicide formation. SBLK prohibits salicide formation at S/D diffusion area of I/O protection circuit. 4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) The SBLK layer is used to block the formation of silicide on poly & diffusion areas of I/O protection circuit to prevent from ESD immunity degradation. Note: The rules defined in this section only describe the technology requirements for SBLK layer. 4A.15 PESD Layer Layout Rules: PESD is required for cascode I/O structures and is optional for single gate I/O structures. PESD can not be used in any other place except the structures mentioned above. The rules defined here are only for technology requirement. For ESD immunity related PESD rules, please refer to the 65/75nm ESD Design Rule (Spec. NO.:G-03E-GENERATION65N-TLR/ESD). none	4A.12 Salicide-Block Layers Layout Rules: SAB layer defines non-salicided resistors, while SBLK layer is created to eliminate ESD degradation due to salicide formation. SBLK prohibits salicide formation at S/D diffusion area of ESD device. 4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) The rules defined in this section only describe the process requirements for SBLK layer. … please refer to the 65nm ESD Design Rule 4A.15 PESD Layer Layout Rules: PESD is only allowed for ESD structures. The CAD_IO_ID_MARK layer is provided for marking ESD structures for ESD design rule check. If customer does not use this layer to mark ESD structures, PESD is only allowed for NMOS ESD structures. The rules defined here are only for process requirements. For ESD immunity related PESD rules, please refer to the 65nm ESD Design Rule (Spec No.:G-03E-GENERATION65N-TLR/ESD) ADD PESD-PLY_G.S2 Spacing of PESD to POLY1 gate S.2 ≧ 0.20 DF-PESD_N.EN1 DIFFUSION enclosure of PESD in NMOS EN.1 ≧ 0.40 PESD.A PESD area ≧ 0.60 PESD.EA PESD enclosed area ≧ 0.60 PESD.R PESD in (P+ DIFFUSION touching POLY1) is not allowed. ≧ Yes	

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1.4	1	06/19/2008	4B. a.6.2 32.5KA thickness Metal Layer For the product with thickness of 32.5KA top metal, please refer to the mask tooling information of "G-06-LOGIC/MIXED_MODE65N-LL-MASKTOOL-12A" for details. 4A.13 CONTACT (CT) Layer 4. Topological Layout Rules: None 3. Mask Layer Definitions: Note: *1, Please refer to 65nm CMOS platform mask tooling rule: G-06-LOGIC/MIXED_MODE65N-LL-MASKTOOL-12A . 4B. a. 1 METAL1 (M1) Layer Layout Rules: M1-CT.EN4 METAL1 line end enclosure of CONTACT, including diagonal enclosure, for four sides if M1-CT.EN1 and M1-CT.EN2 are not fulfilled EN.4 ≧ 0.02 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) 1XMn-1XVm.EN4 METAL_n line end enclosure of MVIA_n-1, including diagonal enclosure, for four sides if 1XMn-1XVm.EN1 and 1XMn-1XVm.EN2 are not fulfilled EN.4 ≧ 0.02 4B. a.3.1 MVIA1 (V1) Layer Layout Rules: M1-V1.EN4 METAL1 line end enclosure of MVIA1, including diagonal enclosure, for four sides if M1-V1.EN1 and M1-V1.EN3 are not fulfilled EN.4 ≧ 0.02 1XMn-1XVn.EN4 METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides if 1XMn-1XVn.EN1, 1XMn-1XVn.EN2 are not fulfilled (n=2,3,4,5) EN.4 ≧ 0.02 4B. a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6,7) 2XMn-2XVn.EN4 METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides, if 2XMn-2XVn.EN1 and 2XMn-2XVn.EN2 are not fulfilled EN.4 ≧ 0.02	4B. a.6.2 32.5KA thickness Metal Layer For the product with thickness of 32.5KA top metal, please refer to the mask tooling information for details. 4A.13 CONTACT (CT) Layer Modify fig.(delete R3) 4. Topological Layout Rules: ADD PLY-DF.OH3 POLY1 overhang of L-shape DIFFUSION, When POLY1 endcap to L-shape DIFFUSION spacing < 0.1um, and POLY1 common run with L-shape DIFFUSION ≧ 0.05um ≧ NA 0.16 3. Mask Layer Definitions: Note: *1, Please refer to 65nm CMOS platform mask tooling rule: DELETE G-06-LOGIC/MIXED_MODE65N-LL-MASKTOOL-12A . 4B. a. 1 METAL1 (M1) Layer Layout Rules: M1-CT.EN4 METAL1 line end enclosure of CONTACT, including diagonal enclosure, for four sides if M1-CT.EN2 is not fulfilled EN.4 ≧ 0.02 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) 1XMn-1XVm.EN4 METAL_n line end enclosure of MVIA_n-1, including diagonal enclosure, for four sides if 1XMn-1XVm.EN2 is not fulfilled EN.4 ≧ 0.02 4B. a.3.1 MVIA1 (V1) Layer Layout Rules: M1-V1.EN4 METAL1 line end enclosure of MVIA1, including diagonal enclosure, for four sides if M1-V1.EN2 is not fulfilled EN.4 ≧ 0.02 4B. a.3.2 MVIA2 and above (1XVn) 1XMn-1XVn.EN4 METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides if 1XMn-1XVn.EN2 is not fulfilled (n=2,3,4,5) EN.4 ≧ 0.02 4B. a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules: (n=6,7) 2XMn-2XVn.EN4 METAL_n line end enclosure of MVIA_n, including diagonal enclosure, for four sides, if 2XMn-2XVn.EN2 is not fulfilled EN.4 ≧ 0.02	

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1.4	1	06/19/2008	4B. a.8.2 Generic Pad Related Layout Guidelines: L2-WELL.S6 Spacing of AL_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule) S.6 ≧ 10 10 L2-Mn.S7 Spacing of Al pad to unrelated METAL_n(n=1~10) (BOAC is excluded from this rule) S.7 ≧ 3 3	4B. a.8.2 Generic Pad Related Layout Guidelines: L3-WELL.S6 Spacing of PASV_RDL to (WELL/DIFFUSION/POLY1) (BOAC and die seal ring are excluded from this rule) S.6 ≧ 12 12 L3-Mn.S7 Spacing of PASV_RDL to unrelated METALn(n=1~10) (BOAC is excluded from this rule) S.7 ≧ 5 5	
			4A.20 HR Layer: SAB-HRP.OH1 SAB overhang of HR-Poly resistor OH.1 ≧ 0.24	4A.20 HR Layer: SAB-HRP.OH1 SAB overhang of HR-Poly resistor OH.1 ≧ 0.17	to align SAB resistor
			4A.12 Salicide-Block Layers Layout Rules: SAB layer defines non-salicided resistors, while SBLK layer is created to eliminate I/O degradation due to salicide formation. SBLK prohibits salicide formation at S/D diffusion area of I/O protection circuit. 4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) The SBLK layer is used to block the formation of silicide on poly & diffusion areas of I/O protection circuit to prevent from ESD immunity degradation. Note: The rules defined in this section only describe the technology requirements for SBLK layer. 4A.15 PESD Layer Layout Rules: PESD is required for cascode I/O structures and is optional for single gate I/O structures. PESD can not be used in any other place except the structures mentioned above. The rules defined here are only for technology requirement. For ESD immunity related PESD rules, please refer to the 65/75nm ESD Design Rule (Spec. NO.:G-03E-GENERATION65N-TLR/ESD). none	4A.12 Salicide-Block Layers Layout Rules: SAB layer defines non-salicided resistors, while SBLK layer is created to eliminate ESD degradation due to salicide formation. SBLK prohibits salicide formation at S/D diffusion area of ESD device. 4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) The rules defined in this section only describe the process requirements for SBLK layer. … please refer to the 65nm ESD Design Rule 4A.15 PESD Layer Layout Rules: PESD is only allowed for ESD structures. The CAD_IO_ID_MARK layer is provided for marking ESD structures for ESD design rule check. If customer does not use this layer to mark ESD structures, PESD is only allowed for NMOS ESD structures. The rules defined here are only for process requirements. For ESD immunity related PESD rules, please refer to the 65nm ESD Design Rule (Spec No.:G-03E-GENERATION65N-TLR/ESD) ADD PESD-PLY_G.S2 Spacing of PESD to POLY1 gate S.2 ≧ 0.20 DF-PESD_N.EN1 DIFFUSION enclosure of PESD in NMOS EN.1 ≧ 0.40 PESD.A PESD area ≧ 0.60 PESD.EA PESD enclosed area ≧ 0.60 PESD.R PESD in (P+ DIFFUSION touching POLY1) is not allowed. ≧ Yes	

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1.4	1	06/19/2008	14.1 Recommended Rules: PLY-CT.EN2.RCM POLY1 enclosure of CONTACT on at least two opposite sides ≧ 0.04 0.06 DF-CT.EN4.RCM DIFFUSION enclosure of CONTACT on at least two opposite sides ≧ 0.04 0.06	14.1 Recommended Rules: PLY-CT.EN2.RCM POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero ≧ 0.04 0.06 DF-CT.EN4.RCM DIFFUSION enclosure of two opposite sides of CONTACT when other sides have enclosure of zero ≧ 0.04 0.06	
1.5	1	10/06/2008	4. Topological Layout Rules: All layout rules are given in um or um^2 and minimum design grid is 5 nm. For DIFFUSION, POLY1, N+, P+, CONTACT, 1X pitch METAL, 1X pitch MVIA, 2X pitch METAL and 2X pitch MVIA layer, 1nm grid is allowed.	4. Topological Layout Rules: All layout rules are given in um or um^2 and minimum design grid is 5 nm. For DIFFUSION, POLY1, N+, P+, CONTACT, METAL1, MVIA1, 1X pitch METAL, 1X pitch MVIA, 2X pitch METAL and 2X pitch MVIA layer, 1nm grid is allowed.	
			4A.3 DEEP_N_WELL (DNW) Layer Layout Rules: DNW-PW.EN3 DEEP_N_WELL enclosure of P_WELL EN.3 ≧0.50	4A.3 DEEP_N_WELL (DNW) Layer Layout Rules: DNW-PW.EN3 DEEP_N_WELL enclosure of P_WELL EN.3 ≧0.40	
			4A.12.1 SAB Layer (SAB) SAB.R4 Non-salicide POLY1 on DIFFUSION is not allowed except ESD structure Yes	4A.12.1 SAB Layer (SAB) SAB.R4 Non-salicide POLY1 on DIFFUSION (SAB over gate) is not allowed Yes	
			4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) SBLK-PLY_G.OL1 SBLK overlap of POLY1 gate OL.1≧0.07 SBLK.R Non-salicide POLY1 on DIFFUSION is not allowed except ESD structure Yes	4A.12.2 SBLK Layer (SBLK) Layout Rules for ESD (Non-tooling) SBLK-PLY_G.OL1 SBLK overlap of POLY1 gate OL.1≧0.06 SBLK.R Non-salicide POLY1 on DIFFUSION (SBLK over gate) is not allowed except ESD structure Yes	
			4A.15 PESD Layer Layout Rules: PESD is only allowed for ESD structures. The CAD_IO_ID_MARK layer is provided for marking ESD structures for ESD design rule check. If customer does not use this layer to mark ESD structures, PESD is only allowed for NMOS ESD structures. The rules defined here are only for process requirements. For ESD immunity related PESD rules, please refer to the 65nm ESD Design Rule (Spec No.:G-03E-GENERATION65N-TLR/ESD) PESD.R PESD in (P+ DIFFUSION touching POLY1) is not allowed. Yes	4A.15 PESD Layer Layout Rules: PESD is only allowed for ESD structures. The rules defined here are only forprocess requirements. For ESD immunity related PESD rules, please refer to the 65nm ESD Design Rule (Spec No.:G-03E-GENERATION65N-TLR/ESD) PESD.R PESD in (P+ DIFFUSION within N_WELL) is not allowed (exclude CAD_PESD_DRC_BLOCK layer(GDS No: 32(1)). Yes	
			4A.17 MIS_IMPLANT_BLOCK Layer MIS-DF.EN2 MIS_IMPLANT_BLOCK enclosure of DIFFUSION EN.2 ≧ 0.2	4A.17 MIS_IMPLANT_BLOCK Layer MIS-DF.EN2 MIS_IMPLANT_BLOCK enclosure of DIFFUSION EN.2 ≧ 0.16	

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
1.5	1	10/06/2008	4A.20 HR Layer: HR-HRP.EN1 HR enclosure of HR-Poly resistor EN.1 ≧0.5 HR-PLY.S2 Spacing of HR to unrelated POLY1 S.2≧2 NSD-HRP.S3 Spacing of N+ IMPLANT to HR-Poly resistor S.3≧1.5 PSD-HR.S4 Spacing of P+ IMPLANT to HR S.4≧0.5 HRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5≧0.5 HR-DF.S6 Spacing of HR to unrelated DIFFUSION S.6≧0.5 NW-HRP.EN2 N_WELL layer enclosure of HR-Poly resistor EN.2≧0.5 HR_PSD- HRP.EN3 HR P+ IMPLANT enclosure of HR-Poly resistor edge where edge is not covered by SAB EN.3≧0.22 PSD-HRP.S7 Spacing of P+ IMPLANT to unrelated HR-Poly resistor S.7≧0.4	4A.20 HR Layer: HR-HRP.EN1 HR enclosure of HR-Poly resistor EN.1≧0.2 HR-PLY.S2 Spacing of HR to unrelated POLY1 S.2≧0.2 NSD-HRP.S3 Spacing of N+ IMPLANT to HR-Poly resistor S.3≧0.2 Delete:PSD-HR.S4 Spacing of P+ IMPLANT to HR S.4≧0.5 HRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5≧0.2 HR-DF.S6 Spacing of HR to unrelated DIFFUSION S.6≧0.18 NW-HRP.EN2 N_WELL layer enclosure of HR-Poly resistor EN.2≧0.2 HRP-NW.S8 Spacing of HR-Poly resistor to N_WELL S.8 ≧0.2 HR_PSD- HRP.EN3 HR P+ IMPLANT enclosure of HR-Poly resistor edge where edge is not covered by SAB EN.3≧0.2 PSD-HRP.S7 Spacing of P+ IMPLANT to unrelated HR-Poly resistor S.7≧0.2	

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1.5	1	10/06/2008	4A.21 MR Layer: MR-MRP.EN1 MR enclosure of MR-Poly resistor EN.1 ≧0.5 MR-PLY.S2 Spacing of MR to unrelated POLY1 S.2≧2 NSD-MRP.S3 Spacing of N+ IMPLANT to MR-Poly resistor S.3≧1.5 PSD-MR.S4 Spacing of P+ IMPLANT to MR S.4≧0.5 MRP_CT-SAB.S5 Spacing of MR-Poly CONTACT to SAB S.5≧0.5 MR-DF.S6 Spacing of MR to unrelated DIFFUSION S.6≧0.5 NW-MRP.EN2 N_WELL layer enclosure of MR-Poly resistor EN.2≧0.5 MR_PSD-MRP.EN3 MR P+ IMPLANT enclosure of MR-Poly resistor edge where edge is not covered by SAB EN.3≧0.22 PSD-MRP.S7 Spacing of P+ IMPLANT to unrelated MR-Poly resistor S.7≧0.4	4A.21 MR Layer: MR-MRP.EN1 MR enclosure of MR-Poly resistor EN.1 ≧0.2 MR-PLY.S2 Spacing of MR to unrelated POLY1 S.2≧0.2 NSD-MRP.S3 Spacing of N+ IMPLANT to MR-Poly resistor S.3≧0.2 Delete :PSD-MR.S4 Spacing of P+ IMPLANT to MR S.4≧0.5 MRP_CT-SAB.S5 Spacing of MR-Poly CONTACT to SAB S.5≧0.2 MR-DF.S6 Spacing of MR to unrelated DIFFUSION S.6≧0.18 NW-MRP.EN2 N_WELL layer enclosure of MR-Poly resistor EN.2≧0.2 MRP-NW.S8 Spacing of MR-Poly resistor to N_WELL S.8 ≧0.2 MR_PSD-MRP.EN3 MR P+ IMPLANT enclosure of MR-Poly resistor edge where edge is not covered by SAB EN.3≧0.2 PSD-MRP.S7 Spacing of P+ IMPLANT to unrelated MR-Poly resistor S.7≧0.2	
			4B.a.11.2 INDUCTOR (Non-tooling): IND.R6 IND shapes must be rectangular and orthogonal Yes	4B.a.11.2 INDUCTOR (Non-tooling): Delete : IND.R6 IND shapes must be rectangular and orthogonal Yes	

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1.6	1	01/20/2009	4. Topological Layout Rules: --	4. Topological Layout Rules: ESD rules Please refer to the Spec. No. G-03E-GENERATION65N-TLR/ESD FLIP CHIP rules Please refer to the Spec. No. G-03FC-GENERATION65N-TLR/FLIP_CHIP BOAC rules Please refer to the Spec. No. G-03B-GENERATION65N-TLR/BOAC Cu Fuse rules Please refer to the Spec. No. G-03F-GENERATION65N-CU-TLR/FUSE	
			4A.1 DIFFUSION DF.S.TG Spacing and notch of DIFFUSION to [DIFFUSION touching TG] ≧ 0.22 DF.W3 Width of 45 degree DIFFUSION ≧ 0.40 DF.S3 Spacing of 45 degree DIFFUSION ≧ 0.40	4A.1 DIFFUSION DF.S.TG Spacing and notch of DIFFUSION to [DIFFUSION touching TG] ≧ 0.18 DF.W3 Width of 45 degree DIFFUSION ≧ 0.18 DF.S3 Spacing of 45 degree DIFFUSION ≧ 0.18	
			4A.2 N_Well NW-N_DF.S5.TG Spacing of N_WELL to [N+ DIFFUSION touching TG] ≧ 0.45 NW-P_DF.EN3.TG N_WELL enclosure of [P+ DIFFUSION touching TG] ≧ 0.45	4A.2 N_Well NW-N_DF.S5.TG Spacing of N_WELL to [N+ DIFFUSION touching TG] ≧ 0.31 NW-P_DF.EN3.TG N_WELL enclosure of [P+ DIFFUSION touching TG] ≧ 0.31	
			4A.3 DEEP_N_WELL (DNW) Layer Layout Rules: PW.S3 Spacing of P_WELL to (P_WELL of non-equal-potential) within DEEP_N_WELL ≧ 1.00 PW.S4.TG Spacing of P_TUB to (P_WELL of non-equal-potential) within (DEEP_N_WELL touching TG) ≧ 1.20 DNW-PW.EN3 DEEP_N_WELL enclosure of P_WELL≧ 0.40 NW.R1 P_WELL = REVERSE (N_WELL) within DEEP_N_WELL Yes	4A.3 DEEP_N_WELL (DNW) Layer Layout Rules: PW.S3 Spacing of P_TUB to (P_TUB or P_WELL of non-equal-potential) within DEEP_N_WELL ≧ 1.00 PW.S4.TG Spacing of P_TUB to (P_TUB or P_WELL of non-equal-potential) within (DEEP_N_WELL touching TG) ≧ 1.20 DNW-NW.S6 Spacing of DEEP_N_WELL to N_WELL of non-equal potential ≧ 1.90 DNW-PW.EN3 DEEP_N_WELL enclosure of P_TUB≧ 0.40 NW.R1 P_WELL = REVERSE (N_WELL) within DEEP_N_WELL Yes Note: 1. P_TUB = (REVERSE (N_WELL)) fully within DEEP_N_WELL 2. P_WELL = (REVERSE (N_WELL)) not fully within DEEP_N_WELL 3. P_TUB can be used in designs for better noise isolation or various back-bias conditions for performance and power optimization.	
			4A.4 LL_HVT (LLH) Layer Layout Rules (Non-tooling): --	4A.4 LL_HVT (LLH) Layer Layout Rules (Non-tooling): add LLH.R3 Point touch of LL_HVT regions is allowed. R.3 Yes LLH.R4 Butting cell with common run length 0.20um is allowed R.4 Yes	
			4A.5 LL_LVT (LLL) Layer Layout Rules (Non-tooling):	4A.5 LL_LVT (LLL) Layer Layout Rules (Non-tooling): add LLL.R3 Point touch of LL_LVT regions is allowed. R.3 Yes LLL.R4 Butting cell with common run length 0.20um is allowed R.4 Yes	

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1.6	1	01/20/2009	4A.13 CONTACT CT.S2 Spacing of CONTACT for 3x3 array group. An array group is an array where spacing < 0.17um. ≧ 0.15 4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Non-tooling): OD.W1 CAD_OD_MARK width W.1 ≧0.36 OD.S1 Spacing and notch of CAD_OD_MARK S.1 ≧ 0.2 OD-PLY_G.S2 Spacing of CAD_OD_MARK to gate S.1 ≧ 0.15 OD-PLY_G.EN1 CAD_OD_MARK enclosure of gate EN.1 ≧ 0.15 OD.R CAD_OD_MARK shapes must be orthogonal Yes 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n 1XMn.W2 Width of 45 degree METAL (NOTE4) W.2 ≧ 0.4 1XMn.S4 Spacing of 45 degree METAL (NOTE4) S.4 ≧ 0.4 1XMn.L1 Length of 45 degree METAL (NOTE4) L.1 ≧ 1.0 14.1 Recommended Rules: -- 14.3 OPC Friendly Design Guidelines: OPC.1-C Avoid using "head-to-head" corners at minimum width or space	4A.13 CONTACT CT.S2 Spacing of CONTACT for 3x3 array group. An array group is an array where spacing < 0.17um. ≧ 0.14 4A.18 CAD_OD_MARK (OD) Layer Layout Rules (Non-tooling): OD.W1 CAD_OD_MARK width W.1 ≧0.36 OD.S1 Spacing and notch of CAD_OD_MARK S.1 ≧ 0.2 OD-PLY_G.S2 Spacing of CAD_OD_MARK to gate S.1 ≧ 0.15 OD-PLY_G.EN1 CAD_OD_MARK enclosure of gate EN.1 ≧ 0.15 OD.R CAD_OD_MARK shapes must be orthogonal Yes OD.R1 Gate of overdrive device must be fully covered by CAD_OD_MARK layer Yes OD.R2 Gate of overdrive device over CAD_UD_MARK layer is not allowed Yes 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n 1XMn.W2 Width of 45 degree METAL (NOTE4) W.2 ≧ 0.2 1XMn.S4 Spacing of 45 degree METAL (NOTE4) S.4 ≧ 0.2 1XMn.L1 Length of 45 degree METAL (NOTE4) L.1 ≧ 0.4 14.1 Recommended Rules: add 2 CT.R.RCM Use redundant CONTACT when layout is allowed YES 14.3 OPC Friendly Design Guidelines: OPC.1-C Avoid using "head-to-head" corners at minimum width or space for DIFFUSION, POLY1, METAL1, 1Xpitch METAL and 2x pitch METAL.	

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1.7	1	06/18/2009	**4A.8 TG Layer Layout Rules:** TG-PLY_G.EN1 TG enclosure of Gate in the direction parallel to Gate width. EN.1≧0.3 TG-PLY_G.EN2 TG enclosure of Gate in the direction parallel to Gate length. EN.2≧0.40 TG-PLY_G.S4 Spacing of TG to unrelated Gate in the direction parallel to Gate length. S.4≧0.40 **4A.9 POLY1 (PLY) Layer Layout Rules:** DF-PLY_G.OH.TG DIFFUSION overhang of POLY1 Gate over TG ≧0.175 **4A.11.1 N+/P+ Butting Rules** N_DF-PSD.OH1 N+ DIFFUSION overhang of P+ IMPLANT OH.1 ≧0.15 PSD-DF.OL1 P+ IMPLANT overlap of DIFFUSION to form P+ region OL.1≧0.15 **4A.10.1 N+/P+ Butting Rules** P_DF-NSD.OH1 P+ DIFFUSION overhang of N+ IMPLANT OH.1 ≧0.15 NSD-DF.OL1 N+ IMPLANT overlap of DIFFUSION to form N+ region OL.1≧0.15 **4A.17 MIS_IMPLANT_BLOCK Layer (Non-tooling):** MIS-DF.S5 Spacing of MIS_IMPLANT_BLOCK to DIFFUSION S.5≧0.15 **4B. a. 1 METAL1 (M1) Layer Layout Rules:** M1.W2 Width of 45 degree METAL1 W.2 ≧0.40 M1.S4 Spacing of 45 degree METAL1 S.4 ≧0.4 M1.L1 Length of 45 degree METAL1 L.1 ≧ 1.0	**4A.8 TG Layer Layout Rules:** TG-PLY_G.EN1 TG enclosure of Gate in the direction parallel to Gate width. EN.1≧0.27 TG-PLY_G.EN2 TG enclosure of Gate in the direction parallel to Gate length. EN.2≧0.34 TG-PLY_G.S4 Spacing of TG to unrelated Gate in the direction parallel to Gate length. S.4≧0.34 **A.9 POLY1 (PLY) Layer Layout Rules:** DF-PLY_G.OH.TG DIFFUSION overhang of POLY1 Gate over TG ≧0.115 **4A.11.1 N+/P+ Butting Rules** N_DF-PSD.OH1 N+ DIFFUSION overhang of P+ IMPLANT OH.1 ≧0.13 PSD-DF.OL1 P+ IMPLANT overlap of DIFFUSION to form P+ region OL.1≧0.13 **4A.10.1 N+/P+ Butting Rules** P_DF-NSD.OH1 P+ DIFFUSION overhang of N+ IMPLANT OH.1 ≧0.13 NSD-DF.OL1 N+ IMPLANT overlap of DIFFUSION to form N+ region OL.1 ≧0.13 **4A.17 MIS_IMPLANT_BLOCK Layer (Non-tooling):** MIS-DF.S5 Spacing of MIS_IMPLANT_BLOCK to DIFFUSION S.5≧0.13 **4B. a. 1 METAL1 (M1) Layer Layout Rules:** M1.W2 Width of 45 degree METAL1 W.2 ≧0.19 M1.S4 Spacing of 45 degree METAL1 S.4 ≧0.19	

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1.7	1	06/18/2009	**4A.13 CONTACT (CT) Layer Layout Rules:** CT.S2 Spacing of CONTACT for 3x3 array group. An array group is an array where spacing < 0.17um. S.2 ≧0.14 **4A.1 DIFFUSION (DF) Layer Layout Rules:** DF.L1 Length of 45 degree DIFFUSION L.1 ≧1.0 **4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6)** 1XMn.L1 Length of 45 degree METAL (NOTE4) L.1 ≧0.4 **4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8)** 2XMn.L1 Length of 45 degree METAL L.1 ≧1.0 **4A.3 DEEP_N_WELL (DNW) Layer Layout Rules** DNW.R2 : Native and MOAT are not allowed within DEEP_N_WELL 4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2)	**4A.13 CONTACT (CT) Layer Layout Rules:** CT.S2 Spacing of CONTACT for 3x3 array group. An array group is an array where spacing < 0.15um. S.2 ≧0.14 **4A.1 DIFFUSION (DF) Layer Layout Rules:** **4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6)** **4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8)** **4A.3 DEEP_N_WELL (DNW) Layer Layout Rules** DNW.R2 : MOAT is not allowed within DEEP_N_WELL 4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE4,5) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6)	

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1.7	1	06/18/2009	METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2) 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(Note2) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2) 7.2 Layout Rules for Al-Metal Routing: L1.SZ1 TMV_RDL size SZ1.1 >= 4.00x4.00 **11. Dummy for Cu Metal Layers** Please refer to Spec. No.: G-03DS-GENERATION65N-METAL-TLR/DUMMY	METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(NOTE4,5) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 7.2 Layout Rules for Al-Metal Routing: L1.SZ1 TMV_RDL size SZ1.1 = 4.00x4.00 **11. Dummy Rules** Please refer to Spec. No.: G-03D-GENERATION65N-METAL-TLR/DUMMY and G-03D-GENERATION65N/55N-DIFFUSION/POLY1-TLR/DUMMY	

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1.7	1	06/18/2009	8. **Cu-Fuse Rules** Please refer to the Spec. No. G-03F-GENERATION65N-CU-TLR/FUSE 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) 1XMn.A1 METAL_n area (n=2,3,4,5,6) >= 0.046 1XMn.EA1 METAL_n enclosed area (n=2,3,4,5,6) >=0.2 4A.20 HR Layer: HRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5>= 0.20 um 4A.21 MR Layer: MRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5>= 0.20 um 6. Electromigration Rules The failure criteria is defined as 20% of resistance increase or 1uA of extrusion leakage. 4B. a.8.1 Wirebond Layout Rules section3 4B. b.8.1 Wirebond Layout Rules section3 **4A.3 DEEP_N_WELL (DNW) Layer Layout Rules:** NW-DNW.EN2 N_WELL enclosure of DEEP_N_WELL 4A.12 Salicide-Block Layers Layout Rules: 4B. a.11.1 MIM capacitor: BDBK-MIMBP.EN3 BM_DUMMY_BLOCK enclosure of MIMBP MIM.R7 All Cu-Metal layers METAL_n (which are not the UM layer) are also recommended to avoid touching MIMBP. 4B. a.8.2 Generic Pad Related Layout Guidelines: L3.W1 Width of pad window (PASV_RDL) L3.L1 **Length of pad window (PASV_RDL)**	8. **Cu-Fuse Rules** Please refer to the Spec. No. G-03F-GENERATION65N-CU-TLR/FUSE 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) 1XMn.A1 METAL_n area (n=2,3,4,5,6) (Non-shrinkable) >= 0.046 1XMn.EA1 METAL_n enclosed area (n=2,3,4,5,6) >=0.11 Add 1XMn.A1s METAL_n area (n=2,3,4,5,6) (Shrinkable) >= 0.052 4A.20 HR Layer: HRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5>= 0.18 um 4A.21 MR Layer: MRP_CT-SAB.S5 Spacing of HR-Poly CONTACT to SAB S.5>= 0.18 um 6. Electromigration Rules The failure criteria is defined as 10% of resistance increase or 1uA of extrusion leakage. 4B. a.8.1 Wirebond Layout Rules 4B. b.8.1 Wirebond Layout Rules **4A.3 DEEP_N_WELL (DNW) Layer Layout Rules:** NW-DNW.EN2 N_WELL enclosure of DEEP_N_WELL (P_WELL cross DEEP_N_WELL edge is allowed) 4A.12 Salicide-Block Layers Layout Rules: SAB layer is also used to block Vt/LDD implant but SBLK area still receives Vt/LDD implant for device performance. SAB.R6 (DIFFUSION touching SAB) touching POLY1 is not allowed 4B. a.11.1 MIM capacitor: Add Shrinkable rule. Add MIMBP-UM.S8 Spacing of METAL DUMMY/METAL_n (all below MIM layer) to MIMBP S8>=0.40. MnBK-MIMBP.EN3 METALn_DUMMY_BLOCK (all below MIM layer) enclosure to MIMBP MIM.R7 METAL DUMMY /METAL_n (all below MIM layer) touching MIMBP are not allowed 4B. a.8.2 Generic Pad Related Layout Guidelines: L3.W1 Width of pad window (PASV_RDL) (non_shrinkable) L3.L1 **Length of pad window (PASV_RDL) (≤ 85°C probing test) (non_shrinkable)** L3.P1 Pad Pitch (non_shrinkable) Add L3.W1s Width of pad window (PASV_RDL) (shrinkable) >=48um L3.L1s Length of pad window (PASV_RDL) (≤ 85°C probing test) (shrinkable) >=63um	

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1.7	1	06/18/2009	L3.P1 Pad Pitch	L3.P1s Pad Pitch (shrinkable) >=56um L3.L2 Length of pad window (PASV_RDL) (>85°C probing test) (non_shrinkable) L.2>=72um L3.L2s Length of pad window (PASV_RDL) (>85°C probing test) (shrinkable) >=80um L3.SP1 The pad center spacing of two close rows pad for multi-row pad (non_shrinkable) >=70um L3.SP1s The pad center spacing of two close rows pad for multi-row pad (shrinkable) >=78um L2.S8 Spacing of corner pad center to center when one side pad to die seal ring corner is 150um >=100um. Tri-tier50/25um	
1.8	1	07/23/2009	4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE4,5) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6) METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5)	4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE5) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE6) METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5)	

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1.8	1	07/23/2009	4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(NOTE4,5) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE4,5)	4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(NOTE5) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5)	

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1.9	1	09/14/2009	4.0.2 Abbreviations N+ DIFFUSION non-salicide resistor (N+ DIFFUSION touching SAB) not touching POLY1 P+ DIFFUSION non-salicide resistor (P+ DIFFUSION touching SAB) not touching POLY1 4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE5) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE6) 4B.a.2.1 METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(NOTE5) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5) 4A.1 DIFFUSION (DF) Layer Layout Rules:	4.0.2 Abbreviations N+ DIFFUSION non-salicide resistor (N+ DIFFUSION touching SAB and touching CONTACT) not touching POLY1 P+ DIFFUSION non-salicide resistor (P+ DIFFUSION touching SAB and touching CONTACT) not touching POLY1 4B. a. 1 METAL1 (M1) Layer Layout Rules: METAL1 density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE5,6) 4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE6,7) 4B.a.2.1 METAL2 and above 1X pitch Metal -- METAL_n (n=2,3,4,5,6): METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6) 4B. a.4 2x pitch METAL_n (2XMn) Layer Layout Rules: (n=7,8) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6) 4B. a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6) 4B. a.6.2 32.5KA thickness Metal Layer: 32.5KA METAL_n (n= for all applicable n)density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments.(NOTE5,6) 4B. b.6 6x pitch METAL_n (6XMn) Layer Layout Rules: (n=9, 10) METAL_n density over 50umx50um area within MnDMBK. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE5,6) 4A.1 DIFFUSION (DF) Layer Layout Rules: Add customer diffusion dummy rule	

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1.9	1	09/14/2009	4A.9 POLY1 (PLY) Layer Layout Rules: 4B BEOL Layout Rules: 6. a.1.3. AC Rules: 6.b Option1: 1P10M2T2H None None 14.3 Antenna Rule and Recommendation: **7.2 Layout Rules for Al-Metal Routing** 4B.a.11.2 INDUCTOR (Non-tooling) : IND.WLX <= 320um	4A.9 POLY1 (PLY) Layer Layout Rules: Add customer Poly dummy rule. 4B BEOL Layout Rules: Add customer 1X, 2X, 4X and UTM metal dummy rule. 6. a.1.3. AC Rules: Update 1P10M2T2F and 1P10M2T1F1U AC rule 6.b Option1: 1P10M2T2H Update 1P10M2T2H AC rule Add 6.1 Pulse Rule Add 8. Short Length Effect 14.3 Antenna Rule and Recommendation: Split define Core and IO **7.2 Layout Rules for Al-Metal Routing** Add L2 density rule >=10%, <=70% 4B.a.11.2 INDUCTOR (Non-tooling) : IND.WLX <= 430um	
1.10	1	10/26/2009	NA	Page:197 14. Antenna Rule (ATN) 14-3 R_L1-PLY.ANT Ratio of L1 area to the poly gate area < 400 + 83x diode area R_L2.SW-PLY.ANT Ratio of L2 sidewall area to the poly gate area < 30000 + 8000x diode area Page:100,101,102 Modify Typo only ➔" commond" modify to "common"	
1.11	1	12/17/2009	**7.2 Layout Rules for Al-Metal Routing** Add L2 density rule >=10%, <=70% 4A FEOL Layout Rules: 4A.1 DIFFUSION (DF) Layer Layout Rule DFDM-TG.S7 Spacing of DIFFUSION_CUSTOMER_DUMMY to TG ≧ 0.4 DFDM-TG.EN3TG enclosure of DIFFUSION_CUSTOMER_DUMMY ≧ 0.4 PLYDM-TG.S12 Spacing of POLY1_CUSTOMER_DUMMY to TG ≧ 0.6 PLYDM-TG.EN3 TG enclosure of POLY1_CUSTOMER_DUMMY ≧ 0.6	**7.2 Layout Rules for Al-Metal Routing** Add L2 density rule >=10% 4A FEOL Layout Rules: 4A.1 DIFFUSION (DF) Layer Layout Rule	

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1.12	1	05/03/2010	**4B BEOL Layout Rules** **M1DM.S5:** Spacing of METAL1_CUSTOMER_DUMMY to METAL1_DUMMY **1XMnDM.S5:** Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY **2XMnDM.S5**: Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY **4XMnDM.S3:** Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY **32.5KAMnDM.S2:** Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY **4B.a.11.2 INDUCTOR (Non-tooling):** None **6.b Option1: 1P10M2T2H** **6XMnDM.S3:** Spacing of METALn_CUSTOMER_DUMMY to METALn_DUMMY **6.1 Pulse Rule** 1. w is metal width in m. 2. Ipeak allows the maximum width of single pulse DC signal to 10 seconds .	**4B BEOL Layout Rules** **M1DM.S5:** Spacing of METAL1_CUSTOMER_DUMMY **1XMnDM.S5:** Spacing of METALn_CUSTOMER_DUMMY **2XMnDM.S5**: Spacing of METALn_CUSTOMER_DUMMY **4XMnDM.S3:** Spacing of METALn_CUSTOMER_DUMMY **32.5KAMnDM.S2:** Spacing of METALn_CUSTOMER_DUMMY **4B.a.11.2 INDUCTOR (Non-tooling):** **IND.R9** **6.b Option1: 1P10M2T2H** **6XMnDM.S3:** Spacing of METALn_CUSTOMER_DUMMY **6.c Pulse Rule** 1. w is drawn metal width in um. 2. Ipeak allows the maximum width of single pulse DC signal to 1 micro second.	**All aligned to 65SP**

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1.12	1	05/03/2010	**6.a.1.3, 6.b.1.3 AC Rules tables** title: max Irms (mA) for line width w (μm) title: max Irms (mA) @ w bottom note: None **6.a.1.4** Note: 2. None **7.2 Layout Rules for Al-Metal Routing:** None **L2.D:** L2 density cross full chip None **8. Short Length Effect table:** Metal Length (m) None	**6.a.1.3, 6.b.1.3 AC Rules tables** title: max Irms (mA) for line width w (μm)* title: max Irms (mA)** @ w bottom note: Note: * w denotes drawn width ** Max Irms is extracted under temperature 110C **6.a.1.4** Note: 2. The valid temperature range is 85~125C. **7.2 Layout Rules for Al-Metal Routing:** **L1.R1**: All TMV_RDL shapes must be orthogonal except LOGO area. TMV_RDL_BAR is is allowed only in die seal ring or inductor area. **L2.D1: Minimum L2 density cross full chip** **L2.D2: Maximum L2 density cross full chip ≦85%** **8. Short Length Effect table:** Metal Length (um) (3) The table is valid for all metal layers.	**All aligned to 65SP**

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1.13	1	10/18/2010	**4B. a. 1 1X pitch Metal Layers: (Maximum 6 levels of thin 1X pitch metal)** **4B. a.1 METAL1 (M1) Layer Layout Rules:** **4B. a.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6)** **4B. a.10 BEOL METAL/MVIA Layer Options** Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options. None **4B.a.11.2 INDUCTOR (Non-tooling)** For INDUCTOR application in top METAL, ….. None IND.R9 Device other than indcuctor is not allowed to overlap IND. None None **6. a.1.3. AC Rules** **Table1: for 1P10M2T2F** old None **Table2: for 1P10M2T1F1U** old None	**4B. a.1 1X pitch Metal Layers: (Maximum 6 levels of thin 1X pitch metal)** **4B. a.1.1 METAL1 (M1) Layer Layout Rules** **4B. a.1.2 METAL2 and above (1XMn) – 1X pitch METAL_n: (n=2,3,4,5,6)** **4B. a.10 BEOL METAL/MVIA Layer Options** Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options Table1: BEOL METAL_n (Mn)/MVIA_n (Vn) layer options (continued) **4B.a.11.2 INDUCTOR (Non-tooling)** For INDUCTOR application, ….. UMC offers INDUCTOR application in either way of top METAL or AL_RDL design. Top METAL INDUCTOR is offered by 32.5KA Cu METAL; AL_RDL INDUCTOR is offered by 25KA or 36KA Al METAL. IND.R9 Gate under IND is not allowed. IND.R10 IND.R11 **6. a.1.3. AC Rules** **Table 6.a.1: for 1P10M2T2F** new table **Table 6.a.1: for 1P10M2T2F (continued)** **Table 6.a.2: for 1P10M2T1F1U** new table **Table 6.a.2: for 1P10M2T1F1U (continued)**	

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1.13	1	**10/18/2010**	**6. b.1.3 AC Rules** **1P10M2T2H** old	**6. b.1.3 AC Rules** **Table 6.b.1: 1P10M2T2H** new table	
			None	**Table 6.b.1: 1P10M2T2H (continued)**	
			Metal width (μm)	Minimum drawn width (μm)	
			max Irms (mA) ** @ w	Max Irms (mA) @ wmin**	
			** Max Irms is extracted under temperature 110C	** Max Irms is extracted under temperature 110℃, wmin denotes the minimum width	
			6. a.2.1 DC Rules L2.W.EM: AL_RDL Metal 2.09mA/um	**6. a.2.1 DC Rules** L2.W.EM: AL_RDL Metal (Al thickness 12KA) 2.09mA/um	
			None	L2.W.EM_25K: AL_RDL Metal (Al thickness 25KA) 4.35mA/um	
			None	L2.W.EM_36K: AL_RDL Metal (Al thickness 36KA) 6.27mA/um	
			None	L1.A1.EM_3: TMV_RDL (3um x 3um) 6.55mA/Via	
			7.2 Layout Rules for Al-Metal Routing L2.L_W1: ≧ 3	**7.2 Layout Rules for Al-Metal Routing** L2.L_W1: ≧ 2.7	
			L2_L.S1: Spacing and notch of Al-metal line	L2_L.S1: Spacing and notch of Al-metal line (Al thickness 12KA)	
			None	L2_L.S1_2: Spacing and notch of Al-metal line (Al thickness 36KA or 25KA) ≧ 1.8	
			L1.SZ1: 4.00 x 4.00	L1.SZ1: 4x4 or 3x3	
			L1.R1: All TMV_RDL shapes must be orthogonal except LOGO area. TMV_RDL_BAR is is allowed only in die seal ring or inductor area.	L1.R1: All TMV_RDL shapes must be orthogonal except in LOGO, IND and die seal ring areas. TMV_RDL_BAR is allowed only in die seal ring and inductor areas.	
			None	Figure for L1.R1	

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1.14	1	12/24/2010	3. Mask Layer Definitions P9C PHF 4. Topological Layout Rules Rules that vary between L55SP and L65LL processes Generic Pad rules …4B.a.8.2&4B.b.5&4B.c.5… None None 6.a.1.3. AC Rules Table 6.a.1: Al (12KA) Max Irms (mA) for line width w (μm) Old Max Irms (mA) @ wmin 18.03 None None 6.a.2.1 DC Rules Table Imax_dc (at 110oC)	3. Mask Layer Definitions None None 4. Topological Layout Rules Rules that vary between L55SP and L65LL processes Generic Pad rules …4B.a.8.2 & 4B.b.8.2… 4B.c Option2: 1P9M (… 4B.d Option3: 1P9M (… 6.A.1.3. AC Rules Table 6.A.1: Al (12KA) Max Irms (mA) for line width w (μm) New Max Irms (mA) @ wmin 17.974 6.C Option2: 1P9M (1x, 2x, 6x Metal; with maximum 7 levels of 1x Metal) 6.D Option3: 1P9M (1x, 2x, 4x Metal; with maximum 7 levels of 1x Metal) 6.A.2.1 DC Rules Table Imax_dc (at 110℃)	 7 levels of 1XMn Correct the typo of last revision AC rules for 7-level 1XMn

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1.15	1	02/20/2012	**1. Contents** 4B.a.2 METAL2 and above (1XMn) – 1X pitch METAL_n 4B.b.2 METAL2 and above (1XMn) -- 1x pitch METAL_n 4B.c.2 METAL2 and above (1XMn) -- 1x pitch METAL_n 4B.d.2 METAL2 and above (1XMn) -- 1x pitch METAL_n	**1. Contents** None None None None	Sectioning optimization
			4. All layout rules are given in… 5 nm None	**4.** All layout rules are given in… 5nm c. 1nm grid is allowed for 4X pitch METAL, 4X pitch MVIA, 6X pitch METAL, 32.5KA METAL, 32.5KA MVIA and AL_RDL, TMV_RDL, PASV_RDL over SEAL_RING_MARK area.	DSR gridding issue due to 45° and shrinkage
			4A.12.1 The SAB mask is used to block the formation of silicide on either selected N+ DIFFUSION or P+ Poly resistor region.	**4A.12.1** The SAB mask is used to block the formation of silicide on either selected N+/P+ Diffusion or N+/P+ Poly resistor regions.	Correction
			4A.10.1 N_DF-P_DF.S9 None	**4A.10.1** N_DF-P_DF.S9 , while N+ IMPLANT overlap of P+ DIFFUSION is not allowed	More specifically
			4A.11.1 P_DF-N_DF.S9 None	**4A.11.1** P_DF-N_DF.S9 , while P+ IMPLANT overlap of N+ DIFFUSION is not allowed	More specifically
			4B.a.2.1	**4B.a.1.3**	Sectioning optimization
			4B.a.1.2 4) UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B.a.2.1.	**4B.a.1.2** 4) UMC also provides X-Architecture rules for 45 degree metal, which are independent of these rules, in section 4B.a.1.3.	Sectioning optimization
			4B.a.1.1 M1-CT.EN5 None **4B.a.1.2** 1XMn-1XVm.EN5 None **4B.a.2.1** M1-V1.EN5 None **4B.a.2.2** 1XMn-1XVn.EN5 None	**4B.a.1.1** M1-CT.EN5 Note: This rule excludes the case d3+EN.5≧0.16um. **4B.a.1.2** 1XMn-1XVm.EN5 Note: This rule excludes the case d3+EN.5≧0.16um. **4B.a.2.1** M1-V1.EN5 Note: This rule excludes the case d3+EN.5≧0.16um. **4B.a.2.2** 1XMn-1XVn.EN5 Note: This rule excludes the case d3+EN.5≧0.16um.	Rule optimization

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1.15	1	02/20/2012	**4B.a.3** **4B.a.3.1** **4B.a.3.2** **4B.a.3.3** **4B.a.4**	**4B.a.2** **4B.a.2.1** **4B.a.2.2** **4B.a.2.3** **4B.a.3**	Sectioning optimization
			4B.a.5 2XMn-2XVn.EN1 2XMn-2XVn.EN2 2XMn-2XVn.EN3 2XMn-2XVn.EN4 METAL_n…. 2XMn-2XVn.EN2	**4B.a.4** Mn-2XVn.EN1 Mn-2XVn.EN2 Mn-2XVn.EN3 Mn-2XVn.EN4 1X METAL_n or 2X METAL_n… Mn-2XVn.EN2	Mn enclosure of 2XVn applicable to 1X & 2X
			4B.a.6 **4B.a.6.1** **4B.a.6.2** 325KA Mn.A1≧4	**4B.a.5** **4B.a.5.1** **4B.a.5.2** 325KA Mn.A1≧9	Sectioning optimization Rule changed as 40N revised
			4B.a.7 **4B.a.7.1** **4B.a.7.2** 4XMn-4XVn.EN1 4X METAL_n enclosure of MVIA_n (n=8,9) 1XMn-4XVn.EN2 Old figure	**4B.a.6** **4B.a.6.1** **4B.a.6.2** Mn-4XVn.EN1 1X METAL_n or 2X METAL_n or 4X METAL_n enclosure of MVIA_n (n=8,9) None New figure	Sectioning optimization Mn enclosure of 4XVn applicable to 1X & 2X & 4X
			4B.a.8 TMV_RDL … Please specially note the section 4B.a.8.4 "Copper Line & Via Support Structure (CLVS) Layout Rules". **4B.a.8.1** **4B.a.8.2** **4B.a.8.3** **4B.a.8.4**	**4B.a.7** TMV_RDL … Please specially note the section 4B.a.7.4 "Copper Line & Via Support Structure (CLVS) Layout Rules". **4B.a.7.1** **4B.a.7.2** **4B.a.7.3** **4B.a.7.4**	Sectioning optimization
			4B.a.9 **4B.a.10** **4B.a.11** **4B.a.11.1** **4B.a.11.2** **4B.a.11.3**	**4B.a.8** **4B.a.9** **4B.a.10** **4B.a.10.1** **4B.a.10.2** **4B.a.10.3**	Sectioning optimization

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1.15	1	**02/20/2012**	**4B.b.2** Please refer to section" 4B.a.2 METAL2 and above (1XMn)" **4B.b.3** Please refer to section" 4B.a.3 1x pitch MVIA Layers" **4B.b.4** Please refer to section" 4B.a.4 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.b.5** Please refer to section" 4B.a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules" **4B.b.6** **4B.b.7** **4B.b.8** **4B.b.8.1** **4B.b.8.2** **4B.b.8.3** **4B.b.8.4** **4B.b.9** **4B.b.10**	None **4B.b.2** Please refer to section "4B.a.2 1x pitch MVIA Layers" **4B.b.3** Please refer to section "4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.b.4** Please refer to section "4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules" **4B.b.5** **4B.b.6** **4B.b.7** **4B.b.7.1** **4B.b.7.2** **4B.b.7.3** **4B.b.7.4** **4B.b.8** **4B.b.9**	Sectioning optimization
			4B.b.8 TMV_RDL … Please specially note the section 4B.a.8.4 "Copper Line & Via Support Structure (CLVS) Layout Rules".	**4B.b.7** TMV_RDL … Please specially note the section 4B.b.7.4 "Copper Line & Via Support Structure (CLVS) Layout Rules".	Sectioning optimization
			4B.b.8.2 Please refer to section" 4B.a.8.2 Generic Pad Related Layout Guidelines"	**4B.b.7.2** Please refer to section" 4B.a.7.2 Generic Pad Related Layout Guidelines"	Sectioning optimization
			4B.b.8.3 Please refer to section" 4B.a.8.3 Bonding Pad Layout Rules"	**4B.b.7.3** Please refer to section" 4B.a.7.3 Bonding Pad Layout Rules"	Sectioning optimization

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1.15	1	02/20/2012	**4B.c.1** Refer to section" 4B.a.1 1x pitch METAL Layers" **4B.c.2** Refer to section" 4B.a.2 METAL2 and above (1XMn)" **4B.c.3** Refer to section" 4B.a.3 1x pitch MVIA Layers" **4B.c.4** Refer to section" 4B.a.4 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.c.5** Refer to section" 4B.a.5 2X pitch MVIA_n (2XVn) Layer **4B.c.6** Refer to section" 4B.b.6 6x pitch METAL_n (6XMn) Layer Layout Rules" Layout Rules" **4B.c.7** Refer to section" 4B.b.7 4x pitch MVIA_n (4XVn) Layer Layout Rules" **4B.c.8** Refer to section" 4B.b.8 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3)" **4B.c.9** **4B.c.10**	**4B.c.1** Refer to section "4B.a.1 1x pitch METAL Layers" with allowed n=7 for 1XMn. None **4B.c.2** Refer to section "4B.a.2 1x pitch MVIA Layers" **4B.c.3** Refer to section "4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.c.4** Refer to section "4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules" **4B.c.5** Refer to section "4B.b.5 6x pitch METAL_n (6XMn) Layer Layout Rules" Layout Rules" **4B.c.6** Refer to section "4B.b.6 4x pitch MVIA_n (4XVn) Layer Layout Rules" **4B.c7** Refer to section "4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3)" **4B.c.8** **4B.c.9**	Sectioning optimization

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1.15	1	02/20/2012	**4B.d.1** Refer to section" 4B.a.1 1x pitch METAL Layers" **4B.d.2** Refer to section" 4B.a.2 METAL2 and above (1XMn)" **4B.d.3** Refer to section" 4B.a.3 1x pitch MVIA Layers" **4B.d.4** Refer to section" 4B.a.4 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.d.5** Refer to section" 4B.a.5 2X pitch MVIA_n (2XVn) Layer Layout Rules" **4B.d.6** Refer to section" 4B.a.6 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules" **4B.d.7** Refer to section" 4B.b.7 4x pitch MVIA_n (4XVn) Layer Layout Rules" **4B.d.8** Refer to section" 4B.b.8 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3)" **4B.d.9** **4B.d.10**	**4B.d.1** Refer to section "4B.a.1 1x pitch METAL Layers" with allowed n=7 for 1XMn. None **4B.d.3** Refer to section" 4B.a.3 1x pitch MVIA Layers" **4B.d.3** Refer to section "4B.a.3 2X pitch METAL_n (2XMn) Layer Layout Rules" **4B.d.4** Refer to section "4B.a.4 2X pitch MVIA_n (2XVn) Layer Layout Rules" **4B.d.5** Refer to section "4B.a.5 4X pitch METAL_n (4XMn)/32.5KA thickness Metal Layer Layout Rules" **4B.d.6** Refer to section "4B.b.6 4x pitch MVIA_n (4XVn) Layer Layout Rules" **4B.d.7** Refer to section "4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3)" **4B.d.8** **4B.d.9**	Sectioning optimization
			4A.6 This layer defines 1.2V,1.8V, 2.5V&3.3V NMOS-like NATIVE devices for Boolean operation only. Both devices are drawn over P-sub and receive no P_WELL implant. Instead….	**4A.6** This layer defines 1.2V, 1.8V, 2.5V, 2.5VOD3.3V and 3.3V NMOS-like NATIVE devices for Boolean operation only. All 65LL NATIVE devices can be drawn over P-sub and receive no P_WELL implant, or drawn within DEEP_N_WELL and receive P_WELL implant. Instead...	NVT/DNW
			4A.6 None Old figure	**4A.6** PLY_NT.W5.TG25_OD33.BPW Figure changed with W.5	Added
			4A.19 EFM-NW.S3: 0.36 EFM-TG.S4: 0.36	**4A.19** EFM-NW.S3: 0.18 EFM-TG.S4: 0.18	ATD & IPDS re-visited

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1.15	1	02/20/2012	**4B.a.8.2** L3-L1.S3: 4.11, 4.11, 4.11	**4B.a.8.2** L3-L1.S3: 2, 2, 2	Consistency to G-03B
			15. DFM 1XMn-1XVn.EN2.RCM METAL_n line end enclosure of MVIA_n (n=2,3,4,5,6)	**15. DFM** 1XMn-Vn.EN2.RCM METAL_n line end enclosure of MVIA_n (n=2, 3, 4, 5, 6, 7)	1XM7 is allowed; and rule specified for all-diemnsion mvia landing on 1XMn
			4. Topological Layout Rules Generic Pad rules: Please refer to section 4B.a.8.2 & 4B.b.8.2 Generic Pad Related Layout Guidelines	**4. Topological Layout Rules** Generic Pad rules: Please refer to section 4B.a.7.2 & 4B.b.7.2 Generic Pad Related Layout Guidelines	Sectioning optimization
			5. Die Seal Ring Rules Please refer to the Spec. No. G-03DSR-GENERATION65N-TLR /DIE_SEAL_RING	**5. Die Seal Ring Rules** Please refer to the Spec. No. G-03DSR-GENERATION65N-TLR /DIE_SEAL_RING and G-03DSR-GENERATION65N-ADV-TLR/DIE_SEAL_RING.	Alternative DSR structure is available
			6.A.1.2 & 6.B.1.2 4XVn.EM 2.42 mA/via 325KVn.EM.I1 5.44 mA/via 325KVn.EM.I2 5.44 mA/via 325KVn.EM.I3 5.44 mA/via	**6.A.1.2 & 6.B.1.2** 4XVn.EM 3.91 mA/via 325KVn.EM.I1 8.63 mA/via 325KVn.EM.I2 8.63 mA/via 325KVn.EM.I3 8.63 mA/via	Rationalized according to silicon data re-visit
			6.E None	**6.E** 6X	New data
			6.A.2.1 DC Rules Old table without shrinkable rules	**6.A.2.1 DC Rules** New table with shrinkable rules	

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1.16	1	10/22/2012	**4A.6** PLY_NT.W4.TG25_OD33 without Note	**4A.6** PLY_NT.W4.TG25_OD33 Note: This rule excludes cases over DEEP_N_WELL	Fixing errors of last revision
			4A.6 PLY_NT.W5.TG25_OD33.BPW Old figure	**4A.6** None (deleted) New figure	Fixing errors of last revision
			4B.a.1.1 M1.D …(NOTE5,6)	**4B.a.1.1** M1.D … (Note 5, 6, 7)	Rationalized
			4B.a.1.1 M1.D1 METAL1 density over 50umx50um area across whole chip.In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments (NOTE2,4)	**4B.a.1.1** M1.D1 METAL1 density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments (Note 2, 4, 7)	Rationalized
			4B.a.1.1 None	**4B.a.1.1** 7) Customers who….	Rationalized
			4B.a.1.2 1XMn.D …(NOTE6,7)	**4B.a.1.2** 1XMn.D …(Note 6, 7, 8)	Rationalized
			4B.a.1.2 1XMn.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,5)	**4B.a.1.2** 1XMn.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 8)	Rationalized
			4B.a.1.2 None	**4B.a.1.2** 8) Customers who….	Rationalized
			4B.a.1.3 1XMn.X.D …(NOTE5,6)	**4B.a.1.3** 1XMn.X.D …(Note 6, 7, 8)	Rationalized
			4B.a.1.3 1XMn.X.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,4)	**4B.a.1.3** 1XMn.X.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)	Rationalized
			4B.a.1.3 None	**4B.a.1.3** 7) Customers who….	Rationalized
			4B.a.3 2XMn.D …(NOTE5,6)	**4B.a.3** 2XMn.D …(Note 5, 6, 7)	Rationalized
			4B.a.3 2XMn.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,4)	**4B.a.3** 2XMn.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)	Rationalized
			4B.a.3 None	**4B.a.3** 7) Customers who….	Rationalized
			7.2 LM-L1.EN1 Last Copper Metal METAL_n enclosure of TMV_RDL	**7.2** LM-L1.EN1 Last Copper Metal METAL_n enclosure of TMV_RDL Note: TMV_RDL must be within Last METAL_n	Rule completeness
			7.2 None	**7.2** L2-L3.R1	Completeness

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1.16	1	10/22/2012	**4B.a.5.1** 4XMn.D …(NOTE5,6)	**4B.a.5.1** 4XMn.D …(Note 5, 6, 7)	Rationalized
			4B.a.5.1 4XMn.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,4)	**4B.a.5.1** 4XMn.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)	Rationalized
			4B.a.5.1 None	**4B.a.5.1** 7) Customers who….	Rationalized
			4B.a.5.2 325KA Mn.D …(NOTE5,6)	**4B.a.5.2** 325KA Mn.D …(Note 5, 6, 7)	Rationalized
			4B.a.5.2 325KA Mn.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,4)	**4B.a.5.2** 325KA Mn.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)	Rationalized
			4B.a.5.2 None	**4B.a.5.2** 7) Customers who….	Rationalized
			4B.b.5 6XMn.D …(NOTE5,6)	**4B.b.5** 6XMn.D …(Note 5, 6, 7)	Rationalized
			4B.b.5 6XMn.D1 METAL_n density over 50umx50um area across whole chip. In checking this local area requirement, the 50umx50um tile must be stepped in 25um increments. (NOTE2,4)	**4B.b.5** 6XMn.D1 METAL_n density over 100umx100um area across whole chip. In checking this local area requirement, the 100umx100um tile must be stepped in 50um increments. (Note 2, 4, 7)	Rationalized
			4B.b.5 None	**4B.b.5** 7) Customers who….	Rationalized
			4A.12.2 SBLK-PLY_G.OH2 ≧0.11um	**4A.12.2** SBLK-PLY_G.OH2 ≧0.1um	Aligned to ESD rule
			4A.12.2 SBLK-PLY_G.OL1 SBLK overlap of POLY1 gate	**4A.12.2** SBLK-PLY_G.OL1 SBLK overlap of POLY1 gate Note: Zero is allowed if not over TG	Aligned to ESD rule
			4B.a.7.2 L2.S8 Spacing of corner pad center to center when one side pad to die seal ring corner is 150um	**4B.a.7.2** L2.S8 Spacing of corner pad center to center when one side pad to die seal ring corner ≦ 150um	Typo
			4A.13 PLY-CT.EN2 POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero	**4A.13** PLY-CT.EN2 POLY1 enclosure of two opposite sides of CONTACT when other sides have enclosure of zero if PLY-CT.EN1 is not fulfilled	Consistency to command file
			4A.13 DF-CT.EN4 DIFFUSION enclosure of two opposite sides of CONTACT when other sides have enclosure of zero	**4A.13** DF-CT.EN4 DIFFUSION enclosure of two opposite sides of CONTACT when other sides have enclosure of zero if DF-CT.EN3 is not fulfilled	Consistency to command file

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1.16	1	10/22/2012	**1.** N+ implant	**1.** N+ IMPLANT	Wording consistency
			4.0.2 None None	**4.0.2** N+ DIFFUSION salicide resistor P+ DIFFUSION salicide resistor	Completeness
			4A.1 figure Diffusion	**4A.1** figure DIFFUSION	Wording consistency
			4A.2 NWR-N_DF.NW.S3 N_WELL RESISTOR	**4A.2** NWR-N_DF.NW.S3 N_WELL_RESISTOR	Wording consistency
			4A.6 figure N+ P+ N+DIFFUSION	**4A.6** figure N+ DIFFUSION P+ DIFFUSION N+ DIFFUSION	Wording specificity & consistency
			4A.9 figure None	**4A.9** figure W.9	Rule-figure consistency
			4A.9 90^{O} L1	**4A.9** 90° L.1	Wording consistency
			4A.10 N+ implant (NSD) Layer	**4A.10** N+ IMPLANT (NSD) Layer	Wording consistency
			4A.10.1 P+ pick-up	**4A.10.1** P+ DIFFUSION pick-up	Wording consistency
			4A.10.1 NSD-DF.OL1 N+ IMPLANT overlap of DIFFUSION…	**4A.10.1** NSD-DF.OL1 N+ IMPLANT overlap of DIFFUSION…	Double spacing typo
			4A.11.1 N+ pick-up	**4A.11.1** N+ DIFFUSION pick-up	Wording consistency
			4A.11.1 PSD-DF.OL1 P+ IMPLANT overlap of DIFFUSION…	**4A.11.1** PSD-DF.OL1 P+ IMPLANT overlap of DIFFUSION…	Double spacing typo
			4A.11.1 PBJ-PLY_PG.S7 …edge PMOS gate	**4A.11.1** PBJ-PLY_PG.S7 …edge PMOS gate	Double spacing typo
			4A.11.1 NPBJ-PLY_PG.S.TG …edge PMOS gate over TG]	**4A.11.1** NPBJ-PLY_PG.S.TG …edge [PMOS gate over TG]	Double spacing typo
			4A.12.1 The SAB mask is used to block the formation of silicide on either selected N+/P+ Diffusion or N+/P+ Poly resistor regions.	**4A.12.1** The SAB mask is used to block the formation of silicide on either selected N+/P+ DIFFUSION or N+/P+ POLY1 resistor regions.	Wording consistency
			4A.12.1 N+/P+_DIFFUSION N+/P+_POLY1 N+_DIFFUSION P+_DIFFUSION N+_POLY1 P+_POLY1 N+ implant P+ implant	**4A.12.1** N+/P+ DIFFUSION N+/P+ POLY1 N+ DIFFUSION P+ DIFFUSION N+ POLY1 P+ POLY1 N+ IMPLANT P+ IMPLANT	Wording consistency
			4A.13 CT.S2 Spacing of CONTACT for 3x3 array group. An array…	**4A.13** CT.S2 Spacing of CONTACT for 3x3 array group. An array…	Double spacing typo
			4A.16 MOAT.R1 MOAT overlap N_WELL ,NATIVE, and DIFFUSION is not allowed	**4A.16** MOAT.R1 MOAT overlap N_WELL ,NATIVE, and DIFFUSION is not allowed	Double spacing typo

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1.16	1	10/22/2012	**4A.17** Figure: MIS_IMPLANT-BLOCK	**4A.17** Figure: MIS_IMPLANT_BLOCK	Wording consistency
			4A.18 CAD_OD_MARK layer CAD_UD_MARK layer	**4A.18** CAD_OD_MARK CAD_UD_MARK	Wording consistency
			4A.19 EFUSE_MARK layer	**4A.19** EFUSE_MARK	Wording consistency
			4A.20 N_WELL layer	**4A.20** N_WELL	Wording consistency
			4B.a.1.2 1XMn.S3 Spacing and…	**4B.a.1.2** 1XMn.S3 Spacing and…	Double spacing typo
			4B.a.7.2 pad window (PASV_RDL) pad window Al via (TMV_RDL) Al pad °C	**4B.a.7.2** PASV_RDL PASV_RDL TMV_RDL AL_RDL ℃	Wording consistency
			4B.a.7.4 1x pitch METAL_n enclosure of MVIA_n in CLVS structure	**4B.a.7.4** 1x pitch METAL_n enclosure of MVIA_n in CLVS structure	Double spacing typo
			4B.a.10.1 MIM layer BM_DUMMY_BLOCK layers	**4B.a.10.1** MIM BM_DUMMY_BLOCK	Wording
			7.3 L2SLOT-Mn.S2 Spacing of slot to METAL edge S.2 Figure with S.2	**7.3** L2SLOT-Mn.EN1 AL_RDL enclosure of slot EN.1 Figure with EN.1	Correction
			7.3 L2SLOT-Mn.SX Spacing of slot to METAL edge	**7.3** L2SLOT-Mn.SX AL_RDL enclosure of slot	Correction
			4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3) TMV_RDL (L1, Terminal Al Via), AL_RDL (L2, Al-Pad) and PASV_RDL (L3, Al-Pad Window) layers define the wirebond pad layers for packaging. Please specially note the section 4B.a.7.4 "Copper Line & Via Support Structure (CLVS) Layout Rules". For BOAC rule, please refer to "G-03B-GENERATION65N-TLR/BOAC" 4B.a.7.1 Wirebond Layout Rules ...If the customer wants to apply it to thin profile packaging or other packaging types, the customer should get confirmation from their selected assembly house & probing subcontractors.	**4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure** (deleted) (deleted) (deleted) ...If customers need to apply it to thin profile packaging or other packaging types, they should confirm with their designated assembly houses and probing subcontractors in advance.	Mask IDs are already deifined in 3. Mask Layer Definitions

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1.16	1	10/22/2012	**4B.a.7.2** Generic Pad Related Layout Guidelines **None** All rules Modes In-line 50um, Staggered 50/25um, Tri-tier 50/25um cloumns Figure old **4B.a.7.3** Bonding Pad Layout Rules	**4B.a.7.1** Generic Wirebond Pad Layout Rules UMC offers BOAC (Bonding Over Active Circuit) for wire bonding structure… All rules except L1.SZ1, L1.S4, L2-DSR.S5, L3-WELL.S6, L3-Mn.S7, L2-L1.EN2, L2-L3.EN3, AC.S, L2.S8 are delete (deleted titles, deleted columns but left only 1 for Rule) Figure new (deleted)	All wirebond pad layout rules refer to G-03B
			4B.a.7.2 L1.SZ1 & L2-L1.EN2 Al via (TMV_RDL)	**4B.a.7.2** L1.SZ1 & L2-L1.EN2 TMV_RDL	Wording
			4B.a.7.2 L2-L3.EN3 pad window (PASV_RDL)	**4B.a.7.2** L2-L3.EN3 PASV_RDL	Wording
			4B.a.7.4 Copper Line and Via Support Structure (CLVS) Layout Rules	**4B.a.7.2 Copper Line and Via Support Structure (CLVS) Layout Rules**	Re-section
			4. Generic Pad rules 4B.a.7.2	**4.** Generic Pad rules 4B.a.7.1	Re-section
			4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3) All	**4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure** Please refer to section “4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure” for all wirebond pad layout rules. (All subsections delete)	Wording
			4B.c.7 & 4B.d.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3) Refer to section ”4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure (Mask ID PL1, PL2, PL3)”	**4B.c.7 & 4B.d.7 Wirebond Pad Layers, Scribe Line and Pad Structure** Refer to section ”4B.b.7 Wirebond Pad Layers, Scribe Line and Pad Structure”	Wording
			4B.a.10.1 MnBK-MIMBP.EN3: enclosure to MIM.R7: …METAL_n (all…	**4B.a.10.1** MnBK-MIMBP.EN3: enclosure of MIM.R7: …METAL_n (all…	Typo & Double spaces
			4B.c & 4B.d …during layout. If customers…	**4B.c & 4B.d** …during layout. If customers…	Double spacing typo
			6.A.1 All °C	**6.A.1** All ℃	Wording
			6.B.1.2 °C	**6.B.1.2** ℃	Wording
			6.A.1.4 **85~125C**	**6.A.1.4** **85~125**℃	Wording
			6.B.1.2 °C	**6.B.1.2** ℃	Wording
			6A.2 & 6.B.2 & 6.C.2 & 6.D.2 AL_RDL metal AL_RDL Metal	**6A.2 & 6.B.2 & 6.C.2 & 6.D.2** AL_RDL AL_RDL	Wording

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1.16	1	10/22/2012	**7.1** The layout rules defined here are for Al-metal routing and for wire bond only.	**7.1** This section defines the layout rules AL_RDL routing for and only for wirebond package types. Refer to Section “4B.a.7 Wirebond Pad Layers, Scribe Line and Pad Structure” for wirebond packaging information.	Wording
			7 Al-Metal Al-Metals Al-metal line Al-metal lines AL_RDL (L2) AL_RDL metal layer	**7** AL_RDL AL_RDL AL_RDL AL_RDL AL_RDL AL_RDL	Wording
			7 L2_L-L1.EN2 Al-metal line at AL_RDL layer enclosure of TMV_RDL	**7** L2_L-L1.EN2 AL_RDL enclosure of TMV_RDL	Wording
			7.2 L2.D1 & L2.D2 L2	**7.2** L2.D1 & L2.D2 AL_RDL	Wording
			7.2 Note: ……	**7.2** Note: For wide AL_RDL, please refer to Section “7.3 AL_RDL Stress Relief Rules”.	Wording
			7.2 Figure with AL_RDL (L2) & TMV_RDL (L1)	**7.2** Figure with AL_RDL & TMV_RDL	Wording
			7.3 Metal Stress Relief Rules for Al-metal lines at AL_RDL Layer	**7.3 AL_RDL Stress Relief Rules**	Double spacing typo
			14.4 P+ diffusion	**14.4** P+ DIFFUSION	Wording
			15.1 M1-CT.EN2.RCM …of CONTACT	**15.1** M1-CT.EN2.RCM …of CONTACT	Double spacing typo
			4.0.2 None None	**4.0.2** N+ DIFFUSION salicide resistor P+ DIFFUSION salicide resistor	They should have been existed

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1.17	1	02/07/2013	**4.** None	**4.** d. Verified SRAM layouts should be waived to their corresponding SRAM rules. Customer who changes the layouts should take all risks. For logic layouts at the boundary between SRAM and logic areas, logic rules need to be followed.	To match real coding
			4B.a.10.2 UMC offers INDUCTOR application in either way of top METAL or AL_RDL design.	**4B.a.10.2** UMC offers rules for INDUCTOR applications of copper METAL and AL_RDL designs.	Optimized wording
			6.A.2.1 Non-shrinkable (for L65SP only) Shrinkable (for L65SP to L55SP) None	**6.A.2.1** Non-shrinkable (for 65nm) Shrinkable (for 55nm) (*1) Note*1 UMC does not offer 90% shrink technology for 65LL. Rules of this column are provided for reference if ever applicable.	Optimized wording
			7.2 L1.R1 All TMV_RDL shapes must be orthogonal except in LOGO, IND and die seal ring areas. TMV_RDL_BAR is allowed only in die seal ring and inductor areas.	**7.2** L1.R1 All TMV_RDL shapes must be orthogonal except in LOGO, IND and die seal ring areas. TMV_RDL_BAR is allowed only in die seal ring area.	Correction
1.17	2	06/20/2013	4B.a.10.2 UMC offers rules for INDUCTOR applications of copper METAL and AL_RDL designs. Top METAL INDUCTOR is offered by 32.5KA Cu METAL; AL_RDL INDUCTOR is offered by 25KA or 36KA Al METAL.	4B.a.10.2 None (deleted)	To avoid confusion

Ver.	Phase	Approved Date	From	To	Remark (Purpose)
1.18	1	01/13/2014	**4** & **4A.9** None	**4** & **4A.9** PLY.W.TG25_UD18 (added)	New device
			4A.1 DF.F DIFFUSION density over 150um x 150um area (stepped in 50um increments across the chip)(exclude CAD_TESTKEY_MARK)	**4A.1** DF.F DIFFUSION density within DIFFUSION_DUMMY_BLOCK over 150um x 150um area (stepped in 50um increments across the chip) Note1: Customers who don't need UMC to add dummy are required to draw DIFFUSION_DUMMY_BLOCK over the whole chip, such that UMC dummy insertion will be excluded and this rule can check DIFFUSION density over the whole chip. Note2: Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside DIFFUSION_DUMMY_BLOCK area after the IP mergence.	UMC dummy rule
			4B.a.1.1 **4B.a.3.2** **4B.a.5.1** **4B.a.5.2** **4B.b.5** 7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC DRC can check METAL_n density over the whole chip. None	**4B.a.1.1** **4B.a.3.2** **4B.a.5.1** **4B.a.5.2** **4B.b.5** 7) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip. 8) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.	UMC dummy rule
			4B.a.1.2 8) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC DRC can check METAL_n density over the whole chip. None	**4B.a.1.2** 8) Customers who don't need UMC to add dummy are recommended to add dummy block layers fulfill the whole chip, such that UMC dummy insertion will be excluded and DRC can check METAL_n density over the whole chip. 9) Customers who need UMC to merge instances (such as IP, eFuse, SRAM, Macro, etc) are required to let UMC insert dummy outside dummy block area after the IP mergence.	UMC dummy rule

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