ADVANCED VLSI DESIGN

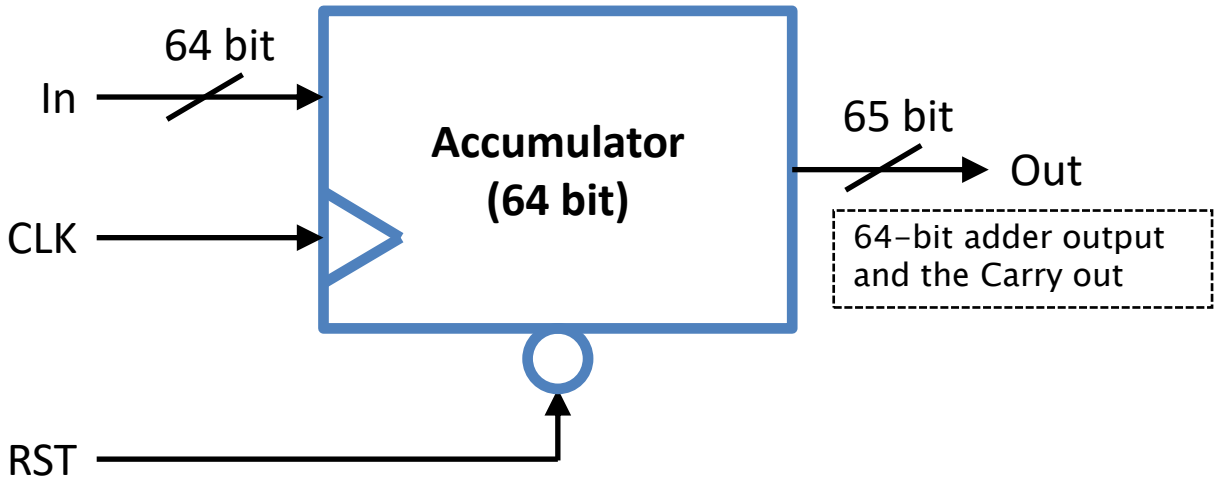
Project Definition

04/03/2025

Contents

- **Design Overview: 64-bit Kogge-Stone Adder (Accumulator)**
- **Reminder on Parallel Prefix Adders**
  - Propagate, Generate Signals
  - Carry Merging
  - 16 Bit Kogge Stone Adder
- **Radix**
- **Sparsity**
- **64 Bit Kogge Stone Carry Merge Block with Radix 4, Sparseness 4**
- **Carry Select Adder**
- **Top Level Blocks**

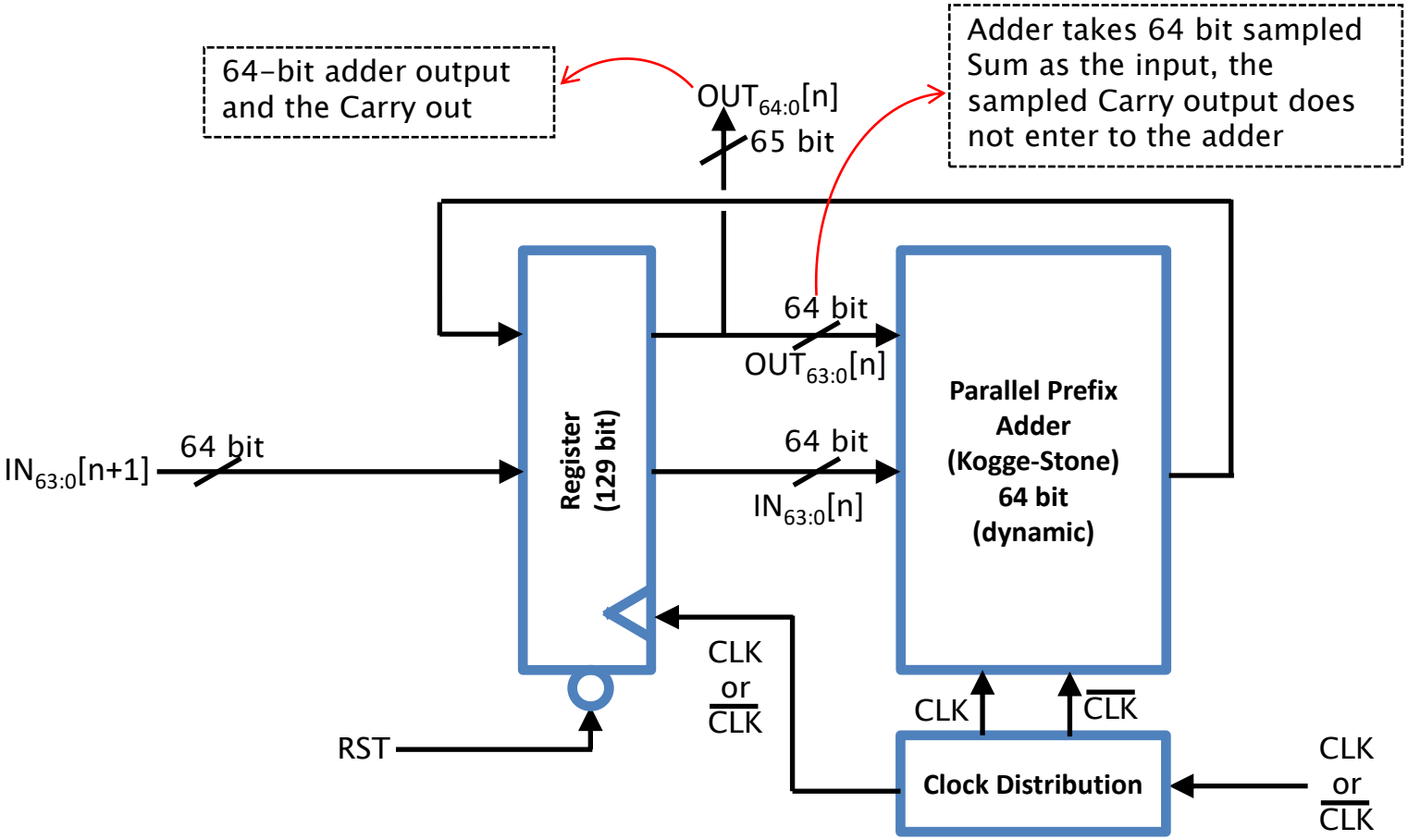
Top Level Diagram: 64-bit Accumulator



Out[n+1] = In[n] + Out[n]

Specification:
Reg-Reg Delay < 500ps

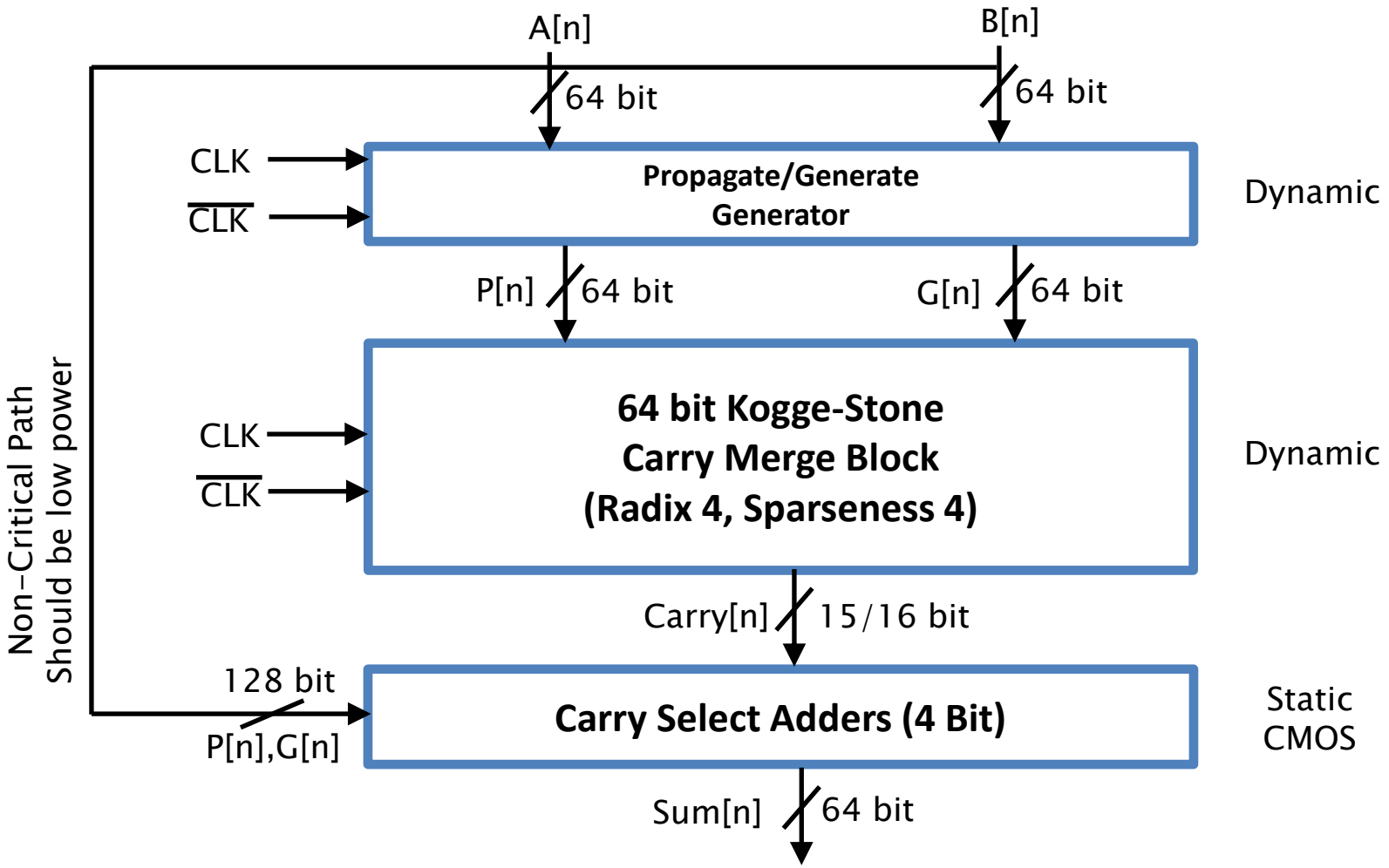
64 Bit Accumulator



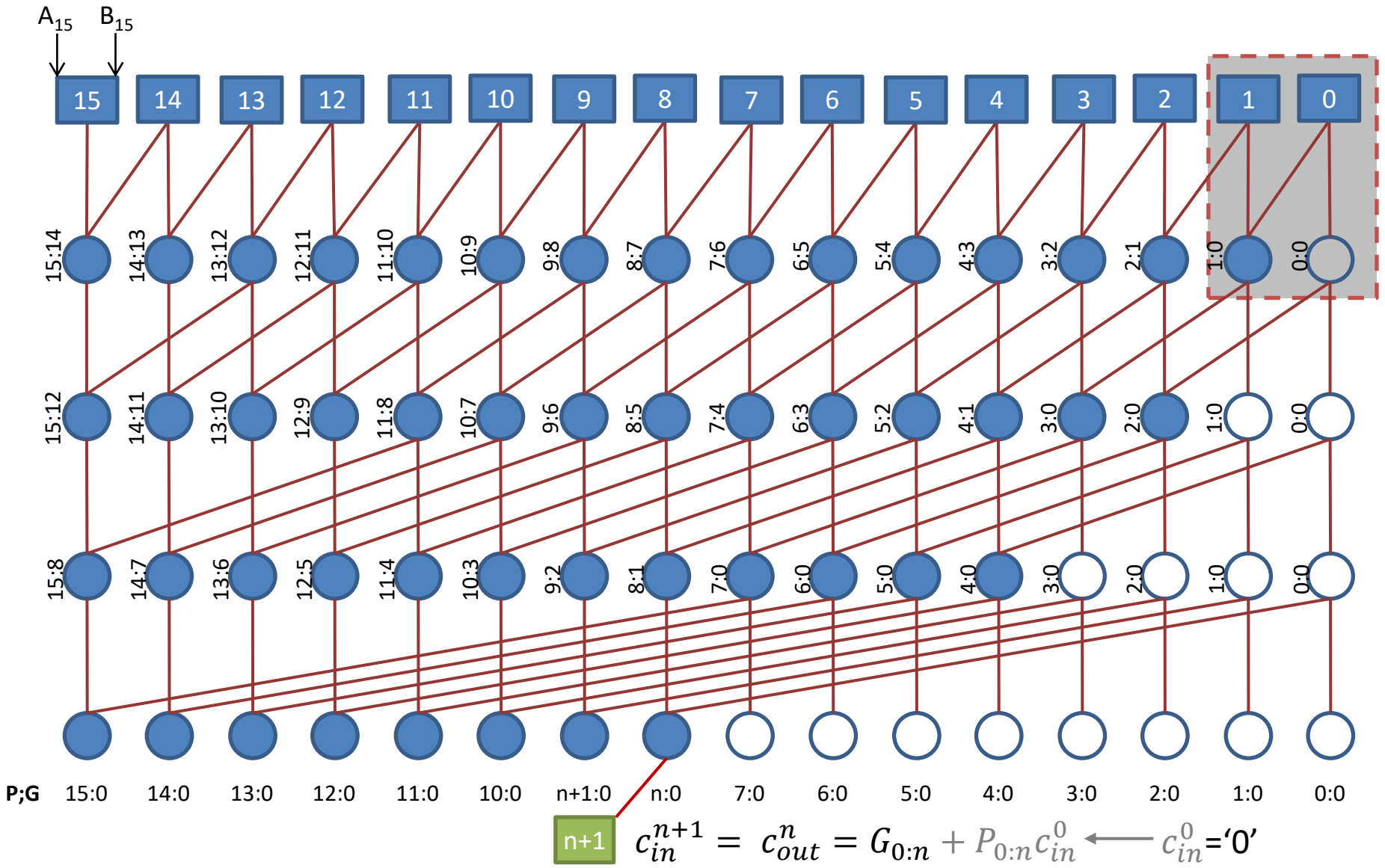
$$OUT_{64:0}[n+1] = OUT_{63:0}[n] + IN_{63:0}[n]$$

n: time index in discrete time domain

64 Bit Adder (Dynamic Logic)



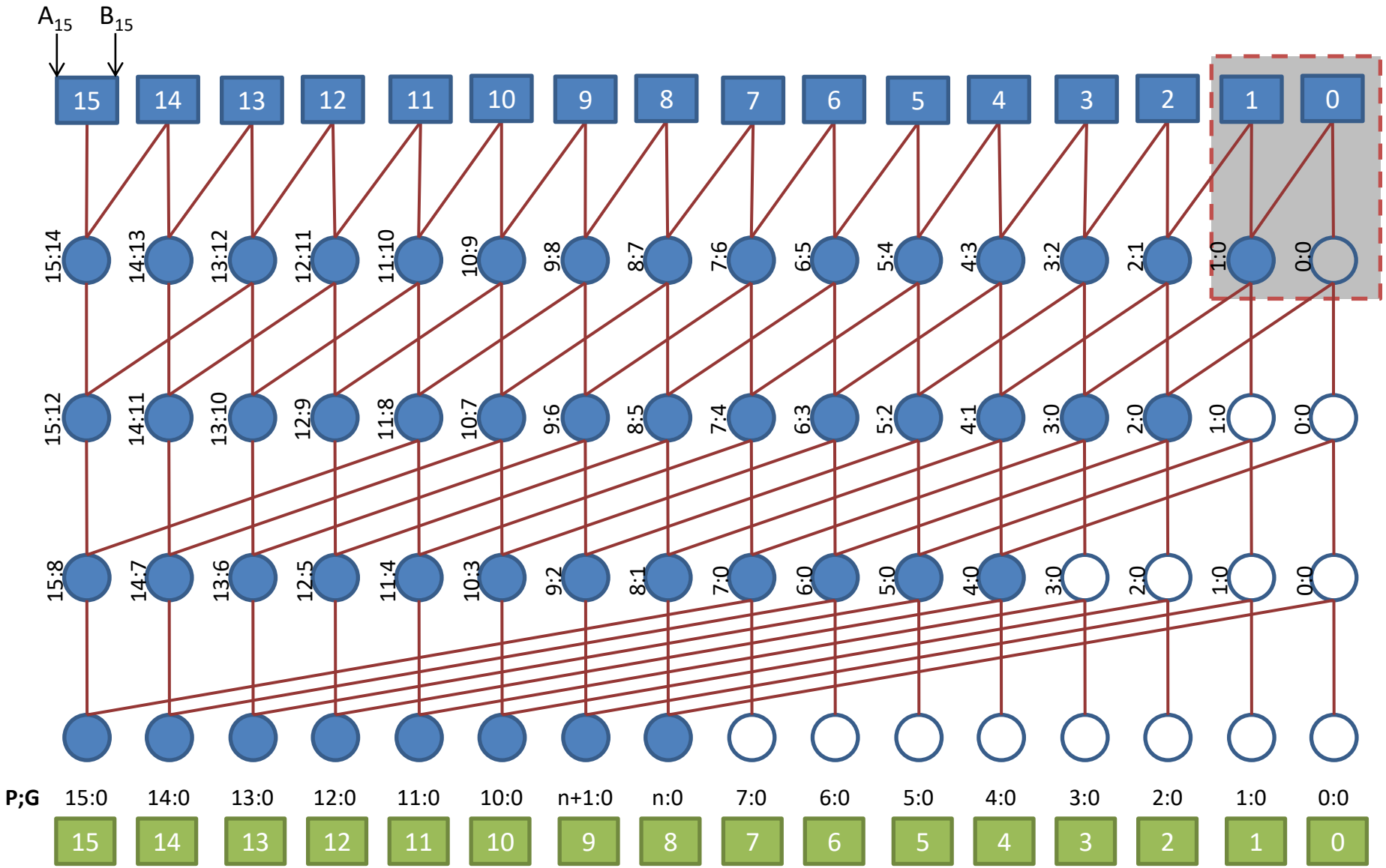
16 Bit Kogge-Stone



$$c_{in}^{n+1} = c_{out}^{n} = G_{0:n} + P_{0:n}c_{in}^{0} \longleftarrow c_{in}^{0}\text{='0'}$$

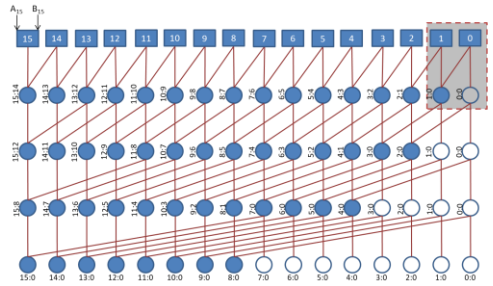
$$S_{n+1} = A_{n+1} + B_{n+1} + c_{in}^{n+1} = P_{n+1} + G_n$$

16 Bit Kogge-Stone



Propagate, Generate, Merging

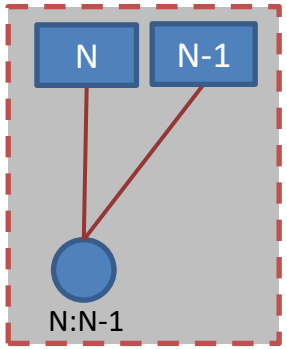
$$\begin{array}{cccccc} & \cdots & A_N & A_{N-1} & \cdots \\ + & \cdots & B_N & B_{N-1} & \cdots \\ \hline \end{array}$$



$P_{N-1} = A_{N-1} + B_{N-1}$
$G_{N-1} = A_{N-1} \bullet B_{N-1}$

$P_N = A_N + B_N$
$G_N = A_N \bullet B_N$

Predict C_N (carry) considering the stages N and N-1

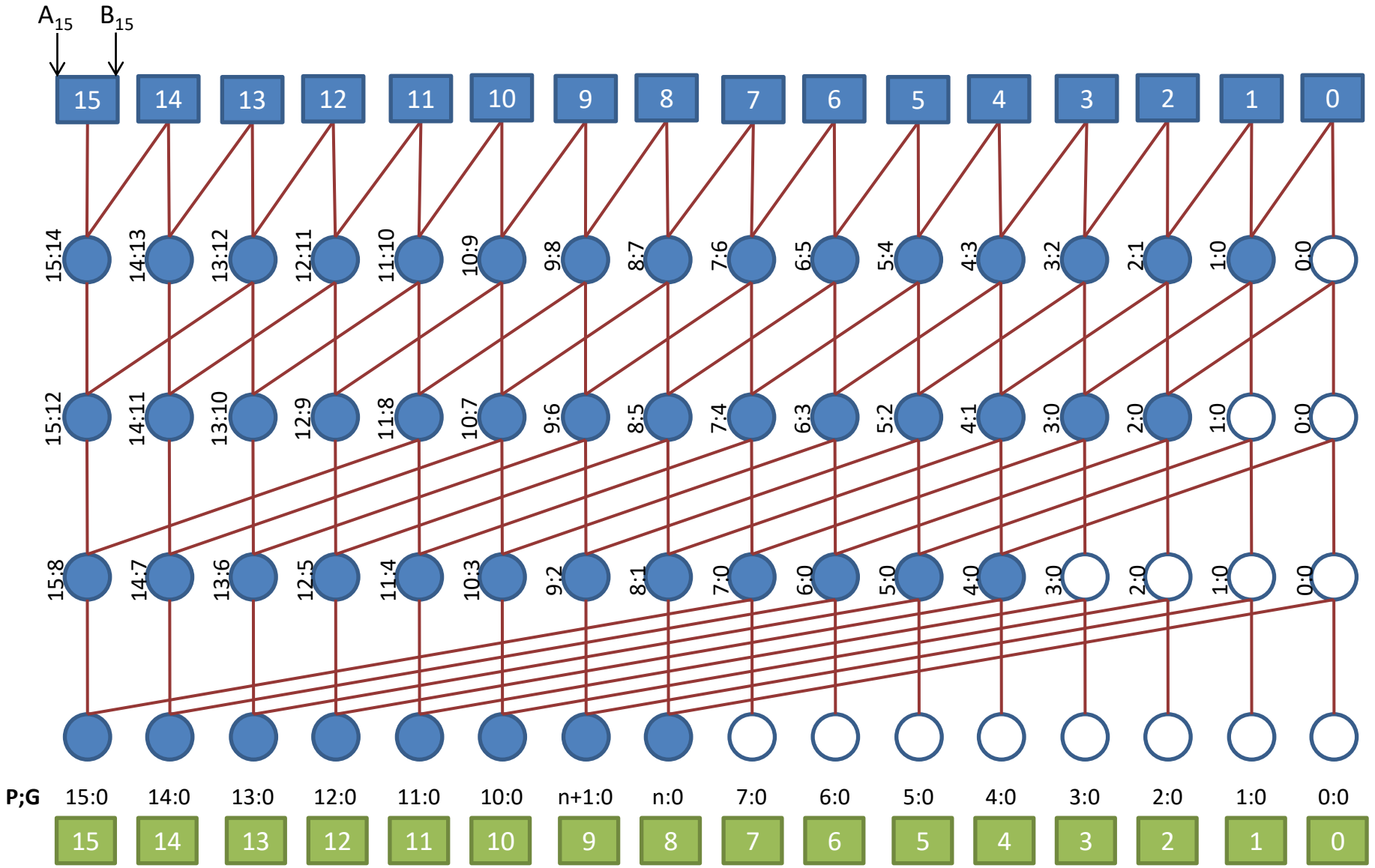


$G_{N:N-1} = G_N + P_N G_{N-1}$
$P_{N:N-1} = P_N P_{N-1}$

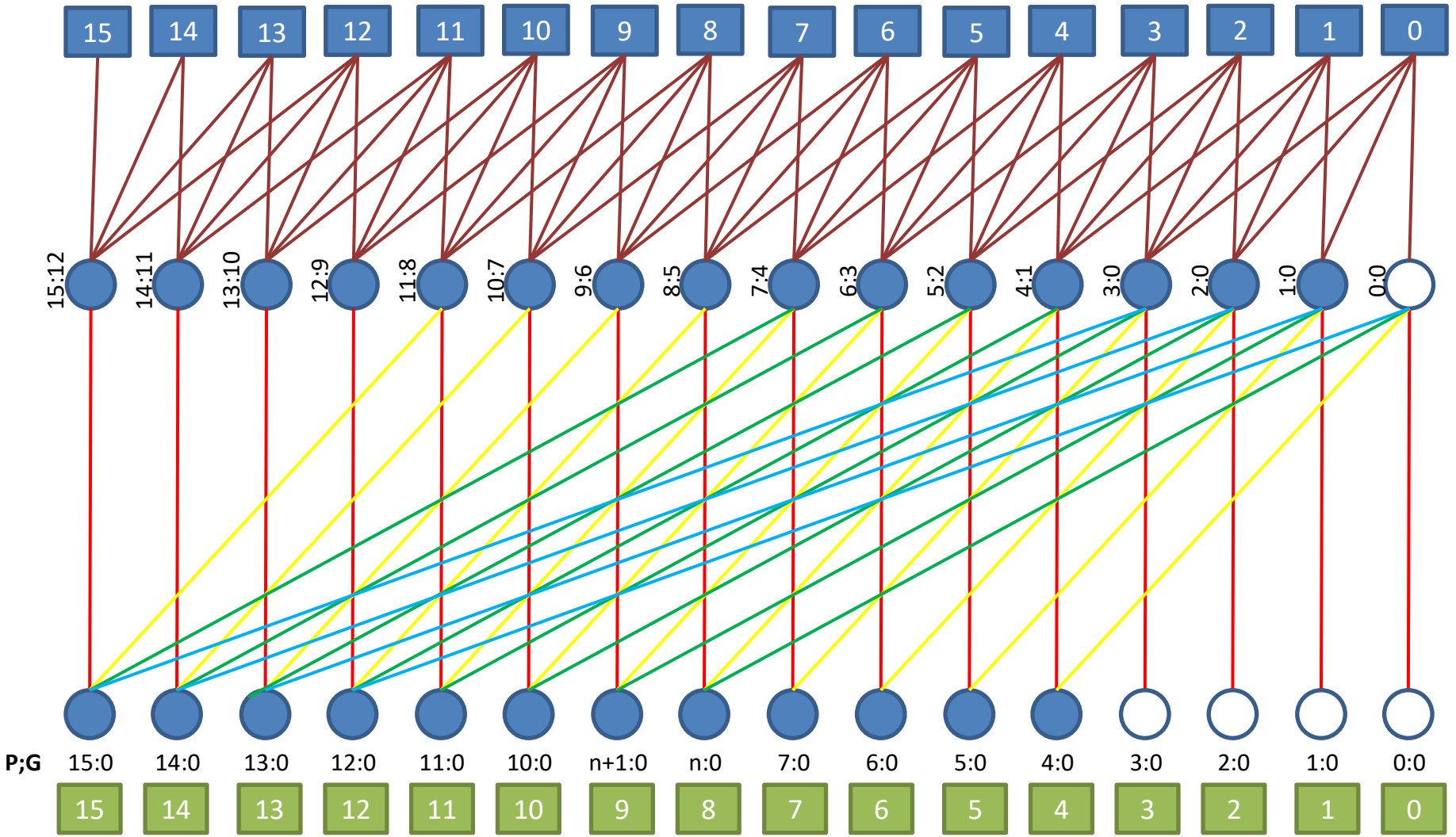
This Week Design!!

Implement with Dynamic Logic

16 Bit Kogge-Stone

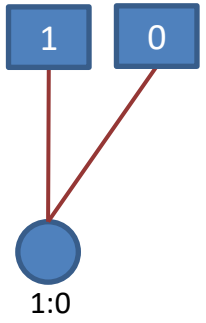


16 Bit Kogge-Stone (Radix 4)



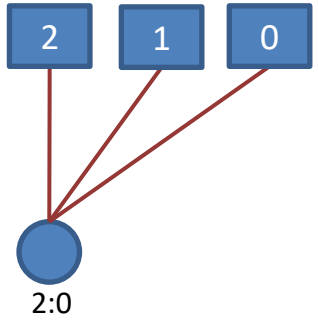
Radix 2,3,4

Radix 2
2 Inputs
Fanout: 2
2 Series MOS



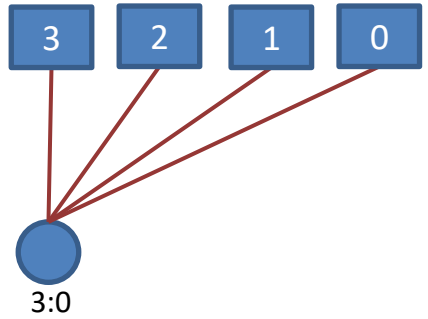
$G_{1:0} = G_1 + P_1 G_0$
$P_{1:0} = P_1 P_0$

Radix 3
3 Inputs
Fanout: 3
3 Series MOS



$G_{2:0} = G_2 + P_2 G_1 + P_2 P_1 G_0$
$P_{2:0} = P_2 P_1 P_0$

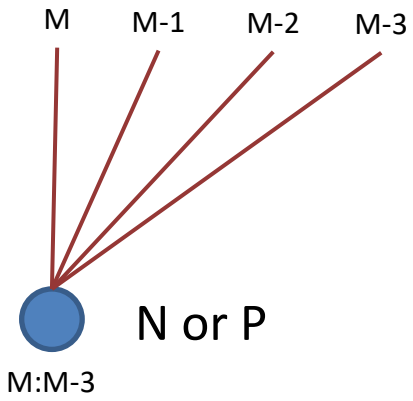
Radix 4
4 Inputs
Fanout: 4
4 Series MOS

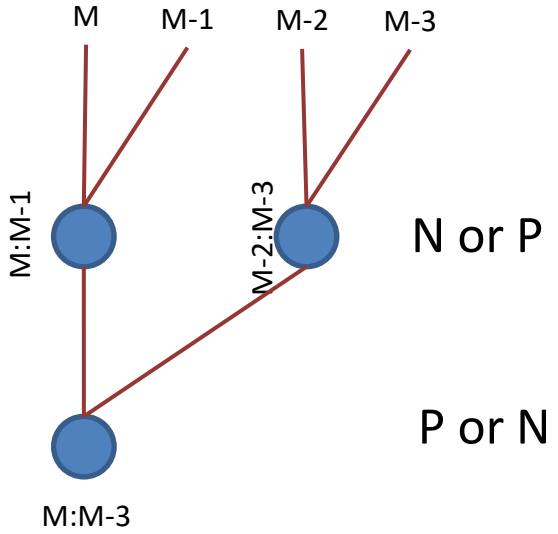


$G_{3:0} = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$
$P_{3:0} = P_3 P_2 P_1 P_0$

↑ Radix
↓Logic depth
↓Area
↑ Number of stacked MOS switches
↑ Fanout
↑ Gate complexity
↑ Top level routing Complexity

Atomic Element (Radix 4)



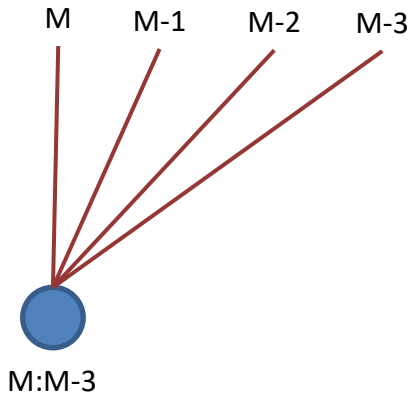


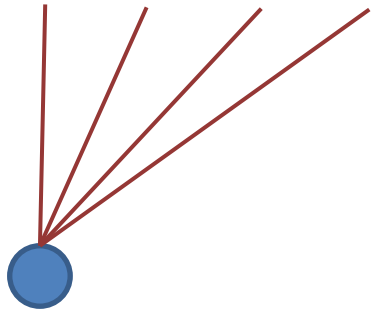
- More inputs per gate
- More stacked switches (4)
- Lower Logic Depth
- Smaller Area

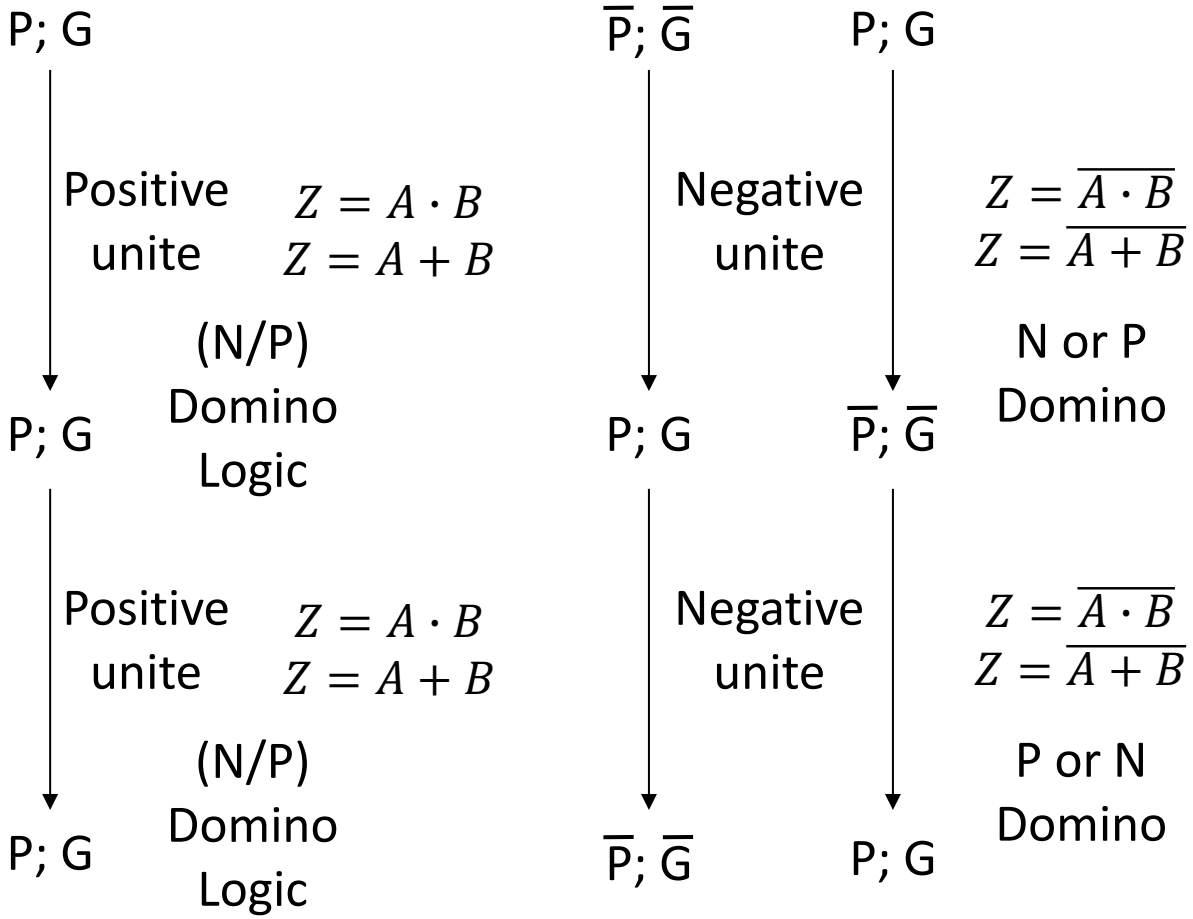
- Less inputs per gate
- Less stacked switches (2)
- Higher Logic Depth
- Bigger Area

- Speed ??? Decision depends on your simulations

Atomic Element (Radix 4)

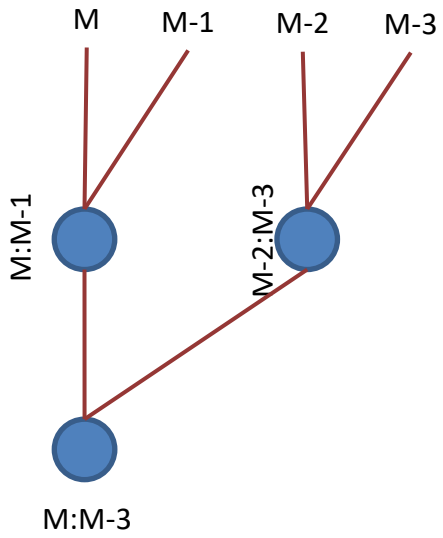


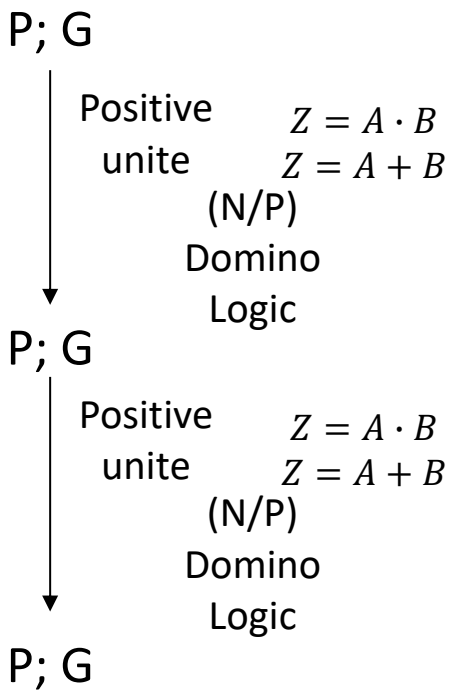


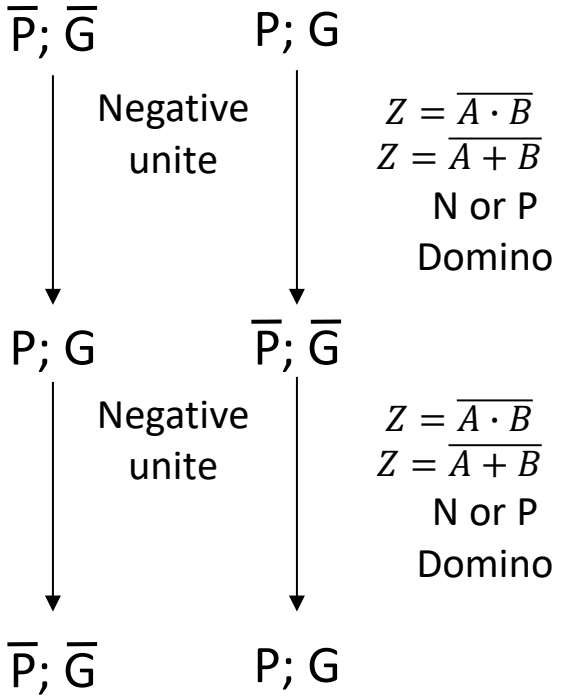


- Speed ??? Decision depends on your simulations

Atomic Element (Radix 4)

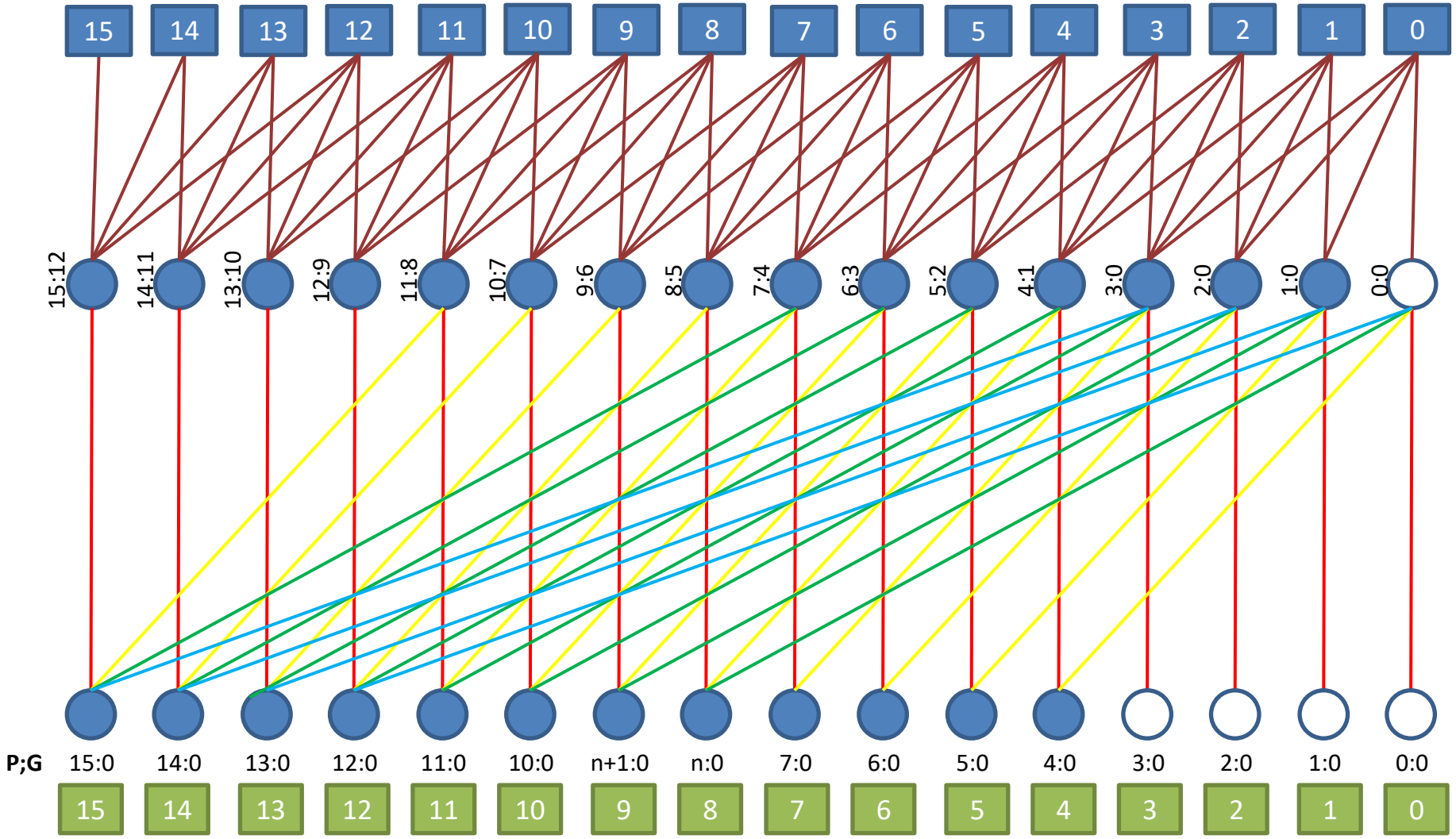






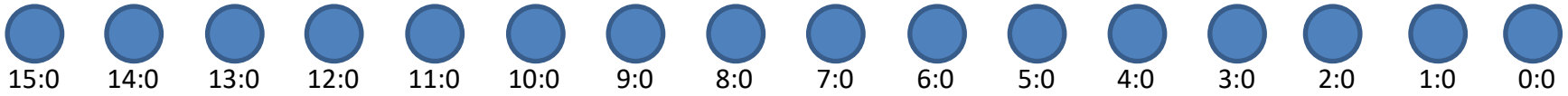
- Speed ??? Decision depends on your simulations

16 Bit Kogge-Stone (Radix 4)



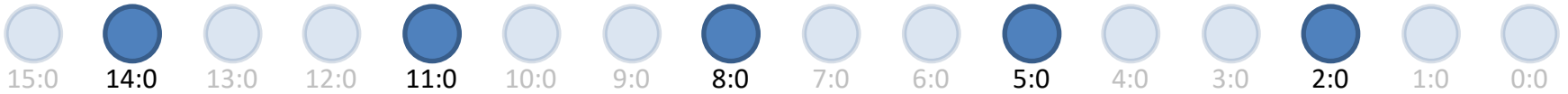
Sparsity

Sparseness 1



Sparseness 2

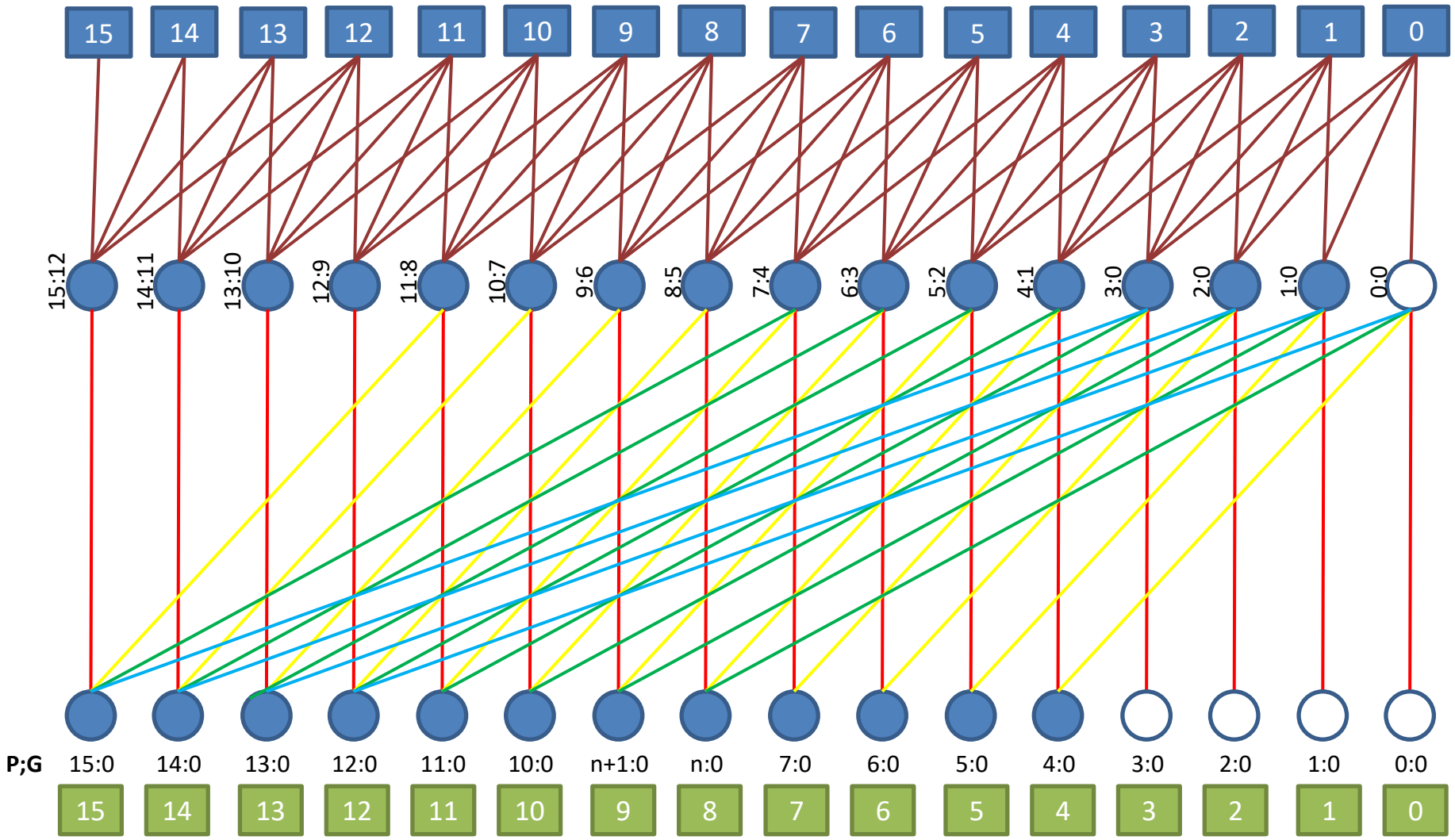
Sparseness 3



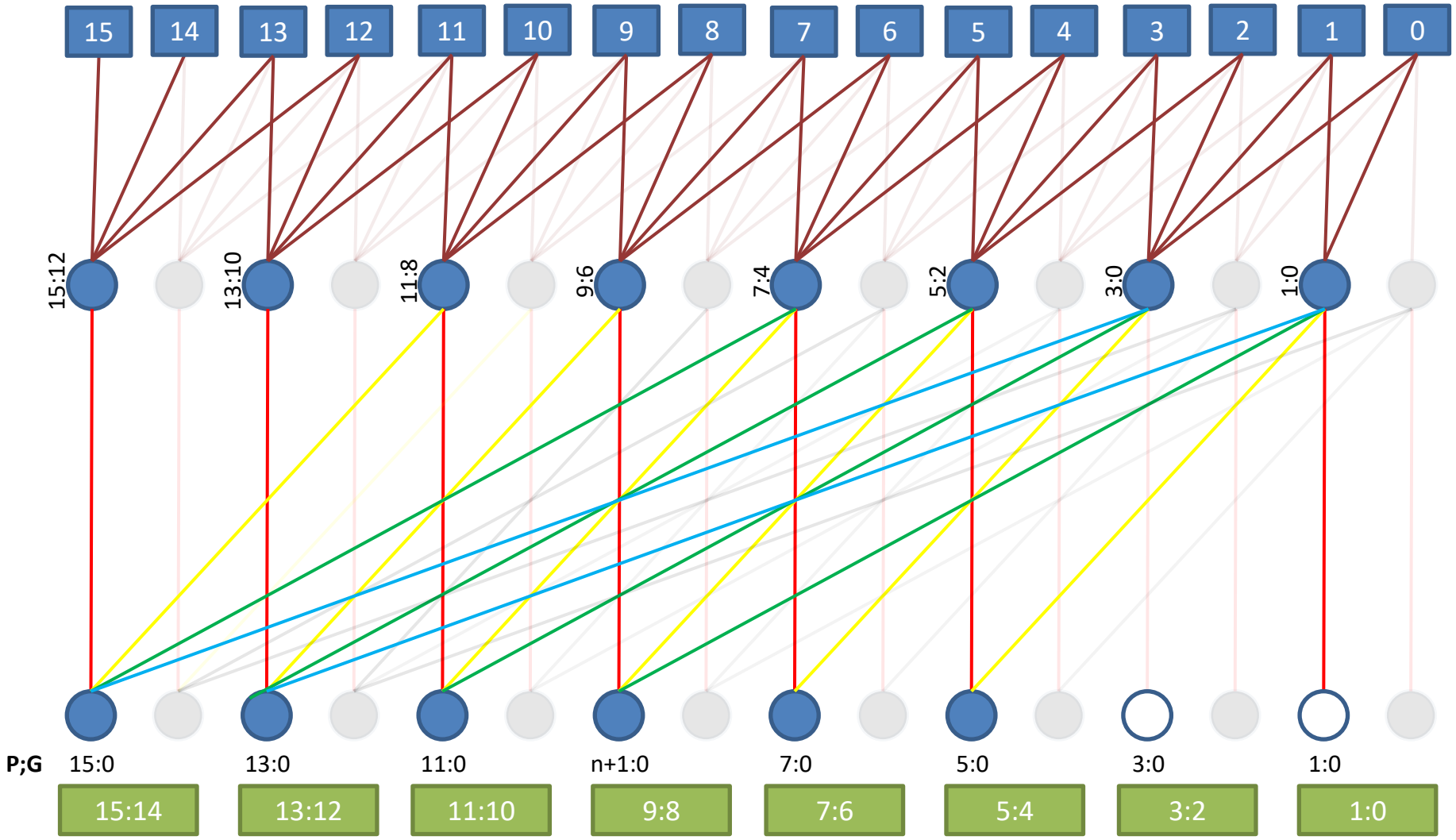
Sparseness 4

↑ Sparseness
↓Routing Complexity
↓Area (Carry Merge Block)
↑Need for Higher Number Bit Carry Select Adders

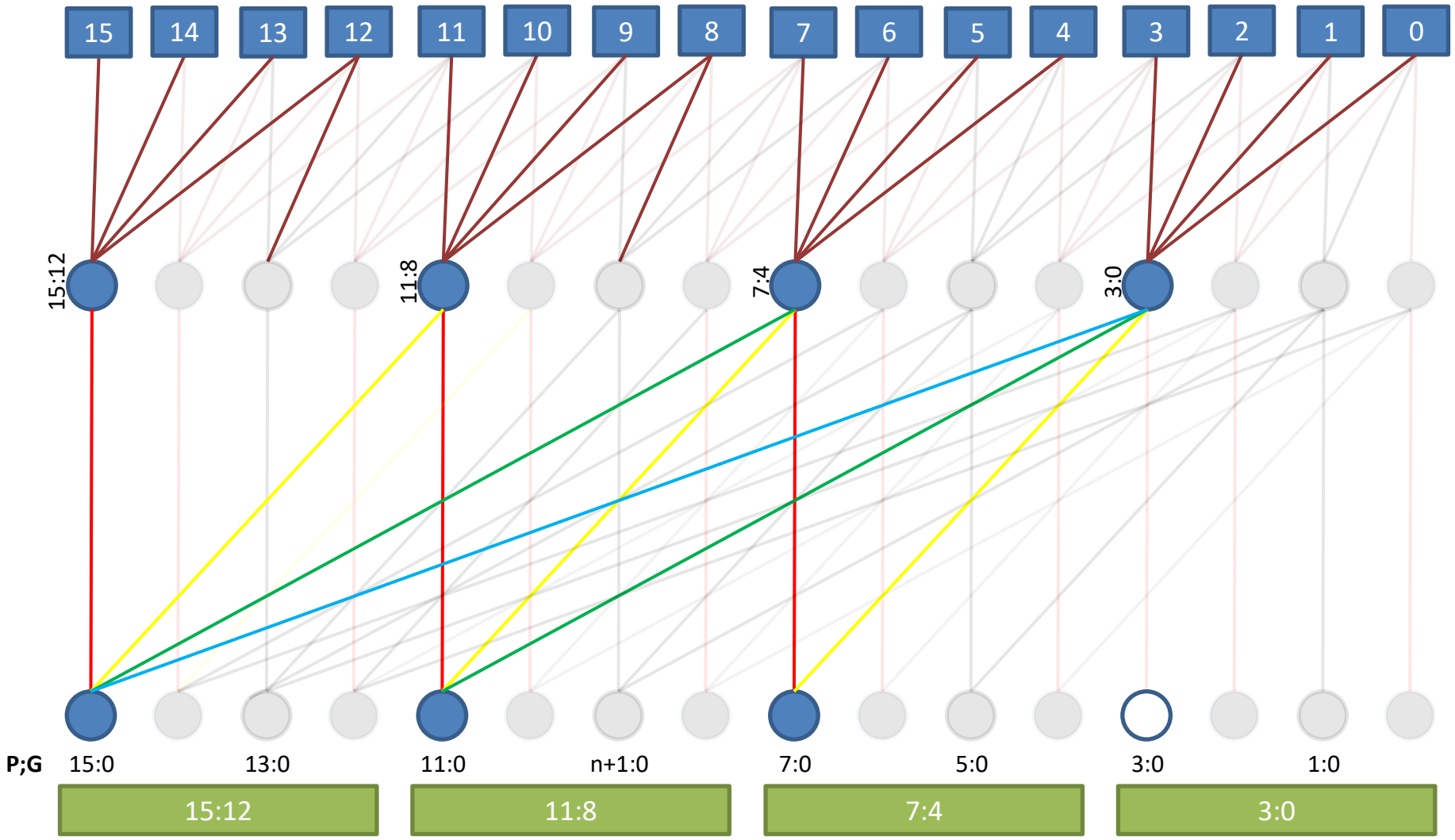
16 Bit Kogge-Stone (Radix 4)



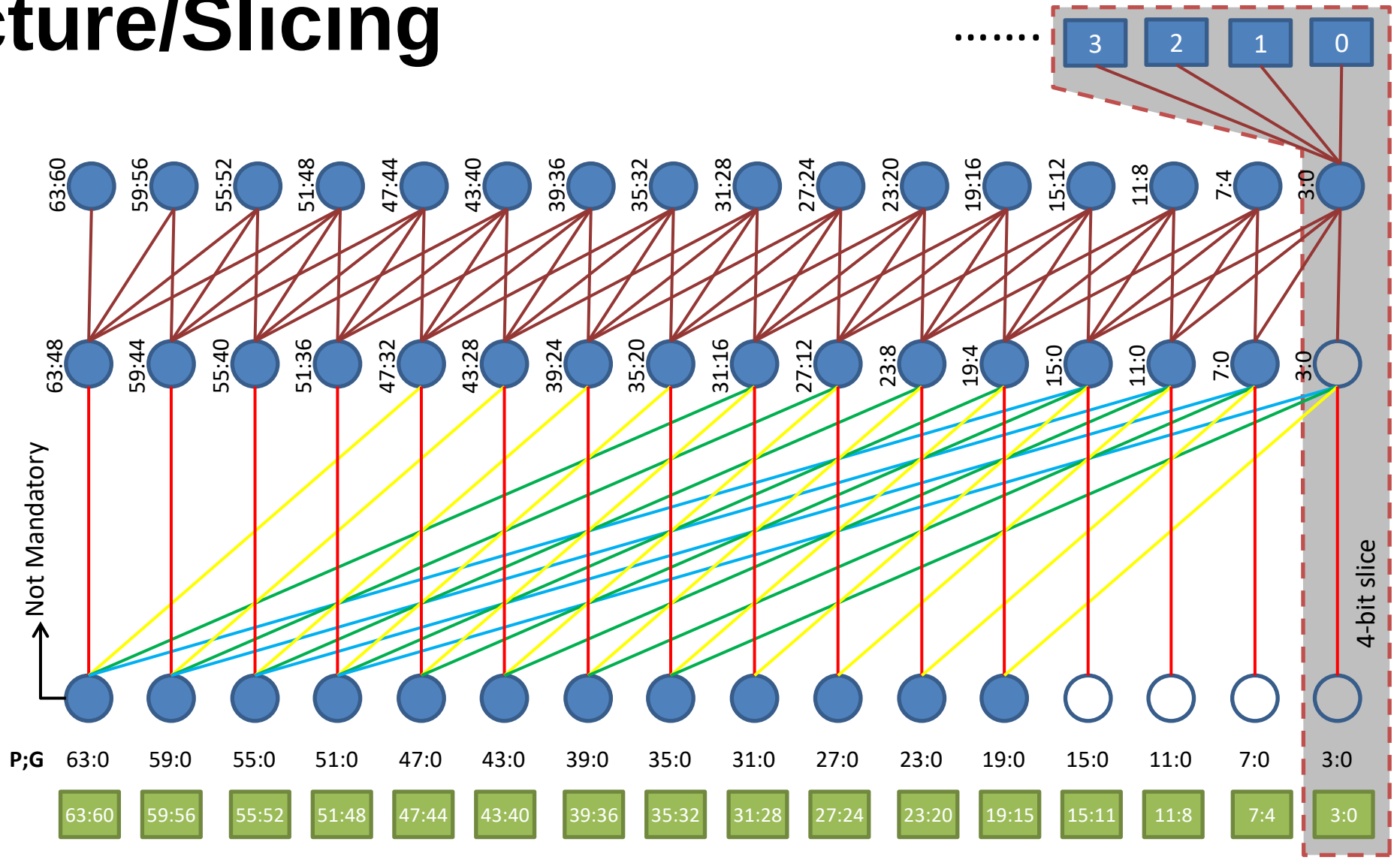
16 Bit Kogge-Stone (Radix 4, Sparsity 2)



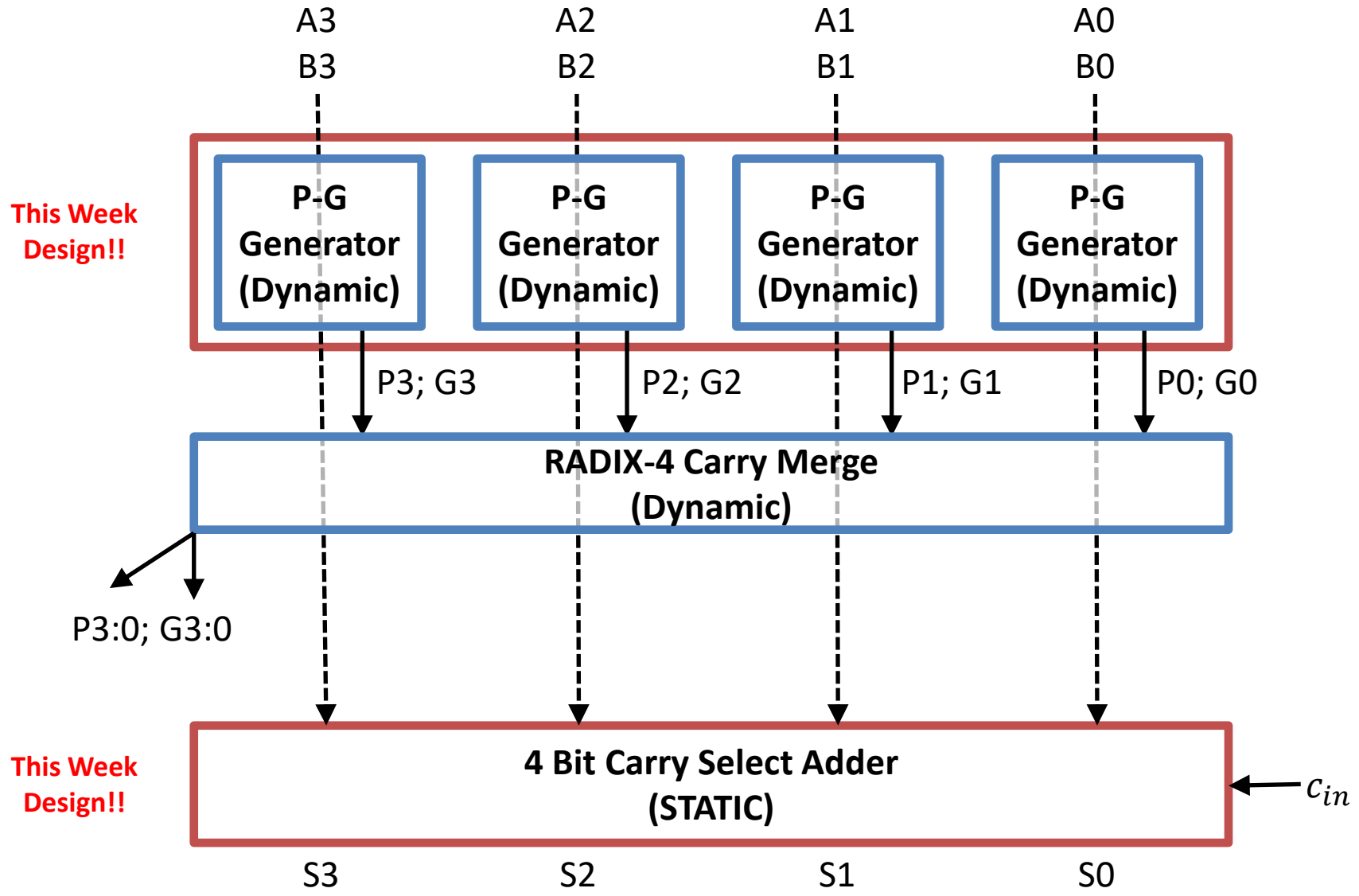
16 Bit Kogge-Stone (Radix 4, Sparsity 4)



64 Bit Kogge-Stone (Radix 4, Sparsity 4) Structure/Slicing



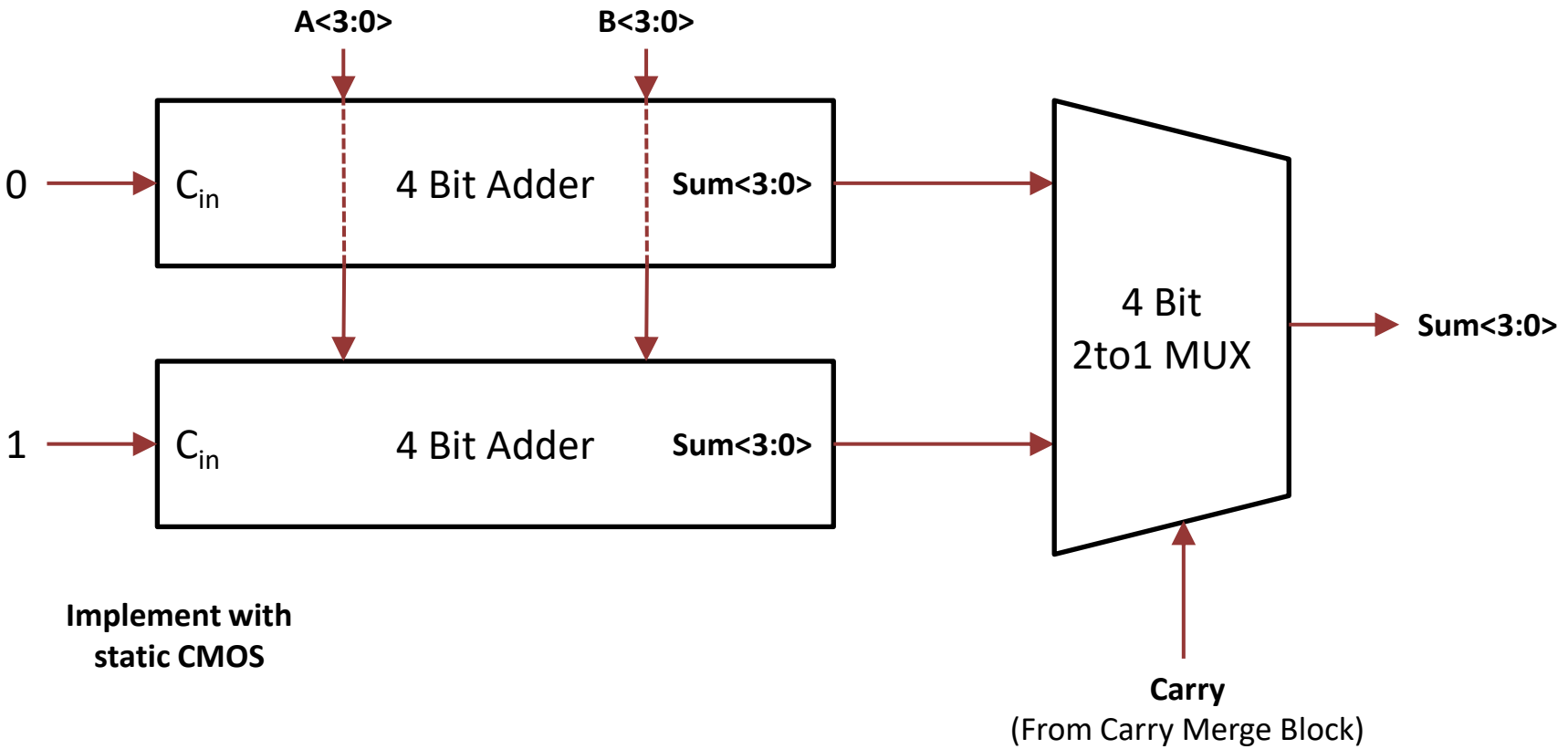
4-Bit SLICE


A3
B3
A2
B2
A1
B1
A0
B0
This Week Design!!
P-G Generator (Dynamic)
P-G Generator (Dynamic)
P-G Generator (Dynamic)
P-G Generator (Dynamic)
P3; G3
P2; G2
P1; G1
P0; G0
RADIX-4 Carry Merge (Dynamic)
P3:0; G3:0
This Week Design!!
4 Bit Carry Select Adder (STATIC)
c_{in}
S3
S2
S1
S0

Carry Select Adder

The result of the 4 bit addition is calculated in advance for both cases where

- Carry = 0
- Carry = 1



Carry Select Adder

- G-P Block & CSA: 1 week (4-bit slice)
- Carry Merge Block: 1 week
- D-FlipFlop: ½ week
- Top-level including clock tree: 1½ weeks

Questions?

16 Bit Kogge-Stone (Radix 2, Sparsity 4)