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Title

EXERCISE 8: PHASE LOCKED LOOP (PLL)

Course Name

EE-465 Industrial Electronics I

1 INTRODUCTION

Measuring the grid votlages phase angle is essential for proper control of a grid connected converter. A phase locked loop (PLL) is used to achieve this phase angle measurement in power electronics systems.
Since grid voltages are sometimes prone to disturbances in the real world, the provided PLECS template generates a set of balanced three-phase voltages with varying phase and amplitude over time, voltages unbalances will be dealt with in a future exercise. You will implement a basic PLL algorithm to estimate the phase angle of these voltages and observe how it reacts to the changes in voltage magnitude and phase.

In the provided skeleton model, the grid voltages in *abc* frame are generated, they are inputs to your PLL. In addition, the real grid frequency and angle are provided as outputs for comparison purpose. The grid voltage expression is

$$v_g = V_g \begin{bmatrix} \cos(\omega t + \varphi) \\ \cos(\omega t - 2\pi/3 + \varphi) \\ \cos(\omega t + 2\pi/3 + \varphi) \end{bmatrix}$$

With V_g and φ varying over the simulation time.

2 TASKS DESCRIPTION

1. Implement a continuous-time PLL based on *dq* coordinate transformation, where the Park transformation acts as quadrature signal generator. Design your PLL for a settling time $t_s = 100$ ms and a damping factor $\xi = \sqrt{2}/2$. Is the PLL settling time impacted by the grid voltage magnitude? If yes which measure has to be taken in order to ensure a constant settling time independently of the grid voltage magnitude? Implement that measure. For the report, provide a schematic capture of your implementation and a capture of the scope provided in the template, and comment what happens if you tune your PLL for a smaller t_s.

2. In a real grid, some voltage harmonics are likely going to be present. The parameter h initially set to 0 in the template can be used to add a harmonic in the generated voltages in the form of $v_g' = v_g + v_h$, where

$$v_h = V_h \begin{bmatrix} \cos(h(\omega t + \varphi) + \varphi_h) \\ \cos(h(\omega t - 2\pi/3 + \varphi) + \varphi_h) \\ \cos(h(\omega t + 2\pi/3 + \varphi) + \varphi_h) \end{bmatrix}$$

   with $V_h = 0.05V_g$. h is therefore the order of the harmonic injected on top of the fundamental frequency. Set h to 3, 5 and 7 and discuss how these affect your PLL. In the report, provide a scope capture of the relevant waveforms. Consider the zero component of the voltages defined as $v_0 = (v_a + v_b + v_c)/3$.
   Again, comment on what happens if you tune your PLL targeting a different t_s