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Title

EXERCISE 2: CONTINUOUS-TIME CONTROL OF THE INPUT BOOST STAGE

Course Name

EE-465 Industrial Electronics I

1 INTRODUCTION

Last week, the relevant transfer function in action in your model have been identified. The cascaded control for the input stage will be implemented, first in continuous-time domain, without considering the actuator limits (no saturations). The converter ratings are unchanged (see Table 1).

C_{PV}	47 µF	L_B	*from Exercise 1*	R_B	2 mΩ
C_{DC}	*from Exercise 1*	R_{load}	*from Exercise 1*	f_{sw}	10 kHz

Table 1 Boost converter parameters.

2 TASKS DESCRIPTION

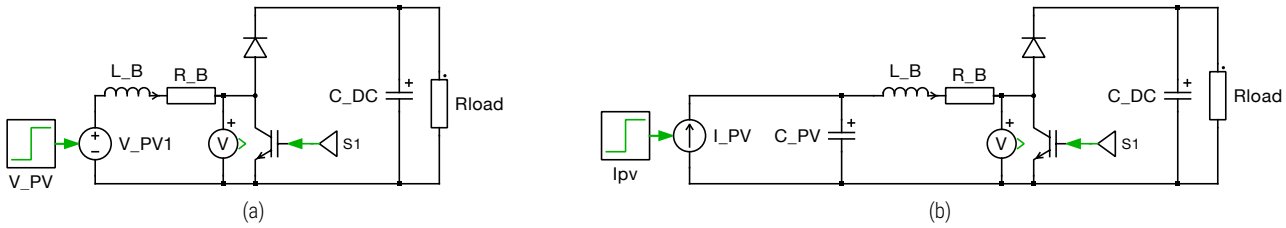

Fig. 1 Circuits to consider for control implementation: (a) inner control loop and (b) cascaded control.

2.1 Tasks Description

1. Determine the gains of the PI controller that you will use for current control. Use the Magnitude Optimum criterion and consider an equivalent time constant for all delays of $T_\Sigma = 1.5T_{sw}$. What values of T_n and T_i do you obtain?
   For the report, write the equations that you used for T_n and T_i, describe their parameters and report the numerical result.

2. Use the "Exercise_2-InnerLoop_skeleton" file to implement the inner loop controller. The three subsystems (PI current, D calculation, Modulator) need to be populated. Modify all the initialization parameters to the correct values.
   Test your controller tuning from the previous point for the following conditions: step in $i^\star_{L,B}$ at $t = 0.05$ s from 100 A to 50 A and step in V_{PV} at $t = 0.1$ s from 200 V to 300 V (these steps are already implemented in the template). What are the overshoot (in %) and settling time (consider from change of reference to +5 % of the reference difference)? Document this in the report and provide a PLECS scope capture around $t = 0.05$ s

3. Determine the gains of the PI controller that you will use for outer control loop (input voltage control). Determine the gains of the controller according to the Symmetrical Optimum criterion. For this task, the inner control loop can be approximated as a first order delay transfer function. What time constant T_Σ should be considered for the delays in the outer loop ? What are the values of T_n and T_i for the voltage control loop?
   For the report, write the equations that you used for T_n and T_i, describe their parameters and report the numerical result. In particular, discuss what T_Σ you considered.

4. Use the "Exercise_2-CascadeLoop_skeleton" file to implement the cascaded control loops. The all subsystems (PI voltage, PI current, D calculation, Modulator) need to be populated, for the inner loop. For the moment, the voltage reference filter is made transparent ($T_{LPF} = 0$).

Test your outer control loop for the following conditions: step in i_{PV} at $t = 0.05$ s from 100 A to 50 A and step in V^{*}_{PV} at $t = 0.1$ s from 200 V to 400 V (these steps are already implemented in the template). What are the overshoot (in %) and settling time? Add a low pass filter $1/(T_{LPF}s + 1)$ on the reference signal, as presented during the lecture, to limit the overshoot. What is the cause of the overshoot? Try out different time constants for the filter and discuss their effect on reference tracking and disturbance rejection performance. You can use the "Hold current trace" function in the PLECS scope to compare different simulation runs (fig. 2).
For the report, reply to these questions, document the rise time and overshoot when using the T_{LPF} that choose to keep, and provide a scope capture for the full simulation time (0.2s).

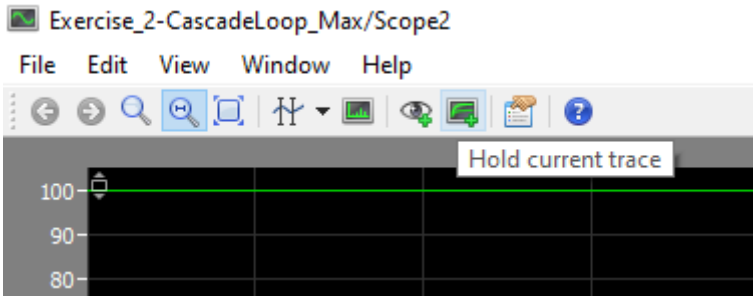

Fig. 2 Hold current trace function in PLECS scope.