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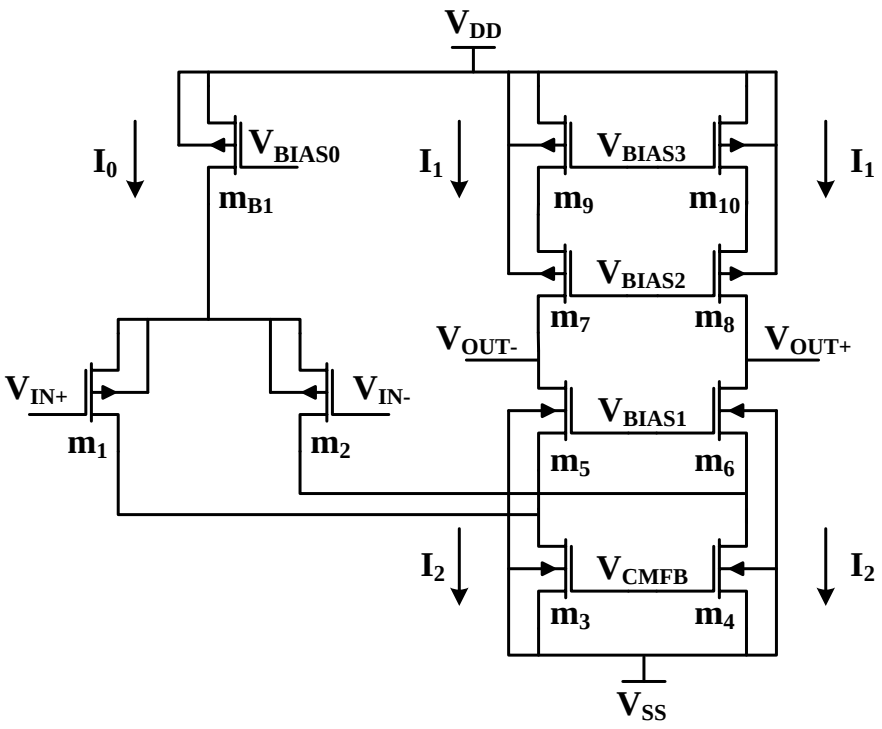
1. Fully differential folded cascode OTA: Procedural sizing

The purpose of this section is to provide the sizing procedure of the following OTA step-by-step. Starting by choosing circuit-level parameters (specifications) and propagating them to transistor level.



The technology used is UMC 180nm 1.8V devices and their parameters are:

Parameter		Unit Extracted	
K_p	PMOS	40	$\mu A/V^2$
	NMOS	208	
U_a	PMOS	16	V/µm
	NMOS	5	
n	PMOS	1.3	-
	NMOS	1.2	
C_{ox}		8.3	$fF/\mu m^2$

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The OTA, have to meet the following specifications.

Parameter	Value Specification		Unit
Open-loop gain	> 70		dB
GBW	60		MHz
Slew rate [**SR**]	50		V/µs
Load capacitance [C_L]	100		fF

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1.1. Bias currents

	Parameter	Expression	Value	Unit	Guideline
Bias	I_o	$SR \times 2C_L$	10	µA	From SR
	I_1	$1,2 \times \frac{I_o}{2}$	6	µA	

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1.2. Differential pair

Determine the transconductance, inversion factor and W/L ratio of the differential pair.

	Parameter	Expression	Value	Unit	Guideline
Differential pair	$g_{m1,2}$	$f_{gbw} \times 2 \times \pi \times C_L$	37.7	μS	From GBW
	$I_{f1,2}$	$\left(\left(\frac{2I_{D1,2}}{(n \times u_T \times g_{m1,2})} - 1\right)^2 - 1\right)\frac{1}{4}$	11.47	-	From $\frac{g_{m2}}{I_{D2}}$
	$\frac{W_{1,2}}{L_{1,2}}$	$\frac{Id_{1,2}}{2 \times n \times K_p \times I_{f1,2} \times u_T^2}$	4.77	-	From I_{f2}

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1.3. Folded cascode load

The 8 transistors composing the folded cascode stage will now be sized.
Determine the inversion factor and W/L ratio of these transistors to:

- Keep all saturation voltages of m10, m8, m6 small
- Minimize the noise and offset contribution of m_3 and m_4
- For simplification, only two values will be chosen for the inversion factor: **I_F= 10 or I_F = 1**.

	Parameter	Expression	Value	Unit	Guideline
Folded	$\frac{W_5}{L_5}$	$\frac{I_1}{2 \times n \times K_{p,n} \times I_{f5} \times u_T^2}$	15		Minimize saturation voltages $I_{f5} = 1$ save area
	$\frac{W_7}{L_7}$	$\frac{I_1}{2 \times n \times K_{p,p} \times I_{f7} \times u_T^2}$	64.1		Minimize saturation voltage $I_{f7} = 1$ save area

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	$\frac{W_9}{L_9}$	$\frac{Id_9}{2 \times n \times K_p \times I_{f9} \times u_T^2}$	64.1		Minimize saturation voltages $I_{f9} = 1$ save area
	$\frac{W_3}{L_3}$	$\frac{Id_3}{2 \times n \times K_p \times I_{f3} \times u_T^2}$	2.8		Minimize noise contribution $I_{f3} = 10$ Operate in strong inversion

2

Calculate the output resistance necessary to meet the open-loop gain specification.

	Parameter	Expression	Value	Unit	Guideline
Rout	R_{out}	$\frac{A_0}{g_{m1,2}}$	84	MΩ	

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Neglecting the conductance of the differential pair (assume $g_{ds1} \approx 0.5 g_{ds3}$), determine the conductance and length of all transistors so that:

- The specified open-loop gain is achieved
- The NMOS and PMOS resistances at the output node are balanced ($R_{up} = R_{down}$)
- The total area of the folded cascade stage is minimized (in the order of 85µm^2)
  - m_7 and m_9 have the same length
  - The length of m_3 is two times the one of m_5

	Parameter	Expression	Value	Unit	Guideline
Rout	$n_{np} \times g_{m5,7}$	$\frac{1}{u_T} \times \frac{2I_1}{1 + \sqrt{1 + 4I_{f5,7}}}$	142.6	µS	
	R_{up}	$\frac{g_{m7}}{g_{ds7} \times g_{ds9}}$	168	MΩ	$R_{up} = R_{down} = 2R_{out}$
	$L_7 \times L_9$	$\frac{2 \times R_{out} \times I_1^2}{g_{m5,7} \times U_{ap}^2}$	0.215	µm^2	
	L_9	$L_7 = L_9 = \sqrt{L_7 \times L_9}$	464	nm	$L_7 = L_9$
	L_7	$L_7 = L_9 = \sqrt{L_7 \times L_9}$	464	nm	$L_7 = L_9$
	R_{down}	$\frac{g_{m5}}{g_{ds5} \times (g_{ds1} + g_{ds3})}$	168	MΩ	$R_{up} = R_{down} = 2R_{out}$

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	$L_3 \times L_5$	$\frac{1.5 \times 2 \times R_{out} \times I_{D3} \times I_{D5}}{g_{m5} \times U_{an}^2}$	5.52	µm^2	
	L_5	$L_5 = \frac{L_3}{2}$	1.66	µm	$L_3 = 2L_5$
	L_3	$L_3 = 2L_5$	3.3	µm	$L_3 = 2L_5$

1

Calculate the width of all transistors.

	Parameter	Expression	Value	Unit	Guideline
Rout	W_3	$\frac{W_3}{L_3} \times L_3$	9	µm	
	W_5	$\frac{W_5}{L_5} \times L_5$	25	µm	
	W_7	$\frac{W_7}{L_7} \times L_7$	29.7	µm	
	W_9	$\frac{W_9}{L_9} \times L_9$	29.7	µm	

1

1.4. Differential pair finalization & Current source

Find the length and the width of the differential pair.

Parameter	Expression	Value	Unit	Guideline
L_1	$2\frac{I_{D1}}{I_{D3}} \times \frac{U_{an}}{U_{ap}} \times L_3$	**850**	nm	$g_{ds1} \leq 0.5 g_{ds3}$
W_1	$\frac{W_1}{L_1} \times L_1$	**4**	µm	

1

Parameter	Expression	Value	Unit	Guideline
L_{B1}	$L_{B1} = L_9$	**464**	nm	Should match with M9

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W_{B1}	$\frac{I_0}{I_1} \times W_9$	**49.5**	µm	Should match with M9	**1**

1.5 Offset Estimation:

In case of the above folded cascade, give the expression of the input referred offset that include the contribution of Differential pair: $m_{1,2}$; Folded cascode: $m_{3,4}$ and Active load: $m_{9,10}$

$$\sigma_{Vos}^{\ 2} = \sigma_{VT}^2 + \left(\frac{I_0}{2gm_{1,2}}\right)^2 \left(\sigma'_{\beta 1,2}\right)^2 + \left(\frac{gm_{3,4}}{gm_{1,2}}\right)^2 \sigma_{VT}^2 + \left(\frac{I_{3,4}}{gm_{1,2}}\right)^2 \left(\sigma'_{\beta 3,4}\right)^2 + \left(\frac{gm_{9,10}}{gm_{1,2}}\right)^2 \sigma_{VT}^2 + \left(\frac{I_{9,10}}{gm_{1,2}}\right)^2 \left(\sigma'_{\beta 9,10}\right)^2$$

1 **2** **2**

$$\sigma'_{\beta i} = \sigma_{\beta i}/\beta_i$$

Theoretical reminder: $\sigma_{V_G}^{\ 2} = \frac{\sigma_{I_D}^{\ 2}}{g_m^2}$

$$\sigma_{I_D(\beta,V_{T0})}^{\ 2} = \sigma_\beta^{\ 2}\left(\frac{\partial I_D}{\partial \beta}\right)^2 + \sigma_{V_{T0}}^{\ 2}\left(\frac{\partial I_D}{\partial V_{T0}}\right)^2$$

$$= \sigma_\beta^{\ 2}\left(\frac{I_D}{\beta}\right)^2 + \sigma_{V_{T0}}^{\ 2}(g_m)^2$$

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1.6 Common-mode feedback CMFB

Propose a CMFB circuit that use two differential pairs to tune the gate voltage of mB1 and set the common-mode output voltage to $V_{DD}/2$. Show how this CMFB circuit is connected to the fully differential cascode OTA (i.e. give the name of its input and output nodes)