

Bandgap References : Supply and Temperature Independent References

Analog Circuits Design I
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Outline

- MOSFET: Temperature dependence
- Supply-Independent Biasing
 - Power supply Sensitivity
 - Temperature sensitivity
- Temperature-Independent References
 - Negative-TC Ref(CTAT)
 - Positive-TC Ref (PTAT)
 - Band Gap Reference Design

MOSFET: Temperature dependence of V_T

- Many parameters of MOSFET vary with temperature, but two of them dominate: V_T and μ
- Threshold voltage is usually defined as the gate voltage for which the channel is as much n-type as the substrate is p-type resulting in:

$$V_{T0} = \phi_{ms} + 2\phi_B + \frac{Q_{dep}}{C_{ox}} = -\frac{kT}{q} \ln\left(\frac{N_{D,poly}}{N_{sub}}\right) + \frac{Q_{dep}}{C_{ox}}$$

$$\frac{\partial V_T}{\partial T} \approx -\frac{k}{q} \ln\left(\frac{N_{D,poly}}{N_{sub}}\right) \quad \text{with} \quad \frac{k}{q} = \frac{\partial U_T}{\partial T} \approx 85 \mu V/^{\circ}C$$

ϕ_{ms} : is gate-substrate work functions difference
 ϕ_B : electrostatic potential of the bulk (p-type substrate)
 Q_{dep} : charge in the depletion region

- V_{T0} decreases when T increases

Ex. For $N_{D,poly}=10^{20} \text{ cm}^{-3}$ and $N_{sub}=10^{17} \text{ cm}^{-3}$

$$\rightarrow \frac{\partial V_T}{\partial T} \approx -0.6 \text{ mV}/^{\circ}C$$

- The temperature coefficient of V_{T0} (TC_{VT}) is defined

$$TC_{VT} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} < 0$$

$$\rightarrow V_T(T) = V_T(T_0)(1 + TC_{VT} (T - T_0))$$

- The threshold voltage of a MOSFET exhibits a negative TC (but not well-defined)

MOSFET: Temperature dependence of μ

- Due to thermal agitation, μ decreases when T increases (@ a first approximation) as:

$$\mu(T) = \mu(T_0) \left(\frac{T_0}{T} \right)^{1.5}, T_0 = 300 \text{ }^\circ\text{K}$$

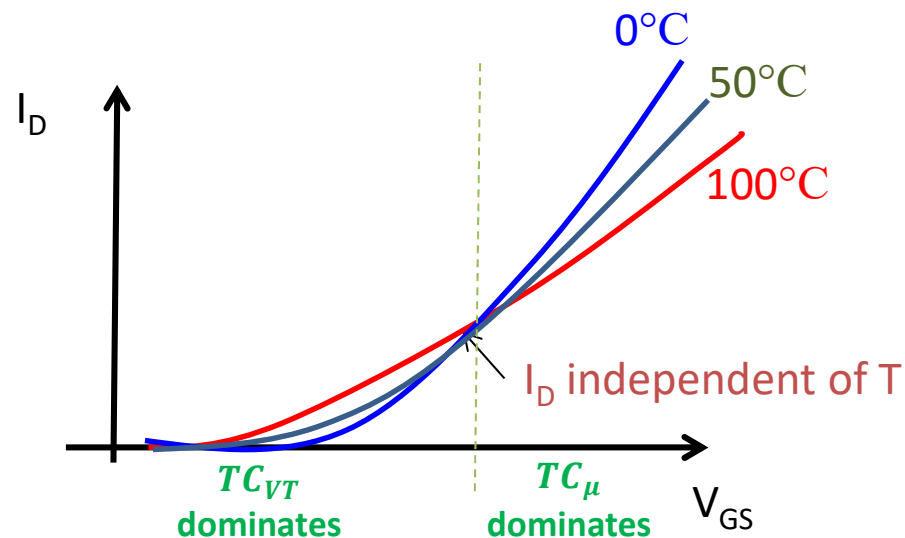
- The channel Mobility exhibits a negative TC

$$\rightarrow TC\mu(T) = \frac{1}{\mu(T)} \frac{\partial \mu(T)}{\partial T} \approx -\frac{1.5}{T}$$

and $\mu(T) = \mu(T_0) \left(1 - \frac{1.5}{T} (T - T_0) \right)$

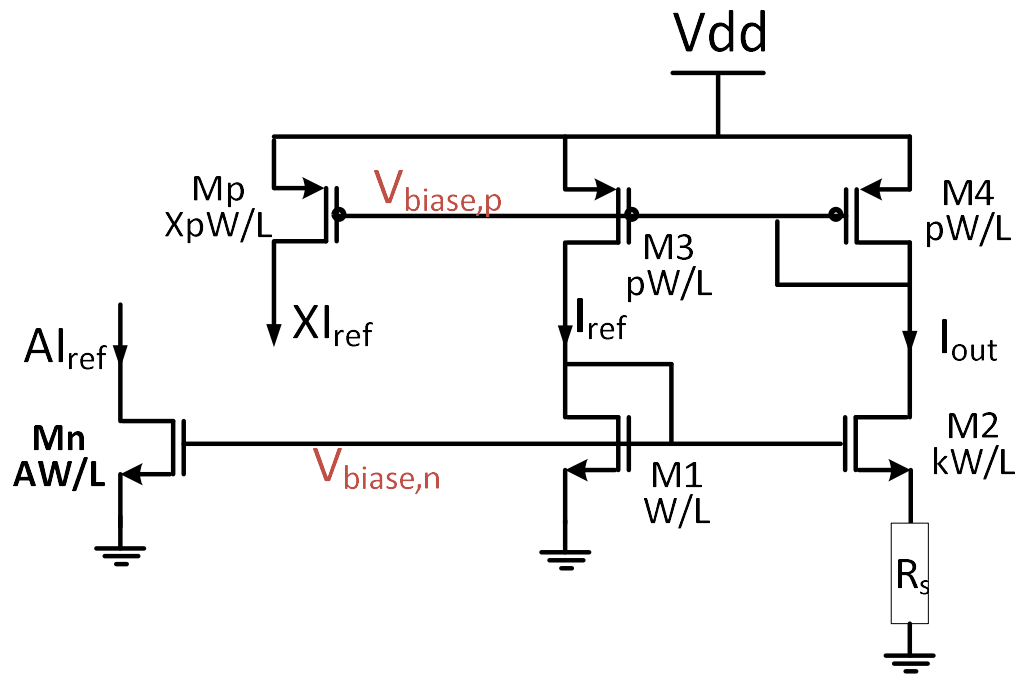
Ex: Temperature behavior of I_D in saturation

$$I_D = \frac{C_{ox} w/L}{2} \mu (V_{GS} - V_{T0})^2$$



- At low V_G , the changes in V_{T0} dominate and the drain current increases with increasing temperature.
- At higher V_G , the mobility dominates and the drain current decreases with increasing temperature.

Exercise: Beta-multiplier (sensitivity to power supply and temperature)



$$I_{\text{out}} = I_{\text{ref}} = \frac{2}{\beta_1 R_s^2} \left(1 - \frac{1}{\sqrt{k}} \right)^2$$

1. Give the relation between g_{m1} , g_{m2} and R_s if $k = 4$?
2. Analyze the variation of i_{out} with power supply v_{dd} ?
3. **Analyze the variation of I_{out} with the temperature and determine $I_{out}(80^\circ\text{C})$ if $I_{out}(27^\circ\text{C})=10\mu\text{A}$ and $TC_{R_s} = 2000 \text{ ppm}/^\circ\text{C}$.**

Temperature Analysis

Determine the temperature coefficient of I_{out} : $TC(I_{out}) = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T}$

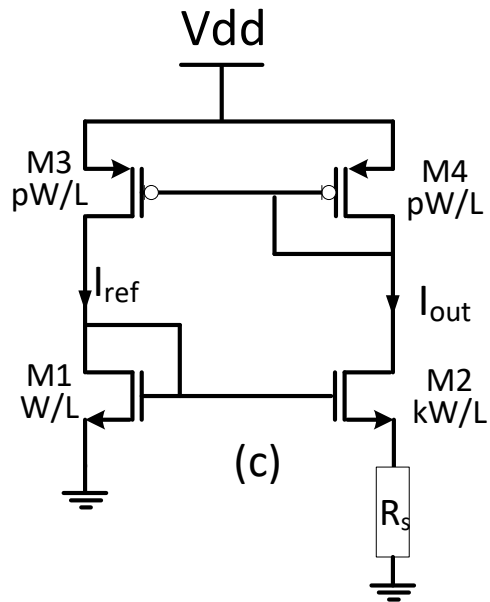
$$I_{out} = \frac{2}{R_s^2 k_p W/L} \left(1 - \frac{1}{\sqrt{k}}\right)^2 \quad \frac{\partial I_{out}}{\partial T} = \frac{\partial I_{out}}{\partial R_s} \frac{\partial R_s}{\partial T} + \frac{\partial I_{out}}{\partial k_p} \frac{\partial k_p}{\partial T}$$

$$\rightarrow TC(I_{out}) = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T} = -2 \frac{1}{R_s} \frac{\partial R_s}{\partial T} - \frac{1}{k_p} \frac{\partial k_p}{\partial T} = - \left(2TC(R_s) + TC(k_p) \right)$$

$$I_{out}(T) = I_{out}(T_0)(1 + TC(I_{out})(T - T_0))$$

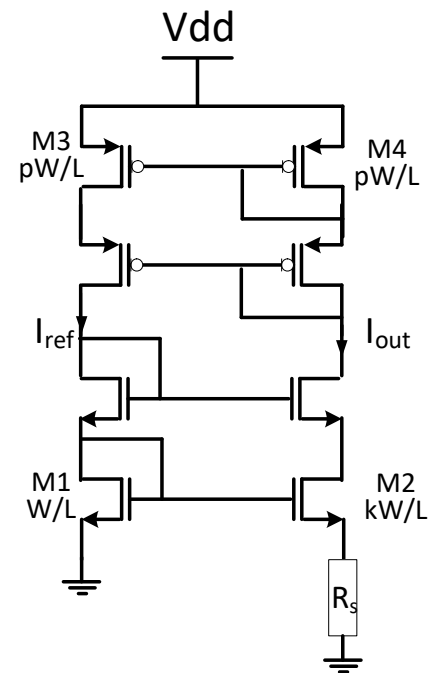
- $TC(k_p)$ (= $TC(\mu)$) is always negative **due to scattering**
 - $\mu(T) \approx \mu(T_0) \left(\frac{T_0}{T}\right)^{1.5} \rightarrow TC(\mu) = -\frac{1.5}{T}$ (T in °kelvin)
- TCR can be positive or negative
 - The silicon resistivity ($\rho = 1/q(n\mu_n + p\mu_p)$) depends on the mobility and carrier concentrations (n and p): n and p increase with T.
 - Ex: in UMC 0.18um, the TC of non-salicide N+ poly resistor is -160 ppm/°C while the TC of N-well resistor is 2000 ppm/°C
- Ex: $I_{out}(80^\circ) = I_{out}(27^\circ)(1 + TC(I_{out})(80 - 27))$ with $TC(I_{out}) = -(4 \cdot 10^{-3} - 1.5/300) = 10^{-3}$
 $I_{out}(80^\circ) = I_{out}(27^\circ) \cdot 1.053 = 10.53 \mu A$.

Supply independent Biasing: Temp. Analysis



$$I_{out} = I_{ref} = \frac{2}{\beta R_s^2} \left(1 - \frac{1}{\sqrt{k}} \right)^2$$

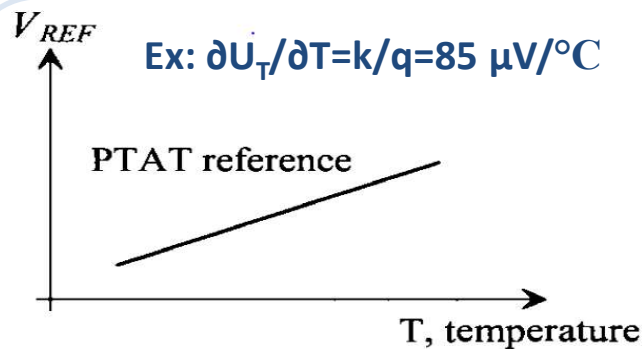
Small V_{dd} dependence



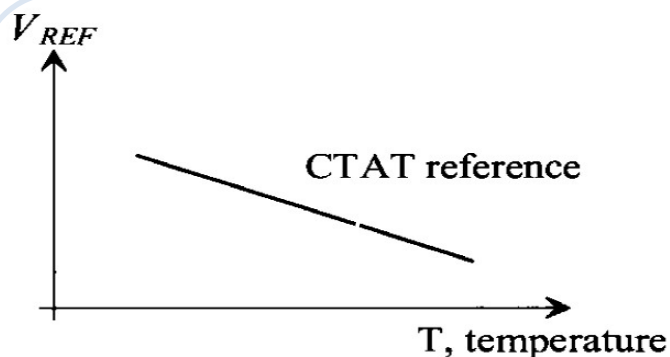
Cascode structure for an improved power supply rejection

Temperature-Independent References

- Ideal I_{ref} and V_{ref} are PVT-independent
- Need two quantities having opposite TempCo: i.e. PTAT and CTAT

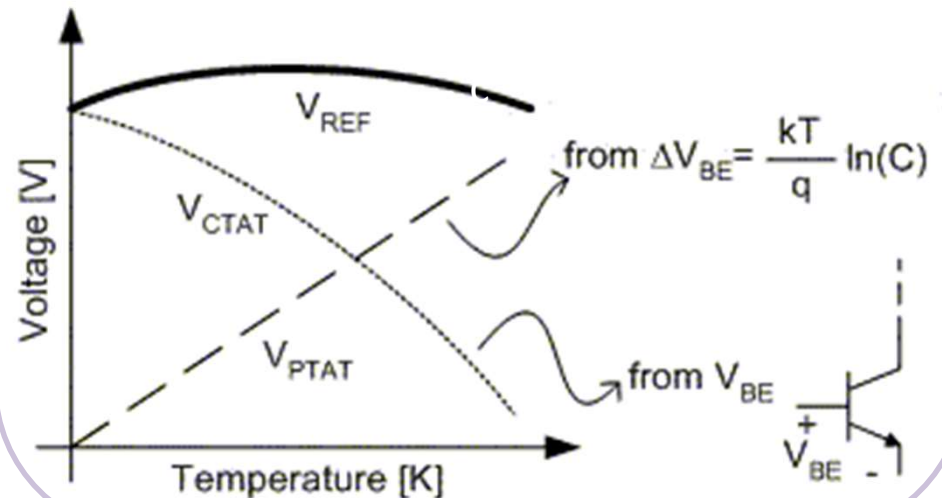


Proportional To Absolute Temperature



Complementary To Absolute Temperature

- T-independent reference (bandgap) are Generated by adding PTAT and CTAT references with proper weighting. (present in every chip)



CTAT Ex:

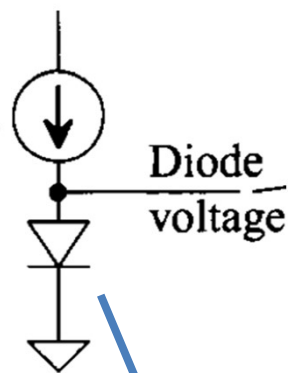
$$\partial V_{BE} / \partial T \approx \partial V_D / \partial T \approx -1.6 \text{ mV}/^\circ\text{C};$$

$$\partial V_{T0} / \partial T \approx -0.6 \text{ mV}/^\circ\text{C};$$

$$\partial k_p / \partial T \approx -k_p 1.5/T \text{ (T in } ^\circ\text{K)}$$

Negative-TC Ref(CTAT)

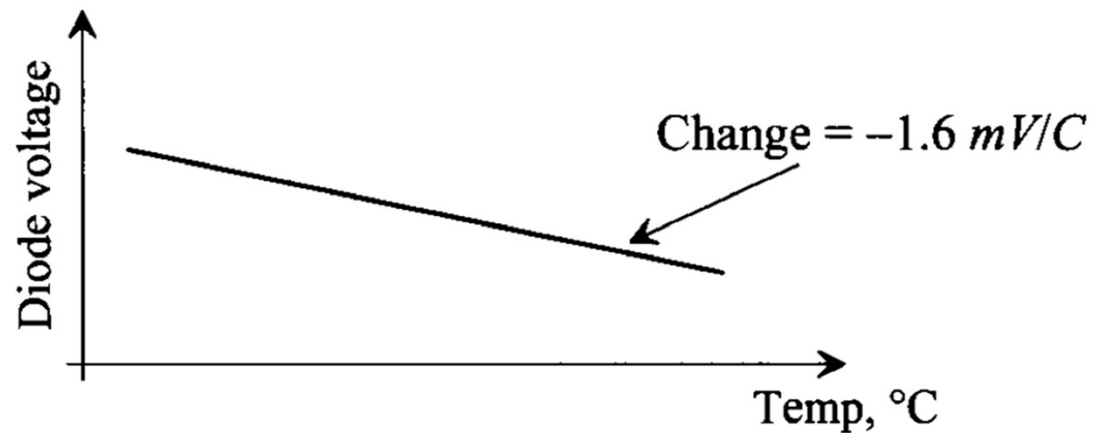
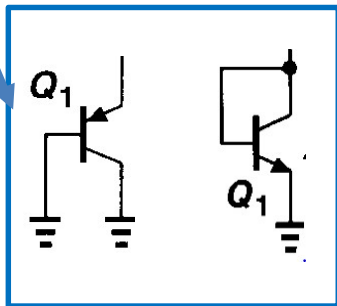
- Base-emitter Voltage of Bipolar (i.e. forward voltage of a diode) exhibits a negative TC (CTAT).



$$\partial V_D / \partial T \approx -1.6 \text{ mV} / ^\circ\text{C}$$

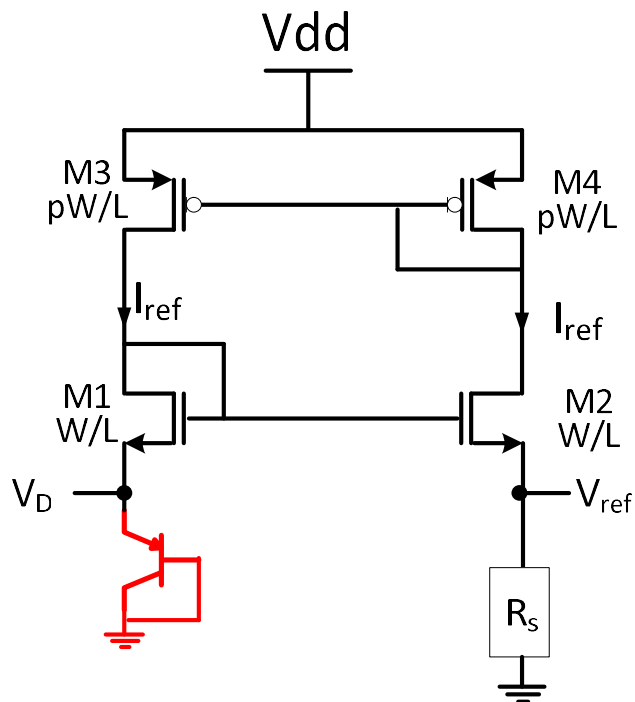
$$I_D = I_S \cdot \exp(V_D / U_T), \quad U_T = kT/q$$

$$V_D = U_T \cdot \ln(I_D / I_S)$$



Note: Bipolar transistors give the most reproducible and **easily tunable positive** and negative TC references and temp-independent references.

Conceptual generation of CTAT-Ref: Diode-referenced self-biasing circuit (CTAT)



- *pMOS mirror forces the same current through each branch.*
- *nMOS mirror forces the voltage across the resistor to be equal to V_D and thus:*
- *We can set the value of I_{ref} by choosing the right value of R_s*

$$I_{ref} = \frac{\overbrace{V_D}^{V_{ref}}}{R_s} = \frac{U_T \ln\left(\frac{I_{ref}}{I_s}\right)}{R_s} \rightarrow R_s = \frac{U_T}{I_{ref}} \ln\left(\frac{I_{ref}}{I_s}\right)$$

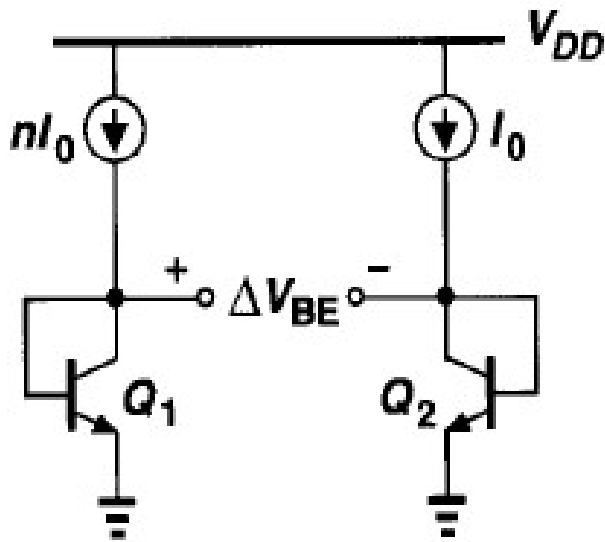
- *The temperature Coefficient of V_{ref} and I_{ref} are:*

$$TC(V_{ref}) = TC(V_D) \approx \frac{-1,6mV/^{\circ}C}{0,7V} \text{ CTAT}$$

$$TC(I_{ref}) = TC(V_D) - TC(R_s) \\ \rightarrow \text{CTAT if } R_s \text{ is PTAT}$$

Conceptual generation of Positive-TC Ref(PTAT)

- The difference between the base-emitter voltages of two BJTs operating at unequal currents is known as PTAT.



$$\begin{aligned}\Delta V_{BE} &= U_T \ln \left(\frac{nI_0}{I_s} \right) - U_T \ln \left(\frac{I_0}{I_s} \right) \\ &= U_T \ln(n) = \frac{kT}{q} \ln(n)\end{aligned}$$

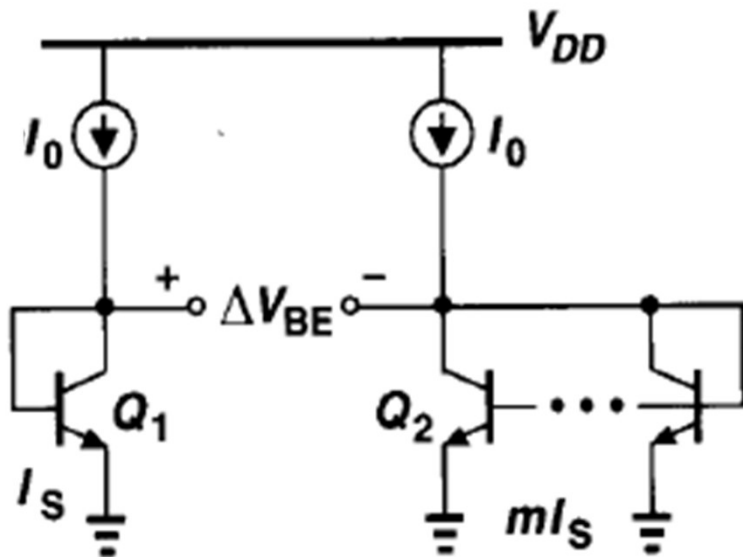
$$\frac{\partial \Delta V_{BE}}{\partial T} = \ln(n) \frac{\partial U_T}{\partial T}$$

$$= \ln(n) 85 \frac{\mu V}{^\circ C} \rightarrow \text{tunable PTAT}$$

- The weighting of ΔV_{BE} is tunable through n .

Conceptual generation of Positive-TC Ref (PTAT): version 2

- The difference between the base-emitter voltages of two BJTs with unequal sizes is also known as PTAT.

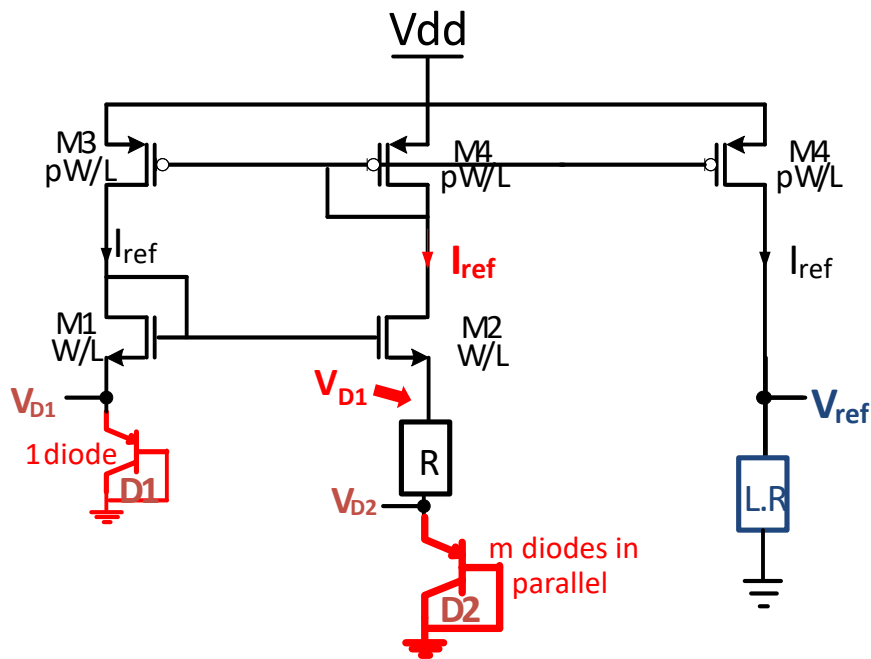


$$\begin{aligned}\Delta V_{BE} &= U_T \ln\left(\frac{I_0}{I_S}\right) - U_T \ln\left(\frac{I_0}{mI_S}\right) \\ &= U_T \ln(m) = \frac{kT}{q} \ln(m)\end{aligned}$$

$$\begin{aligned}\frac{\partial \Delta V_{BE}}{\partial T} &= \ln(m) \frac{\partial U_T}{\partial T} = \ln(m) 85 \frac{\mu V}{^\circ C} \\ &\rightarrow \text{tunable PTAT}\end{aligned}$$

- The weighting of ΔV_{BE} is tunable through m .
- ΔV_{BE} is a floating voltage 🤔?

Thermal Current and Voltage referenced self-biasing PTAT-Ref



- The difference between the base-emitter voltages of two BJTs can be achieved through a resistor:

$$\Delta V_D = \overbrace{V_{D1}}^{V_{S(M2)}} - V_{D2} = U_T \ln(m) = R I_{ref}$$

$$V_{ref} = L R I_{ref} = U_T L \ln(m)$$

$$\frac{\partial V_{ref}}{\partial T} = L \ln(m) \frac{\partial U_T}{\partial T} = L \ln(m) 85 \frac{\mu V}{^\circ C}$$

\rightarrow tunable PTAT

- The value of I_{ref} is set by choosing the right value of R as:

$$I_{ref} = \frac{V_{D1} - V_{D2}}{R} = \frac{U_T \ln(m)}{R} \rightarrow R = \frac{U_T \ln(m)}{I_{ref}}$$

Band Gap Reference Design

- The bandgap reference (BGR) is formed by adding a diode D_3 (i.e., CTAT) to a PTAT reference. The reference voltage is then the sum of tunable PTAT and CTAT voltages:

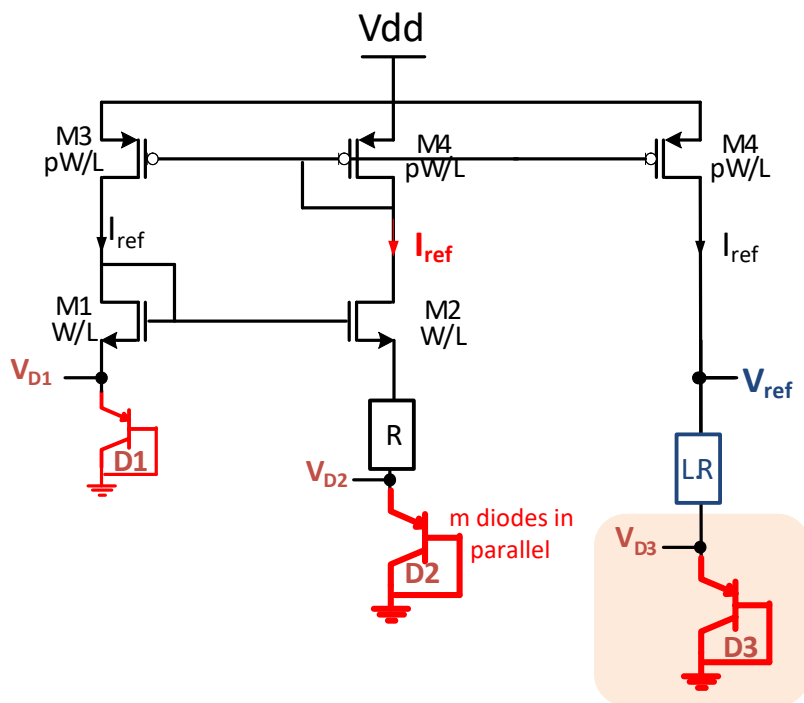
$$V_{ref} = LRI_{ref} + V_{D3} = U_T L \ln(m) + V_{D3}$$

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} &= L \ln(m) \frac{\partial U_T}{\partial T} + \frac{\partial V_{D3}}{\partial T} \\ &= L \ln(m) 85 \frac{\mu V}{^{\circ}C} - 1,6 \frac{mV}{^{\circ}C} \end{aligned}$$

- L is tuned to have $\frac{\partial V_{ref}}{\partial T} = 0$

$$L = \frac{1,6}{\ln(M) 85 \cdot 10^{-3}} \approx 9 \text{ for } M = 8$$

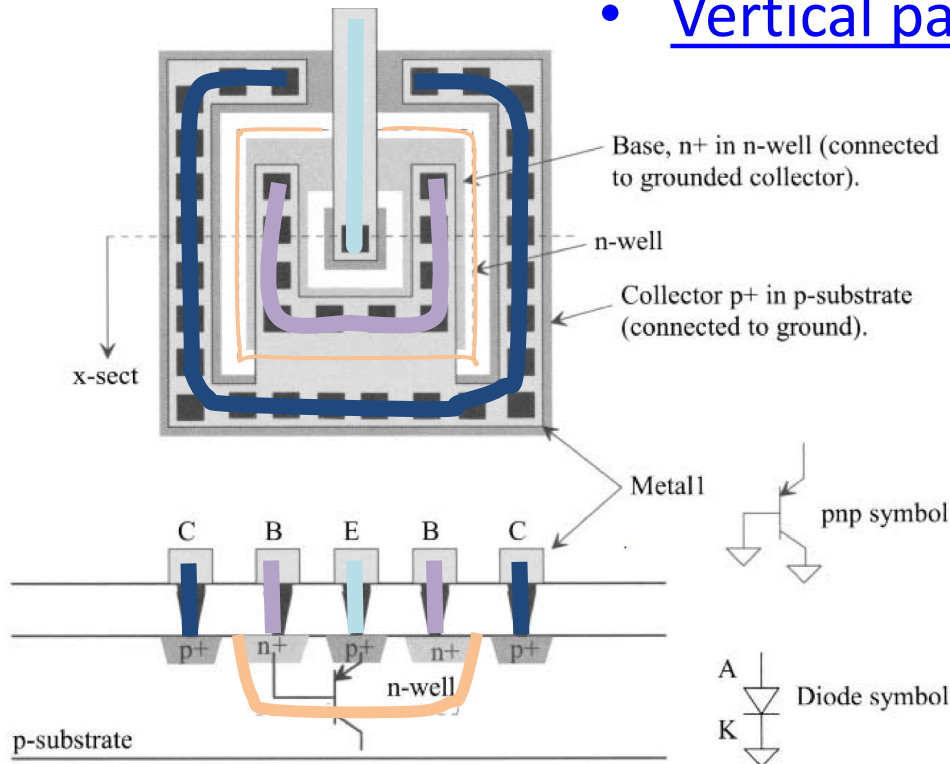
- Note that as for Beta Multiplier, the PTAT, CTAT and Bandgap circuits based on the self-biasing structure require start-up circuits.



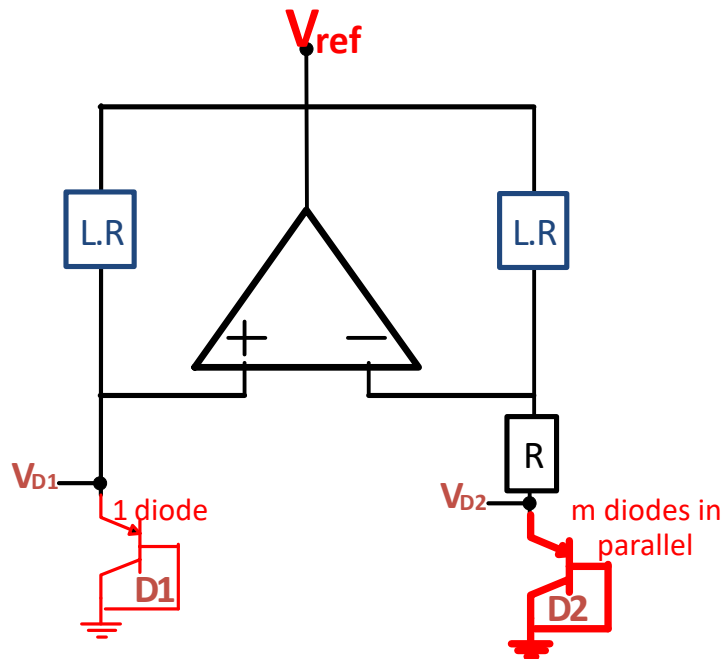
Bipolar implementation in CMOS process

- *Our derivation of a temperature-independent voltage relies on the exponential characteristics of Bipolar for both PTAT and CTAT.*
- *We must therefore seek structures in a standard CMOS technology that exhibit such characteristics.*

- Vertical parasitic pnp Bipolar



Alternative Bandgap for Low-Voltage ICs



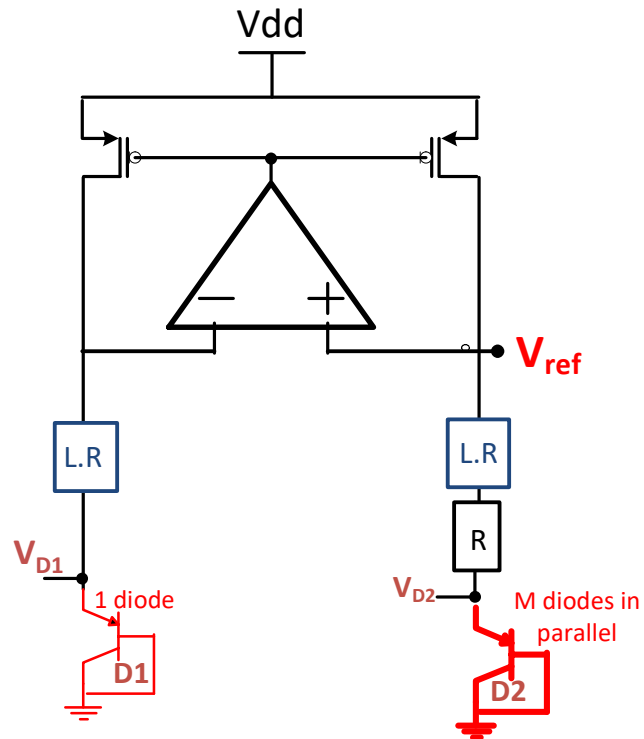
- Instead of using a PMOS mirror, we can use an amplifier to hold the voltage across the resistors (LR) constant and thus force the current through each branch of the reference to be the same.

$$V_{ref} = (L + 1)RI_{ref} + V_{D2}$$

$$= U_T(L + 1) \ln(m) + V_{D2}$$

- The benefit of this topology over the other topologies is that we can generate higher V_{ref} (closer to V_{DD}).
- While its drawback is that the amplifier must be capable of driving a resistive load (which requires a current amplifier at the output stage).

Alternative Bandgap for Low-Voltage ICs



- This alternative avoids the resistive load since the amplifier drives the oxide capacitances of the pMOS amplifier.*