SECTION OF ELECTRICAL ENGINEERING

EPFL STI – SEL
ELG
Station nº 11
CH-1015 Lausanne

Téléphone : +4121 693 13 46
Fax :
E-mail : alexandre.levisse@epfl.ch
Site web : https://sti.epfl.ch/fr/sel/

Fundamentals of VLSI – project Full Custom, session 1
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Full Custom Project
Session 2 : Verification of the functionality and Sizing

1. BASIC RULES OF ENGINEERING

- **Engineers are lazy**

If something takes too long, you are doing something wrong.

- **Divide and Conquer**

Divide complex problems into a collection of smaller simpler problems, solve one by one.

- **Simple and Regular**

Try simple and regular structures, they are easier to design and debug.

- **Engineering is not a religion**

Find the solution that best fits your problem

2. VERIFICATION OF THE FUNCTIONALITY

Use the previously design testbenches to verify the functionality of the 1bit logic, 1bit adder and 8bit ALU.

You could add an intermediate step in which you test the functionality of the 8bit logic in order to check the critical paths. This will also you do size it and identify the overhead of adding the MUX.

A good approach consists in always saying that everything that has not been tested does not work.

3. CHARACTERIZATION AND OPTIMIZATION OF THE CRITICAL PATH

3.1. LOGIC BLOCK 1BIT

Characterize the speed of the logic block and derive a sizing strategy.

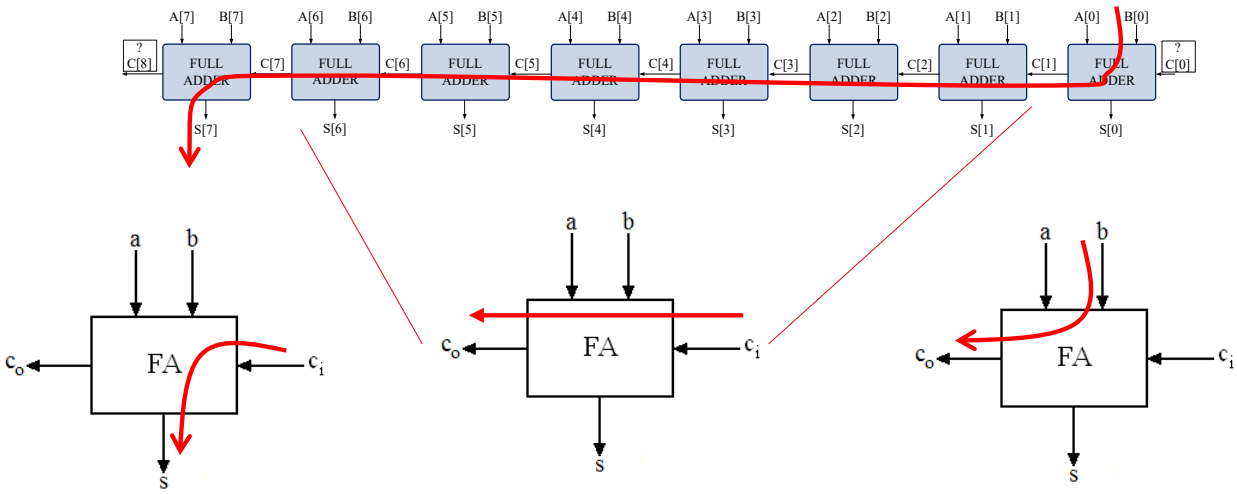
Ask yourself the following questions :

- Is this block in the critical path ?
- Do I need to balance the rising and falling edges ?
- What could be the best sizing ratio for the P and NMOS?
- What size do I need for the NMOS ?

3.2. ADDER 1BIT AND ADDER 8BIT

Characterize the speed of the 1bit adder block for all the possible critical paths.

From the following figure, derive an optimization/pruning strategy.



Hint 1 : you may want to have different cells for the last, middle, and last adders of the chain. i.e., prune the un-necessary parts of the adder.

Hint 2 : you may want to specifically size the transistors in the critical path of the 1bit adder. Based on hint 1, these could be different for FA[0], FA[1-6] and FA[7].

Hint 3 : if you are running out of time, or if you are lost, keep things simple. Most of the gains can be obtained from the Cin to Cout critical path. Focus on this one. You can optimize the first and last cells later if you have time.

Hint 4 : if you simulate the 8bit adder, do it with a realistic environment. Ask yourself the following question : what circuit will be connected to S[7:0] ?

A good sizing strategy can consist in starting from a minimum size (say W=120nm for the NMOS – take a sizing that enables a balanced rising/falling transition). And only upsize the transistors in the critical path. To identify the good size, you could for e.g. run a parametric analysis as you did in the tutorial. Or iteratively run simulations until you are satisfied with the timing you find.

3.3. MUX

The MUX makes the interface between the adder/logic and the output capacitance. You should have verified its functionality in the tutorials.

Think about your sizing strategy for that block. It has 3 stages. Each of its outputs is connected to a 10fF capacitance. You do not specifically need to size it now, but when simulating the entire 8bit ALU, remember that this can degrade your performances.

3.4. ALU 1BIT AND ALU 8BIT

You may want to check the functionality of the ALU 1bit, and then confirm the performance of your circuit using the ALU 8bit.

How to know when to stop optimizing ?

- In order to evaluate the performance of your circuit. Consider that the layout step will add between 30 and 50% (generally) of timing overhead on your design. It could be more if your layout is particularly bad.
- Target something between 400 and 600ps for the critical path of 8bit ALU. Remember that the slower you are pre-layout, the more you will need to be careful with the layout.
- Try not using transistors larger than W=600-700um (at least for the NMOS). Keep in mind that increasing the W also increases the load on the previous gate. Larger is not always better.