



Lab. On HW-SW Digital Systems Codesign EE-390(a)

Final Co-Design Project

Prof. David Atienza

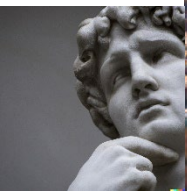
Dr. Denisa Constantinescu, Dr. Miguel Peón-Quirós

Mr. Rubén Rodríguez-Álvarez, Ms. Stasa Kostic, Mr. Karan Pathak

- Exercises and grading – Continuous evaluation format:
 - Weekly exercises (not graded)
 - Midterm exercise (individual evaluation): **30 % of the final grade**
 - Must be delivered at most ~~two~~ three weeks after the corresponding class
 - Delivered in GitLab and a report answering questions
 - The TAs will ask you questions to assess your understanding
 - Final guided projects (in groups of two students): **70 % of the final grade**
 - Delivered in GitLab and presented in class during the last session of the semester (May 22nd)
 - Last git commit at 12:00 (pm) on May 22nd
- Final hardware (HW) / software (SW) co-design project
 - Must cover the topics seen during the course:
 - Integration of both SW and HW
 - Optimization of HW with HLS (loops, internal arrays)
 - Management of memory coherence between processors and HW
 - Access to the peripherals with MMIO and kernel drivers (optional)
 - Broad topic proposed, multiple solutions are possible
 - The final presentation itself with questions is part of the evaluation (exam)
 - The solutions will be evaluated on their originality, efficiency (Pareto front), use of the course concepts

Reminder: Use of GIT and TCL scripts

- All exercises and projects will be delivered through a git repository
 - Git must be used for daily development, as a way to track your individual work
 - **Do not simply push your code at the end!**
- If submitting multiple solutions:
 - Tag the commits in the repository as “Solution <...>” **AND** notify us about the commit
 - We will evaluate the solutions and let you know as soon as possible if they work
- Upload to the repository only the project sources (use TCL scripts)
 - For the solutions, ALSO upload the bitstream files (.bit and .hwh) and the SW application, including driver sources if applicable
 - Otherwise, we cannot test your solutions



Questions?

Prof. David Atienza

EPFL — Embedded Systems Laboratory
david.atienza@epfl.ch
miguel.peon@epfl.ch