EE-365 - W11
CONTROL LOOPS
COMPENSATION NETWORK

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2-SWITCH FLYBACK CONVERTER

Practical updates and guidelines...

VOLTAGE-MODE VS. CURRENT-MODE CONTROL.

- Both Voltage-mode and Current-mode control are used for Switched Mode Power Supplies
- Actual choice will depend on topology and applications
- Yet, Current-mode is extremely popular and extensively used

Voltage-mode control

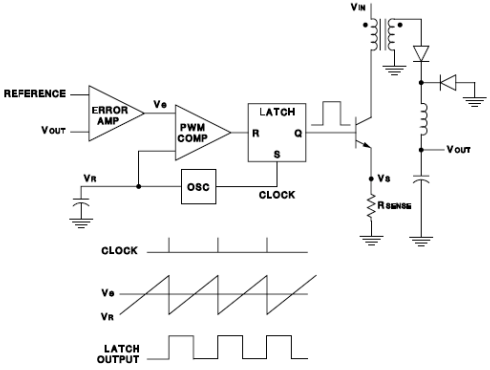

Figure 1 Voltage mode control principles

Current-mode control

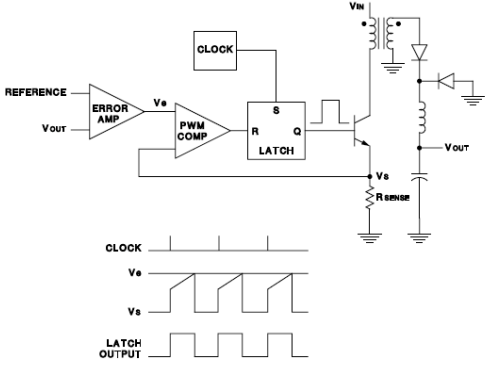

Figure 2 Current mode control principles

Source: UNITRODE Design Note DN-62: "Switching Power Supply Topology Voltage Mode vs. Current Mode"

VOLTAGE-MODE CONTROL

Voltage-mode control characteristics

- Single voltage feedback
- PWM generated by comparing voltage error with constant ramp waveform
- Current limiting must be done separately

Advantages

- A single feedback loop is easier to design and analyze
- A large-amplitude ramp waveform provides good noise margin for a stable modulation
- A low-impedance power output provides better cross-regulation for multiple output supplies process.

Disadvantages

- Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response.
- The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation.
- Compensation is further complicated by the fact that the loop gain varies with input voltage.

Voltage-mode control

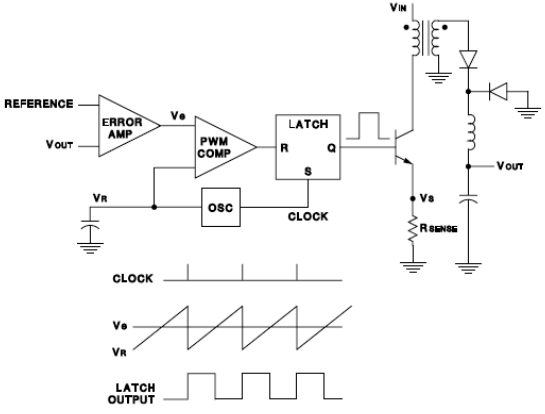

Figure 3 Voltage mode control principles

CURRENT-MODE CONTROL.

Current-mode control characteristics

- Current measurement is part of the feedback loop
- Control uses the oscillator only as a fixed-frequency clock
- Ramp waveform is replaced with a signal derived from output inductor current

Advantages

- Since inductor current rises with a slope determined by $V_{in} - V_o$, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
- Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop (at least in the normal region of interest). This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.
- Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the Error Amplifier, and the ease of providing load sharing when multiple power units are paralleled.

- **Current-mode control**

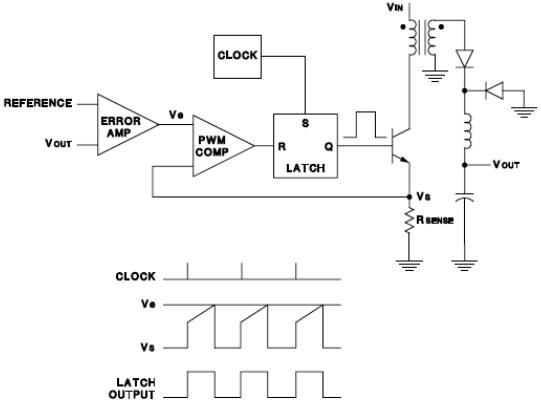

Figure 4 Current mode control principles

CURRENT-MODE CONTROL..

Current-mode control characteristics

- Current measurement is part of the feedback loop
- Control uses the oscillator only as a fixed-frequency clock
- Ramp waveform is replaced with a signal derived from output inductor current

Disadvantages

- There are now two feedback loops, making circuit analysis more difficult.
- The control loop becomes unstable at duty cycles above 50% unless **slope compensation** is added.
- Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop.
- A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
- With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross-regulation with multiple outputs.

Current-mode control

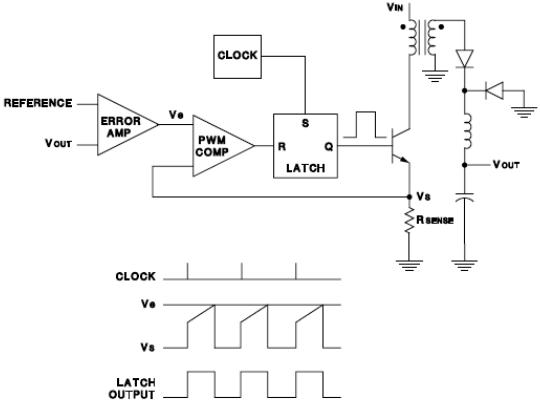

Figure 5 Current mode control principles

VOLTAGE-MODE VS. CURRENT-MODE CONTROL..

- Both Voltage-mode and Current-mode control are used for Switched Mode Power Supplies
- Actual choice will depend on topology and applications
- Yet, Current-mode is extremely popular and extensively used

Voltage-mode control (when to use)

- There are wide input line and/or output load variations possible.
- Particularly with low line - light load conditions where the current ramp slope is too shallow for stable PWM operation.
- High power and/or noisy applications where noise on the current waveform would be difficult to control.
- Multiple output voltages are needed with relatively good cross-regulation.
- Saturable reactor controllers are to be used as auxiliary secondary-side regulators.
- Applications where the complexities of dual feedback loops and/or slope compensation is to be avoided.

Current-mode control (when to use)

- The power supply output is to be a current source or very high output voltage.
- The fastest dynamic response is needed with a given switching frequency.
- The application is for a DC/DC converter where the input voltage variation is relatively constrained.
- Modular applications where parallel operation with load sharing is required.
- In push-pull circuits where transformer flux balancing is important.
- In low-cost applications requiring the absolute fewest components.

Source: UNITRODE Design Note DN-62: "Switching Power Supply Topology Voltage Mode vs. Current Mode"

SLOPE COMPENSATION.

Slope compensation can mitigate several shortcomings of current-mode control

- Open loop instability above 50% duty cycle (D).
- Less than ideal loop response caused by peak instead of average inductor current sensing.
- Tendency towards subharmonic oscillation.
- Noise sensitivity, particularly when inductor ripple current is small.

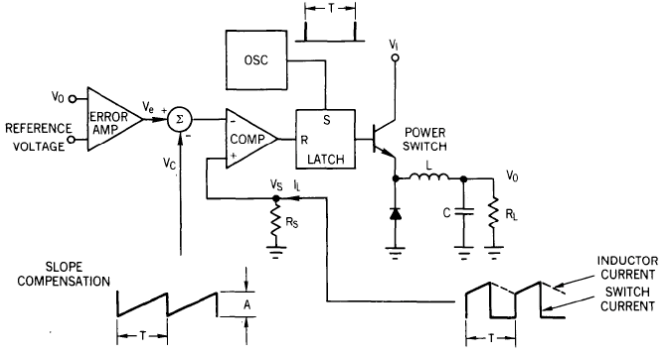

Figure 6 A Current mode controlled Buck regulator with slope compensation

Source: UNITRODE Application Note U-97: "Modelling, analysis and compensation of the current-mode converter"

SLOPE COMPENSATION..

Relevant variables:

- I_L - inductor current waveform
- V_e - error voltage at output of voltage error amplifier
- m_1, m_2 - ascending and descending inductor current slopes, respectively
- ΔI - inductor current perturbation (e.g. measurement error)

A) Operation with $D < 0.5$

- Initial pertubation will decrease with time (cycle by cycle) - stable mode
- $\Delta I_0 > \Delta I_1 > \Delta I_2 > \ldots$ - OK

B) Operation with $D > 0.5$

- Initial pertubation will increase with time (cycle by cycle) - unstable mode
- $\Delta I_0 < \Delta I_1 < \Delta I_2 < \ldots$ - Not OK

C) Slope compensation

- Adding linear slope $-m$ counteracts the problem
- Compensating slope can be added to current waveform or
- Compensating slope can be subtracted from the error voltage

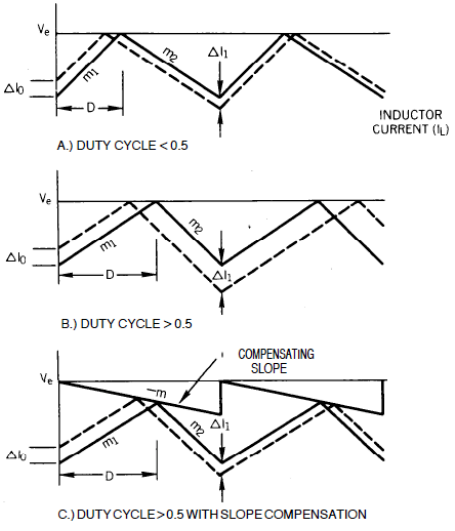

Figure 7 Open loop instability in a converter with current mode control

SLOPE COMPENSATION...

Slope compensation

- Adding linear slope $-m$ counteracts the problem
- Compensating slope can be added to current waveform or
- Compensating slope can be subtracted from the error voltage

Without slope compensation:

$$\Delta I_1 = -\Delta I_0 \frac{m_2}{m_1}$$

After addition of linear slope $-m$

$$\Delta I_1 = -\Delta I_0 \frac{m_2 + m}{m_1 + m}$$

Normally, slope compensation (Buck converter) needs to satisfy:

$$m > -\frac{1}{2} m_2$$

For the Buck converter:

- up-slope: $m_1 = \frac{V_{in} - V_{out}}{L} R_s$
- down-slope: $m_2 = \frac{V_{out}}{L} R_s$
- R_s - models the total current sense gain (Shunt + INA200)

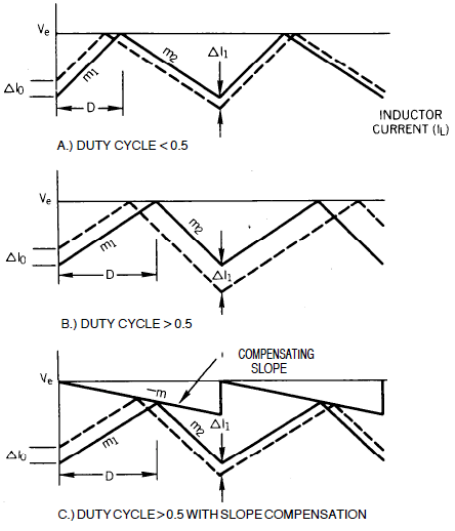

Figure 8 Open loop instability in a converter with current mode control

COMPENSATION NETWORK

Closed loop system design

PWM IC - UCC28C44

The closed-loop feedback control of the output voltage is here achieved with a **Type II compensation network**, built upon:

- a TL431 shunt amplifier, with the aim to measure and process the output voltage
- a Vishay VO617A-3X016 optocoupler, with the aim to provide the desired insulation between the primary and secondary side circuits of the Flyback converter
- the pins FB and COMP of the UCC28C44 integrated circuit, with the aim to compute the control action

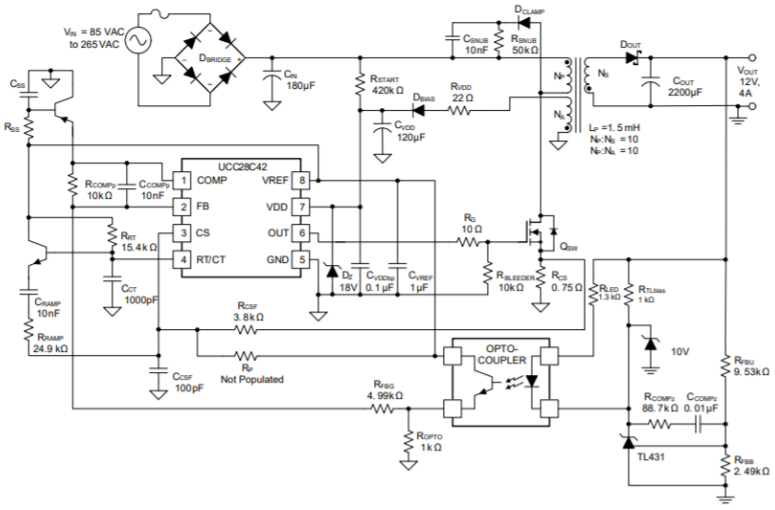

Figure 9 Flyback Scheme from the UCC28C44 Application Note.

Source: Refer to the circuit scheme shown in *UCCx8C4x BiCMOS Low-Power Current-Mode PWM Controller.pdf* (Figure 31 of the application note)

For the design of the **feedback compensation network**, the Flyback converter can be modeled as a controllable dynamic system.

- The voltage V_{COMP} (applied between the COMP and GND pins of the UCC28C44 IC) is the control input signal.
- The Flyback voltage U_{out} is the output signal of the dynamic system.
- This equivalent dynamic model intrinsically considers both the converter power operation and the Peak-Current Mode Control of the UCC28C44.
- All the other operating conditions (e.g., output power, input voltage) are treated as internal parameters of the dynamical system.

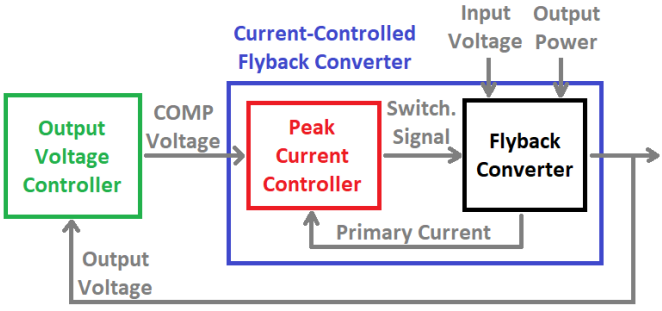

Figure 10 Simplified block diagram of the controlled Flyback converter.

Since the system is inherently non-linear, the design process has to consider:

- **a large-signal analysis**, to identify the desired steady-state equilibrium point and verify that it is compatible with the operating ranges of the circuit components, and
- **a small-signal analysis**, to guarantee that the controlled system is stable and robust around the desired operating point.

Both aspects are dependent on the operating conditions (e.g., input voltage, output power), and influence one another.

CONTROL-TO-OUTPUT CHARACTERISTICS

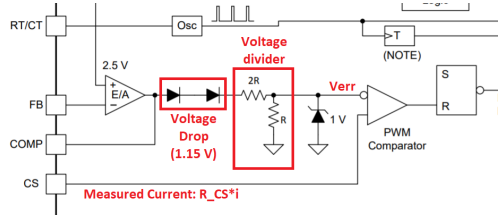

Figure 11 Internal scheme of the comparator of the UCC28C44.

- The voltage at the COMP pin is first subject to a 1.15 V drop
- ...and then to a R/2R voltage divider (with a gain $A_{CS} = 3$)
- By considering V_{err} the voltage at the input of the comparator, we have:

$$V_{COMP} = A_{CS} \cdot V_{err} + 1.15\,\text{V}$$

In the steady-state conditions:

- the voltage V_{err} is equal to the peak voltage at the CS pin, which is the sum of the measured peak primary current $R_{CS} \cdot i_{peak}$.
- Therefore:

$$V_{err} = R_{CS} \cdot i_{peak}$$

- where, as already computed in R1, the duty-cycle is:

$$D = \frac{U_{out}}{U_{out} + (N_S/N_P) \cdot U_{in}}$$

- and the peak primary current is:

$$i_{peak} = \frac{P_{out}}{U_{in} \cdot D} + \frac{U_{in} \cdot D}{2 \cdot L_m \cdot f_{sw}}$$

- It is sufficient to evaluate these expressions in multiple operating conditions of the converter to compute the ideal value of the voltage V_{COMP}.

CONTROL-TO-OUTPUT TRANSFER FUNCTION.

For a given steady-state operating point, the small-signal control-to-output transfer function can be identified in a way to link small perturbations of V_{COMP} to small perturbations of U_{OUT}. The small-signal control-to-output transfer function is:

$$\tilde{H}(s) = G_0 \cdot \frac{\left(1 + \frac{s}{\omega_{ESR,z}}\right) \cdot \left(1 - \frac{s}{\omega_{RHP,z}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \cdot \left(1 + \frac{s}{Q_P \cdot \omega_{P2}} + \frac{s^2}{\omega_{P2}^2}\right)}$$

With the help of the application note *UCCx8C4x BiCMOS Low-Power Current-Mode PWM Controller.pdf* (Section 9.2.2.10) compute, for the converter nominal operating point, the following quantities:

- the static gain G_0;
- the frequency $f_{P1} = \omega_{P1}/2\pi$ of the dominant pole;
- the frequency $f_{P2} = \omega_{P2}/2\pi$ of the switching-related pole;
- the frequency $f_{ESR,z} = \omega_{ESR,z}/2\pi$ of the output capacitor related zero;
- the frequency $f_{RHP,z} = \omega_{RHP,z}/2\pi$ of the right half-plane zero;
- the quality coefficient Q_P of the slope-compensation.

CONTROL-TO-OUTPUT TRANSFER FUNCTION..

All these expressions can be found from the UCC28C44 application note.

- The expression of the static gain is:

$$G_0 = \frac{R_{load}}{A_{CS} \cdot R_{CS} \cdot (N_S/N_P)} \cdot \frac{1}{(D_{off}^2/(2 \cdot \tau_L)) \cdot (1 + 2 \cdot S_e/S_n) + 2 \cdot M + 1}$$

- with the following parameters:
  $R_{load} = U_{out}^2/P_{out}$,
  $D_{off} = 1 - D$,
  $M = U_{out}/[(N_P/N_S) \cdot U_{in}]$, and
  $\tau_L = [L_m \cdot (N_S/N_P)^2]/[R_{load} \cdot T_{sw}]$.
- The frequency f_{P1} of the dominant pole is depending on the operazing conditions of the converter:

$$f_{P1} = \frac{1}{2\pi} \cdot \frac{(\frac{D_{off}^3}{2 \cdot \tau_L}) \cdot (1 + 2 \cdot \frac{S_e}{S_n}) + 1 + D}{R_{load} \cdot C_{out}}$$

- The frequency f_{P2} of the switching-related pole is half of the switching frequency:

$$f_{P2} = \frac{f_{sw}}{2}$$

- The frequency $f_{ESR,z}$ of the output capacitor related zero is:

$$f_{ESR,z} = \frac{1}{2\pi} \cdot \frac{1}{ESR \cdot C_{out}}$$

- The frequency $f_{RHP,z}$ of the right half-plane zero is also depending on the operating conditions of the converter:

$$f_{RHP,z} = \frac{1}{2\pi} \cdot \frac{D_{off}^2 \cdot R_{load}}{D \cdot L_m \cdot (N_S/N_P)^2}$$

- The quality factor Q_p of the slope compensation (already computed before) is:

$$Q_p = \frac{1}{\pi \cdot [M_c \cdot (1 - D) - 1/2]}$$

- with $M_c = S_e/S_n + 1$.

Please note that previous expressions were derived considering slope compensation. Without it being used: $S_e = 0$

CONTROL-TO-OUTPUT TRANSFER FUNCTION...

We have provided Matlab files resulting in Bode Diagrams and many useful information for different operating points.

```
CONTROL TO OUTPUT TRANSFER FUNCTION EVALUATION
-----------------------------------------------------------------
Input Voltage:  V_in = 50 V
Output Voltage: V_out = 24 V
Output Power:   P_out = 50 W
Duty Cycle:     D = 32.4324 %
Required Voltage at the COMP pin: V_COMP = 2.1966 V
-----------------------------------------------------------------
Small Signal DC Gain: G_0 = 18.3602
-----------------------------------------------------------------
Left Half-Plane Zero Frequency:  f_Z1 = 23843437.1673 Hz
Right Half-Plane Zero Frequency: f_Z2 = 64522.2742 Hz
-----------------------------------------------------------------
First-Order Pole Frequency:  f_P1 = 4387.3293 Hz
Second-Order Pole Frequency: f_P2 = 250000 Hz
-----------------------------------------------------------------
Second-Order Pole Quality Factor: Q_p = 1.8119
-----------------------------------------------------------------
```

Figure 12 Console results obtained in Matlab (Program 1) - Example

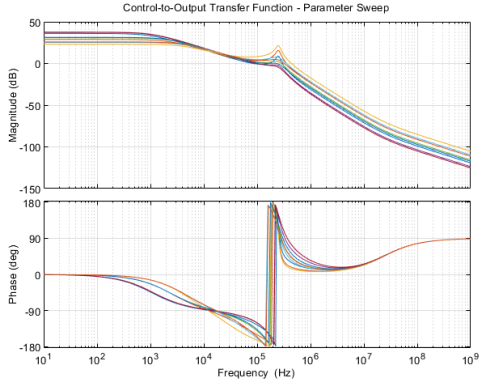

Figure 13 Bode Diagram obtained in MATLAB (Program 1) - Example

TYPE 2 COMPENSATION

Zero-Pole pair with or without extra elements

TYPE 2 COMPENSATOR

To control the converter, a Type II compensation network is used. The transfer function of an ideal Type II compensation network is:

$$\tilde{C}_{Type2}(s) = K_P \cdot \frac{1}{s\,\tau_z} \cdot \frac{1 + s\,\tau_z}{1 + s\,\tau_p}$$

- This transfer function must be designed to achieve a desired bandwidth frequency f_{BW} and to guarantee the controller robustness.
- The integral action guarantees a zero steady-state error, while a zero and a pole can be placed at the frequencies $f_z = 1/2\pi\tau_z$ and $f_p = 1/2\pi\tau_p$ to compensate for the dynamical behavior of $\tilde{H}(s)$.
- In general, the higher the bandwidth, the faster is the system to respond to input changes and to react to disturbances. However, too high bandwidth may weaken the closed loop control robustness and lead to instability.
- Considering the Control-to-Output transfer function $\tilde{H}(s)$, select:
  - the desired bandwidth frequency f_{BW};
  - the frequency f_z of the transfer function zero;
  - the frequency f_p of the transfer function pole;
  - the controller gain K_P to achieve the desired bandwidth.
- The Type II controller is a Proportional-Integral with an additional high-frequency pole. The design is given in the hint.
- The bandwidth f_{BW} should be chosen to be low enough with respect to the frequency $f_{RHP,z}$ of the right-half plane zero of the control-to-output transfer function. Generally speaking, lower values can improve the stability of the system, but may weaken the dynamic performances during transients. A safe choice is to set f_{BW} to be from 10 to 20 times lower than $f_{RHP,z}$.
- The frequency f_z of the transfer function zero should be low enough with respect to the bandwidth frequency f_{BW}. A good choice is to set f_z to be from 5 to 15 times lower than f_{BW}.
- The frequency f_p of the transfer function pole should be high enough with respect to the bandwidth frequency f_{BW}, and it should be close to the lowest frequency between $f_{RHP,z}$ and $f_{ESR,z}$.

TYPE 2 COMPENSATOR IMPLEMENTATION

We need to derive small-signal transfer function of the Type II compensation network
The overall control circuit:

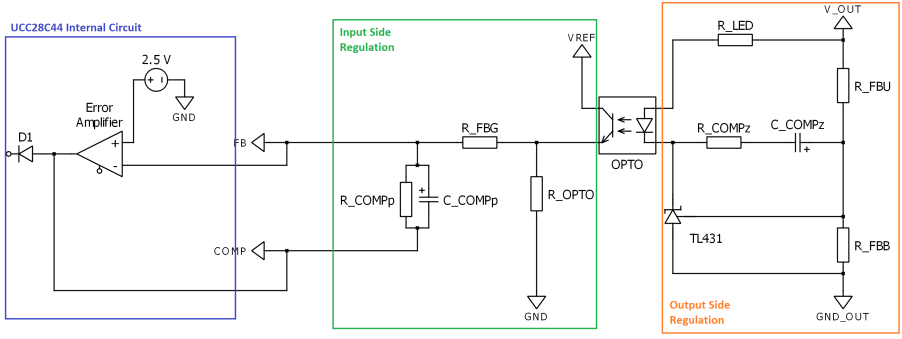

Figure 14 Scheme of the Compensation Network.

In the sense of small-signal modeling:

- we want to observe how small perturbations of U_{out} generate small perturbations of the V_{COMP} signal.
- it is possible to neglect all the other constant sources (e.g. internal voltage reference, etc), and simplify the diagram (next slide).
- The TL431 behaviour can be modeled as a simple operational amplifier
- The optocoupler behaviour can be modeled as a controlled current source, and the voltage drop on the LED can be neglected.

TYPE 2 COMPENSATOR - DERIVING THE MODEL

The equivalent small-signal simplified model is represented below.

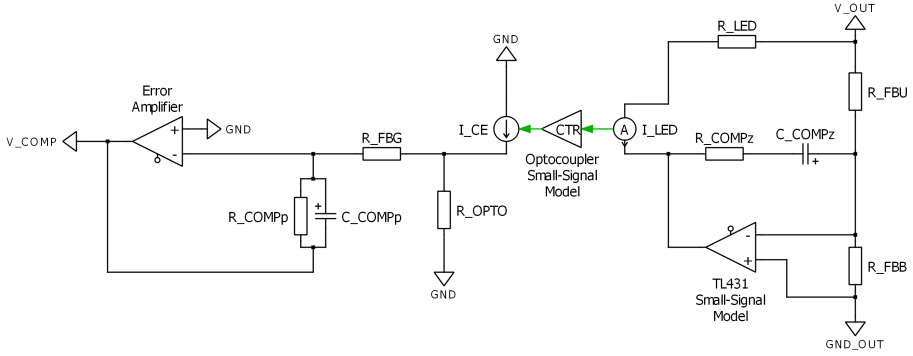

Figure 15 Simplified Small-Signal scheme of the Compensation Network.

We still have three parts to analyse:

- Internal PWM IC part
- Input side regulation
- Output side regulation

OP AMP - SHORT NOTE

Considering a generic Operational Amplifier in an Inverting configuration, it is possible to use description referring to just two impedances in the Laplace domain:

- the "Parallel" impedance Z_p, connected between the output and the inverting input,
- the "Series" impedance Z_s, connected between the input voltage source and the inverting input.
- In this case, it is easy to demonstrate that the output voltage, with respect to the ground, is:

$$V_{out} = -V_{in} \cdot \frac{Z_p}{Z_s}$$

- This approach can be applied to the different schemes of the simplified small-signal circuit by replacing the source V_{in} and R_s with the equivalent Thevenin circuit.

Recall some basics on OP-AMPS

- No current flows into the OP-AMP input terminals
- The differential input voltage is zero as V+ = V- = 0 (virtual ground)

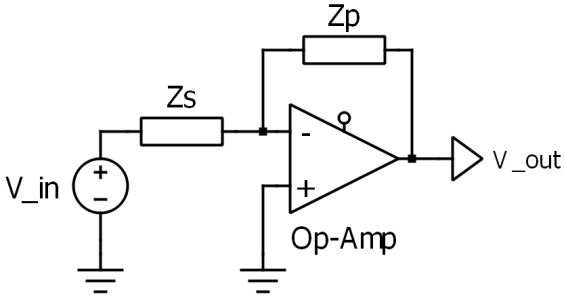

Figure 16 Op-Amp in Inverting configuration.

INPUT SIDE REGULATION CIRCUIT.

Input-side regulation block

- the OP-AMP is the internal Error Amplifier of the UCC28C44 circuit
- the output voltage is V_{COMP},
- the impedance Z_p is the parallel impedance given by R_{COMPp} and C_{COMPp}:

$$Z_p = \frac{R_{COMPp} \cdot \frac{1}{s\,C_{COMPp}}}{R_{COMPp} + \frac{1}{s\,C_{COMPp}}} = \frac{R_{COMPp}}{1 + s\,R_{COMPp}\,C_{COMPp}}$$

- the impedance Z_s is the equivalent impedance seen from the FB pin (i.e., the inverting input of the error amplifier) when no current I_{CE} circulates in the Optocoupler output:

$$Z_s = R_{FBG} + R_{OPTO}$$

- the input source V_{in} is the open-circuit voltage seen from the FB pin (i.e., the inverting input of the error amplifier) when only I_{CE} is active:

$$V_{in} = I_{CE} \cdot R_{OPTO}$$

- By combining this formulas, we have:

$$V_{COMP} = -I_{CE} \cdot \frac{R_{OPTO}}{R_{FBG} + R_{OPTO}} \cdot R_{COMPp} \cdot \frac{1}{1 + s\,R_{COMPp}\,C_{COMPp}}$$

INPUT SIDE REGULATION CIRCUIT..

Previous derivations are graphically illustrated in the following figure.

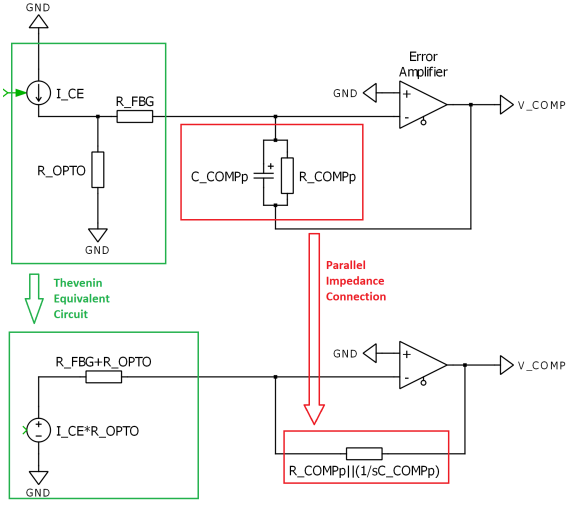

Figure 17 Equivalent model of the Input-Side regulation circuit.

OUTPUT SIDE REGULATION CIRCUIT.

Output-side regulation block

The same procedure can be done to find the AK voltage of the TL431. In this case:

- the OP-AMP is the TL431 model,
- the output voltage is the TL431 AK voltage,
- the impedance Z_p is the series impedance given by R_{COMPz} and C_{COMPz}:

$$Z_p = R_{COMPz} + \frac{1}{s\,C_{COMPz}} = \frac{1 + s\,R_{COMPz}\,C_{COMPz}}{s\,C_{COMPz}}$$

- the impedance Z_s is the equivalent impedance seen from the TL431 REF pin (i.e., the inverting input of the OP-AMP) when U_{out} is grounded:

$$Z_s = \frac{R_{FBU} \cdot R_{FBB}}{R_{FBU} + R_{FBB}}$$

- the input source V_{in} is the open-circuit voltage seen from the TL431 REF pin (i.e., the inverting input of the OP-AMP) when only U_{out} is active:

$$V_{in} = U_{out} \cdot \frac{R_{FBB}}{R_{FBU} + R_{FBB}}$$

- By combining these formulas, it results:

$$V_{AK,TL431} = -U_{out} \cdot \frac{R_{FBB}}{R_{FBU} + R_{FBB}} \cdot \frac{1 + s\,R_{COMPz}\,C_{COMPz}}{s\,C_{COMPz}} \cdot \frac{R_{FBU} + R_{FBB}}{R_{FBU} \cdot R_{FBB}} = -U_{out} \cdot \frac{1 + s\,C_{COMPz}\,R_{COMPz}}{s\,C_{COMPz}\,R_{FBU}}$$

OUTPUT SIDE REGULATION CIRCUIT..

Previous derivations are graphically illustrated in the following figure.

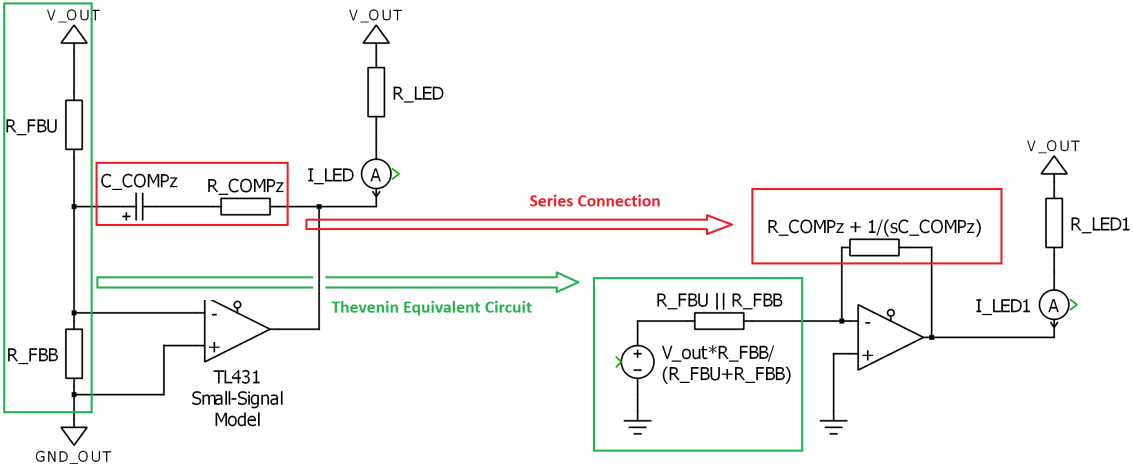

Figure 18 Equivalent model of the Output-Side regulation circuit.

TYPE 2 COMPENSATOR - DERIVING THE MODEL..

- the LED current, which is the input of the optocoupler, can be found as:

$$I_{LED} = \frac{U_{out} - V_{AK,TL431}}{R_{LED}} = U_{out} \cdot \frac{1}{R_{LED}} \cdot \left(1 + \frac{1 + s\,C_{COMPz}\,R_{COMPz}}{s\,C_{COMPz}\,R_{FBU}}\right) =$$

$$= U_{out} \cdot \frac{1}{R_{LED}} \cdot \frac{1 + s\,C_{COMPz}\,R_{COMPz} + s\,C_{COMPz}\,R_{FBU}}{s\,C_{COMPz}\,R_{FBU}} =$$

$$= U_{out} \cdot \frac{1}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \cdot \frac{1 + s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})}{s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})}$$

- Finally, by linking the optocoupler input and output current through the simple formula: $I_{CE} = CTR \cdot I_{LED}$, the relationship between small perturbations of U_{out} and small perturbations of V_{COMP} is:

$$V_{COMP} = -U_{out} \cdot CTR \cdot \frac{R_{COMPp}}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \cdot \frac{R_{OPTO}}{R_{OPTO} + R_{FBG}} \cdot$$

$$\cdot \frac{1 + s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})}{s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})} \cdot \frac{1}{1 + s\,C_{COMPp}\,R_{COMPp}}$$

- which is the provided expression of the transfer function $\tilde{C}_{FB}(s)$ in R2.
- Note that the minus sign is intrinsically stabilizing for the system, because it is just as if V_{COMP} is obtained by multiplying $\tilde{C}_{FB}(s)$ with the error $(0 - U_{out})$ (and 0 is a "reference perturbation signal").

TYPE 2 COMPENSATOR - DERIVING THE MODEL...

- The small-signal transfer function of the implemented Type II compensation network is:

$$\tilde{C}_{FB}(s) = \frac{V_{COMP}}{-U_{out}} CTR \cdot \frac{R_{COMPp}}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \cdot \frac{R_{OPTO}}{R_{OPTO} + R_{FBG}} \cdot$$

$$\cdot \frac{1 + s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})}{s\,C_{COMPz}\,(R_{COMPz} + R_{FBU})} \cdot \frac{1}{1 + s\,C_{COMPp}\,R_{COMPp}}$$

- These parameters must be chosen in a way to match the ideal Type II transfer function $\tilde{C}_{TypeII}(s)$.
- By comparing $\tilde{C}_{FB}(s)$ and $\tilde{C}_{TypeII}(s)$, identify the expressions of
  - the gain K_P;
  - the frequency of the transfer function zero f_z;
  - the frequency of the transfer function pole f_p.
- The actual question is quite simple. It only requires to compare the expression of the ideal Type II transfer function with the expression of the implemented one (which is already provided):

$$K_P = CTR \cdot \frac{R_{COMPp}}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \cdot \frac{R_{OPTO}}{R_{OPTO} + R_{FBG}}$$

$$f_z = \frac{1}{2\pi} \cdot \frac{1}{C_{COMPz}\,(R_{COMPz} + R_{FBU})}$$

$$f_p = \frac{1}{2\pi} \cdot \frac{1}{C_{COMPp}\,R_{COMPp}}$$

REFERENCE OUTPUT VOLTAGE

- The REF voltage is given by a simple voltage divider between R_{FBU} and R_{FBB}.
- The aim is to get the REF voltage as close as possible to the TL431 internal voltage, which is around 2.495 V (and can be approximated as 2.5 V).
- In order to get a current absorption of 1 mA, the resistance R_{FBB} is simply calculated as:

$$R_{FBB} = 2.5\,\text{V} / 1\,\text{mA} = 2.5\,\text{k}\Omega$$

- The voltage divider relationship is:

$$2.5\,\text{V} = U_{out} \cdot \frac{R_{FBB}}{R_{FBU} + R_{FBB}}$$

- This expression can be inverted to find the needed value of R_{FBU}:

$$R_{FBU} = R_{FBB} \cdot \left(\frac{U_{out}}{2.5\,\text{V}} - 1 \right)$$

- Consult data sheet for details and more thorough explanations

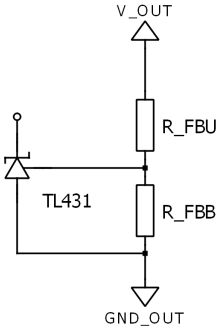

Figure 19 Reference Voltage Setting with the TL431.

LED RESISTOR

Few things to consider:

- typical optocoupler input voltage drop is around 1 V.
- the minimum TL431 anode-cathode voltage required to guarantee the proper functioning is around 2.5 V.
- Therefore, the maximum voltage drop on R_{LED} is:

$$V_{R,LED} = U_{out} - 1\,\text{V} - 2.5\,\text{V}$$

- By assuming a LED current value $I_{R,LED}$, the led resistance can be computed as:

$$R_{LED} = V_{R,LED}/I_{R,LED}$$

- For example, if $U_{out} = 12$ V, then $V_{R,LED} = 8.5$ V. Assuming a maximum LED current of 10 mA, the resistance is around $R_{LED} = 850\,\Omega$.
- Important. Note that this computed resistance is only a "first try" value. Indeed, it is not yet possible to know what would be the real anode-cathode voltage of the TL431 required for the regulation and the LED current. According to the other chosen components of the compensation network, it is likely that R_{LED} is to be changed later on.

Further complications: What are the effects of changing R_{LED} without changing the other parameters of the compensation network?

- Decreasing R_{LED} leads, for the same optocoupler current, to a decrease of the voltage drop $V_{R,LED}$. This leads to the increase of the steady-state anode-cathode voltage of the TL431, and can be helpful in case of saturation below 2.5 V.
- However, since R_{LED} appears at the denominator of the small-signal transfer function of the controller, decreasing its value leads to an increase of the static gain, which generally leads to an increase of the crossover frequency and to a decrease of the phase margin (i.e., less stability robustness).
- Vice versa, increasing R_{LED} can be beneficial for the small-signal stability of the closed-loop system, but may increase the voltage drop and lead to a large-signal saturation of the TL431.
- The proper value is to be chosen as a trade-off between these two opposite requirements.

COMPENSATION ZERO COMPONENTS

Components defining the zero:

- The frequency f_z of the zero has already been chosen previously (in the ideal Type II controller design phase).
- the initial value of R_{COMPz} can be chosen as $5 \cdot R_{FBU}$.
- The capacitor C_{COMPz} can be therefore chosen as:

$$C_{COMPz} = \frac{1}{2\,\pi\,f_z\,(R_{COMPz} + R_{FBU})}$$

- Important. Note that this computed resistance and capacitance are only "first try" values. According to the other chosen components of the compensation network, it is likely that R_{COMPz} is to be changed later on. In case the resistance R_{COMPz} is changed, the capacitor C_{COMPz} needs to be properly re-calculated in a way to keep the same value of f_z.

Few Considerations

- What are the effects of changing R_{COMPz} without changing the other parameters of the compensation network?
- For this compensation network design, R_{COMPz} is the only parameter that can influence the gain of the small-signal transfer function $\tilde{C}_{FB}(s)$ without affecting the large-signal behaviour of the system (e.g., saturation, biasing, etc...).
- Since R_{COMPz} appears at the numerator of the transfer function gain, decreasing it can lead to a decrease of the gain K_P, which generally leads to a decrease of the crossover frequency and to an increase of the phase margin. Vice-versa, increasing R_{COMPz} leads to an increase of K_P, which leads to an increase of the crossover frequency and, likely, to a dectease of the phase margin.
- However, note that the effects of decreasing R_{COMPz} are limited by the resistance R_{FBU}, which also appears at the numerator summed by R_{COMPz}. This means that it is not possible to decrease the gain K_P below a certain value.

COMPENSATION POLE COMPONENTS.

Components defining the pole:

- The frequency f_p of the pole has already been chosen previously (in the ideal Type II controller design phase).
- the initial value of R_{COMPz} can be chosen as 1 kΩ.
- The capacitor C_{COMPp} can be therefore chosen as:

$$C_{COMPp} = \frac{1}{2\,\pi\,f_p\,R_{COMPp}}$$

- Important. Note that this computed resistance and capacitance are only "first try" values. According to the other chosen components of the compensation network, it is likely that R_{COMPp} is to be changed later on. In case the resistance R_{COMPp} is changed, the capacitor C_{COMPp} needs to be properly re-calculated in a way to keep the same value of f_p.
- By the knowledge of R_{COMPp} and of the voltage V_{COMP} (that has already been computed previously) it is possible to compute the current sinked or sourced from the COMP pin of the UCC28C44 device.
- the steady-state current sinked from the COMP pin can be computed as:

$$I_{COMP} = \frac{V_{FB} - V_{COMP}}{R_{COMPp}} \approx \frac{2.5\,\text{V} - V_{COMP}}{R_{COMPp}}$$

- and, in case $I_{COMP} < 0$ the current is sourced by the COMP pin.
- For example, if (from the previous analysis), it results that $V_{COMP,min} = 1.7$ V and $V_{COMP,max} = 2.7$ V, then, by choosing a resistance $R_{COMPp} = 1$ kΩ, the current I_{COMP} ranges between 0.8 mA (sinked) and −0.2 mA (sourced). Both values are within the range of the UCC28C44.

COMPENSATION POLE COMPONENTS..

Few Considerations

- What are the effects of changing R_{COMPp} (and C_{COMPp}) without changing the other parameters of the compensation network?
- Increasing R_{COMPp} leads, for the same V_{COMP} values, to a reduction of the I_{COMP} current. This can be helpful in the several cases.
- If the currents are outside the feasible range of the UCC28C44 device (max 10 mA sinked and max 1 mA sourced), they need to be reduced.
- Since the current I_{COMP} is also flowing on R_{FBG}, by decreasing I_{COMP} it is possible to reduce the voltage drop on R_{FBG} itself, and the optocoupler collector-emitter voltage becomes closer to 2.5 V (i.e., far from the optocoupler saturated conditions).
- Since the optocoupler output current is given by the sum of the current $I_{COMP} = I_{FBG}$ and the current I_{OPTO}, by decreasing I_{COMP}, this current is also decreased. Then, for a given CTR, the reduction of I_{CE} leads to a reduction of I_{LED}, which leads to a reduction of the voltage drop on R_{LED} and to an increase of the AK voltage of the TL431 (far from the lower saturation at 2.5 V).
- However, since R_{COMPp} appears at the numerator of the small-signal transfer function $\tilde{C}_{FB}(s)$, increasing its value also leads to an increase of the crossover frequency and, likely, to a decrease of the phase margin of the controlled system.
- Vice-versa, increasing R_{COMPp} can be beneficial for the small-signal stability of the system, but can weaken the large-signal property of the controller (i.e., the system may be closer to operating limits, optocoupler saturation and TL431 voltage saturation).
- The proper value can be chosen as a trade-off between these two opposite requirements.

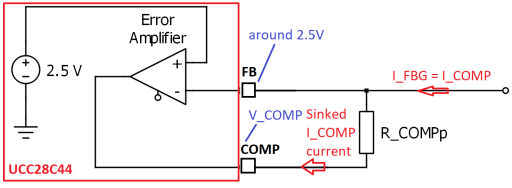

Figure 20 Steady-State circuit of the Error Amplifier.

FEEDBACK PIN RESISTOR.

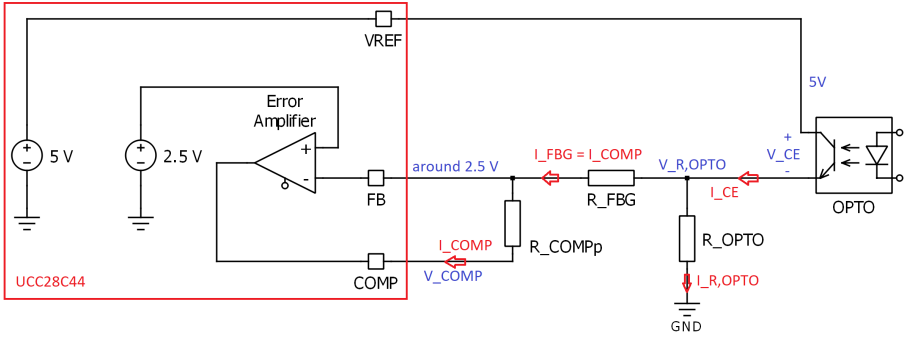

Figure 21 Equivalent model of the steady-state input-side regulation circuit.

- The current $I_{COMP} = I_{FBG}$ has already been computed as:

$$I_{COMP} = I_{FBG} = \frac{2.5\,\text{V} - V_{COMP}}{R_{COMPp}}$$

- The voltage on R_{OPTO} is:

$$V_{R,OPTO} \approx 2.5\,\text{V} + R_{FBG} \cdot I_{FBG} = 2.5\,\text{V} + 2.5\,\text{V} \cdot \frac{R_{FBG}}{R_{COMPp}} - V_{COMP} \cdot \frac{R_{FBG}}{R_{COMPp}}$$

- The Collector-Emitter voltage of the Optocoupler output is:

$$V_{CE} = 5\,\text{V} - V_{R,OPTO} = 2.5\,\text{V} - 2.5\,\text{V} \cdot \frac{R_{FBG}}{R_{COMPp}} + V_{COMP} \cdot \frac{R_{FBG}}{R_{COMPp}} = 2.5\,\text{V} - \frac{R_{FBG}}{R_{COMPp}} \cdot (2.5\,\text{V} - V_{COMP})$$

FEEDBACK PIN RESISTOR..

- If $V_{COMP} < 2.5\ \text{V}$, the voltage V_{CE} is less than 2.5 V.
- To guarantee the proper functioning of the optocoupler, this voltage must be greater than 0.4 V (which is the saturation voltage of the optocoupler). Therefore:

$$2.5\ \text{V} - \frac{R_{FBG}}{R_{COMPp}} \cdot (2.5\ \text{V} - V_{COMP}) \geq 0.4\ \text{V} \qquad \Rightarrow \qquad R_{FBG} \leq R_{COMPp} \cdot \frac{2.5\ \text{V} - 0.4\ \text{V}}{2.5\ \text{V} - V_{COMP}}$$

- Vice versa, if $V_{COMP} > 2.5\ \text{V}$, the voltage V_{CE} is greater than 2.5 V.
- To guarantee the proper functioning of the optocoupler, this voltage must be less than 5 V (which is the VREF voltage of the UCC28C44 device). Therefore:

$$2.5\ \text{V} - \frac{R_{FBG}}{R_{COMPp}} \cdot (2.5\ \text{V} - V_{COMP}) \leq 5\ \text{V} \qquad \Rightarrow \qquad R_{FBG} \leq R_{COMPp} \cdot \frac{5\ \text{V} - 2.5\ \text{V}}{V_{COMP} - 2.5\ \text{V}}$$

- For example, if (from the previous analysis), it results that $V_{COMP,min} = 1.7\ \text{V}$ and $V_{COMP,max} = 2.7\ \text{V}$, and if $R_{COMPp} = 1\ \text{k}\Omega$, then:
  - from the minimum $V_{COMP} < 2.5\ \text{V}$, it results: $R_{FBG} \leq 2.63\ \text{k}\Omega$;
  - from the maximum $V_{COMP} > 2.5\ \text{V}$, it results: $R_{FBG} \leq 12.5\ \text{k}\Omega$
- the first case is more restrictive, and the "first try" value of R_{FBG} can be chosen to be around 1.3 kΩ.

OPTOCOUPLER RESISTOR, CURRENT

- the value of K_p has been already found to be:

$$K_P = CTR \cdot \frac{R_{COMPp}}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \cdot \frac{R_{OPTO}}{R_{OPTO} + R_{FBG}}$$

- all the values, except R_{OPTO}, have already been found, and the desired value of K_p had been chosen to set the bandwidth frequency f_{bw} in the design of the ideal Type II controller. Then, the previous equation can be inverted to find the "first try" value of R_{OPTO}:

$$R_{OPTO} = \frac{R_{FBG}}{1 - \left(\frac{CTR}{K_P} \cdot \frac{R_{COMPp}}{R_{LED}} \cdot \frac{R_{COMPz} + R_{FBU}}{R_{FBU}} \right)}$$

- Sometimes it may be possible to assume $R_{FBG} \gg R_{OPTO}$, and the previous expression become much easier to solve.
- from the expression of the voltage on R_{OPTO} it is possible to find the current flowing in R_{OPTO} as:

$$I_{R,OPTO} = \frac{V_{R,OPTO}}{R_{OPTO}} = \frac{2.5\,\text{V}}{R_{OPTO}} + \frac{(2.5\,\text{V} - V_{COMP})}{R_{COMPp}} \cdot \frac{R_{FBG}}{R_{OPTO}}$$

- the collector-emitter current of the optocoupler output is the sum of $I_{R,OPTO}$ and of I_{FBG}, and its expression is:

$$I_{CE,OPTO} = I_{R,OPTO} + I_{FBG} =$$

$$= \frac{2.5\,\text{V}}{R_{OPTO}} + \frac{(2.5\,\text{V} - V_{COMP})}{R_{COMPp}} \cdot \frac{R_{FBG}}{R_{OPTO}} + \frac{2.5\,\text{V} - V_{COMP}}{R_{COMPp}} = \frac{2.5\,\text{V}}{R_{OPTO}} + \frac{(2.5\,\text{V} - V_{COMP})}{R_{COMPp}} \cdot \left(1 + \frac{R_{FBG}}{R_{OPTO}}\right)$$

- the optocoupler LED current is instead simply expressed as:

$$I_{LED,OPTO} = \frac{I_{CE,OPTO}}{CTR}$$

- these two expressions can be used to verify if both currents are within the specified ranges.

TL431 VOLTAGE

- the expression of the TL431 anode-cathode voltage has already been provided before, although implicitly (sizing of R_{LED}). It is:

$$V_{AK,TL431} = U_{out} - 1\text{V} - R_{LED} \cdot I_{LED,OPTO}$$

- the worst case is obtained for the highest $I_{LED,OPTO}$.
- to guarantee the correct functioning, it must result $V_{AK,TL431} \geq 2.5$ V.
- In case the computed voltage is lower than 2.5 V, the changes that can be made are:
- decrease the optocoupler currents (see previous question);
- decrease the resistor R_{LED} (which leads to a lower voltage drop).
- It is sufficient to compare the values of $i_{LED,OPTO}$ with 1 mA.
- In many cases, the use of a bias resistor can help anyway (even if the current is already greater than 1 mA).
- if the Bias resistor is placed in parallel to the optocoupler LED (R_{Bias2} in the figure), it exploits the LED voltage drop (of around 1 V) to provide the current. In this case R_{Bias} is simply chosen to be:

$$R_{Bias2} \approx \frac{1\text{V}}{1\text{mA}} = 1\text{k}\Omega$$

- If, instead, the Bias resistor is placed between the output terminal and the TL431 (R_{Bias1} in the figure) its value can be computed as:

$$R_{Bias1} = \frac{U_{out} - V_{AK,TL431,max}}{1\text{mA}}$$

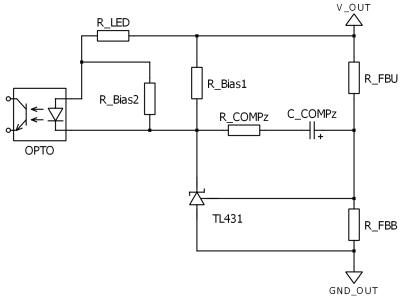

Figure 22 Connection of the TL431 bias resistors.