

Lecture 9

Microelectronic Devices

MOSFET – summary (linear and saturation regimes)

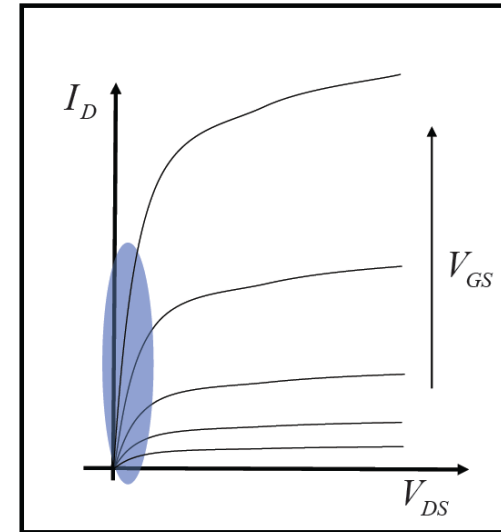
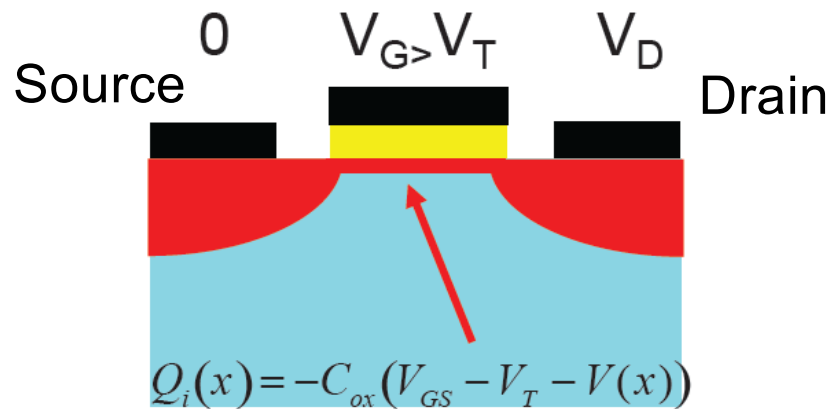
MOSFET – short channel effect

MOSFET – low signal model

MOSFET – subthreshold slope, a fundamental performance limitation

MOSFET vs BJT

MOSFET in linear region, strong inversion @ $V_{GS} > V_T$ and low drain voltage, V_{DS}



$$I_D = \frac{W}{L} \mu_{eff} C_{ox} (V_{GS} - V_T) V_{DS}$$

Also modeled as resistor:

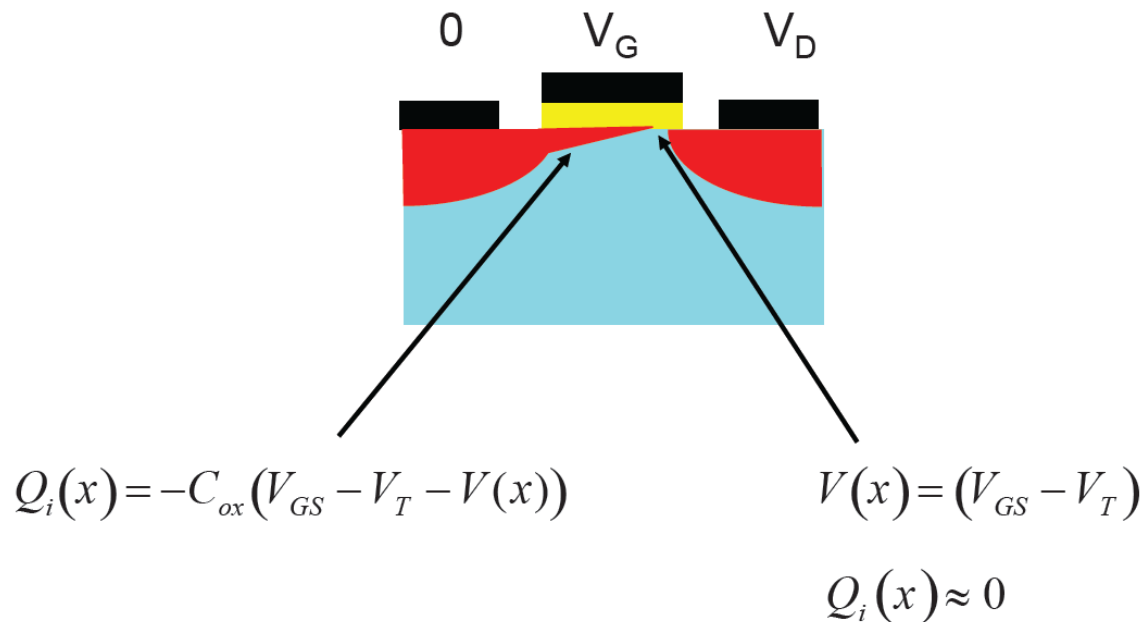
$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{L}{W \mu_{eff} C_{ox} (V_G - V_T)}$$

μ_{eff} is the **effective electron mobility**

MOSFET: pinch-off at high V_{DS}

Cross-over between the linear and saturation regimes

(note that in BJT devices totally different terminology is adopted)

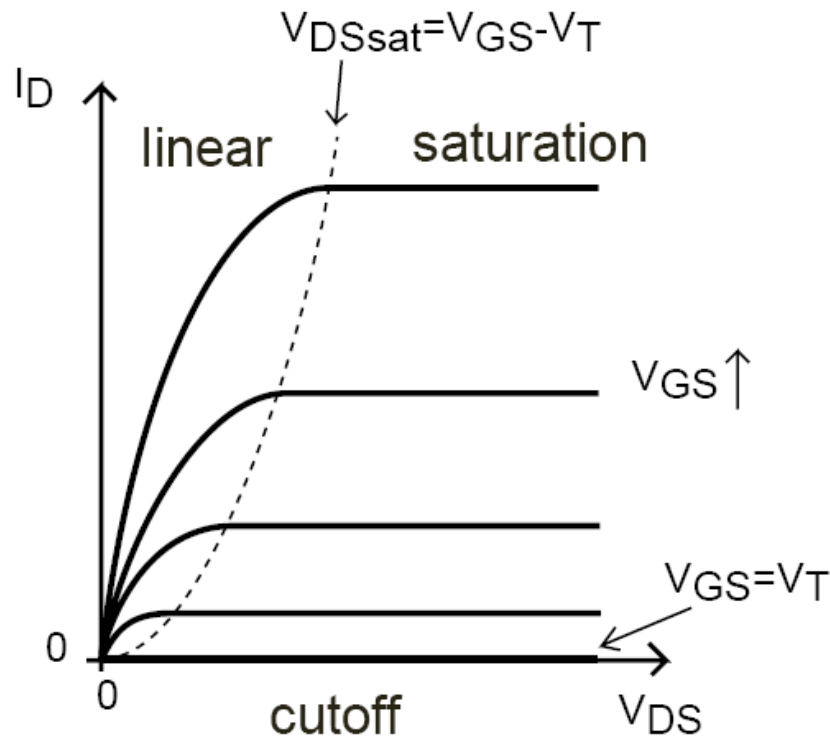


Saturation occurs when $V_{DSsat} = V_{GS} - V_T$

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$

The channel is not cut off, but the current is saturated

MOSFET: regions of operation



- **Cutoff:** $V_{GS} < V_T$ ($V_{GD} < V_T$): no inversion layer anywhere underneath gate

$$I_D = 0$$

- **Linear:** $V_{GS} > V_T$, (with $V_{DS} > 0$): inversion layer everywhere underneath gate

$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_{GS} - \frac{V_{DS}}{2} - V_T \right) V_{DS}$$

- **Saturation:**
 $V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T = V_{Dsat}$

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$

Saturation (2)

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$

Drain current at pinchoff:

\propto lateral electric field

$\propto V_{DSsat} = V_{GS} - V_T$

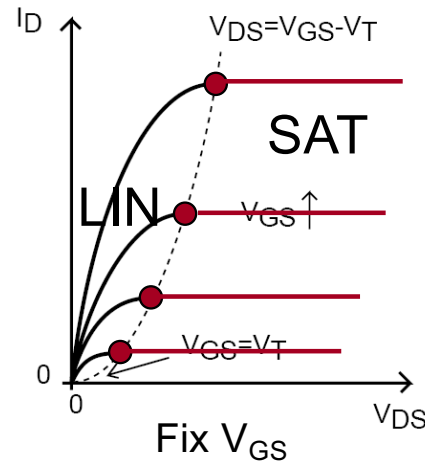
\propto electron concentration

$\propto V_{GS} - V_T$

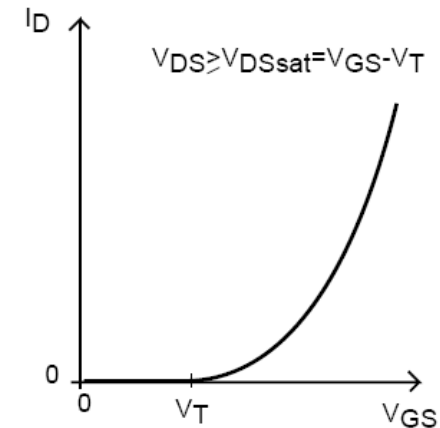
$$\Rightarrow I_{Dsat} \propto (V_{GS} - V_T)^2$$

- $I_{Dsat} \propto 1/L$

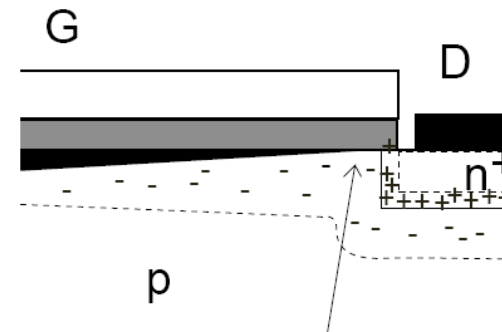
Output charact.



Transfer charact.



Only one curve for V_{DS} above saturation

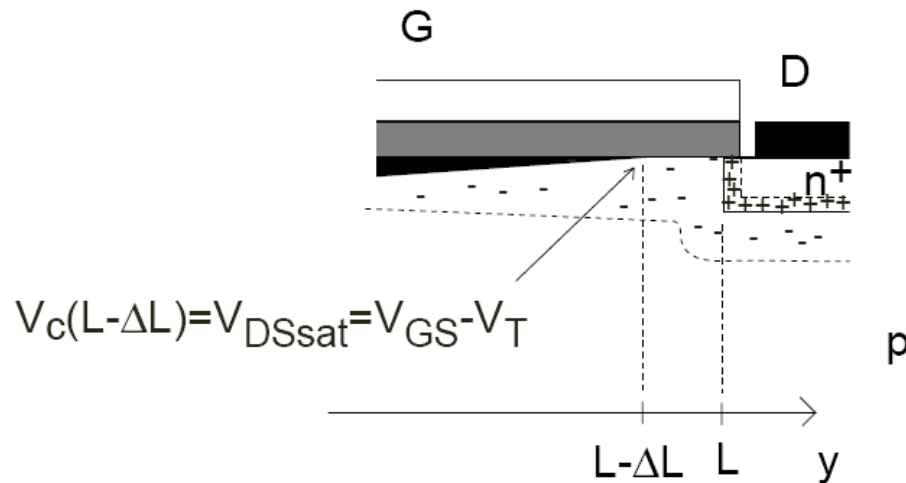


$$V_c(L) = V_{DSsat} = V_{GS} - V_T$$

MOSFET: channel length modulation

What happens if $V_{DS} > V_{DSsat} = V_{GS} - V_T$?

Depletion region separating pinch-off point and drain widens (just like in reverse biased pn junction)



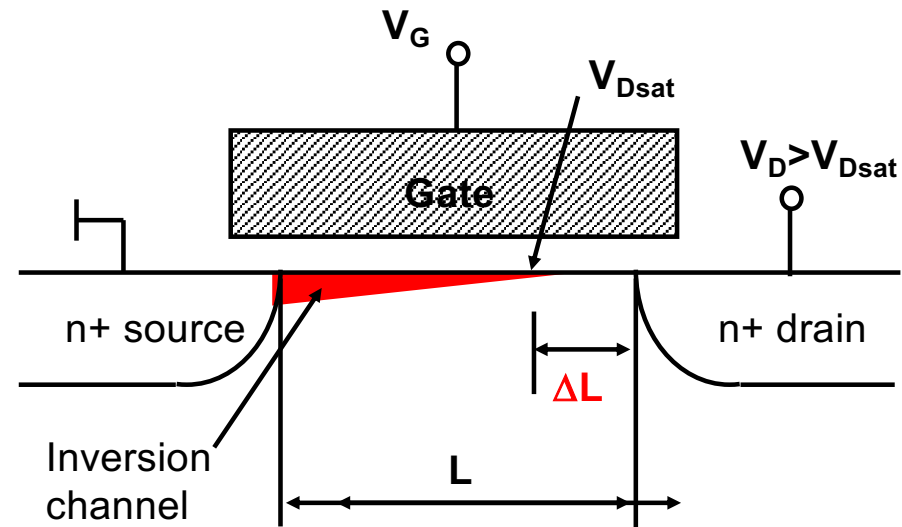
Channel length modulation: $V_{DS} \uparrow \Rightarrow L_{channel} \downarrow \Rightarrow I_D \uparrow$

MOSFET: channel length modulation

Drain current continues to increase after saturation ($V_D > V_{Dsat}$)

- Pinch-off
- Equivalent length: $L - \Delta L$

$$I_D = \frac{I_{Dsat}}{1 - (\Delta L / L)}$$



Long channel

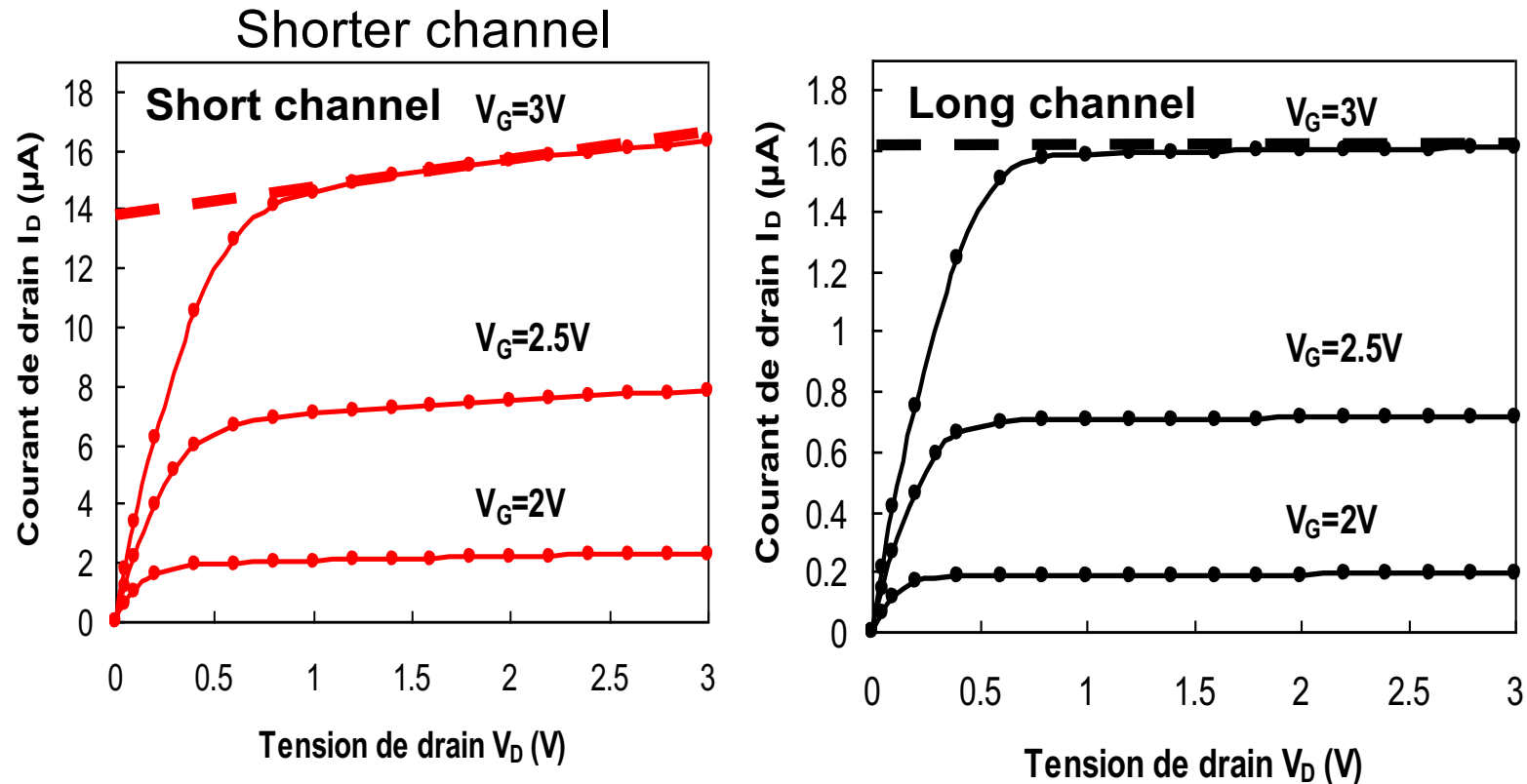
$\Delta L \ll L \rightarrow I_D \approx I_{Dsat} = \text{ct. } (V_D)$

Short channel

$\Delta L \nearrow \text{ with } V_D \rightarrow I_D \nearrow \text{ with } V_D$

MOSFET: channel length modulation

How it looks like and is modeled?



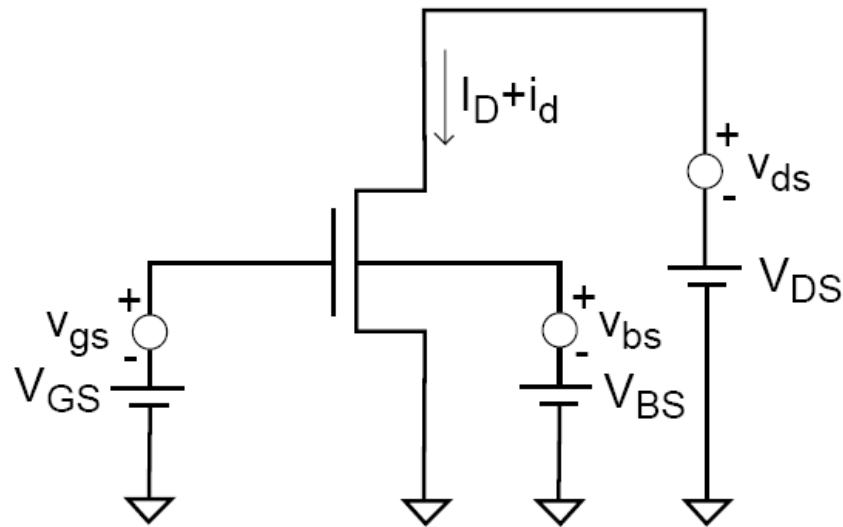
$$I_D = I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda (V_{DS} - V_{DSsat})]$$

Small signal model for MOSFETs

- When we analyze MOSFET circuits (especially amplifiers), we often care about how the MOSFET behaves for small variations around a fixed operating point .
- To simplify analysis, we linearize the MOSFET's behavior around that point — that's called the ***small-signal model***
- We assume the MOSFET is in saturation (active mode), meaning: it acts like a voltage-controlled current source.
- The small-signal model replaces the MOSFET with a **controlled current source**

MOSFET: small signal equivalent circuit

Low frequency

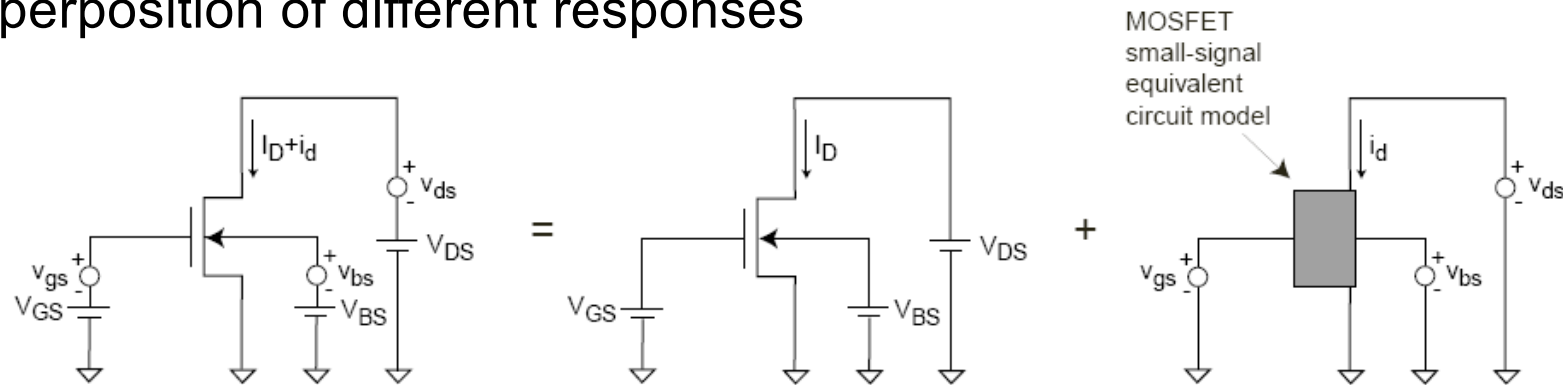


Key points:

- Small-signal fulfils: $v_{gs} \ll V_{GS}$
so that response of non-linear components becomes linear
- Can separate response of MOSFET to bias and small signal.
- Since response is linear, superposition can be used and effects of different small signals are independent from each other

MOSFET: small signal equivalent circuit (2)

Superposition of different responses



$$i_D(V_{GS} + v_{gs}, V_{DS} + v_{ds}, V_{BS} + v_{bs}) \simeq$$

$$I_D(V_{GS}, V_{DS}, V_{BS}) + \frac{\partial I_D}{\partial V_{GS}} \bigg|_Q v_{gs} + \frac{\partial I_D}{\partial V_{DS}} \bigg|_Q v_{ds} + \frac{\partial I_D}{\partial V_{BS}} \bigg|_Q v_{bs}$$

where $Q \equiv \text{bias point } (V_{GS}, V_{DS}, V_{BS})$

$$i_d \simeq g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs}$$

$g_m \equiv \text{transconductance } [S]$

$g_o \equiv \text{output or drain conductance } [S]$

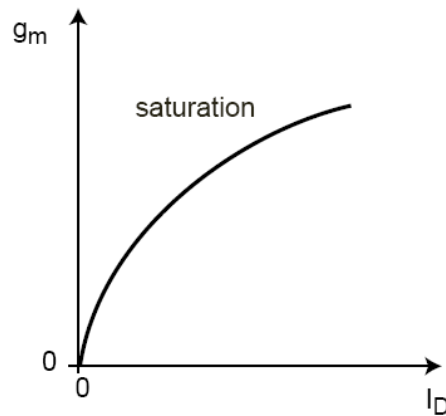
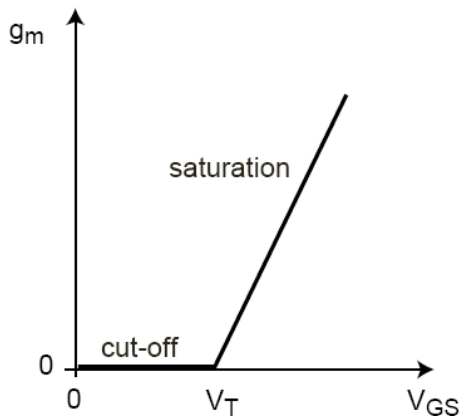
$g_{mb} \equiv \text{backgate transconductance } [S]$

MOSFET: small signal transconductance

- The small-signal model is mainly used when the MOSFET is operating in *saturation*
 - the MOSFET behaves like a voltage-controlled current source
 - The drain current depends primarily on V_{GS}
 - This gives a **high gain** and **linear** response → good for amplifier design

$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda(V_{DS} - V_{DSsat})]$$

Then, neglecting channel length modulation:



$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_Q \simeq \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T)$$

$$g_m = \sqrt{2 \frac{W}{L} \mu_n C_{ox} I_D}$$

MOSFET: small signal output conductance

In saturation:

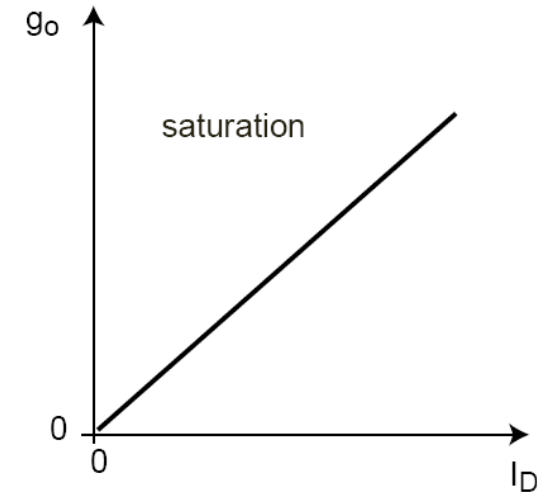
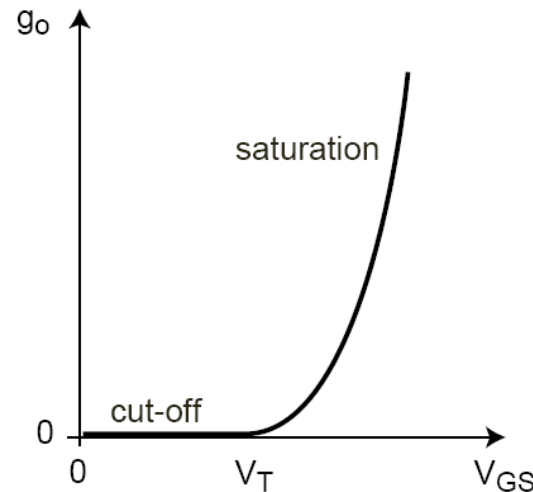
$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda(V_{DS} - V_{DSsat})]$$

$$g_o = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_Q = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 \lambda \simeq \lambda I_D \propto \frac{I_D}{L}$$

$$r_o = \frac{1}{g_o} \propto \frac{L}{I_D}$$

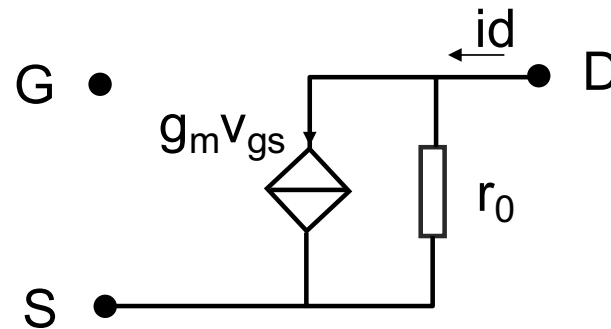
The output behaves like a resistor between drain and source

The output resistance models the fact that even in saturation, the MOSFET isn't a perfect current source due to the channel length modulation



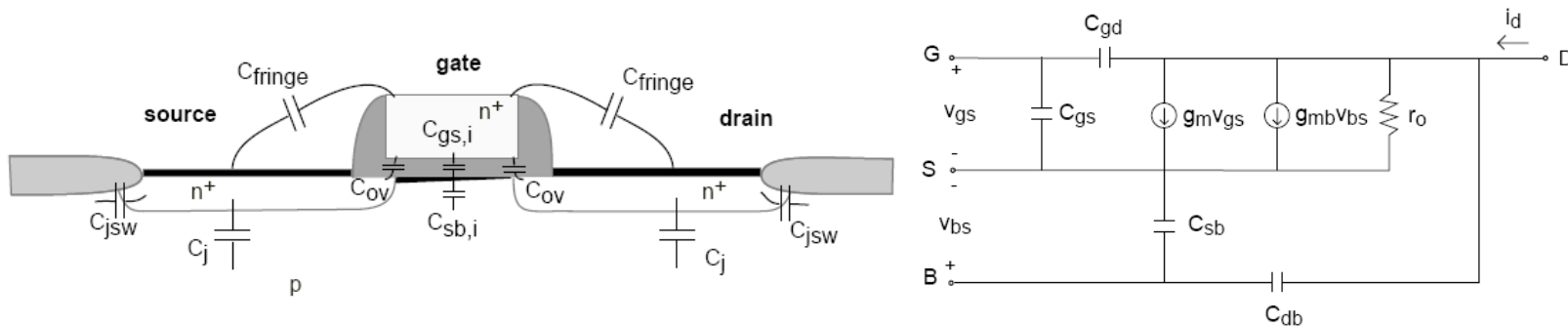
MOSFET: small signal equivalent circuit

Low frequency small signal equivalent circuit (without back-gating):



High frequency small signal equivalent circuit:

- need to add capacitances: more complex circuit



MOSFET: the problem of the subthreshold slope

From the drift/diffusion balance:

$$-q\mu_n n_o \frac{d\phi}{dx} + qD_n \frac{dn_o}{dx} = 0$$

We established:

$$\frac{\mu_n}{D_n} \frac{d\phi}{dx} = \frac{1}{n_o} \frac{dn_o}{dx}$$

using the Einstein relation:

$$\rightarrow \frac{q}{kT} \frac{d\phi}{dx} = \frac{d(\ln n_o)}{dx}$$

Integrating:

$$\frac{q}{kT}(\phi - \phi_{ref}) = \ln n_o - \ln n_o(ref) = \ln \frac{n_o}{n_o(ref)}$$

$$n_o = n_o(ref) e^{q(\phi - \phi_{ref})/kT}$$

Boundary conditions: $\phi_{ref} = 0$ at $n_o(ref) = n_i$.

\rightarrow

$$n_o = n_i e^{q\phi/kT}$$

\rightarrow

$$p_o = n_i e^{-q\phi/kT}$$

“Boltzmann Tyranny” a fundamental limitation of silicon technology

60 mV rule (at 300K)

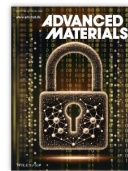
ADVANCED MATERIALS

Research Article

Overcoming the Unfavorable Effects of “Boltzmann Tyranny:” Ultra-Low Subthreshold Swing in Organic Phototransistors via One-Transistor-One-Memristor Architecture

Shuyuan Yang, Jiangyan Yuan, Zhaofeng Wang, Xianshuo Wu, Xianfeng Shen, Yu Zhang, Chunli Ma, Jiamin Wang, Shengbin Lei, Rongjin Li, Wenping Hu

First published: 28 February 2024 | <https://doi.org/10.1002/adma.202309337> | Citations: 1



Volume 36, Issue 23
June 6, 2024
2309337

References Related Information

Recommended

[Conjugated Polymer Heteroatom](#)

Nano Letters > Vol 21/Issue 7 > Article

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LETTER | March 29, 2021

Overcoming Boltzmann's Tyranny in a Transistor via the Topological Quantum Field Effect

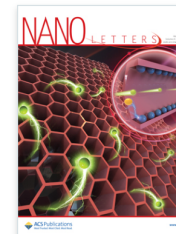
Muhammad Nadeem*, Iolanda Di Bernardo, Xiaolin Wang, Michael S. Fuhrer*, and Dimitrie Culcer*



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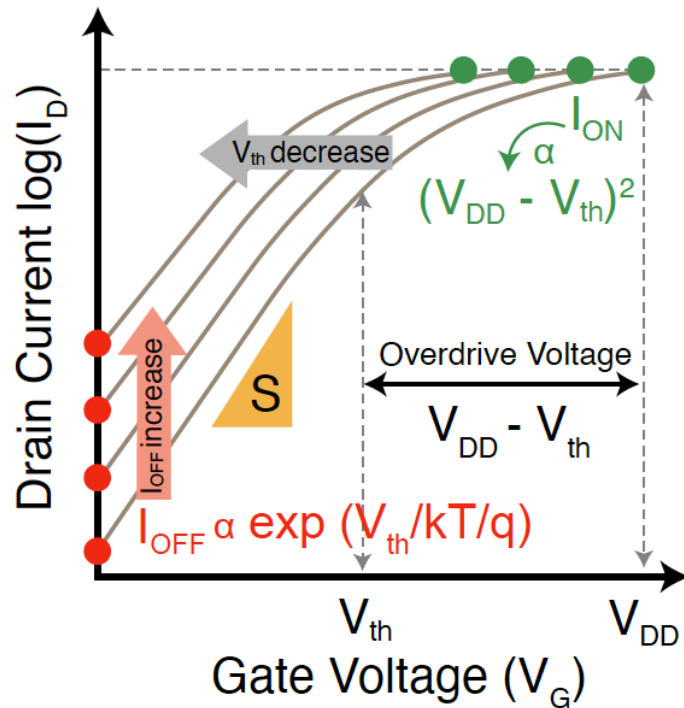
Supporting Information (1)



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For every decade of increase in n_0 , ϕ increases by 60 mV at 300K.

Subthreshold slope: a fundamental limitation of MOSFETs



$$SS = \frac{\partial V_{GS}}{\partial \log I_{DS}} \geq 60 \text{ mV/dec}$$

There is a fundamental limitation for the subthreshold slope, which is determined by Boltzmann's statistics (60= mV/dec is calculated at the room temperature)

An ideal switch must have a steep slope (i.e. smallest possible voltage per current decade), the “Boltzmann's tyranny” is an important limitation for modern MOSFETs

This limitation cannot be overcome by any technological improvements without changing the physical principles

New device physics is needed

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$

MOSFETs vs BJT

$$I_C \propto \exp \frac{qV_{BE}}{kT}$$

- Output current I_D controlled by voltage
- Main current flow Source to Drain
- Very high input impedance (ideal gate draws zero current)
- Power consumption is low (ideal gate draws zero current)
- Better thermal stability (positive temp. coefficient)
- Linear gain is lower
- unipolar device (single type of carriers)
- main applications: Switching, digital logic
- Output current I_C controlled by base current
- Main current flow Collector to Emitter
- Moderate input impedance (base draws electric current)
- Power consumption is higher (base draws electric current)
- Worse thermal stability (thermal runaway risk)
- Linear gain is higher
- Bipolar (both electrons and holes involved)
- analog amplification (gain + linearity)