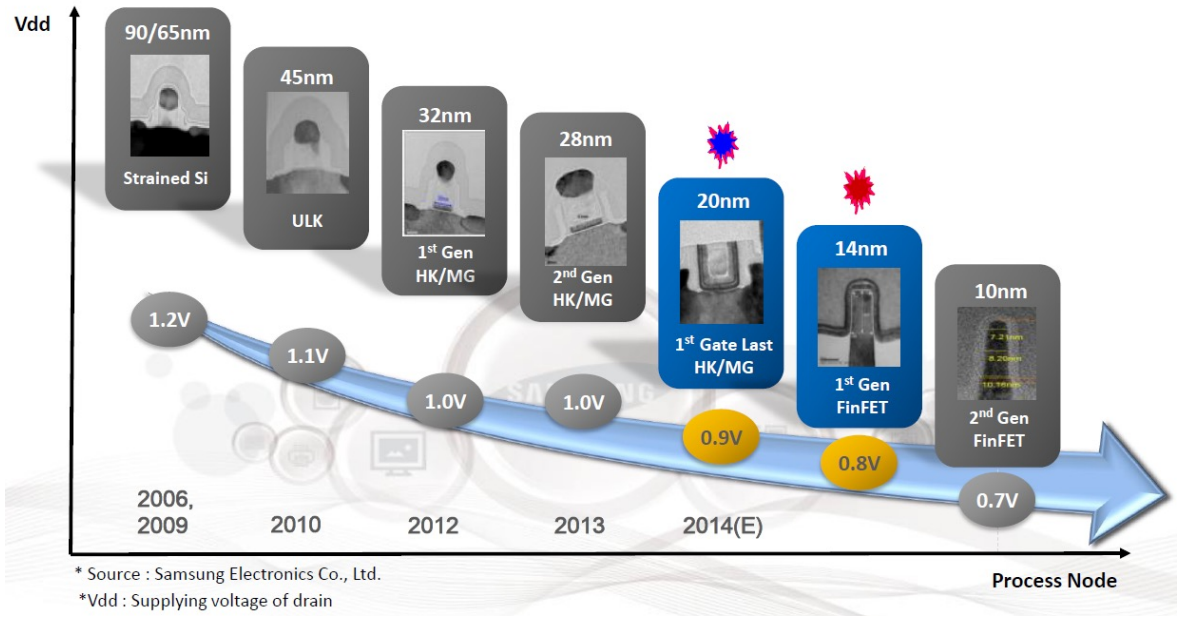
Lecture 7
Micro(Nano)electronic Devices

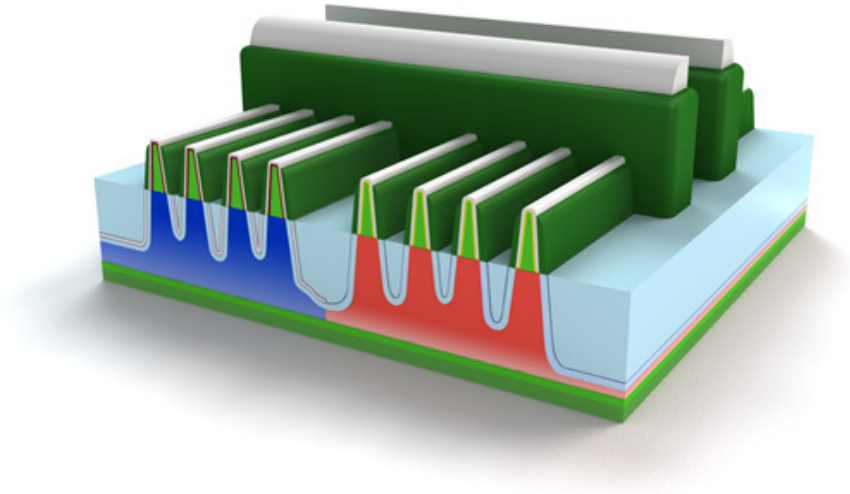
MOS structure

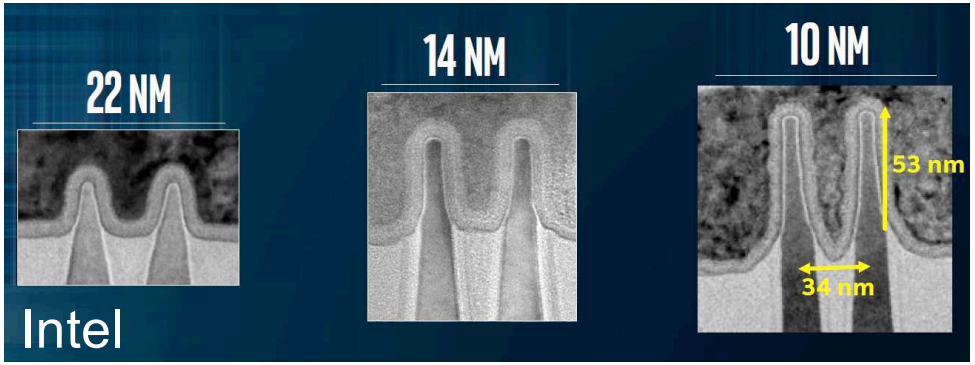
- Electrostatics of MOS structures

- Different operation regimes of MOS structures
  - Accumulation
  - Depletion
  - Inversion
- CV – characteristics of MOS structures
- MOSFET introduction

From bulk to nanometer **Fin**FETs: MOSFET **body** is today a 3D device



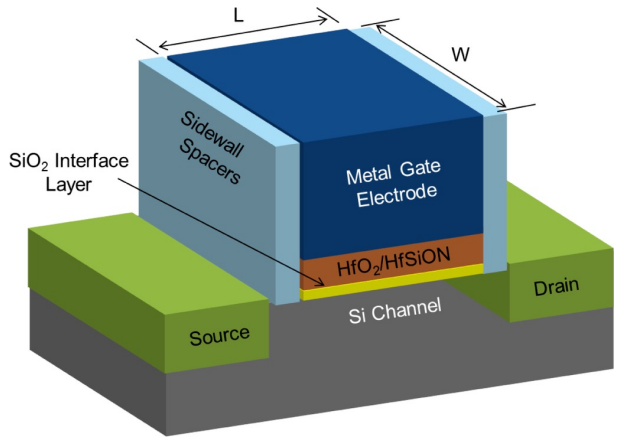


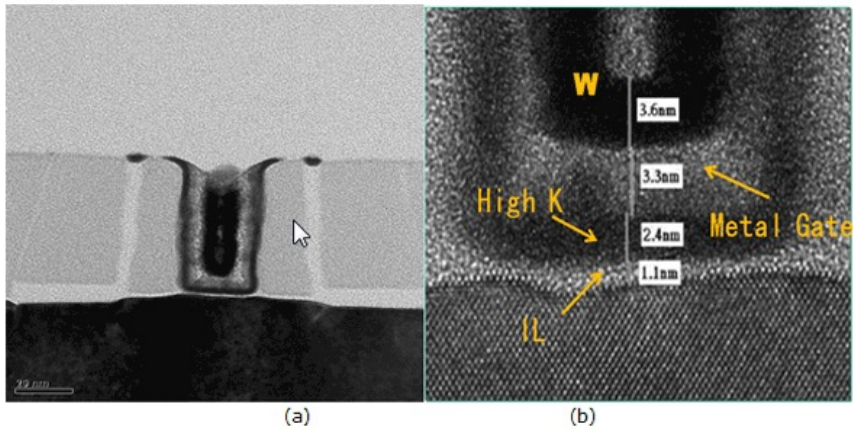


Nanometer (<100nm) MOSFET **gate stack**: high-k/metal gate

Materials of gate stack changed for nanometer scale MOSFET:

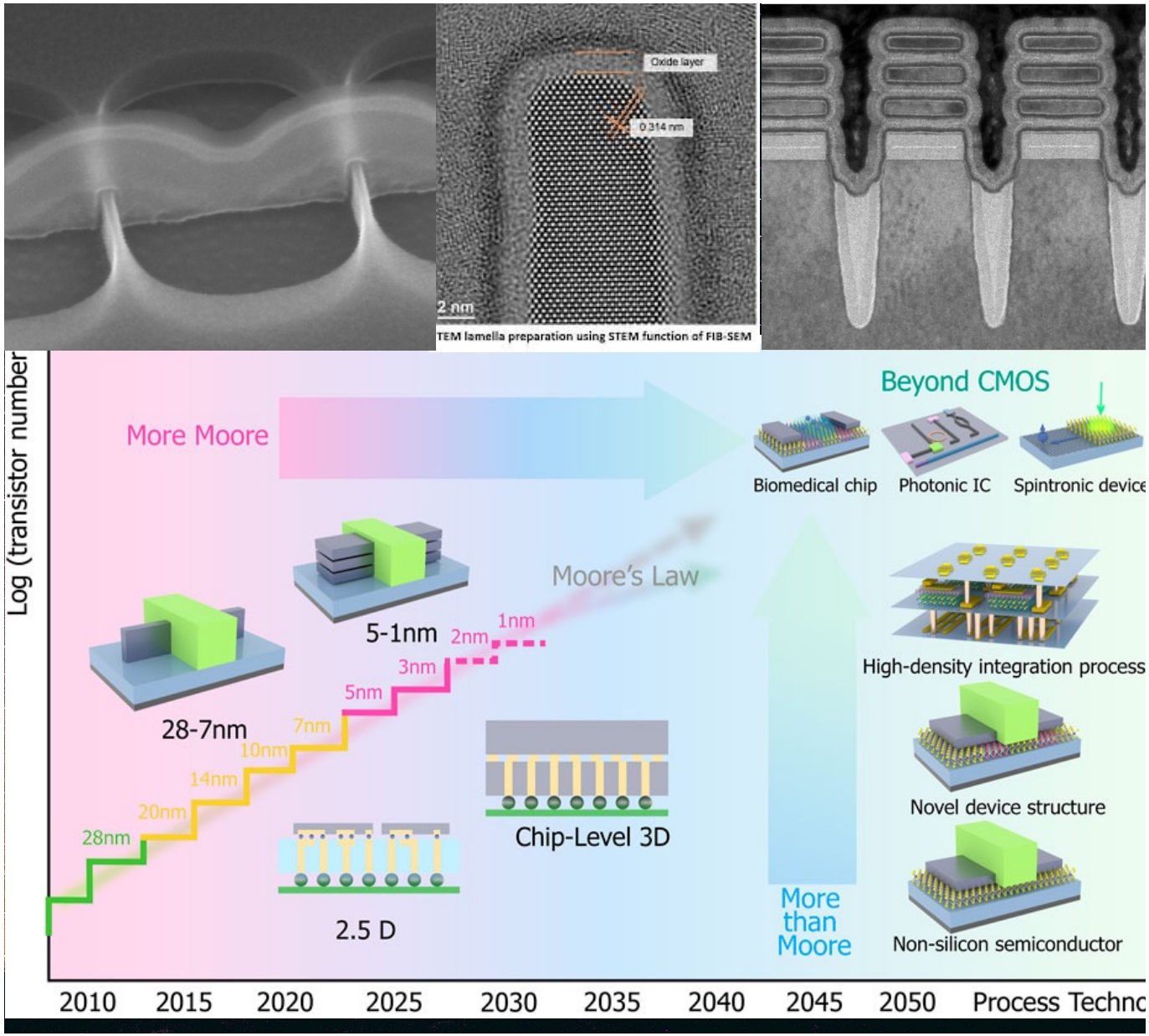
- Polysilicon/SiO2 replaced by Metal/high-k dielectric
- Channels are strained (from dimensions < 90nm)





Moore's law and nano-processors

- 10^9 x more transistors than stars in Milky Way
- From 100 micrometers down to few nanometers in 60 years
- 100M to 1B transistors/mm^2

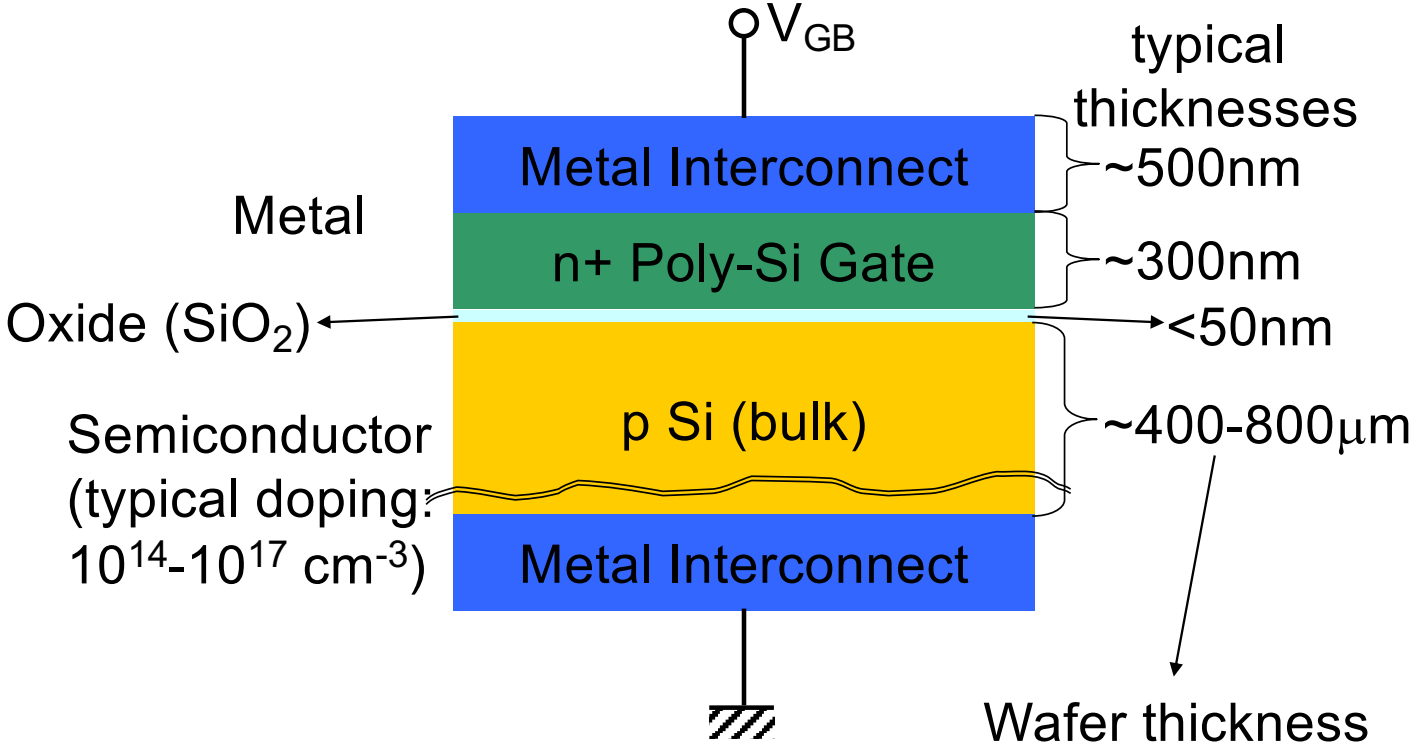


Metal Oxide Semiconductor (MOS) structure

(MOS capacitor)

- Electrostatics
- MOS under bias
- Energy bands
- Depletion/accumulation/inversion

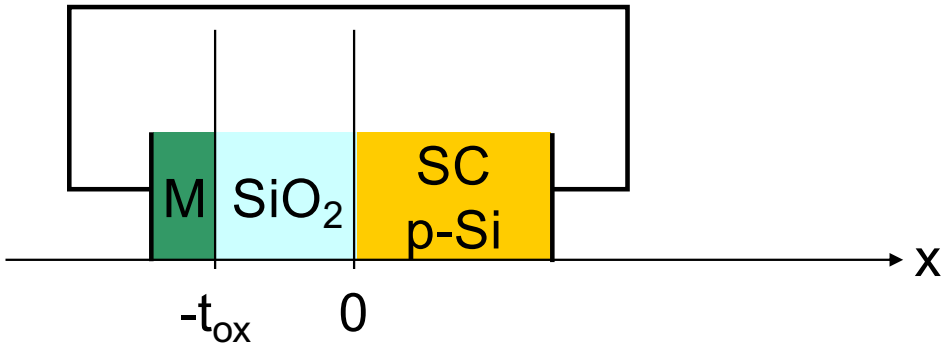
Metal-Oxide-Semiconductor (MOS) typical (classic) structure



Basic applications of MOS

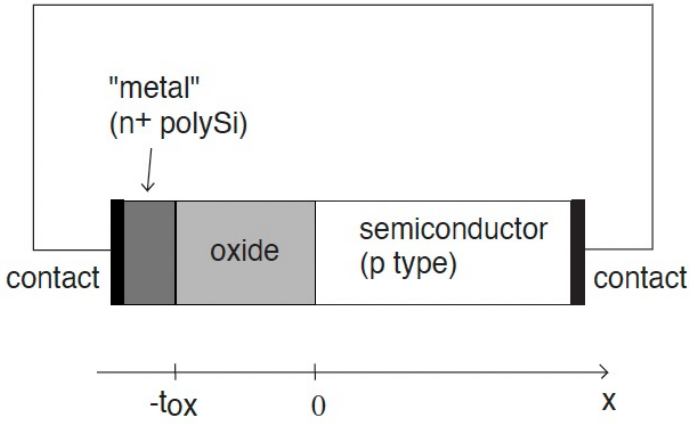
- Digital and analog integrated circuits: MOS Field-Effect Transistor (MOSFET) is the key element in Complementary MOS (CMOS) circuitry.
- Memories: FLASH, DRAM, EPROM
- Image sensors CCD and CMOS
- …..

MOS electrostatics at $V_{GB}=0$

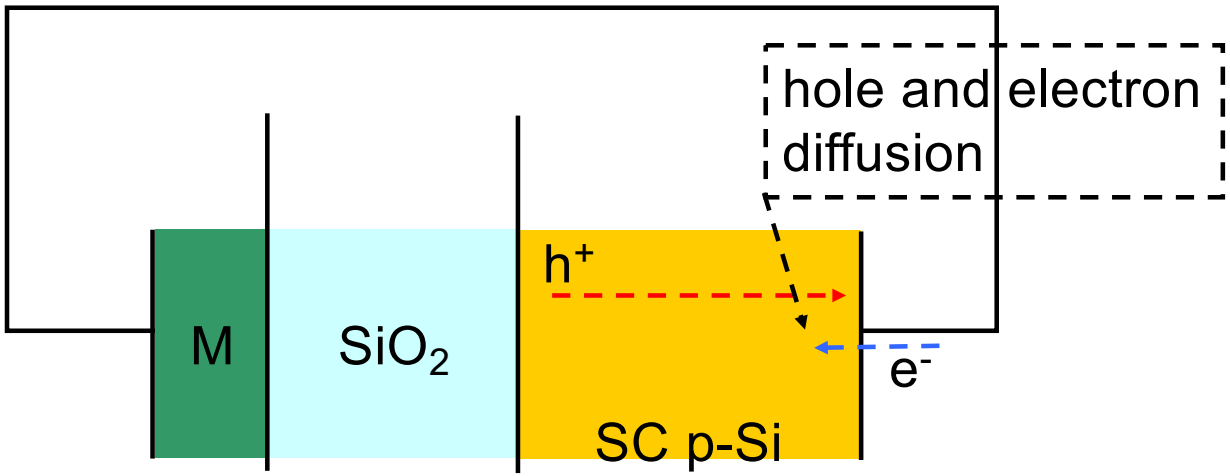


- Established MOSFET technology uses PolySi as a gate electrode
- **Polysilicon** stands for *polycrystalline silicon, it is a conductive material that can be heavily doped*

– Metal (M): charges only at the interface with the oxide (SiO_2)
– Oxide (O): No free carriers inside (insulator)
– Semiconductor (SC): Can have volume charges ir a space-charge region (depletion region).



Establishing thermal equilibrium

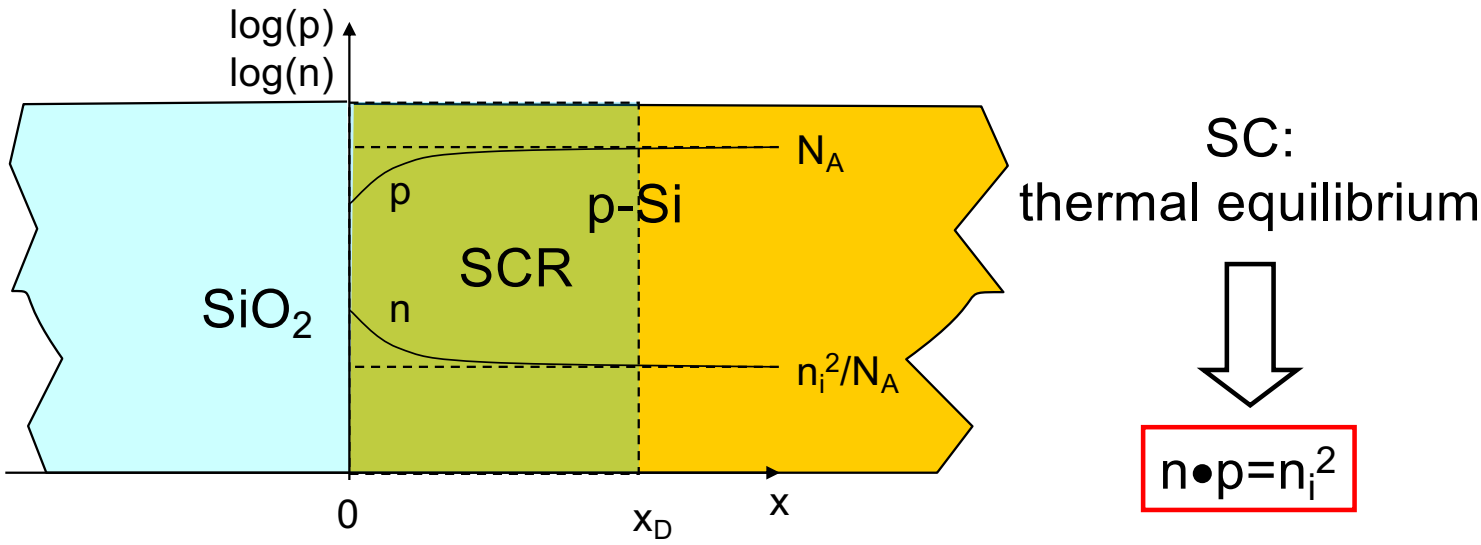


– Thermal equilibrium could not be established through SiO_2 (***insulator***). To do so one needs to connect M and SC.
– MOS: dissimilar materials in contact ⇨ carrier transfer ⇨ space-charge region formed even at zero bias ⇨ potential built-in

– What is the electrostatics of this system?

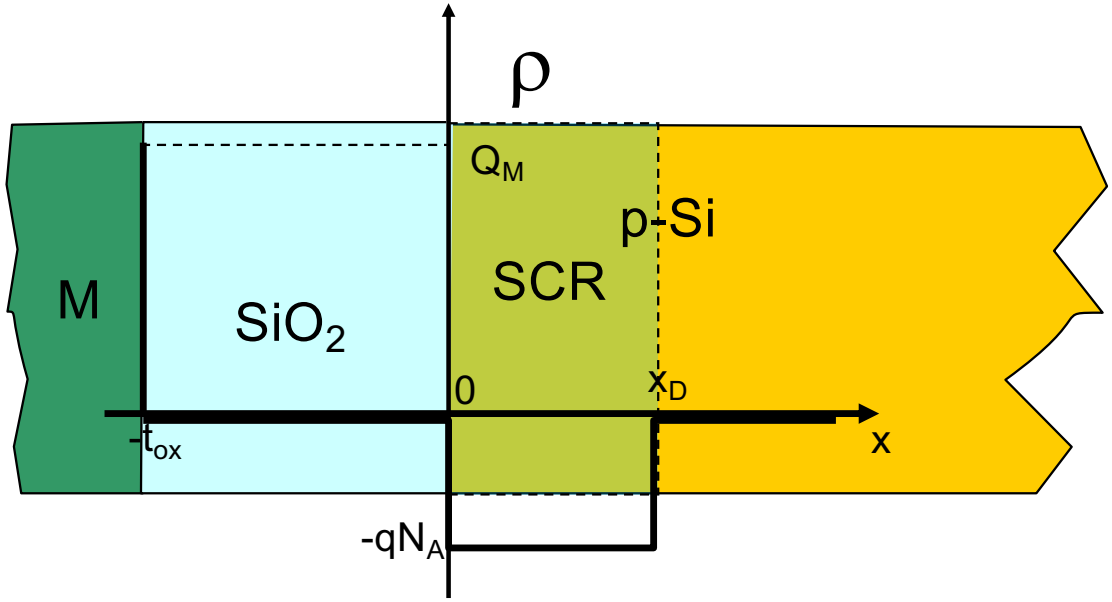
SCR formed at the Si-SiO_2 interface

p-doped Si: equilibrium is often achieved by electrons diffusing from metal to semiconductor



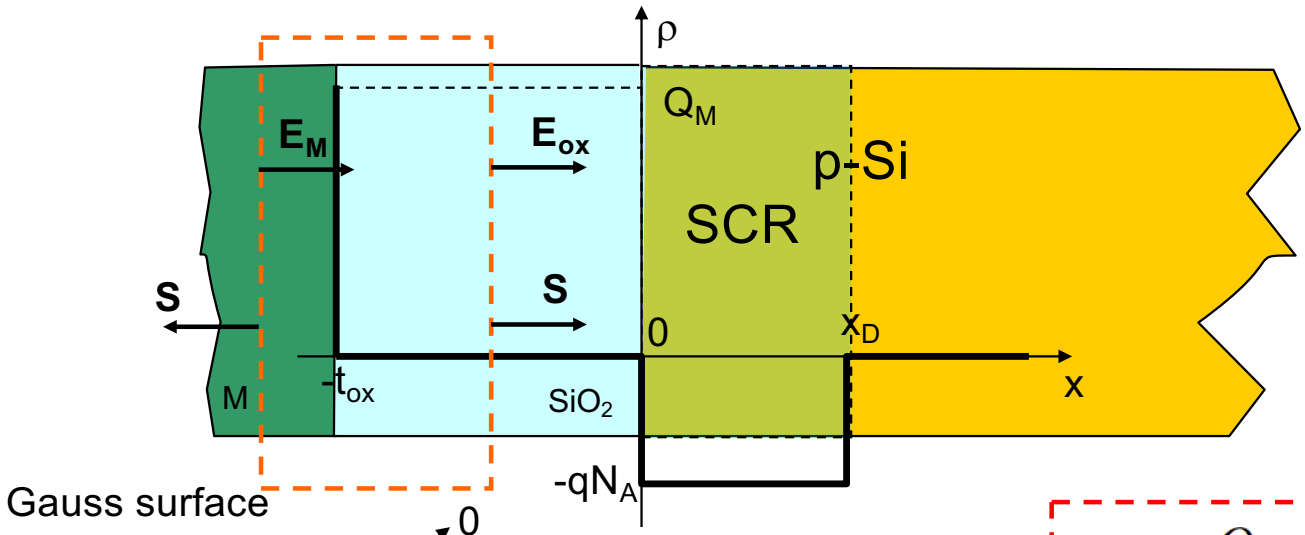
- Holes diffused towards metal leaving behind the ionized acceptor atoms and creating a space-charge region (SCR)
- Fewer holes near Si/SiO2 interface ⇒ ionized acceptors (volume space charge)

Electrostatic analysis (1)

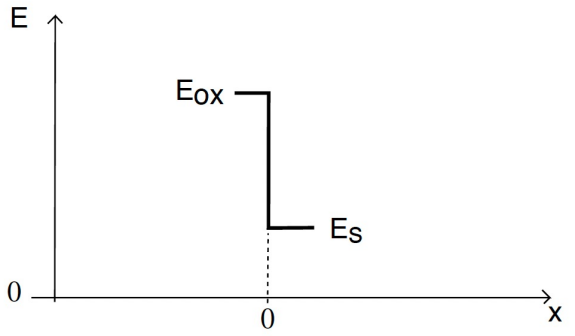


– SC: space-charge region close to the Si-SiO2 interface
  • (we use the depletion approximation)
– M: charge sheet at the interface M-SiO2
– Charge neutrality in the whole structure

Electrostatic analysis (2): electric field



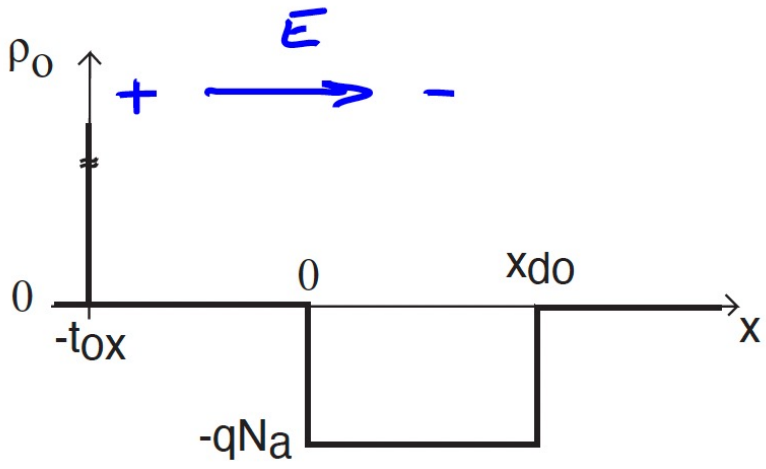
$$\epsilon_{ox}\vec{E}_{ox}\,\vec{S} + \epsilon_M\vec{E}_M\,\vec{S} = Q_M S \Rightarrow \epsilon_{ox}\,E_{ox} = Q_M \Rightarrow E_{ox} = \frac{Q_M}{\epsilon_{ox}}$$

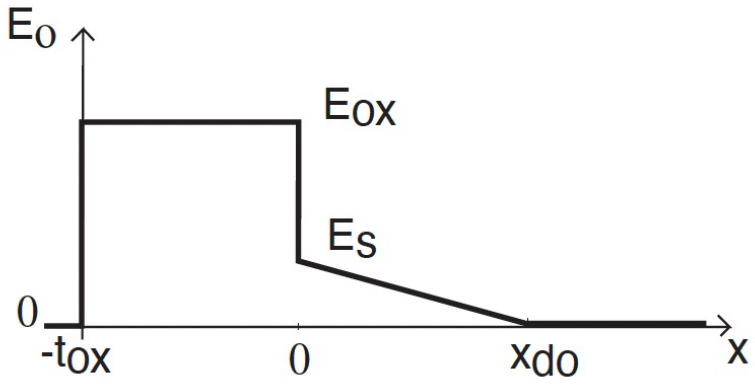


Elec. displacement vector continuity at Si-SiO_2 interface

$$\vec{D}_{ox} = \vec{D}_{sc,int} \Rightarrow \epsilon_{ox}E_{ox} = \epsilon_{sc}E_{sc,int} \Rightarrow \frac{E_{ox}}{E_{sc}} = \frac{\epsilon_{r,sc}}{\epsilon_{r,ox}} = \frac{11.9}{3.9} \simeq 3$$

Electrostatic analysis (3): electric field





$$\frac{E_{ox}}{E_s} = \frac{\epsilon_s}{\epsilon_{ox}} \simeq 3$$

$$E_o(x_2) - E_o(x_1) = \frac{1}{\epsilon}\int_{x_1}^{x_2} \rho_o(x)dx$$

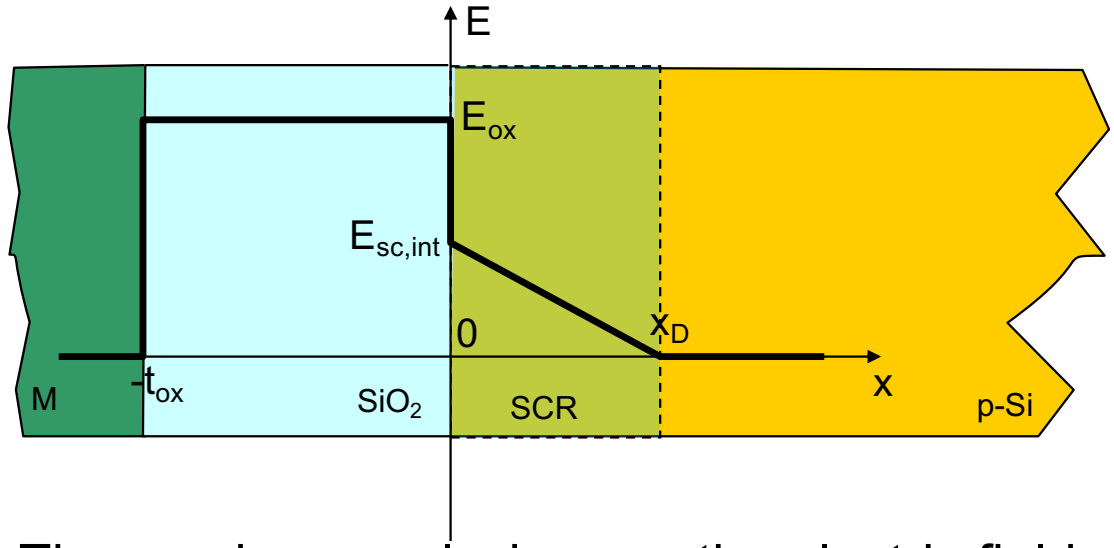
$$x_{do} < x \qquad E_o(x) = 0$$

$$0 < x < x_{do} \qquad E_o(x) = -\frac{qN_a}{\epsilon_s}(x - x_{do})$$

$$-t_{ox} < x < 0 \qquad E_o(x) = \frac{\epsilon_s}{\epsilon_{ox}}E_o(x = 0^+) = \frac{qN_a x_{do}}{\epsilon_{ox}}$$

$$x < -t_{ox} \qquad E_o(x) = 0$$

Electrostatic analysis (4) - potential

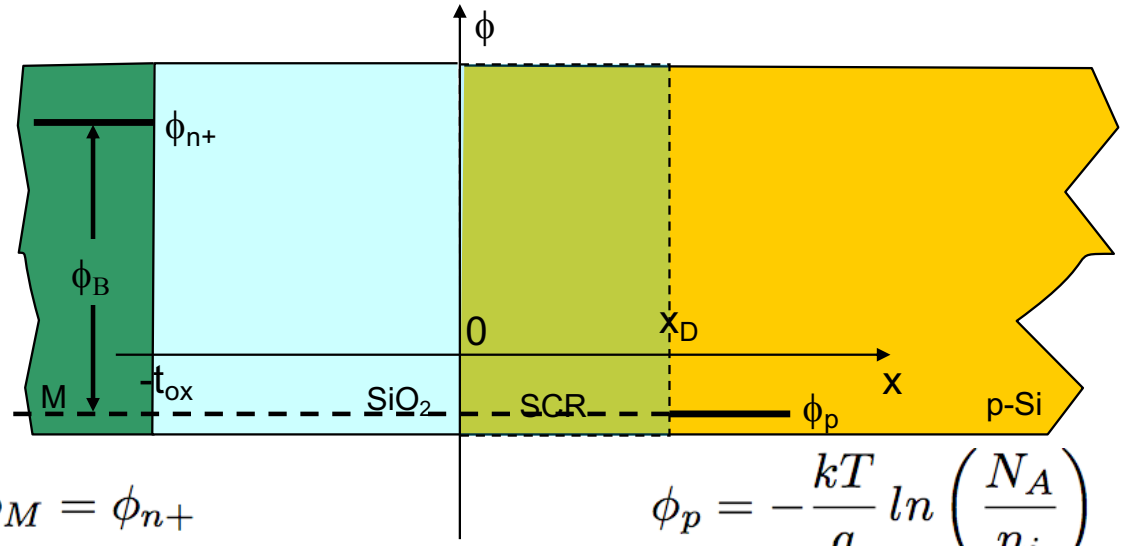


- The previous analysis gave the electric field across the MOS structure.
- In order to obtain the potential distribution across the structure one has to integrate the electric field as a function of x.

Electrostatic potential (1)

one can determine “zero” potential:

$$\phi = 0 \;@\; n_o = p_o = n_i$$



$$\phi = \frac{kT}{q} \ln \frac{n_o}{n_i} \qquad \phi = -\frac{kT}{q} \ln \frac{p_o}{n_i}$$

then the potentials at the edges (QNRs) can be determined

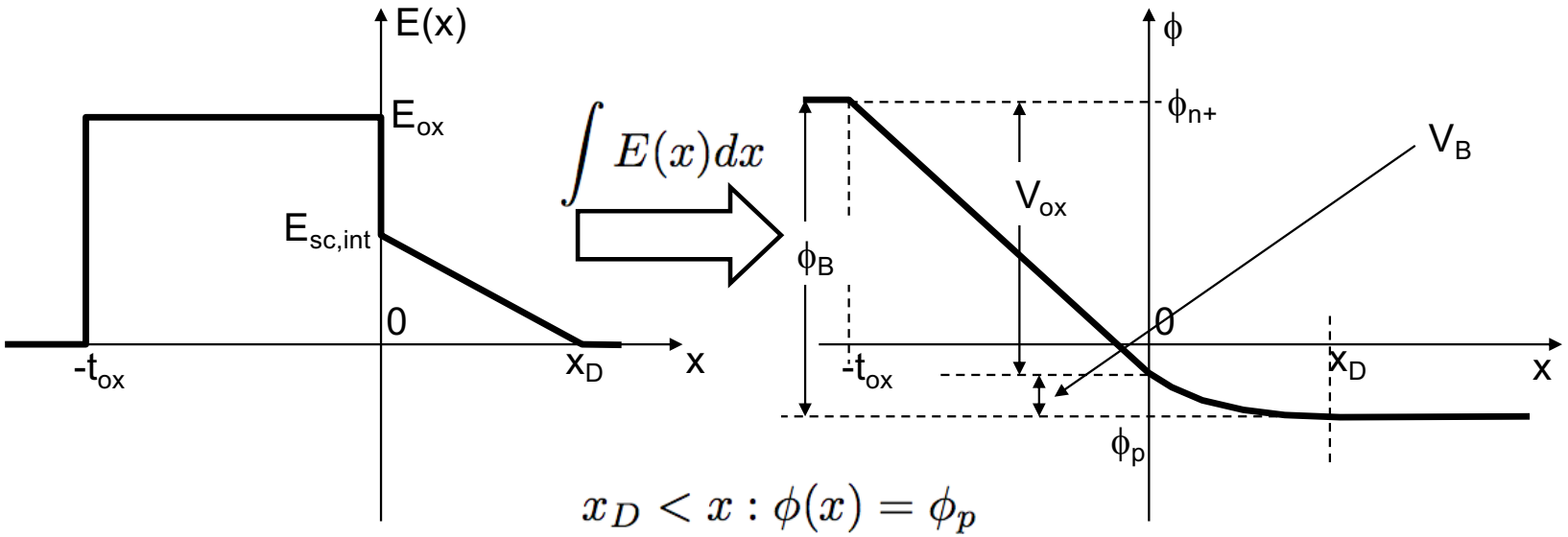
$$\phi_g = \phi_M = \phi_{n+} \qquad \phi_p = -\frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$$

$$\phi_B = \phi_M - \phi_p = \phi_{n+} + \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$$

– From the doping of the poly-Si gate and of the p-Si one can determine the barrier height.

Electrostatic potential (2)

$$\phi_o(x_2) - \phi_o(x_1) = -\int_{x_1}^{x_2} E_o(x)dx$$



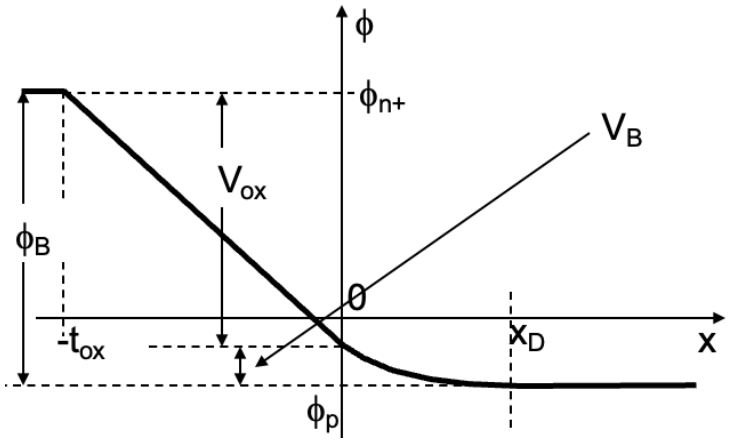
$$x_D < x : \phi(x) = \phi_p$$

$$0 < x < x_D : \phi(x) = \phi_p + \frac{q\,N_A}{2\,\epsilon_{sc}}\,(x - x_D)^2$$

$$-t_{ox} < x < 0 : \phi(x) = \phi_p + \frac{q\,N_A}{2\,\epsilon_{sc}} x_D^2 - \frac{q\,N_A\,x_D}{\epsilon_{ox}} x$$

$$x < -t_{ox} : \phi(x) = \phi_{n+}$$

Electrostatic potential (3)



The potential difference across structure:

$$\phi_B = V_B + V_{ox} = \frac{q\,N_A\,x_D^2}{2\,\epsilon_{sc}} + \frac{q\,N_A\,x_D\,t_{ox}}{\epsilon_{ox}}$$

⇩ From this equation one can find x_D :

$$x_D = \frac{\epsilon_{sc}}{\epsilon_{ox}} t_{ox} \left(\sqrt{1 + \frac{2\,\epsilon_{ox}^2\,\phi_B}{\epsilon_{sc}\,q\,N_A\,t_{ox}^2}} - 1 \right) = \frac{\epsilon_{sc}}{C_{ox}} \left(\sqrt{1 + \frac{4\,\phi_B}{\gamma^2}} - 1 \right)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \left[\frac{F}{m^2} \right]$$

Oxide capacitance per unit area

$$\gamma = \frac{1}{C_{ox}} \sqrt{2\,\epsilon_{sc}\,q\,N_A} \left[V^{\frac{1}{2}} \right]$$

Body factor coefficient

Example

$$N_D = 10^{20}\,cm^{-3},\ N_A = 10^{17}\,cm^{-3},\ t_{ox} = 8\,nm,\ T = 300K$$

$$\phi_B \simeq 576\,mV + 403\,mV \simeq 979\,mV$$

$$C_{ox} \simeq 4.3 \times 10^{-7}\,F/cm^2$$

$$\gamma \simeq 0.43\,V^{1/2}$$

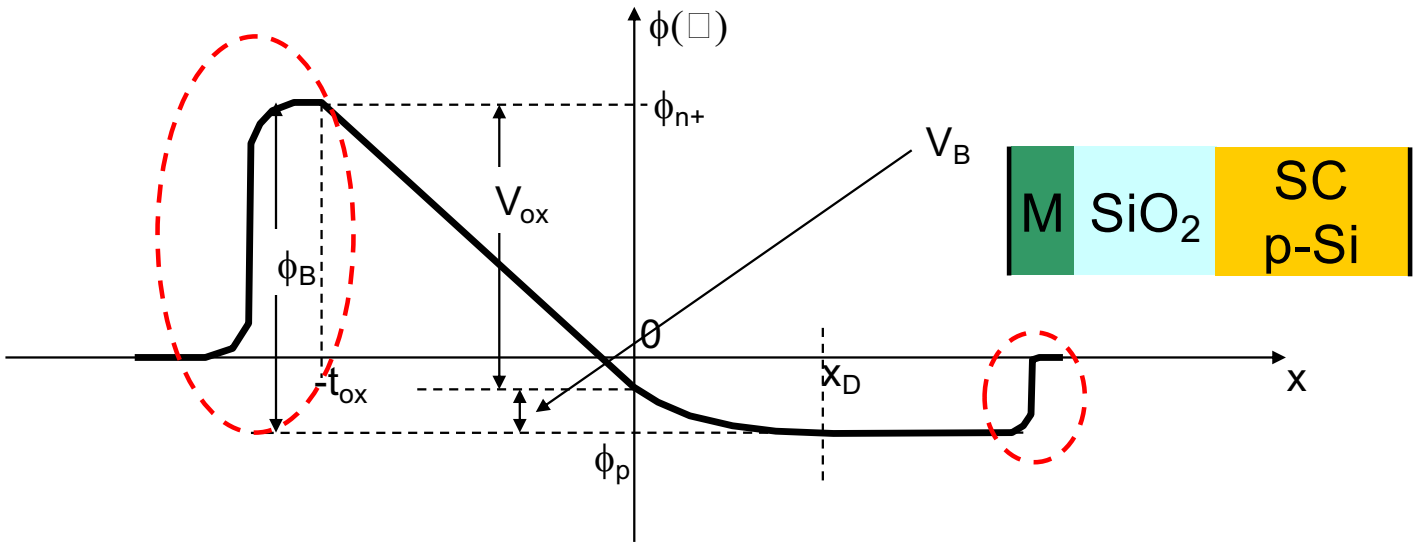
$$x_D \simeq 92nm$$

Note that much thinner dielectrics are used in MOSFET technology

90 nm	~2.0 – 2.5 nm
45 nm	~1.4 – 1.6 nm
22 nm & below	~1.0 – 1.2 nm

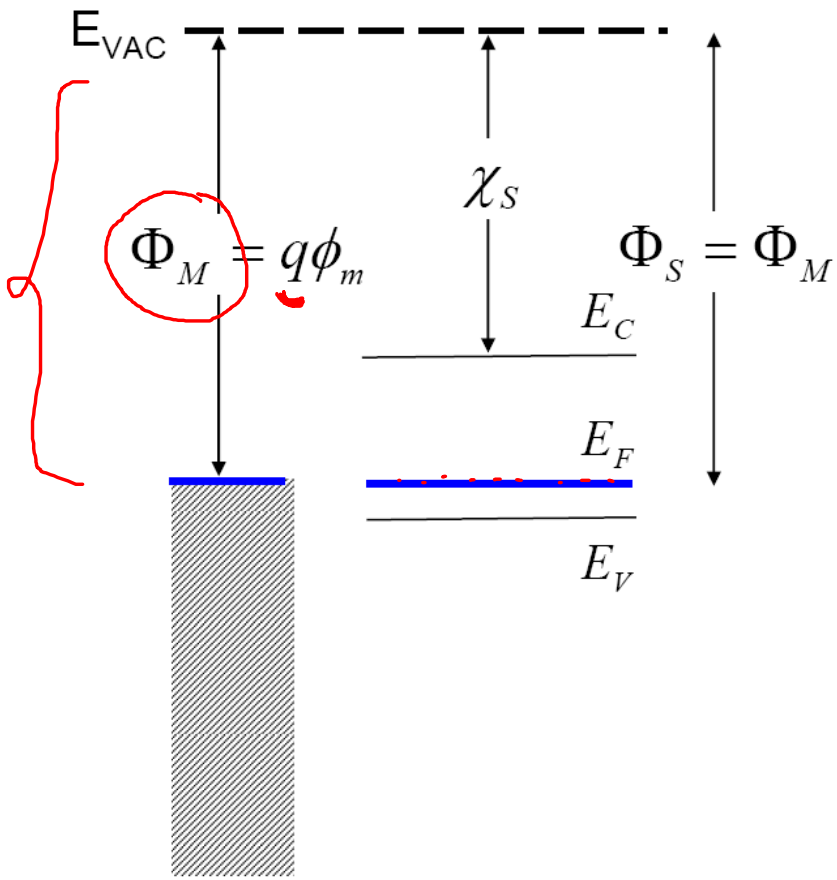
In 5-7nm node we approach 0.6-0.8nm equivalent oxide thickness (EOT) $\mathrm{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} \cdot t_{high-k}$

Contact potentials

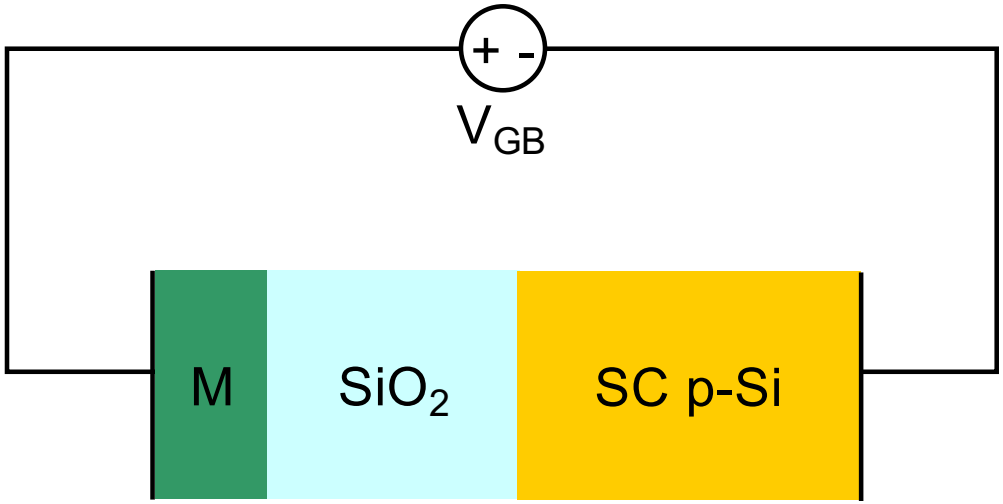


- Don’t forget the contact potentials!
- Contact-to-contact potential difference is zero!

Gate-semiconductor workfunction differences



MOS under bias (1)

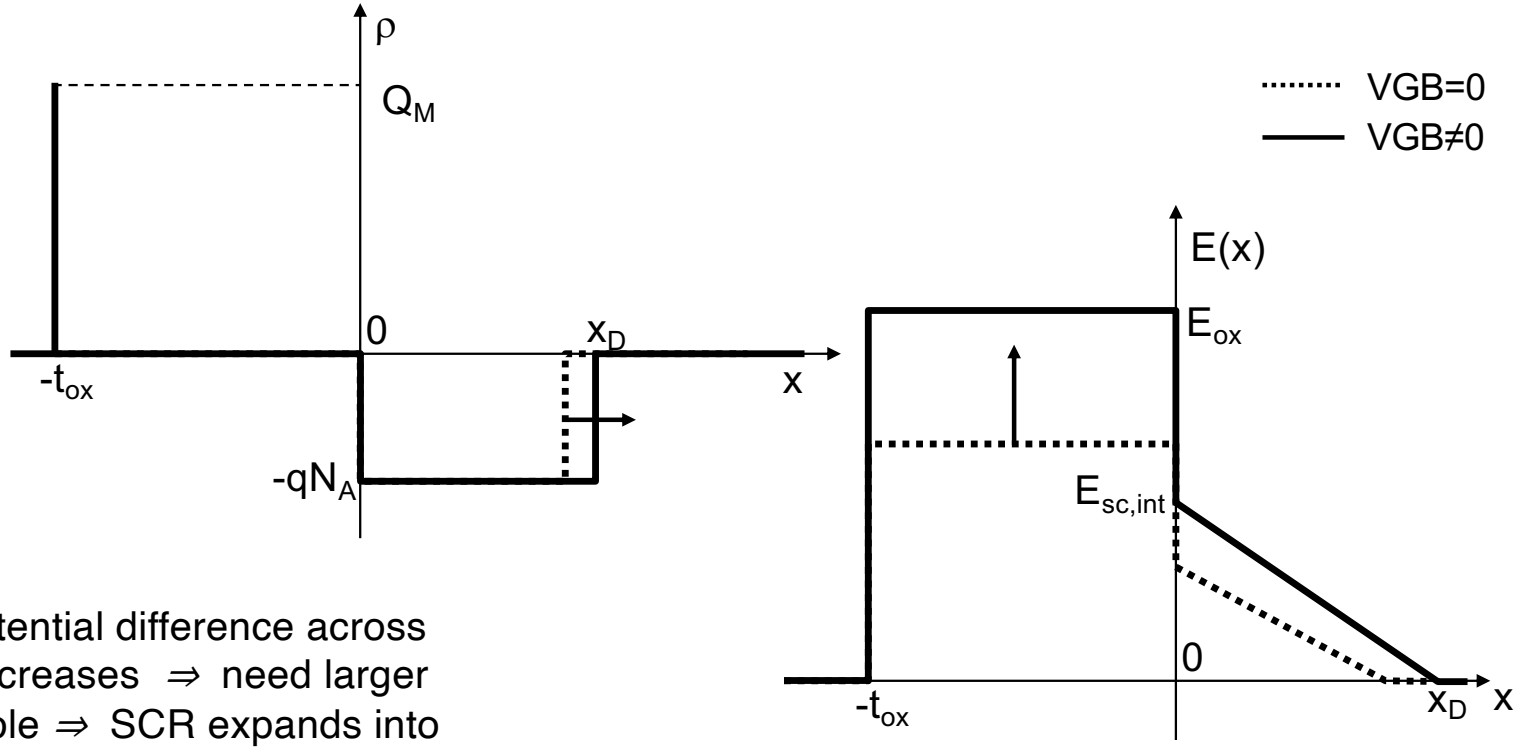


- Electrostatics of the MOS structure affected
- Where can the potential drop?

MOS under bias (2)

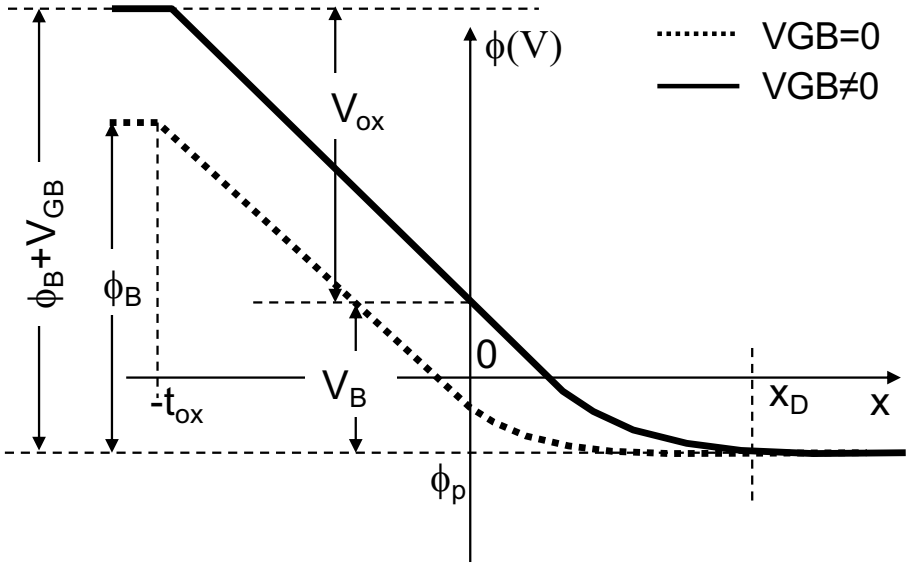
- Potential difference appears across SiO_2 and space-charge region in SC
- SiO_2 is an insulator so no current flows even under bias.
- VGB≠0 modulates the SCR leading to a charge redistribution
- No current flow, thermal equilibrium equation for free carrier densities in SCR still holds: $np=n_i^2$

MOS under bias (3)



$V_{GB} > 0$: potential difference across structure increases ⇒ need larger charge dipole ⇒ SCR expands into semiconductor substrate

MOS under bias (4)



- VGB>0
- SCR expands
- Gate attracts electrons and repels holes
- Qualitatively, physics unchanged

$$\phi_B \rightarrow \phi_B + V_{GB}$$

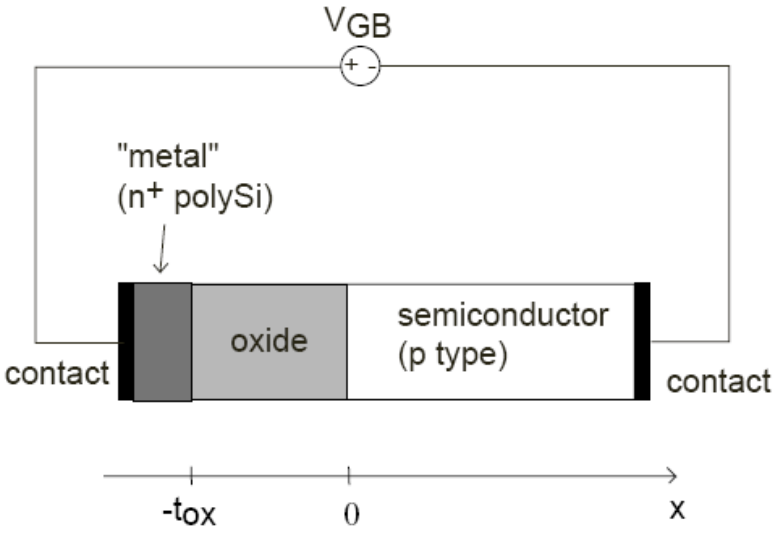
$$x_D(V_{GB}) = \frac{\epsilon_{sc}}{C_{ox}} \left[\sqrt{1 + \frac{4\,(\phi_B + V_{GB})}{\gamma^2}} - 1 \right]$$

$$V_{GB} \uparrow \rightarrow \; x_d \uparrow$$

Overview

- **MOS electrostatics under bias**
  - Depletion regime
  - Flatband
  - Accumulation regime
  - Threshold
  - Inversion regime
- **MOSFET: cross-section, layout, symbols**
- **Qualitative operation**
- **Basic I-V characteristics**

Overview of MOS electrostatics



Quasi-equilibrium situation with potential build up across MOS equal to $\varphi_B + V_{GB}$

Important consequences of quasi-equilibrium:

$$n(x) = n_i e^{q\phi(x)/kT}$$

$$p(x) = n_i e^{-q\phi(x)/kT}$$

$$np = n_i^2 \text{ at every } x$$

not the case in p-n junction or BJT under bias

- built-in potential across MOS structure increases from ϕ_B to $\phi_B + V_{GB}$
- oxide forbids current flow: J=0 in semiconductor

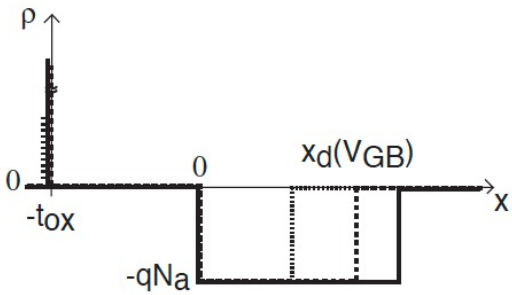
must maintain boundary condition at Si/SIO_2 interface: E_{ox}/E_s ~3

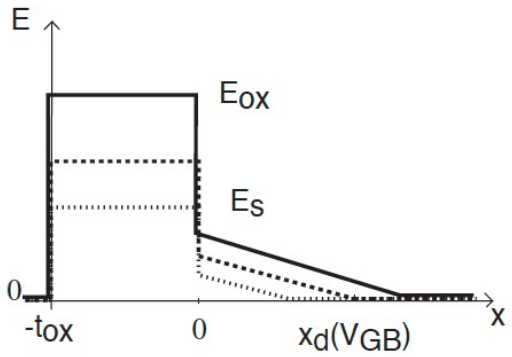
Depletion regime (1)

- For V_{GB}> 0 gate ”attracts” electrons, ”repels” holes ⇒ depletion region widens

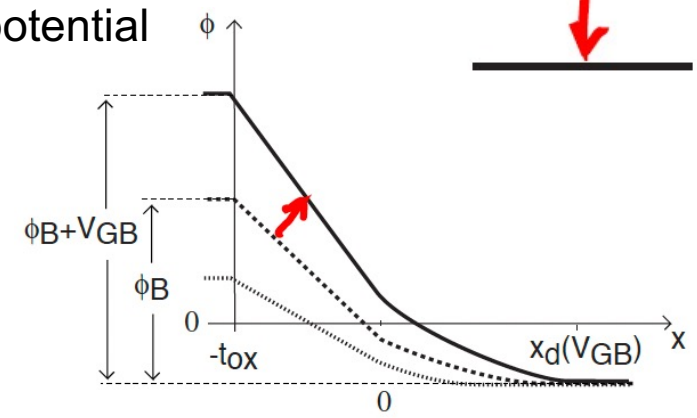
- For V_{GB}< 0 gate ”repels” electrons, ”attracts” holes ⇒ depletion region shrinks

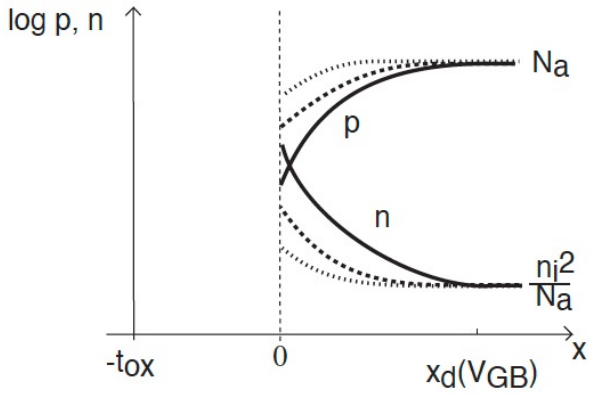
Charge and electric field

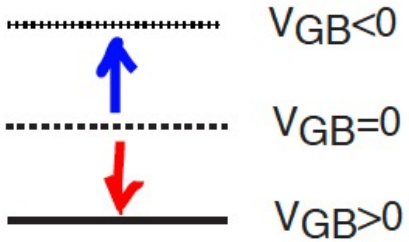




potential







Depletion regime (2)

Depletion regime, all results obtained for zero bias apply if:

$\varphi_B \rightarrow \varphi_B + V_{GB}$

- Depletion width:

$$x_d(V_{GB}) = \frac{\epsilon_s}{C_{ox}}\left[\sqrt{1 + \frac{4(\phi_B + V_{GB})}{\gamma^2}} - 1\right]$$

- Potential drop across semiconductor SCR:

$$V_B(V_{GB}) = \frac{qN_a x_d^2(V_{GB})}{2\epsilon_s}$$

- Potential drop across oxide:

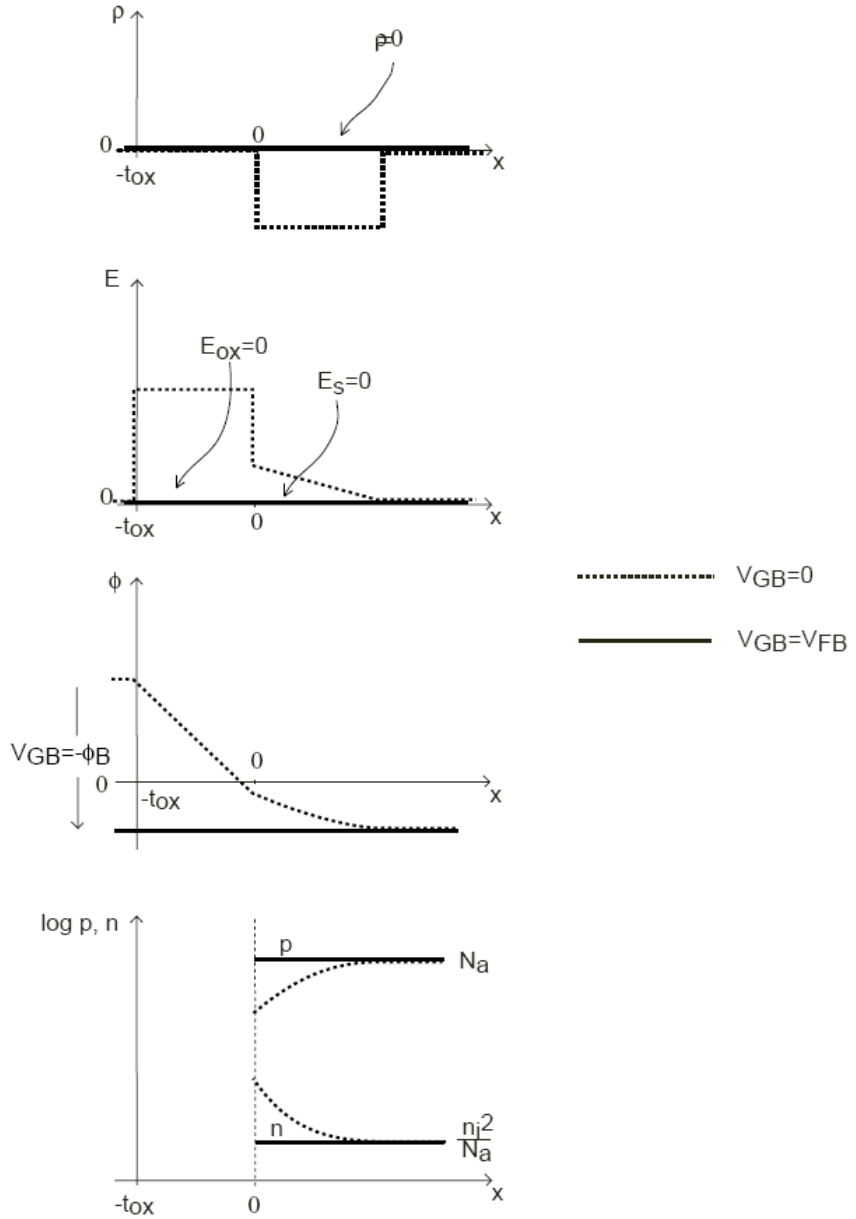
$$V_{ox}(V_{GB}) = \frac{qN_a x_d(V_{GB}) t_{ox}}{\epsilon_{ox}}$$

Flatband regime

At a certain **negative V_{GB}**, depletion region is wiped out:

→ **Flatband voltage**

$$V_{FB} = -\phi_B$$



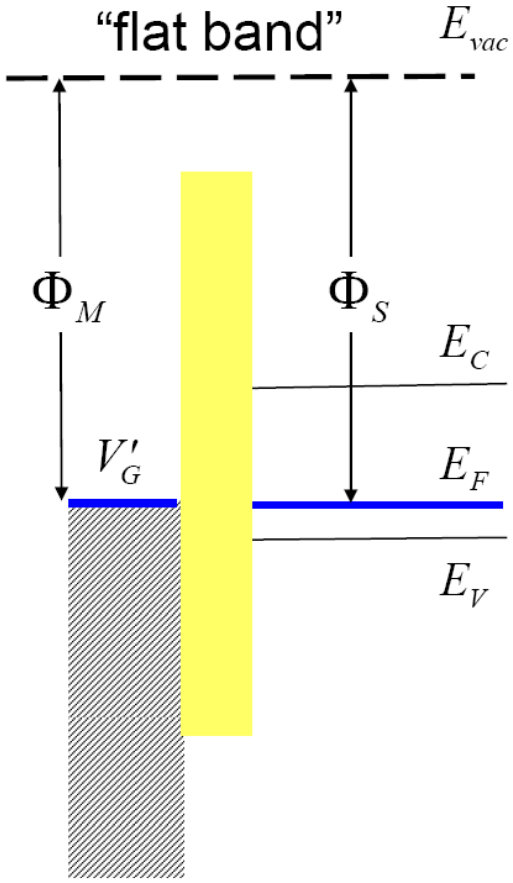
Flatband regime: bands!

- when the gate electrode Fermi level lines up with the semiconductor Fermi level, the bands are flat in the semiconductor

- this occurs at $V'_G = 0$ when the gate electrode workfunction equals the semiconductor workfunction

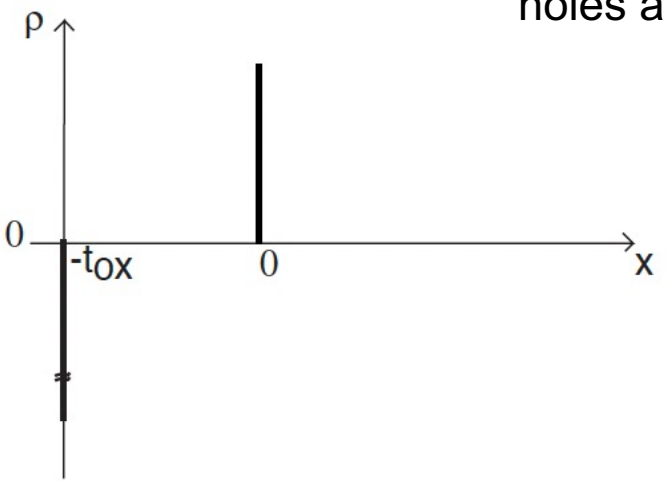
$$\Phi_M = \Phi_S \quad \text{eV}$$

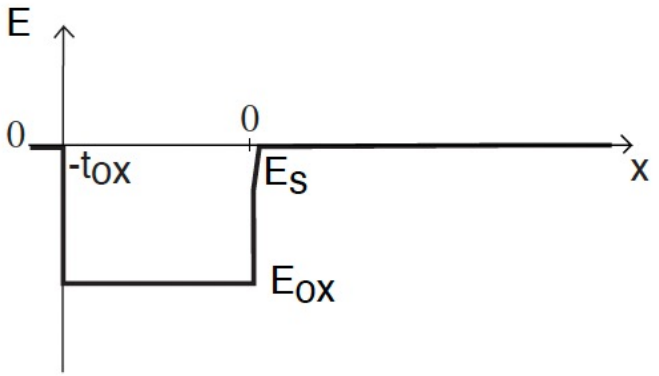
$$\phi_M = \phi_S \quad \text{V}$$

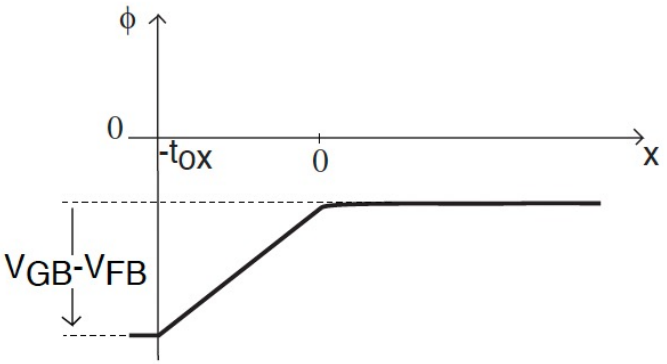


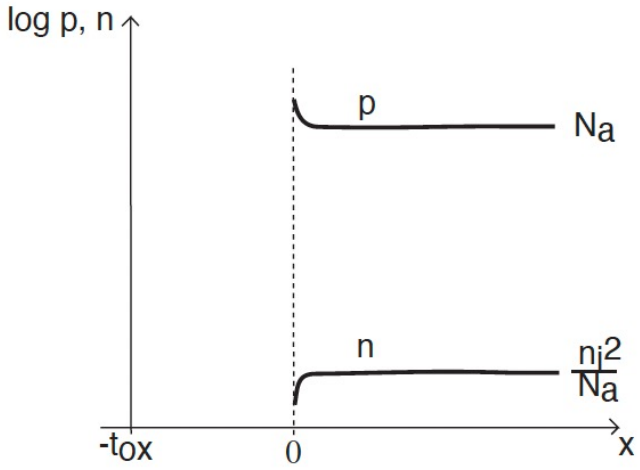
Accumulation regime

• If $V_{GB} < V_{FB}$ **accumulation** of holes at Si/SiO_2 interface







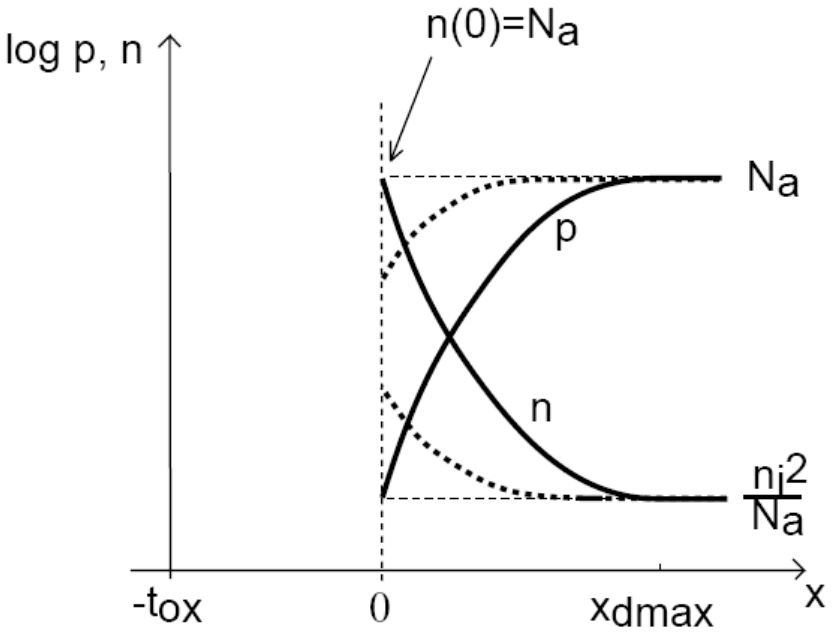


Threshold voltage (1) – turn again to the case $V_{GB}>0$

- For sufficiently large VGB> 0, electrostatics change when

$n(0) = N_a \Rightarrow$ threshold.

- Beyond threshold, cannot neglect contributions of electrons towards electrostatics.



What is the V_G that leads to n(0) = Na? Will call it threshold voltage, V_T!

Threshold voltage (2)

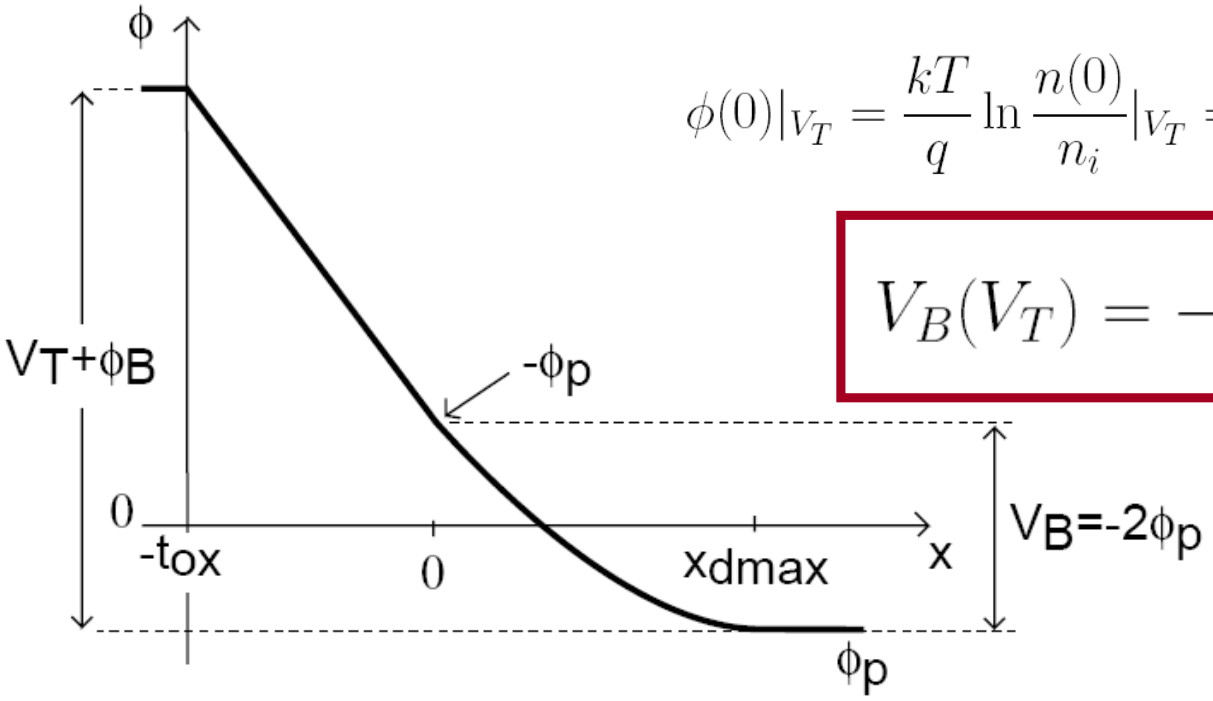
Calculation of threshold voltage

- potential drop in semiconductor at threshold:

$$n(0) = n_i e^{q\phi(0)/kT}$$

$$\phi(0)|_{V_T} = \frac{kT}{q} \ln \frac{n(0)}{n_i}|_{V_T} = \frac{kT}{q} \ln \frac{N_a}{n_i} = -\phi_p$$

$$V_B(V_T) = -2\phi_p$$



Threshold voltage (3)

- potential drop in oxide at threshold:

Obtain xd(VT) using relationship between VB and xd in depletion:

$$V_B(V_T) = \frac{qN_a x_d^2(V_T)}{2\epsilon_s} = -2\phi_p$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \left[\frac{F}{m^2}\right]$$

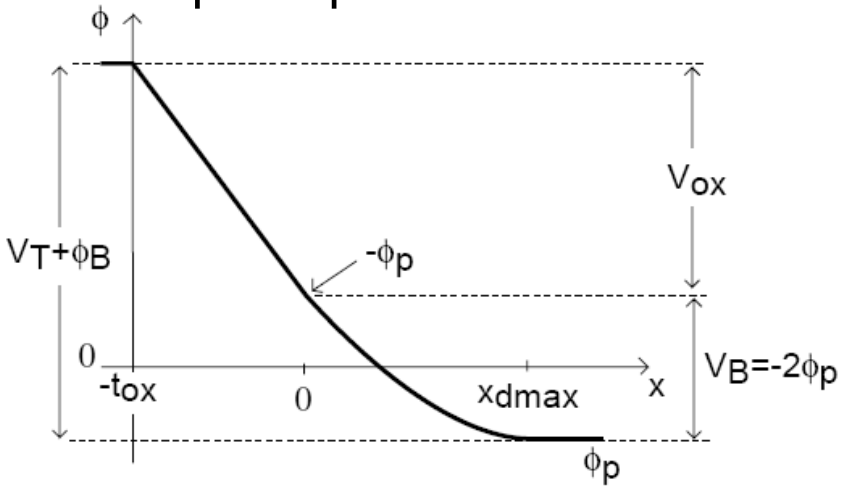
$$x_d(V_T) = x_{dmax} = \sqrt{\frac{2\epsilon_s(-2\phi_p)}{qN_a}}$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\,\epsilon_{sc}\,q\,N_A} \left[V^{\frac{1}{2}}\right]$$

$$V_{ox}(V_T) = E_{ox}(V_T)t_{ox} = \frac{qN_a x_d(V_T)}{\epsilon_{ox}}t_{ox} = \gamma\sqrt{-2\phi_p}$$

Threshold voltage (4)

- Sum up the potentials across the structure



$$V_T + \phi_B = V_B(V_T) + V_{ox}(V_T) = -2\phi_p + \gamma\sqrt{-2\phi_p}$$

$$\boxed{V_T = V_{FB} - 2\phi_p + \gamma\sqrt{-2\phi_p}}$$

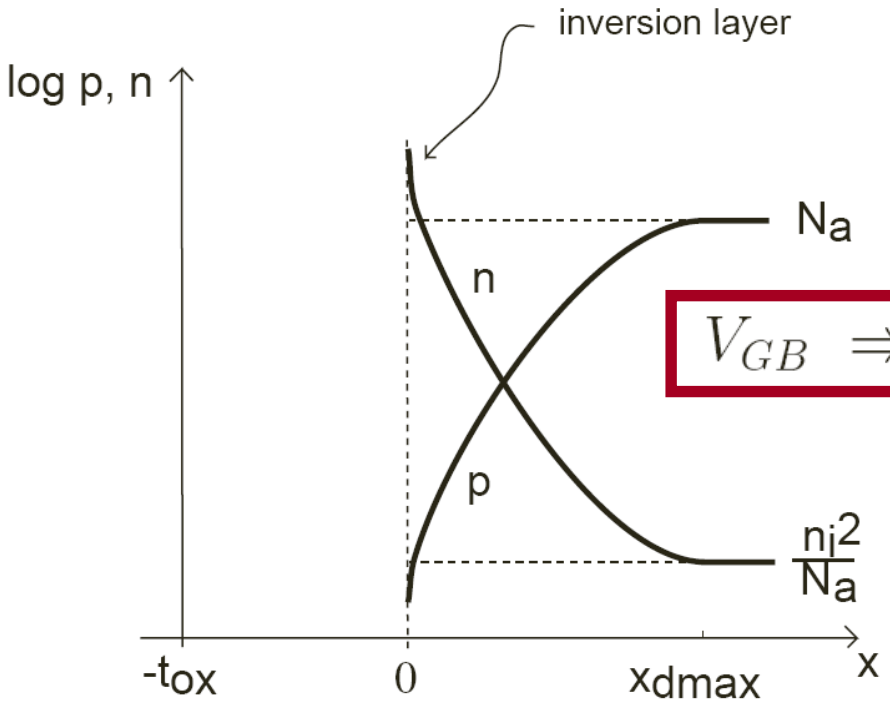
$$\text{If } N_a \uparrow \rightarrow \ V_T \uparrow$$

$$\text{If } C_{ox} \uparrow \ (t_{ox} \downarrow) \rightarrow \ V_T \downarrow$$

- The higher the doping level, the more voltage required
- The thinner the oxide, the less voltage dropped across it

Inversion regime (1)

- What happens for $V_{GB} > V_T$?
- More electrons at Si/SiO_2 interface than acceptors - *inversion*.

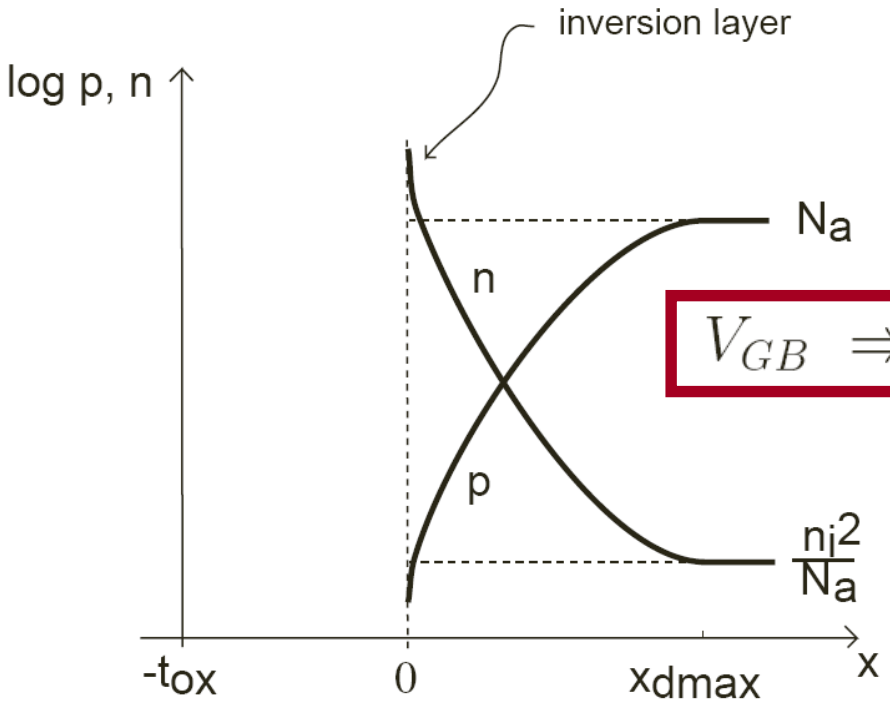


- Electron concentration at Si/SiO2 interface modulated by:

$$V_{GB} \Rightarrow V_{GB} \uparrow \rightarrow n(0) \uparrow \rightarrow |Q_n| \uparrow$$

Strong inversion regime (1)

- What happens for $V_{GB} > V_T$?
- More electrons at Si/SiO_2 interface than acceptors inversion.



- Electron concentration at Si/SiO2 interface modulated by:

$$V_{GB} \Rightarrow V_{GB} \uparrow \rightarrow n(0) \uparrow \rightarrow |Q_n| \uparrow$$

field-effect control of mobile charge!(essence of MOSFET)

Inversion regime – key observations

- Want to compute Qn vs. V_{GB}
- Make sheet charge approximation: electron layer at semiconductor surface is much thinner than any other dimension in problem (t_{ox}, x_d)

V_B does not increase much beyond $V_B(V_T) = -2\phi_p$ (*a thin sheet of electrons does not contribute much to* V_B)

$$|Q_n| \propto n(0) \propto e^{q\phi(0)/kT}$$

$$|Q_B| \propto \sqrt{\phi(0)}$$

← Changes a lot with V_{GB}

Charge in depletion layer changes very little for $V_{GB} > V_T$

x_d does not increase much beyond threshold:

$$x_d(inv.) \simeq x_d(V_T) = \sqrt{\frac{2\epsilon_s(-2\phi_p)}{qN_a}} = x_{dmax}$$

Inversion regime - capacitance

All extra voltage beyond V_T used to increase inversion charge Qn. Think of it as capacitor:

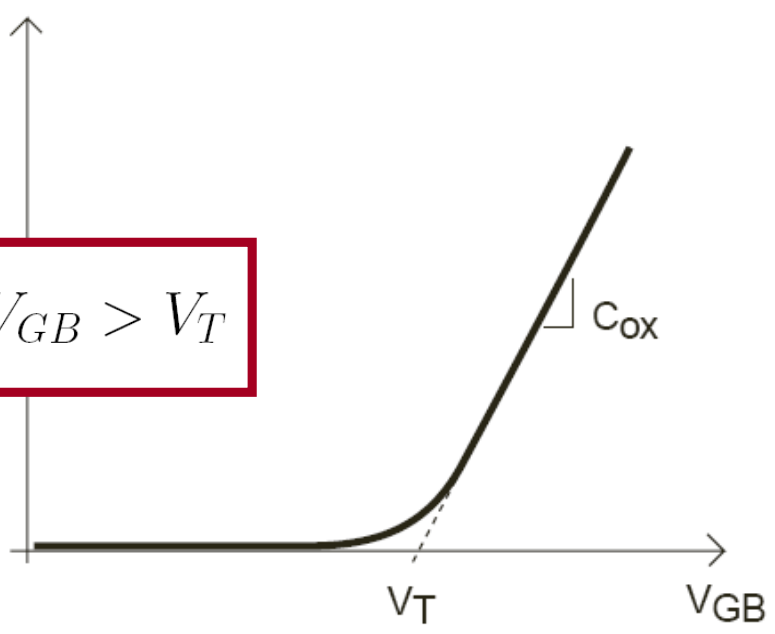
– top plate: metal gate

– bottom plate: inversion layer

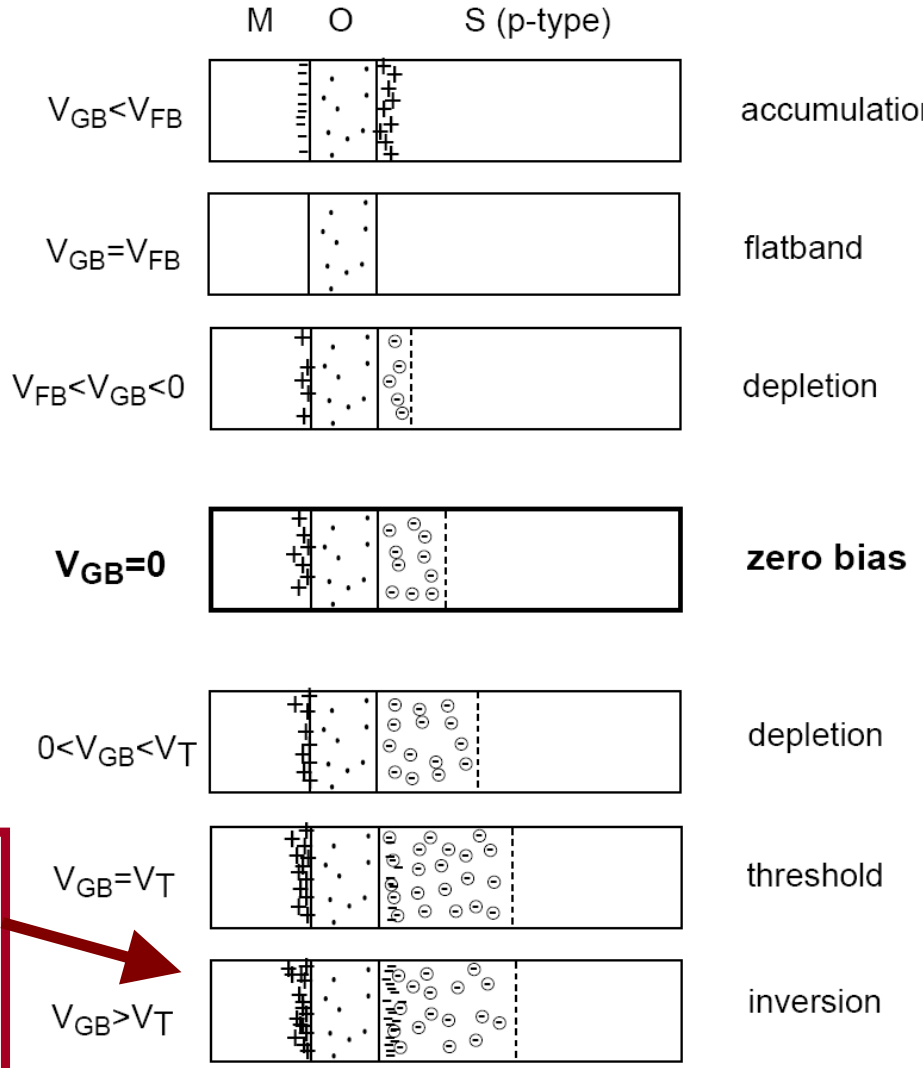
Q= CV

Inversion charge (electrons):

$$Q_n = -C_{ox}(V_{GB} - V_T) \quad \text{for } V_{GB} > V_T$$



Key conclusions: different operation regimes of MOS structure



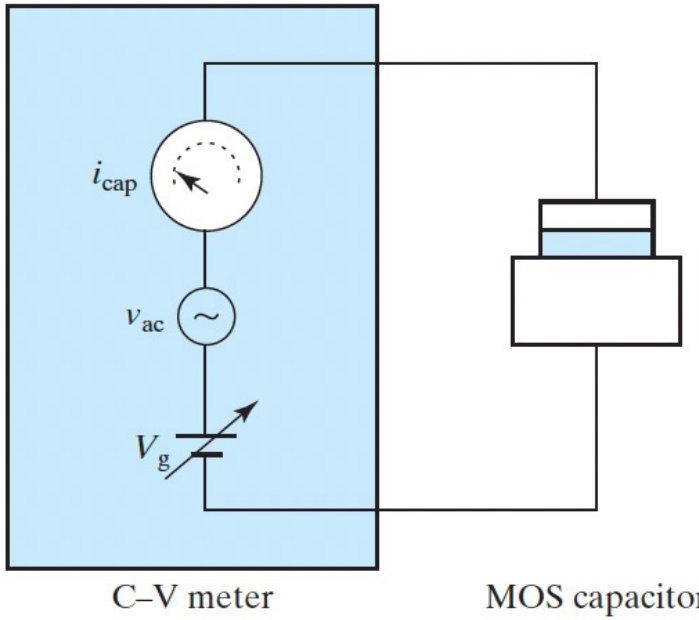
Inversion charge

Strong inversion:

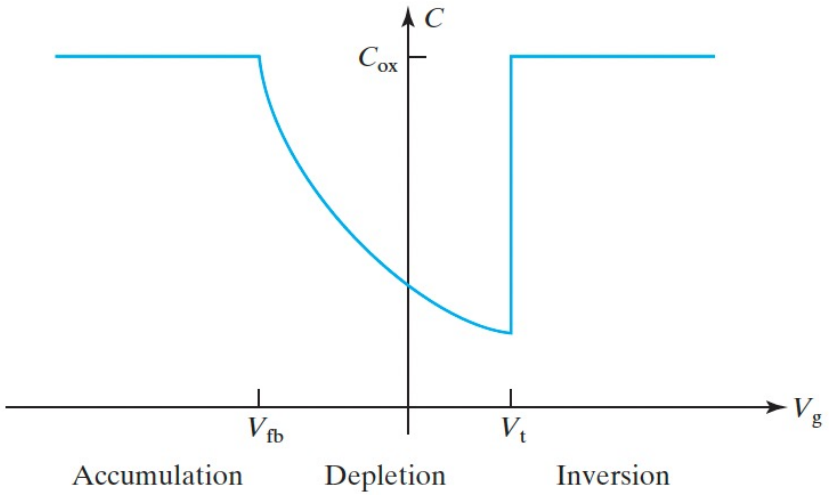
$$|Q_n| = C_{ox}(V_{GB} - V_T)$$
$$\text{for } V_{GB} > V_T$$

MOSFET capacitance

Setup for capacitance measurements



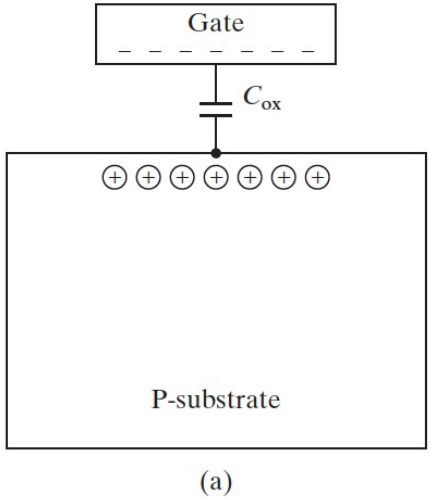
Quasistatic C-V Curve



CV - a powerful characterization techniques (thickness of oxide and other important parameters)

MOSFET capacitance

Accumulation



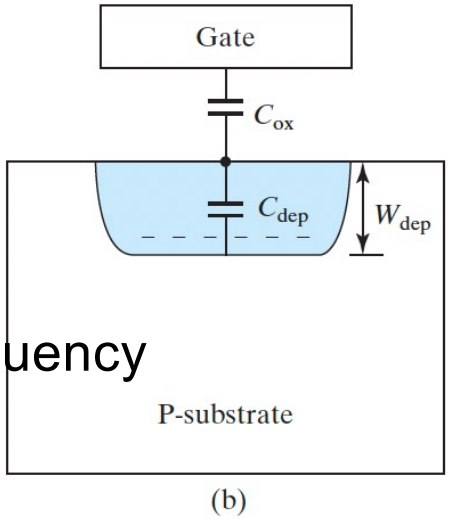
Capacitors of oxide layer and semiconductor in series:

$$C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$

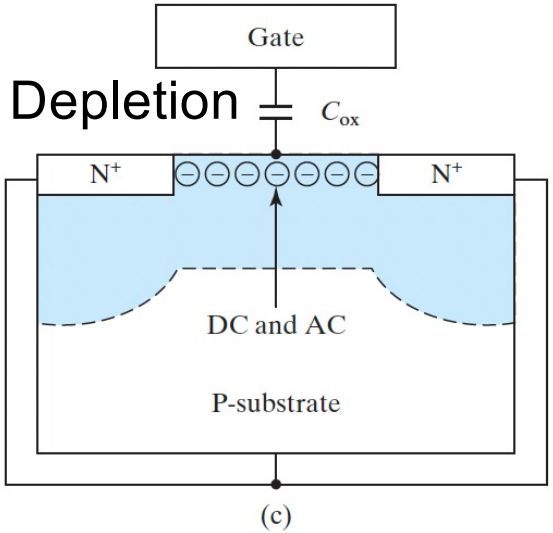
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^{\,2}} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}}$$

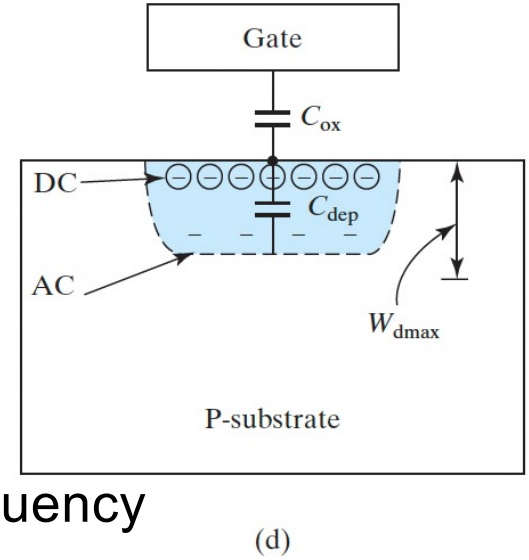
Inversion
High-frequency



Depletion

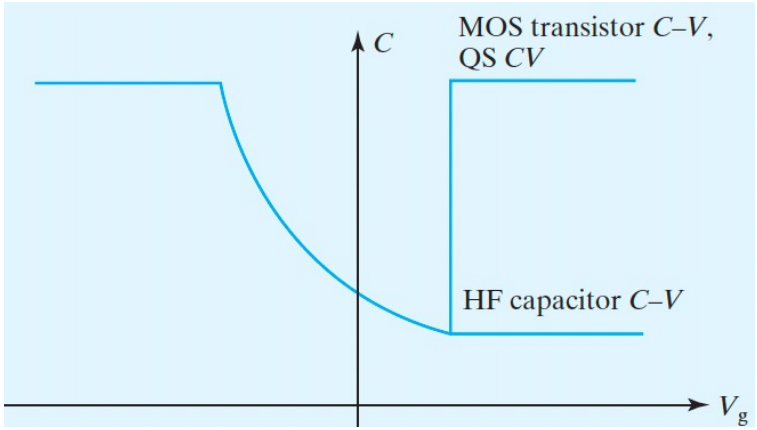


Inversion
Low -frequency

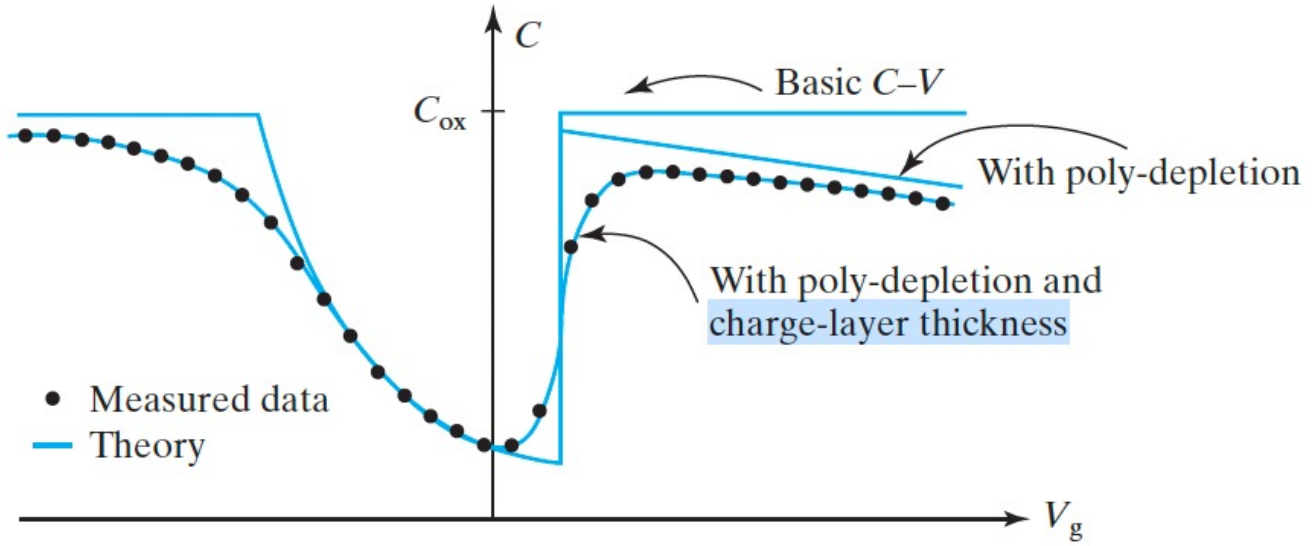


MOSFET Capacitance: simple theory vs real measurements

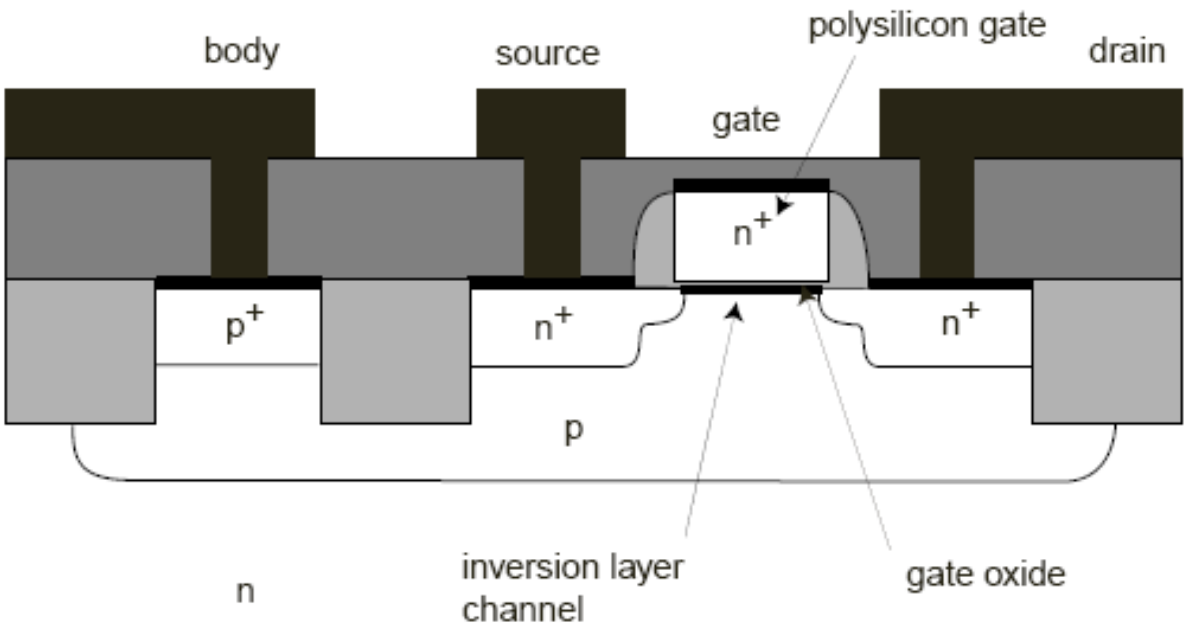
C-V: theory: quasistatic vs Hi-Freq.



Quasistatic C-V: theory vs measurements



Classic MOSFET: cross-section

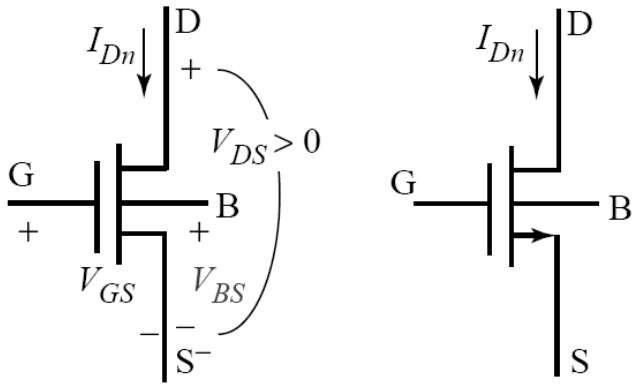


Key elements:

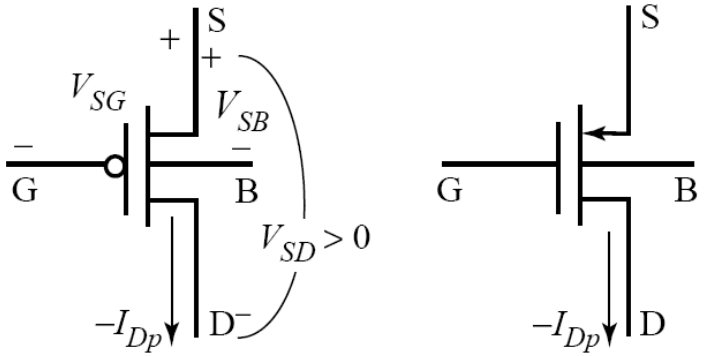
- inversion layer under gate (depending on gate voltage)
- heavily-doped regions reach underneath gate) inversion layer electrically connects source and drain
- 4-terminal device: body voltage important

MOSFET: (circuit) symbols

n-channel device (n-MOSFET) on p-Si substrate (uses electron inversion layer)



p-channel device (p-MOSFET) on n-Si substrate(uses hole inversion layer)



- sometimes the body contact is not figured

Summary

- Charge redistribution in MOS structure at zero bias:
- SCR in semiconductor
- built-in potential across MOS structure.
- In most cases, the depletion approximation in semiconductor SCR is valid.
- Application of voltage modulates depletion region width in semiconductor. No current flows.

Summary

- Operation regimes for MOS structures
  - accumulation
  - flat band
  - depletion
  - inversion
- C-V of MOS – a useful tool for analysis of the structure
- C-V of MOS in the inversion regime is strongly frequency-dependent – it depends on the ability of minority carriers to follow the ac signal