Lecture 4
Microelectronic Devices

pn junctions and diodes : lectures 4-5

- pn junction under bias
- Depletion capacitance
- reverse-biased pn-junction
- pn-junction: breakdown mechanisms

Comments for the exercise: Series2/ex4

We consider a p-type silicon sample doped with boron at a concentration of $N_A = 10^{16}\,[cm^{-3}]$. The energy difference between the valence level E_v and the acceptor ionization level E_A is $E_a = 45\,[meV]$. The impurity level degeneracy factor is $\beta_a = 4$ in this case.

Find the temperature where 90% of dopants are ionized

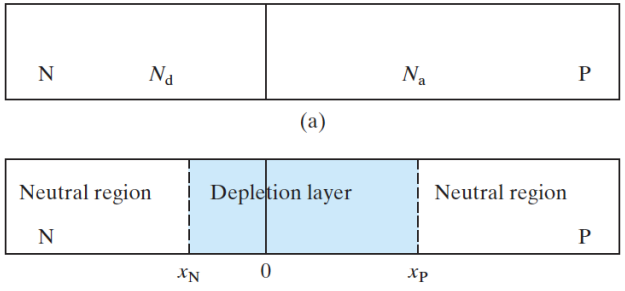
- Typically in this situation $\frac{N_A - N_A^-}{N_A}$, approximated with $\beta_a N_A \cdot e^{-\frac{E_f - E_A}{kT}}$
- difficulty - E_F is unknown!
- typically we determine from the hole concentration $E_F - E_v = kT \cdot \ln(N_v/p)$
- difficulty - ***T*** is unknown!

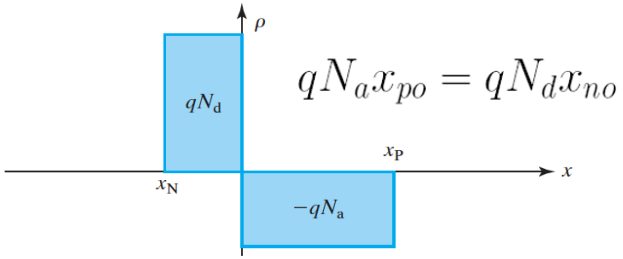
- Solution: cancel out the Fermi level: $p_0 + N_A - N_A^- \approx N_A \rightarrow \frac{N_A - N_A^-}{p_0 + N_A - N_A^-} = 0.1$

$$\frac{\beta_a N_A \cdot e^{-\frac{E_f - E_A}{kT}}}{N_v(T) \cdot e^{-\frac{E_f - E_v}{kT}} + \beta_a N_A \cdot e^{-\frac{E_f - E_A}{kT}}} \rightarrow \boxed{\frac{N_A - N_A^-}{p_0 + N_A - N_A^-} = \frac{1}{\frac{N_v(T)}{\beta_a N_A} \cdot e^{-\frac{E_A - E_v}{kT}} + 1} = 0.1}$$

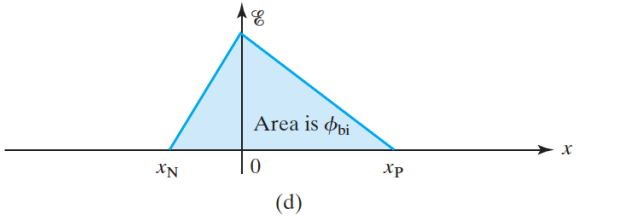
Can be solved!

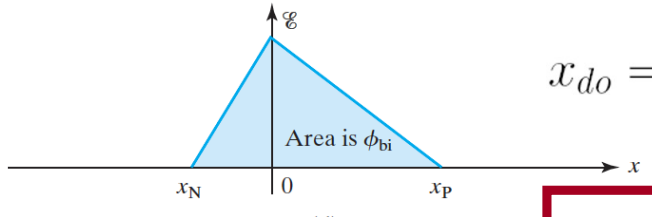
pn junction: depletion regions, built-in field and potential profile



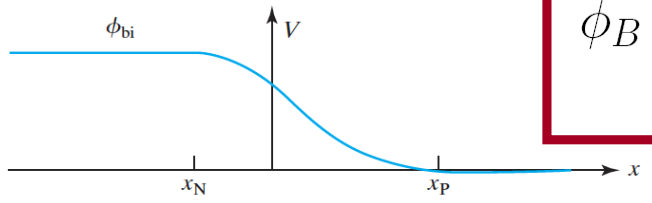


$$qN_a x_{po} = qN_d x_{no}$$

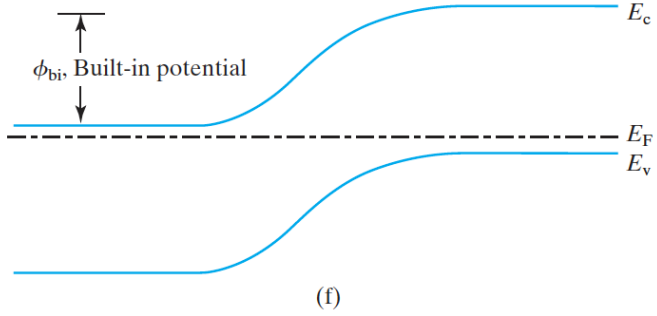




$$x_{do} = x_{no} + x_{po} = \sqrt{\frac{2\epsilon_s \phi_B (N_a + N_d)}{qN_a N_d}}$$



$$\phi_B = \phi_n - \phi_p = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$



pn junction (with no applied bias): numerical example

A p^+n junction has $N_A = 10^{20}\ cm^{-3}$ and $N_D = 10^{17} cm^{-3}$. What is a) its built in potential, b) W, c) x_n, and d) x_p ?

$$\phi_{bi} = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2} \approx 0.026\ \text{V} \ln \frac{10^{20} \times 10^{17} \text{cm}^{-6}}{10^{20} \text{cm}^{-6}} \approx 1\ \text{V}$$

$$W_{dep} \approx \sqrt{\frac{2\varepsilon_s \phi_{bi}}{qN_d}} = \left(\frac{2 \times 12 \times 8.85 \times 10^{-14} \times 1}{1.6 \times 10^{-19} \times 10^{17}} \right)^{1/2}$$

$$= 1.2 \times 10^{-5} \text{cm} = 0.12\ \mu\text{m} = 120\ \text{nm} = 1200\ \text{Å}$$

$$|x_P| = |x_N| N_d / N_a = 0.12\ \mu\text{m} \times 10^{17} \text{cm}^{-3} / 10^{20} \text{cm}^{-3} = 1.2 \times 10^{-4}\ \mu\text{m}$$

$$= 1.2\ \text{Å} \approx 0$$

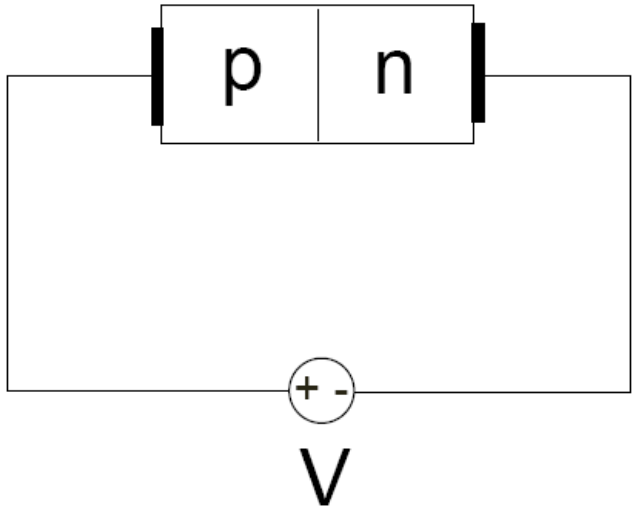
It is useful to remember that $W_{dep} \approx 0.1\ \mu m$ for $N = 10^{17}\ cm^{-3}$

What happens if voltage is applied to a pn junction?

- electrostatics of a pn junction if a voltage is applied across its terminals
- Why does a pn junction behave in some way like a capacitor?

Introduction to pn junction

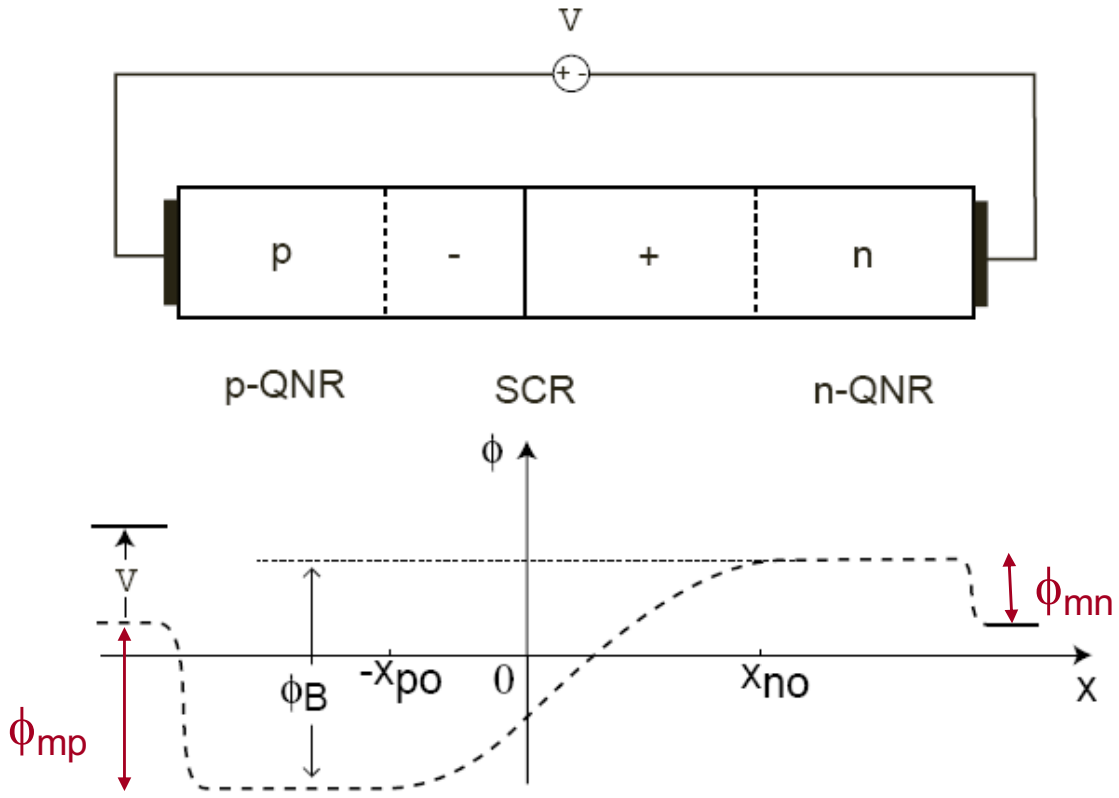
Convention for pn junction bias:



- $V > 0$ called **forward bias (polarisation directe)**
- $V < 0$ called **reverse bias (polarisation inverse)**

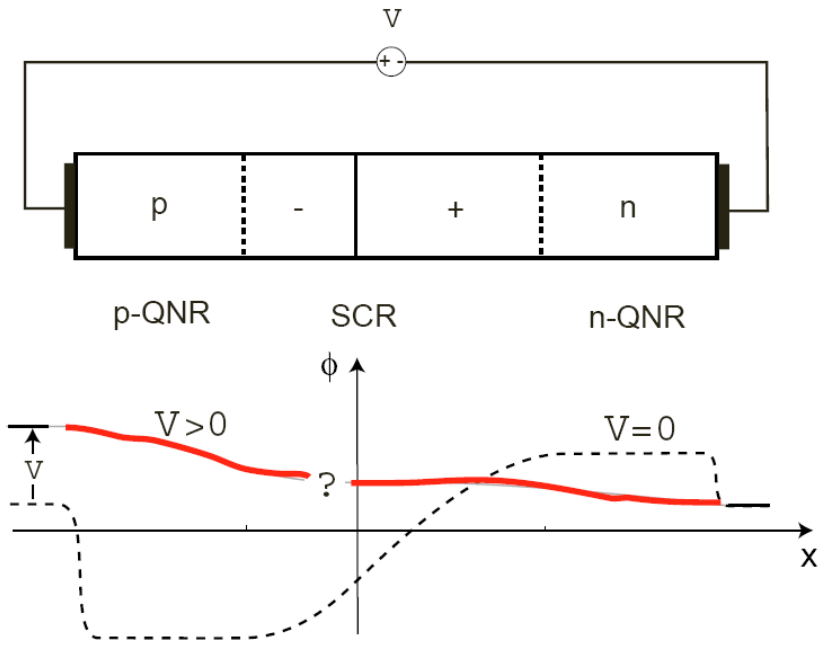
pn junction: forward bias (1)

Positive voltage applied to p-side with respect to n-side: what's the effect of applying a V forward bias?



pn junction: forward bias (2)

How does potential distribution inside junction change as a result of bias? Where V drops the most?

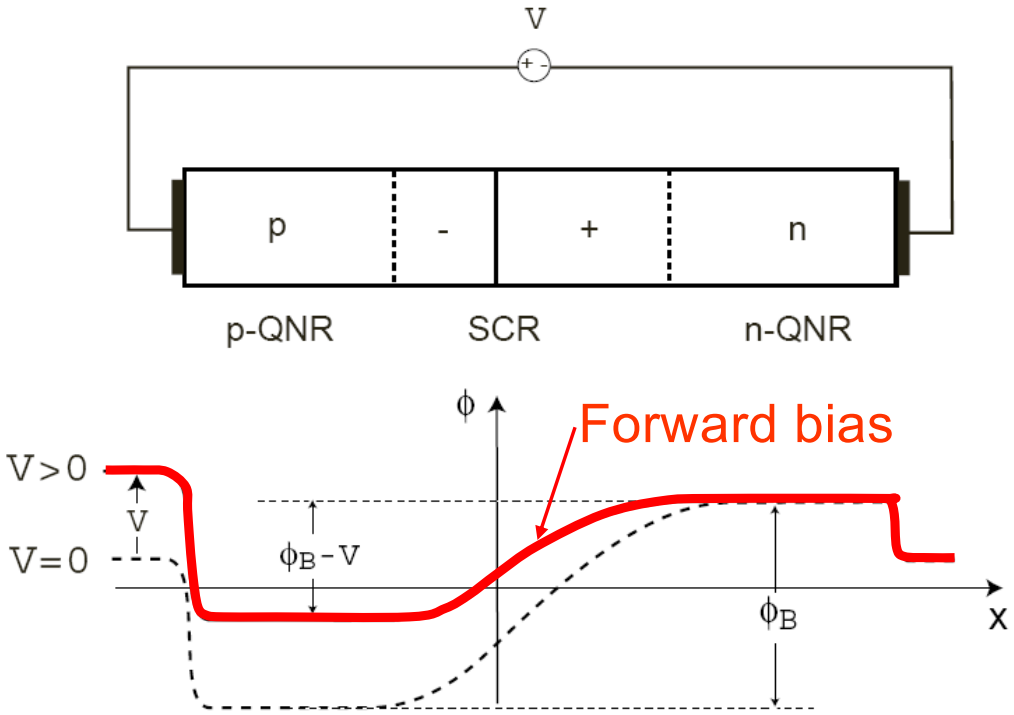


How V is distributed across:

- metal/p-QNR contact?
- p-QNR?
- SCR?
- n-QNR?
- metal/n-QNR contact?

pn junction: forward bias (3)

Answer: essentially all the voltage drops across the space charge region (SCR)



The potential across the junction (potential barrier) is:

- in equilibrium (no bias) :

$$\phi_B$$

- @ forward bias:

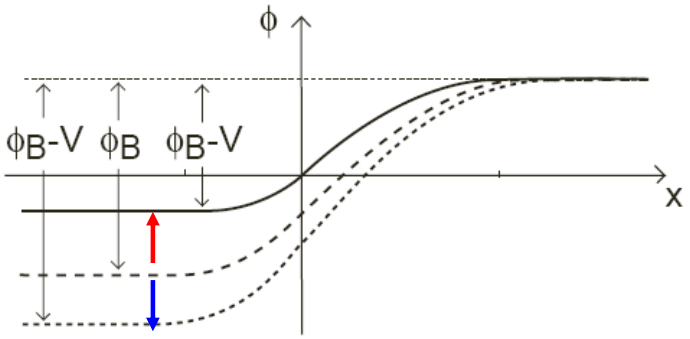
$$\phi_B - V < \phi_B \qquad V>0$$

- @ reverse bias:

$$\phi_B - V > \phi_B \qquad V<0$$

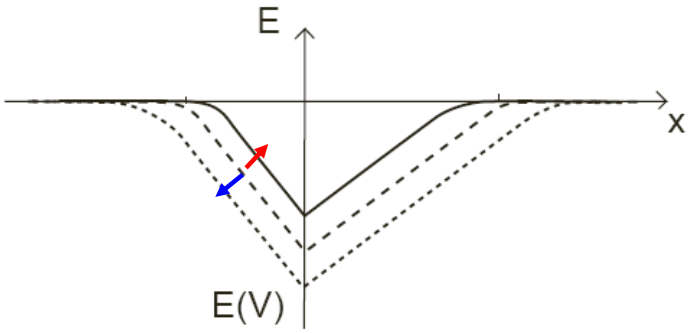
SCR electrostatics (1)

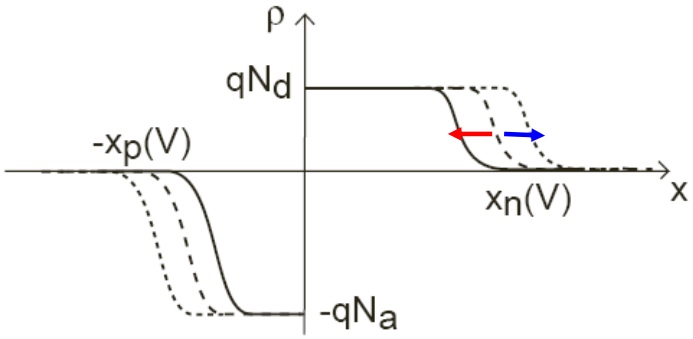
Forward bias — V>0
0-bias — V=0
Reverse bias — V<0



Main effects

- forward bias:
  - *Built-in potential decreases*
  - *Electrical field decreases*
  - *Depletion width decreases*
- reverse bias:
  - *Built-in potential increases*
  - *Electrical field increases*
  - *Depletion width increases*





SCR electrostatics (2)

Analytical formulation of electrostatics of SCR identical to that of thermal equilibrium with:

$$\phi_B \longrightarrow \phi_B - V$$

$$x_n(V) = \sqrt{\frac{2\epsilon_s(\phi_B - V)N_a}{q(N_a + N_d)N_d}} \qquad x_p(V) = \sqrt{\frac{2\epsilon_s(\phi_B - V)N_d}{q(N_a + N_d)N_a}}$$

Other results that can be derived:

$$x_d(V) = \sqrt{\frac{2\epsilon_s(\phi_B - V)(N_a + N_d)}{qN_aN_d}}$$

$$|E|(V) = \sqrt{\frac{2q(\phi_B - V)N_aN_d}{\epsilon_s(N_a + N_d)}}$$

SCR electrostatics (2) simplified formulas

$$x_d(V) = \sqrt{\frac{2\epsilon_s(\phi_B - V)(N_a + N_d)}{qN_aN_d}}$$

$$|E|(V) = \sqrt{\frac{2q(\phi_B - V)N_aN_d}{\epsilon_s(N_a + N_d)}}$$

$$x_n(V) = x_{no}\sqrt{1 - \frac{V}{\phi_B}}$$

$$x_p(V) = x_{po}\sqrt{1 - \frac{V}{\phi_B}}$$

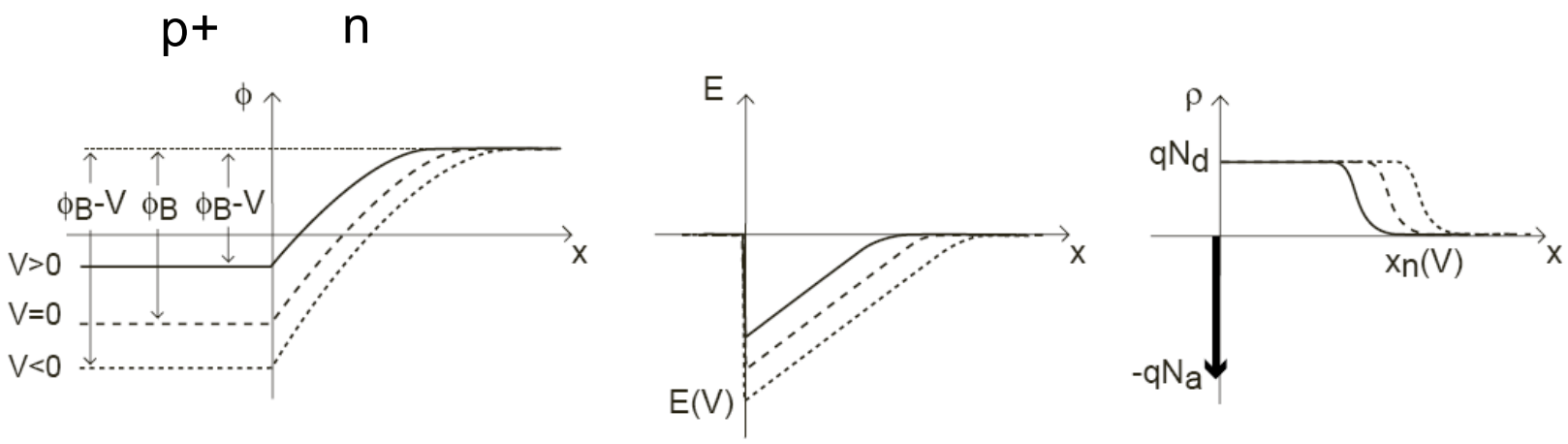
Rules of square root:

$$x_d(V) = x_{do}\sqrt{1 - \frac{V}{\phi_B}}$$

$$|E|(V) = |E_o|\sqrt{1 - \frac{V}{\phi_B}}$$

Case of strongly asymmetric junctions: p+n

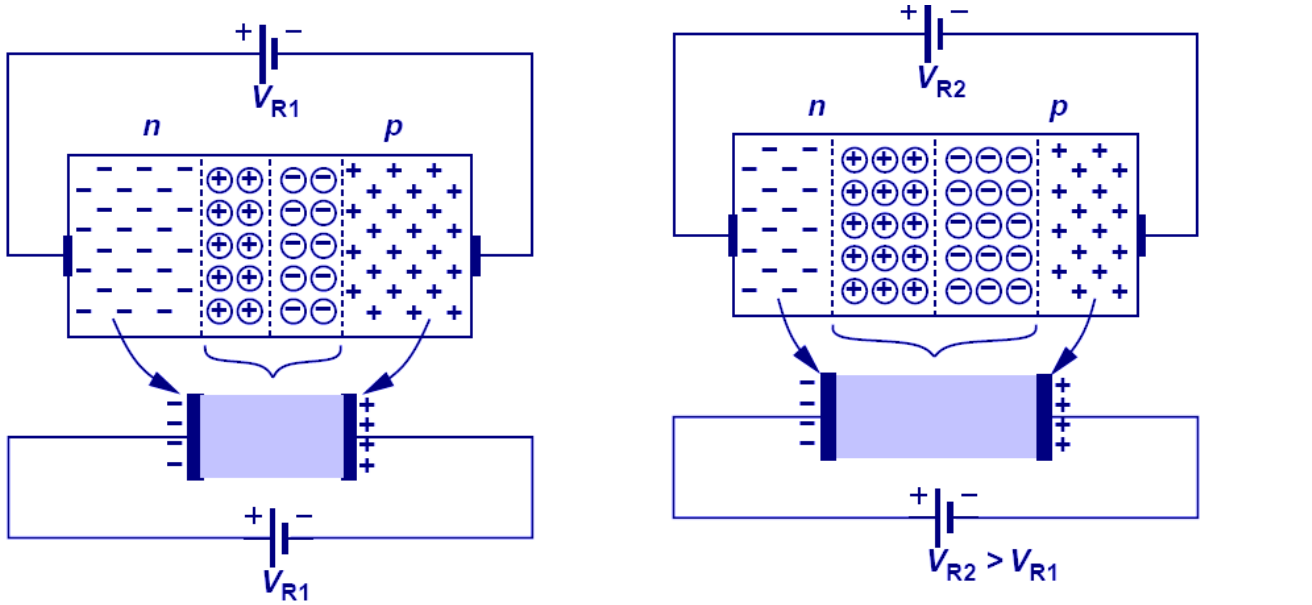
All changes take place in lowly doped side!



$$x_n(V) = x_{no}\sqrt{1 - \frac{V}{\phi_B}}$$

PN Junction Small-Signal Capacitance

- A reverse-biased PN junction can be viewed as a capacitor, for incremental changes in applied voltage.



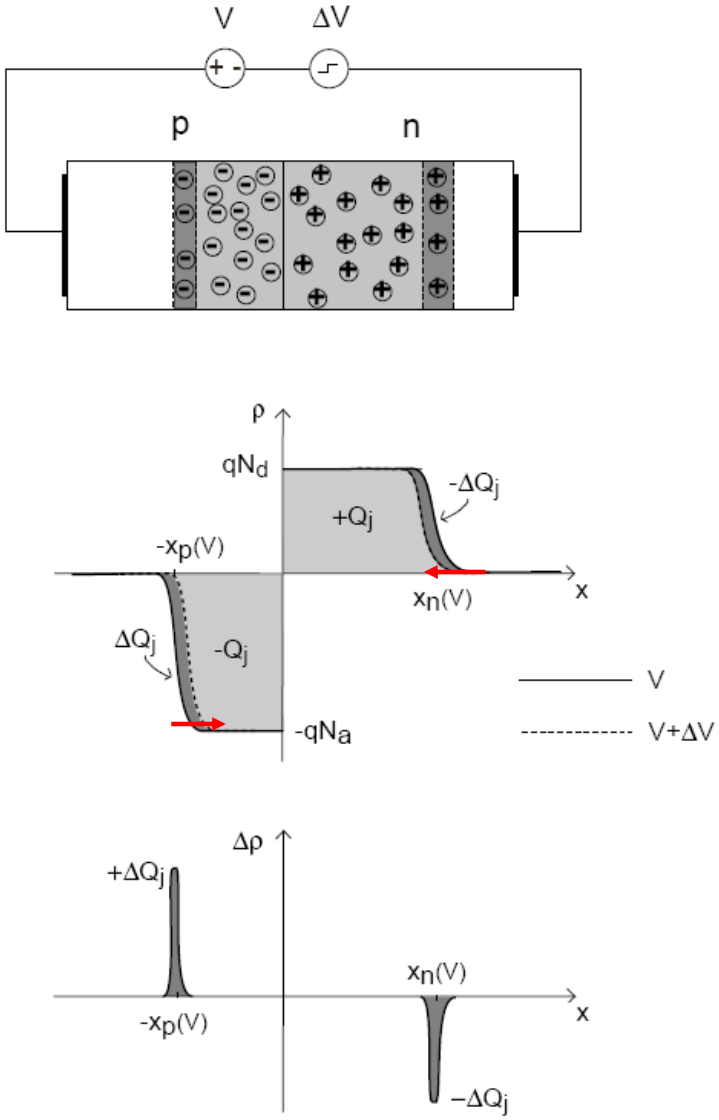
$$C_j = \frac{\varepsilon_{si}}{W_{dep}}$$

Disambiguation: here we follow the notation used in most of textbooks, where C_j stands for capacitance density rather than capacitance. To calculate the final capacitance value one should multiply it by the area: S x C_j

Depletion capacitance (1)

• Suppose a small signal, $\Delta V>0$ is applied on top of DC bias:

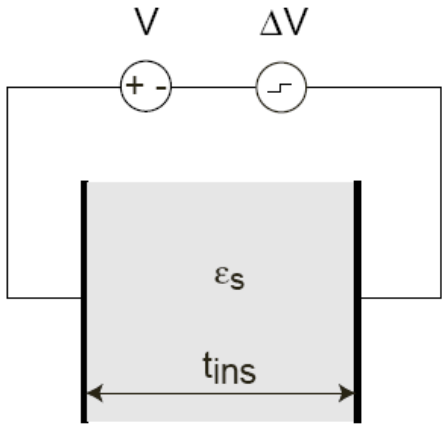
$$\Rightarrow \text{change of } \Delta Q_j \text{ at } -x_p$$
$$\Rightarrow \text{change of } -\Delta Q_j \text{ at } x_n$$



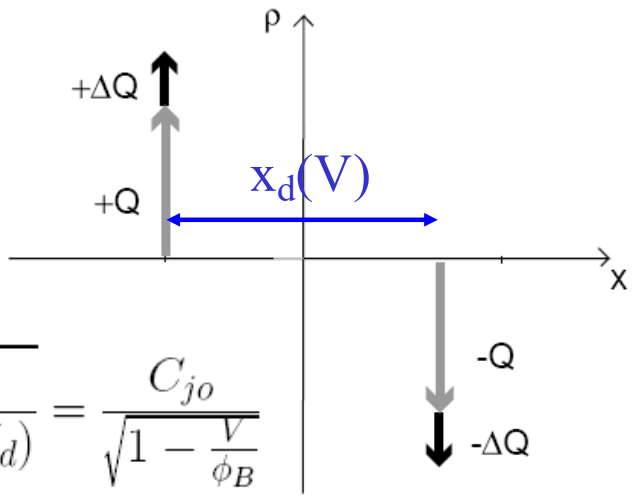
Depletion capacitance (2)

Analogy with a plate capacitor with capacity per unit of area:

$$C = \frac{\epsilon_s}{t_{ins}}$$



$$x_d(V) = \sqrt{\frac{2\epsilon_s(\phi_B - V)(N_a + N_d)}{qN_aN_d}}$$



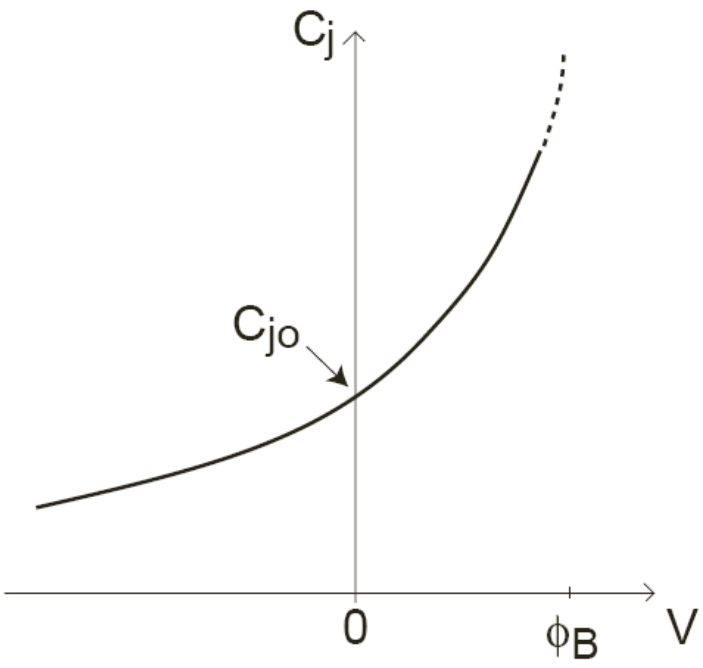
Depletion capacitance is:

$$C_j(V) = \frac{\epsilon_s}{x_d(V)} = \sqrt{\frac{q\epsilon_s N_a N_d}{2(\phi_B - V)(N_a + N_d)}} = \frac{C_{jo}}{\sqrt{1 - \frac{V}{\phi_B}}}$$

where C_{j0} is C_j at $V=0$

Depletion capacitance (3)

$$C_j(V) = \frac{\epsilon_s}{x_d(V)} = \sqrt{\frac{q\epsilon_s N_a N_d}{2(\phi_B - V)(N_a + N_d)}} = \frac{C_{jo}}{\sqrt{1 - \frac{V}{\phi_B}}}$$



C_j depends on:

- bias, V
- doping, N_A, N_D
- in strongly asymmetric junction (i.e. p+n) is dominated by the low doped part:

$$C_j(V) \simeq \sqrt{\frac{q\epsilon_s N_d}{2(\phi_B - V)}}$$

Why capacitance-voltage characteristics of p-n junction are important?

- pn diode= variable capacitor (varicaps, *varactors*):

⇒ useful for *voltage-controlled oscillators, other applications where tunable capacitance is useful*

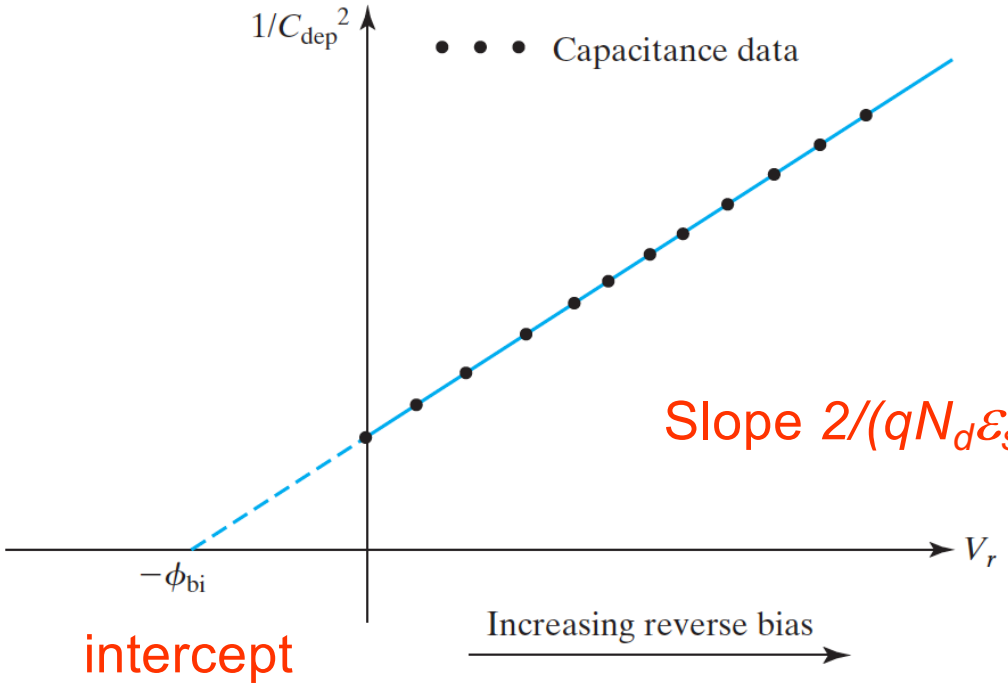
- C_j: important consideration in dynamics of pn diode

- powerful characterization technique:

i.e. $1/C_j^2$ *vs.* V yields ϕ_B and N_d in asymmetric p^+-n junctions

Depletion capacitance (4)

Plot of $1/C_j^2$ *vs.* *V known* *as* the Mott–Schottky plot yields ϕ_B and N_d in strongly asymmetric p^+-n junction:

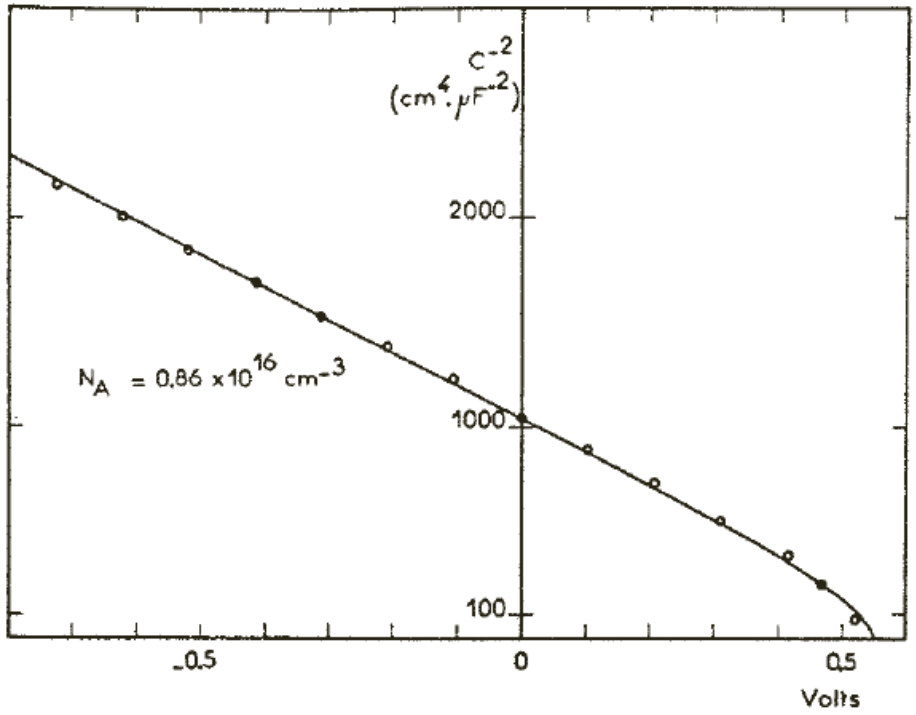


$$\frac{1}{C_j^2} \simeq \frac{2(\phi_B - V)}{q\epsilon_s N_d}$$

- Note that the plotted values represent capacitance density
  If capacitance is plotted, then the slope will be $2/(qN_d\mathcal{E}_sA^2)$, *where A is the area*

Depletion capacitance (5), numerical example

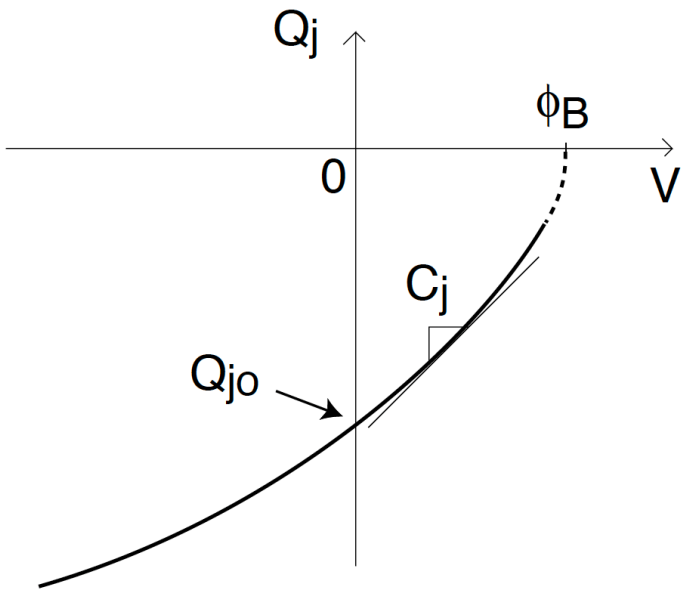
pn+: Calculate ϕ_B and N_A



Experimental data: Fortini et al., IEEE Trans. Electron Dev. ED-29, 1604

Viewing capacitance of p-n junction in terms of charge

$$Q_j(V) = \sqrt{\frac{2q\epsilon_s N_a N_d(\phi_B - V)}{N_a + N_d}} = Q_{jo}\sqrt{1 - \frac{V}{\phi_B}}$$



$$C_j = \frac{dQ_j}{dV}$$

$$C_j = \frac{Q_j}{V}$$

Wrong!

Use of varactors (also known as varicap diodes)

• Microwave Circuits: voltage-controlled oscillators for frequency tuning, phase-locked loops (PLLs) for frequency synthesis.

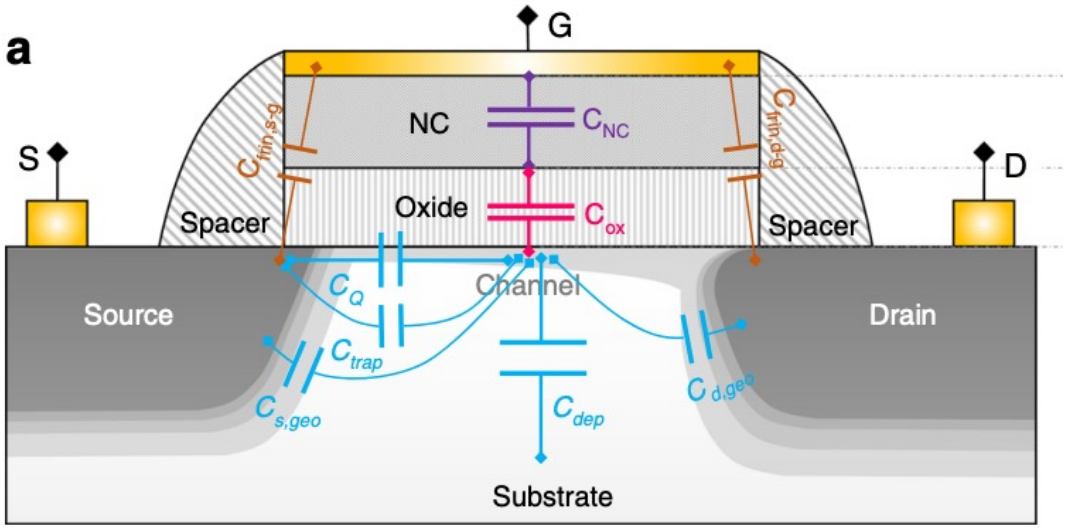
• Tunable Filters: radio receivers and transmitters to adjust bandpass filters, e.g. to tune antenna matching networks.

• Frequency Modulation (FM) and Phase Modulation Circuits

• TV and Radio Receivers: tuners for channel selection in televisions and radios.

Capacitance of p-n junction has to be considered in FET design

Some of the capacitances within FET are related to the pn junctions



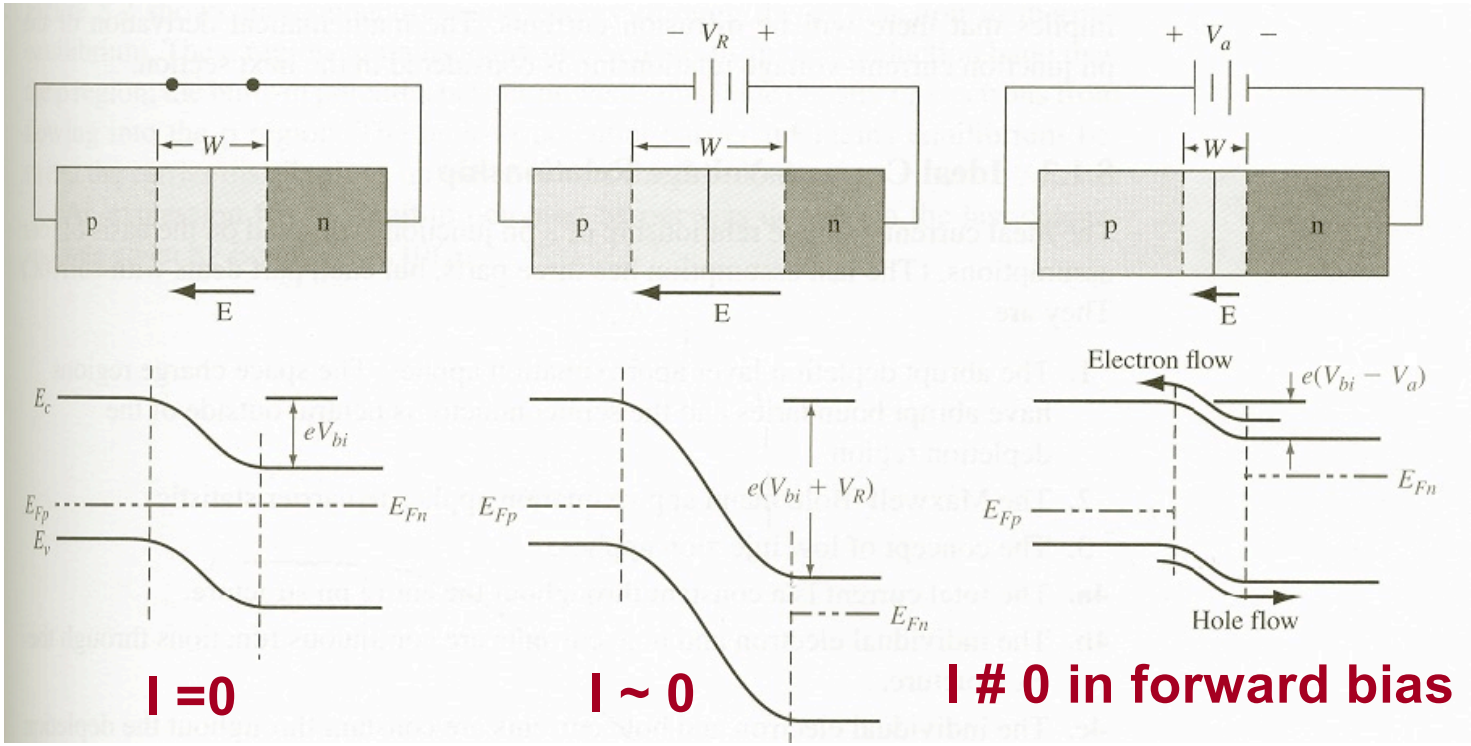
How Junction Capacitance Affects MOSFET Performance:

- Slower Switching Speed: The charge storage in the depletion region of the PN junction introduces parasitic capacitance
- Increased Power Consumption: More capacitance means higher power dissipation (charge/discharge)
- Limits High-Frequency Operation

NATURE COMMUNICATIONS | (2020) https://doi.org/10.1038/s41467-019-13797-9

Transport in pn juntions: Band diagrams

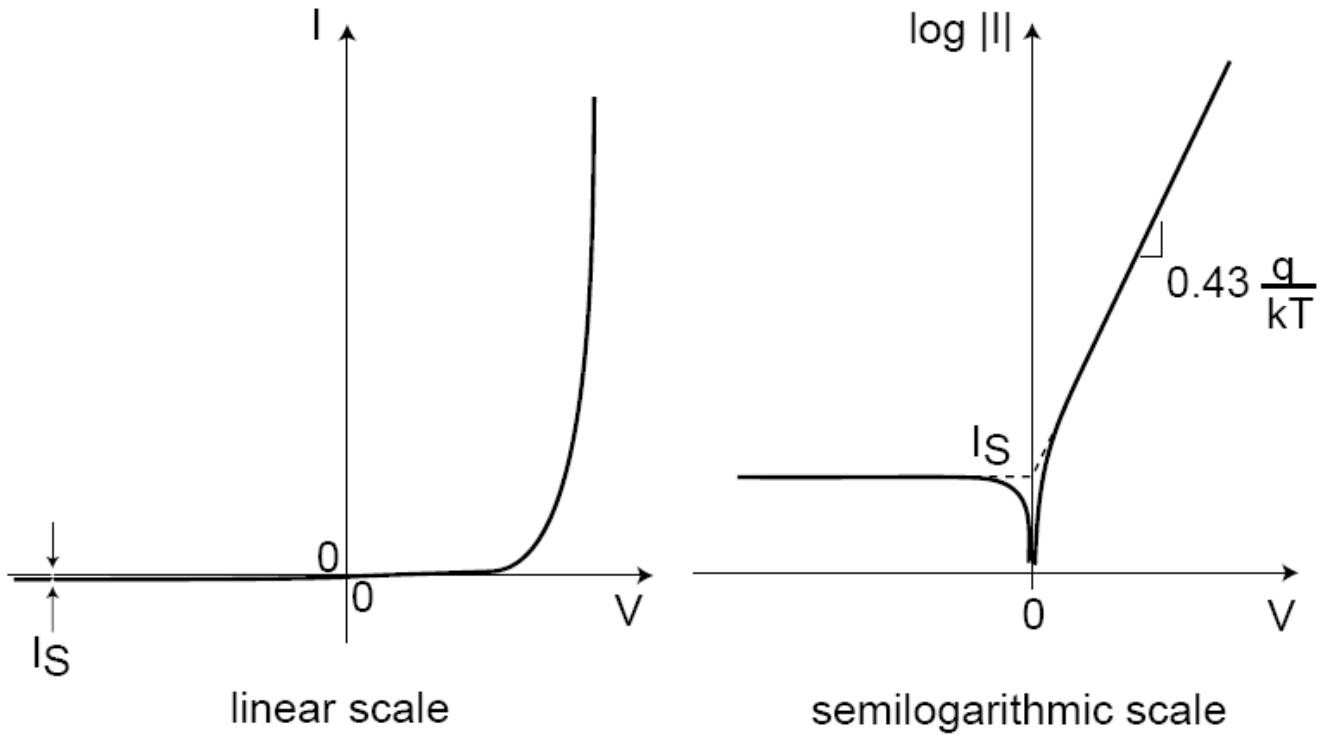
V=0 Reverse Forward

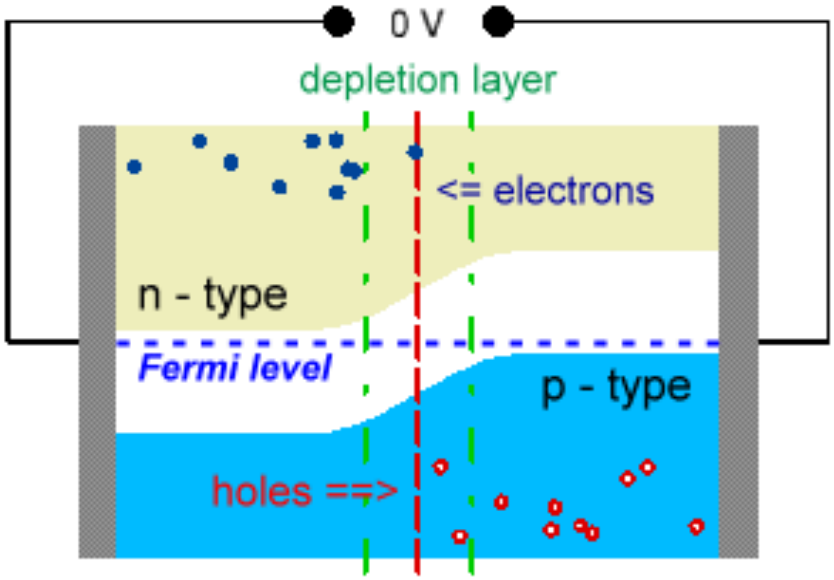


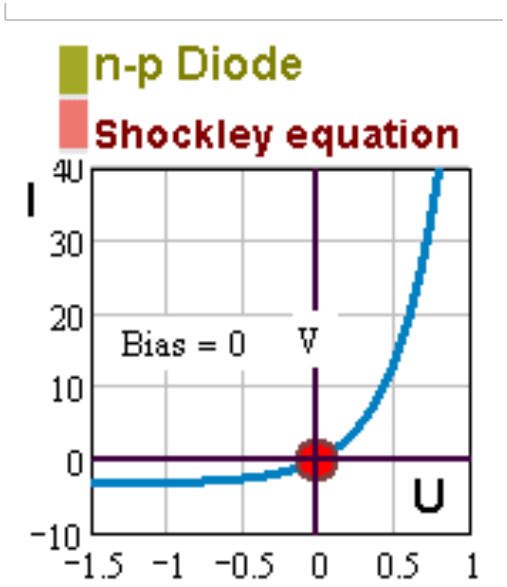
I =0 I ~ 0 I # 0 in forward bias

pn junction = pn diode

Application of voltage to pn junction also results in current (will be studied later → diode): **pn diode**!







In summary, the most important point to remember about the p-n junction diode is its ability to offer very little resistance to current flow in the forward-bias direction but maximum resistance to current flow when reverse biased.

pn junction under bias: key points

• Voltage applied to pn junction drops across SCR:

⇒ SCR electrostatics modified
– in forward bias: xd ↓, |E|↓
– in reverse bias: xd ↑, |E|↑

• Analytical formulation for SCR electrostatics in thermal equilibrium valid under bias if:

$$\phi_B \rightarrow \phi_B - V$$

• As V changes, SCR charge changes too:

⇒ depletion capacitance, C_j

• pn junction depletion capacitance depends on bias

• in pn junction, current flows for forward bias (V>0), very low current in reverse bias

pn junction under bias: conduction

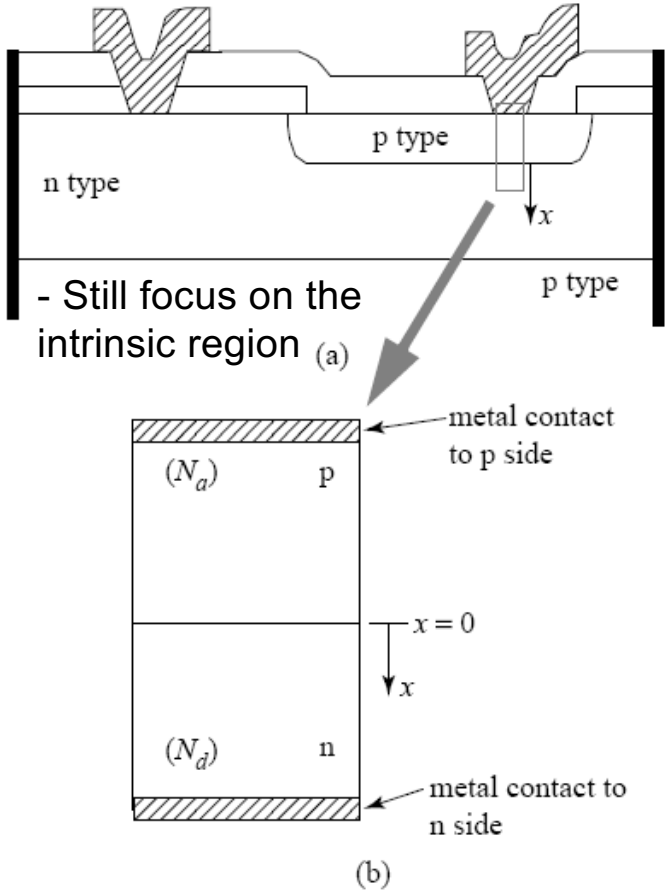
- pn junction under bias: diode
- I-V characteristics
- Forward conduction
- Breakdown

Key questions

- Why does the pn junction diode exhibit current rectification?
- Why does the junction current in forward bias increase as:

  $I \sim \exp(qV/kT)$?
- What are the leading dependences of the saturation current (the factor in front of the exponential)?

Pn junction under bias

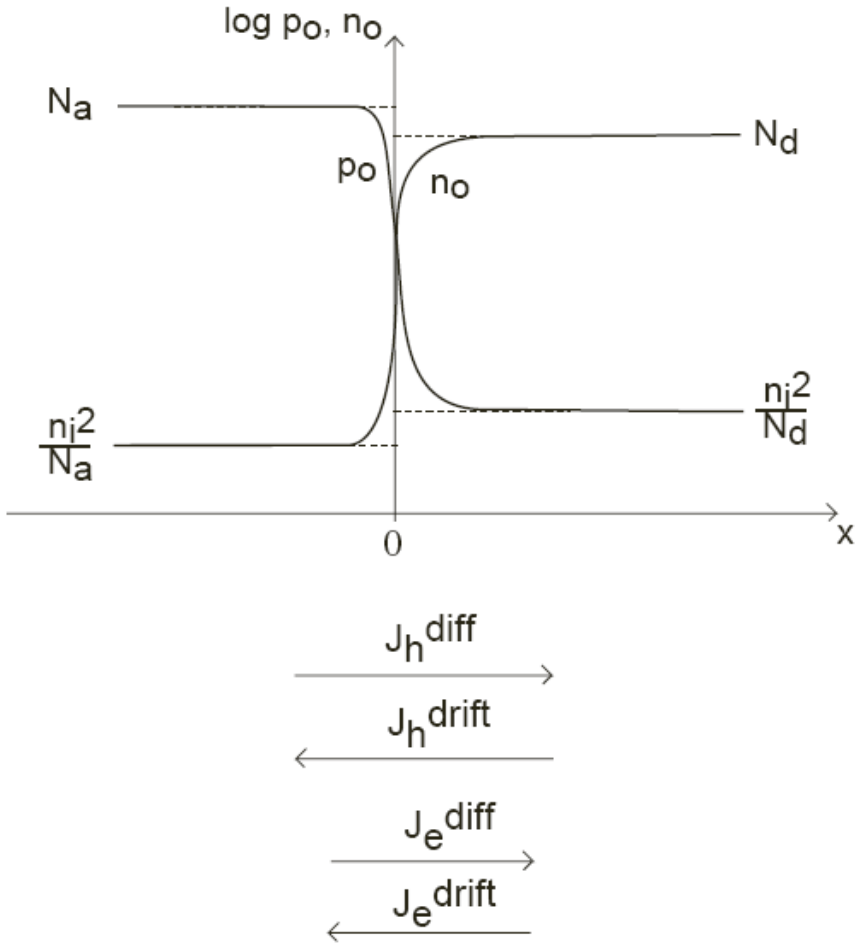


- Still focus on the intrinsic region

Upon application of voltage:

- electrostatics upset: depletion region widens or shrinks
- current flows (with rectifying behavior)
- carrier charge storage

Carrier profiles @ thermal equilibrium (recall)



Inside SCR in thermal equilibrium: dynamic balance between drift and diffusion for electrons and holes:

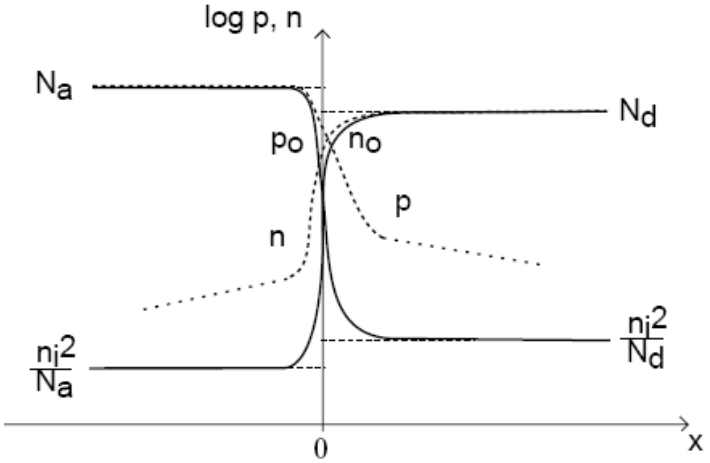
$$|J_{drift}| = |J_{diff}|$$

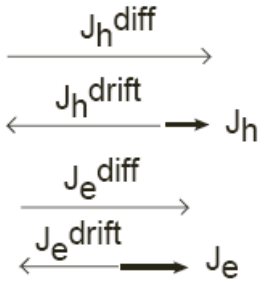
Carrier concentrations under bias (1)

Forward bias, V >0

$$V > 0,\ \phi_B - V \downarrow \Rightarrow\ |E_{SCR}| \downarrow \Rightarrow |J_{drift}| \downarrow$$

+





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Current balance in SCR broken:

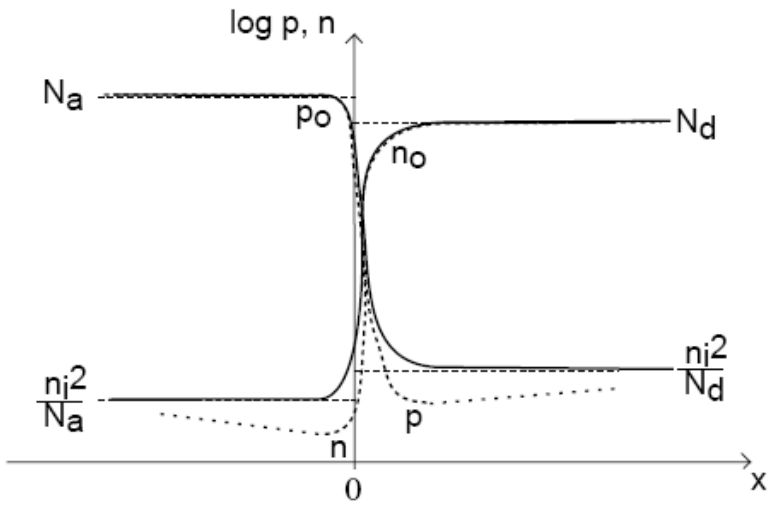
$$|J_{drift}| < |J_{diff}|$$

- **Net diffusion current in SCR**
  - ➢ **minority carrier** injection into QNR's
  - ➢ **excess minority** carrier concentrations in QNR's

Carrier concentrations under bias (2)

Reverse bias, V <0

$$V < 0,\ \phi_B - V \uparrow \Rightarrow\ |E_{SCR}| \uparrow \Rightarrow |J_{drift}| \uparrow$$



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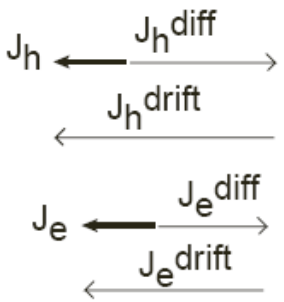


+

$$|J_{drift}| > |J_{diff}|$$

- Net drift current in SCR:
  - ➢ **minority carrier** extraction from QNR's
  - ➢ **deficit of minority carrier** concentrations in QNR's
- **Few minority carriers in QNR's: current small**

What happens if minority carrier conc. change from equilibrium in QNR?

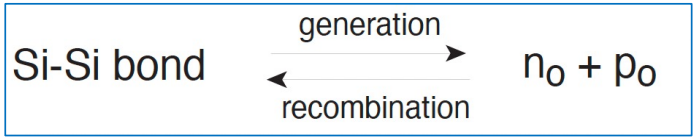
- In thermal equilibrium: rate of break up of Si-Si bonds balanced by rate of formation of bonds

- minority carrier injection:

⇒ - carrier concentration above equilibrium
- recombination prevails

- minority carrier extraction:

⇒ - carrier concentration below equilibrium
- generation prevails



The system is out of thermal equilibrium

What happens if minority carrier conc. change from equilibrium in QNR?

• Balance between generation and recombination broken: where does recombination & generation take place?

• In modern devices, **recombination mainly takes place at surfaces**:

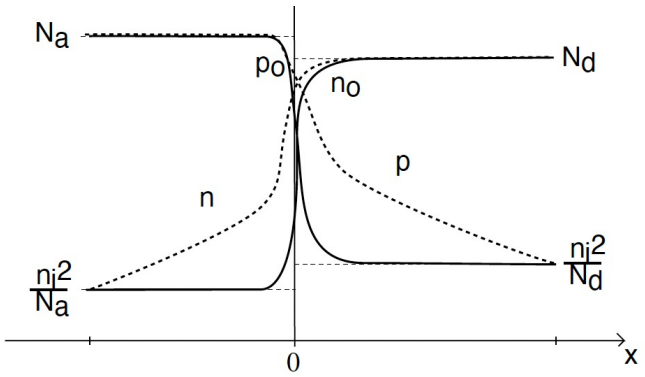
- nearly perfect crystalline periodicity broken at a surface, lots of broken bonds: generation and recombination centers
- modern devices are very small with high area to volume ratio.

• High generation and recombination activity at surfaces, so that carrier concentrations cannot deviate much from equilibrium values

$$n(s) \simeq n_o, \quad p(s) \simeq p_o$$

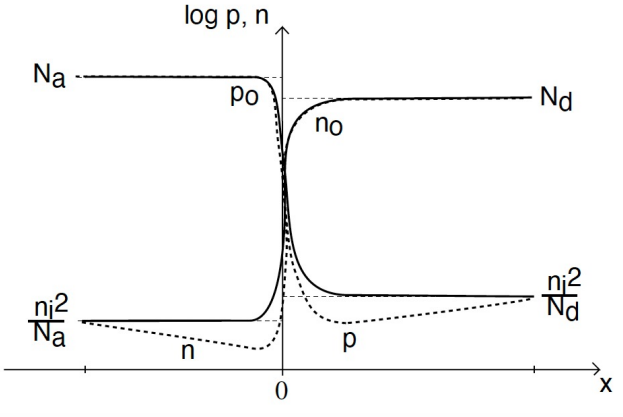
pn diode current: qualitative view

Forward bias



Forward bias: injected minority carriers diffuse through QNR ⇒ recombine at semiconductor surface

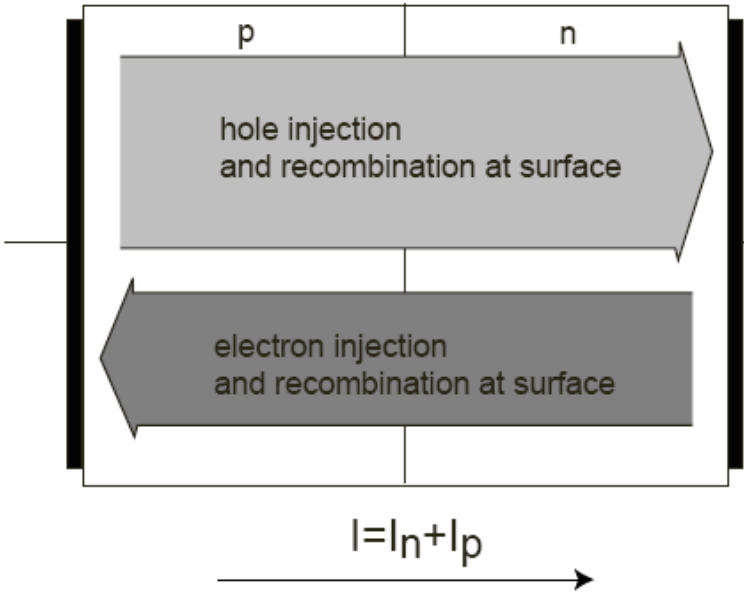
Reverse bias



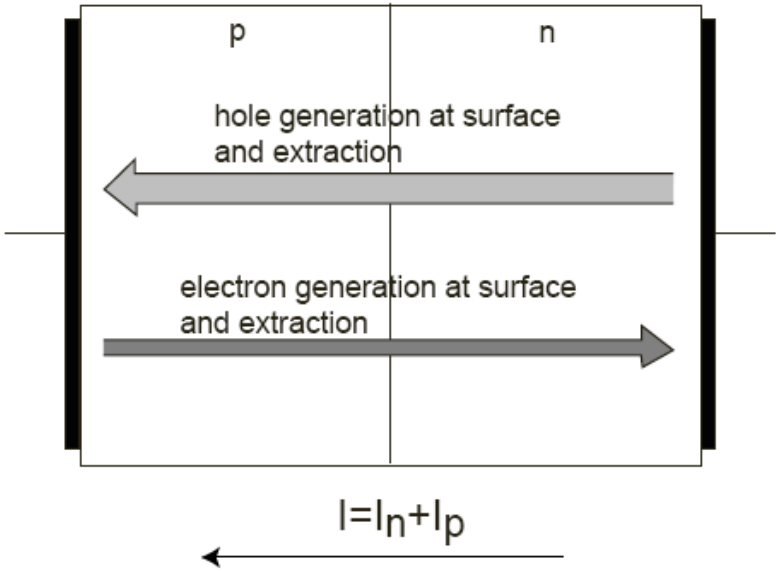
Reverse bias: minority carriers extracted by SCR
-generated at surface and diffuse through QNR

pn diode current: qualitative view

Forward bias



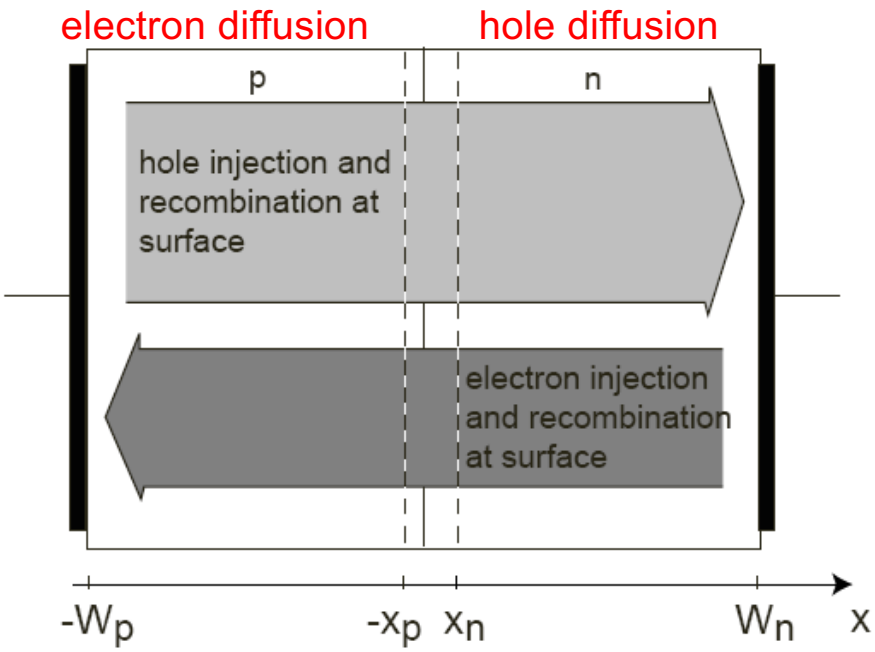
Reverse bias



pn diode current: magnitude/calculation

What limits the magnitude of the diode current?

- not generation or recombination rate at surfaces
- not injection or extraction rates through SCR
- **<u>diffusion rate through QNR's</u>**



Development of analytical current model, I-V:

1. Calculate concentration of minority carriers at edges of SCR, $p(x_n)$ and $n(-x_p)$
2. Calculate minority carrier diffusion current in each QNR, In and Ip
3. Sum electron and hole diffusion currents, I = In + Ip

Diode current calculation (1)

Step 1: computation of minority carrier boundary conditions at edges of SCR

Thermal equilibrium

From L2, slides 14-19:

$$\frac{n_o(x_1)}{n_o(x_2)} = \exp\frac{q[\phi(x_1) - \phi(x_2)]}{kT}$$

$$\frac{p_o(x_1)}{p_o(x_2)} = \exp\frac{-q[\phi(x_1) - \phi(x_2)]}{kT}$$

Quasi-equilibrium under bias

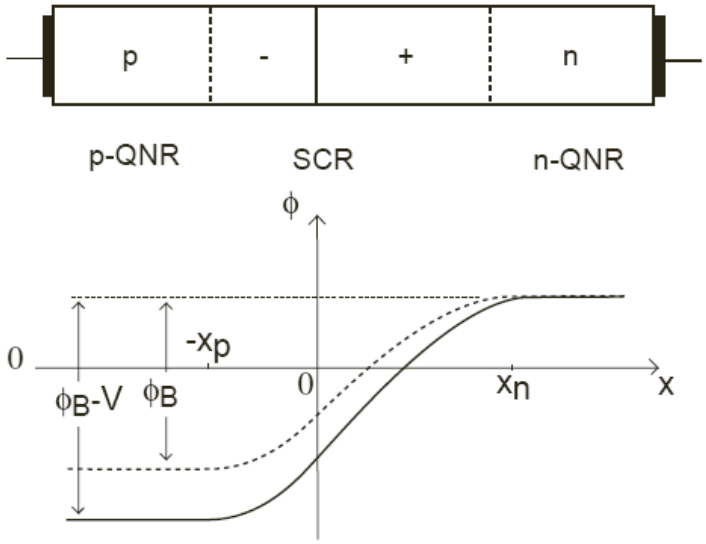
$$|J_{drift}| \neq |J_{diff}|$$

but if difference small with respect to absolute values of current:

$$\frac{n(x_1)}{n(x_2)} \simeq \exp\frac{q[\phi(x_1) - \phi(x_2)]}{kT}$$

$$\frac{p(x_1)}{p(x_2)} \simeq \exp\frac{-q[\phi(x_1) - \phi(x_2)]}{kT}$$

Diode current calculation (2)



$$n(-x_p) \simeq N_d \exp \frac{q(V-\phi_B)}{kT}$$

$$p(x_n) \simeq N_a \exp \frac{q(V-\phi_B)}{kT}$$

At edges of SCR, then:

$$\frac{n(x_n)}{n(-x_p)} \simeq \exp \frac{q[\phi(x_n)-\phi(-x_p)]}{kT} = \exp \frac{q(\phi_B - V)}{kT}$$

$$\frac{p(x_n)}{p(-x_p)} \simeq \exp \frac{-q[\phi(x_n)-\phi(-x_p)]}{kT} = \exp \frac{-q(\phi_B - V)}{kT}$$

$$p(-x_p) \simeq N_a \quad \text{and} \quad n(x_n) \simeq N_d$$

Diode current calculation (3)

$$n(-x_p) \simeq N_d \exp \frac{q(V-\phi_B)}{kT}$$

With: $\phi_B = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2}$

$$n(-x_p) \simeq \frac{n_i^2}{N_a} \exp \frac{qV}{kT}$$

$$p(x_n) \simeq \frac{n_i^2}{N_d} \exp \frac{qV}{kT}$$

Equilibrium, V=0

$$n(-x_p) = \frac{n_i^2}{N_a} \qquad p(x_n) = \frac{n_i^2}{N_d}$$

Forward, V>0

$$n(-x_p) \gg \frac{n_i^2}{N_a} \qquad p(x_n) \gg \frac{n_i^2}{N_d}$$

Reverse, V<0

$$n(-x_p) \ll \frac{n_i^2}{N_a} \qquad p(x_n) \ll \frac{n_i^2}{N_d}$$

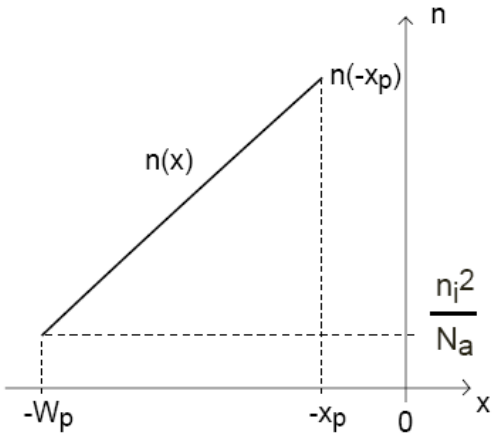
Rectification property of pn diode (V>0 = high current and V<0 = low current) arises from minority carrier boundary conditions at edges of SCR.

Diode current calculation (4)

Step 2: Diffusion current in QNR

Diffusion equation (for electrons in p-QNR): $J_n = qD_n \frac{dn}{dx}$

Why n(x) is linear?



$$n(x = -W_p) = n_o = \frac{n_i^2}{N_a}$$

$$n(-x_p) = \frac{n_i^2}{N_a} \exp \frac{qV}{kT}$$

$$n_p(x) = n_p(-x_p) + \frac{n_p(-x_p) - n_p(-W_p)}{-x_p + W_p}(x + x_p)$$

Diode current calculation (5)

$$J_n = qD_n \frac{dn}{dx} = qD_n \frac{n_p(-x_p) - n_p(-W_p)}{W_p - x_p}$$

$$= qD_n \frac{\frac{n_i^2}{N_a} \exp \frac{qV}{kT} - \frac{n_i^2}{N_a}}{W_p - x_p}$$

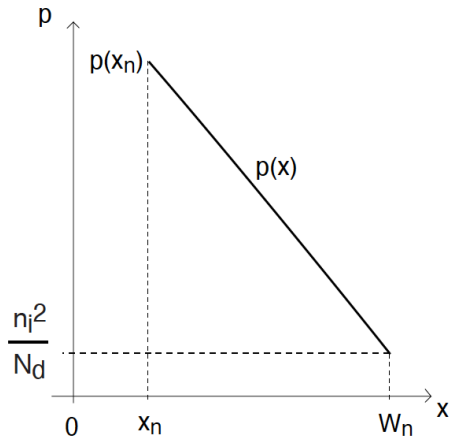
$$\boxed{J_n = q \frac{n_i^2}{N_a} \frac{D_n}{W_p - x_p} (\exp \frac{qV}{kT} - 1)}$$

Diode current calculation (6)

For electrons we just got:

$$J_n = q\frac{n_i^2}{N_a}\frac{D_n}{W_p - x_p}(\exp\frac{qV}{kT} - 1)$$

For holes - same logic:



$$J_p = q\frac{n_i^2}{N_d}\frac{D_p}{W_n - x_n}(\exp\frac{qV}{kT} - 1)$$

sum both current components:

$$J = J_n + J_p = qn_i^2(\frac{1}{N_a}\frac{D_n}{W_p - x_p} + \frac{1}{N_d}\frac{D_p}{W_n - x_n})(\exp\frac{qV}{kT} - 1)$$

Diode current calculation (6)

Step 3: sum both current components:

$$J = J_n + J_p = qn_i^2\left(\frac{1}{N_a}\frac{D_n}{W_p - x_p} + \frac{1}{N_d}\frac{D_p}{W_n - x_n}\right)\left(\exp\frac{qV}{kT} - 1\right)$$

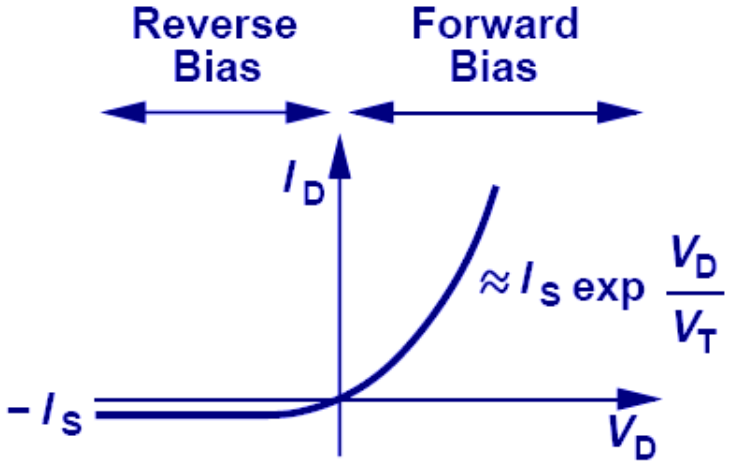
$$I = I_o\left(\exp\frac{qV}{kT} - 1\right)$$

I_o is called saturation current [A]

This formula is valid for forward and reverse bias

Summary I-V characteristics of p-n junction

- Current increases exponentially with applied forward bias voltage, and “saturates” at a relatively small negative current level for reverse bias voltages.



“Ideal diode” equation:

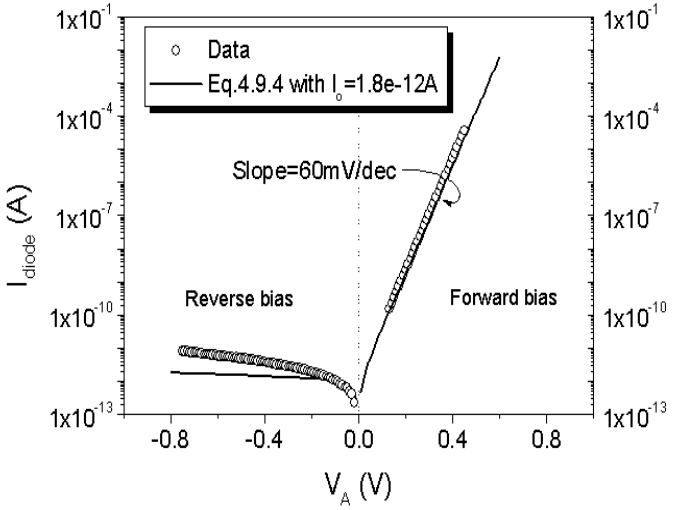
$$I_D = I_S\left(e^{V_D/V_T} - 1\right)$$

$$I_S = AJ_S = Aqn_i^2\left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)$$

A – area, Ln, Lp – SCR length

Practical PN Junctions

- Typically, pn junctions in IC devices are formed by counter-doping. The equations provided in class (and in the textbook) can be readily applied to such diodes if
  - $N_A \equiv$ net acceptor doping on p-side $(N_A\text{-}N_D)_{\text{p-side}}$
  - $N_D \equiv$ net donor doping on n-side $(N_D\text{-}N_A)_{\text{n-side}}$



$$I_D = I_S(e^{qV_D/kT} - 1)$$

$$I_S = Aqn_i^2\left(\frac{D_n}{L_nN_A} + \frac{D_p}{L_pN_D}\right)$$

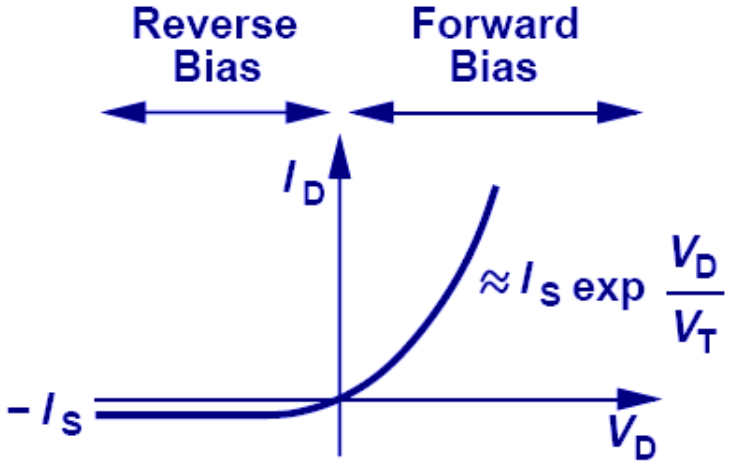
Diode Saturation Current I_S

$$I_S = Aqn_i^2\left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)$$

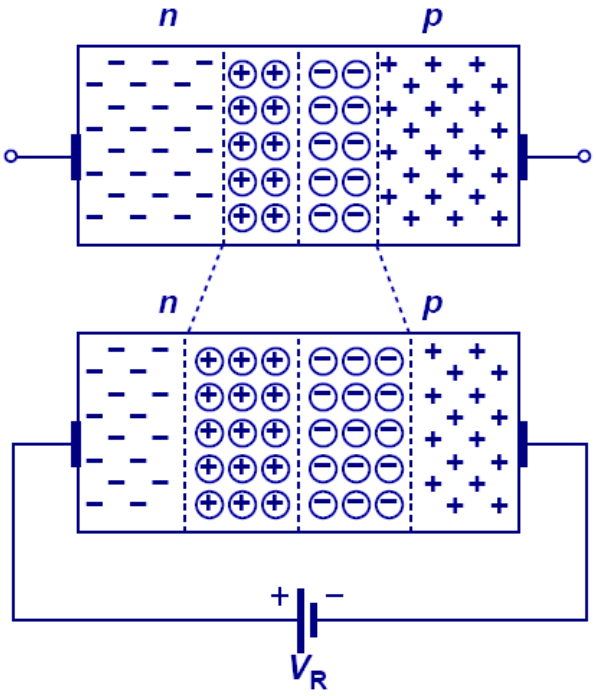
- I_S can vary by orders of magnitude, depending on the diode area, semiconductor material, and net dopant concentrations.
  - typical range of values for Si PN diodes: 10^{-14} to 10^{-17} A/μm^2
- In an asymmetrically doped PN junction, the term associated with the more heavily doped side is negligible:
  - If the P side is much more heavily doped, $I_S \cong Aqn_i^2\left(\frac{D_p}{L_p N_D}\right)$
  - If the N side is much more heavily doped, $I_S \cong Aqn_i^2\left(\frac{D_n}{L_n N_A}\right)$

PN Junction under Reverse Bias

- A reverse bias increases the potential drop across the junction. As a result, the magnitude of the electric field in the depletion region increases and the width of the depletion region widens.

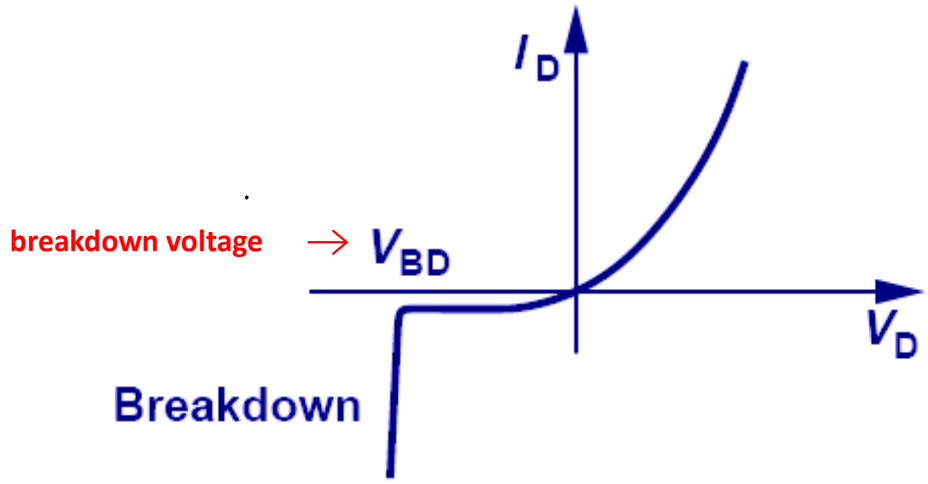


$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_R)}$$



Reverse Breakdown

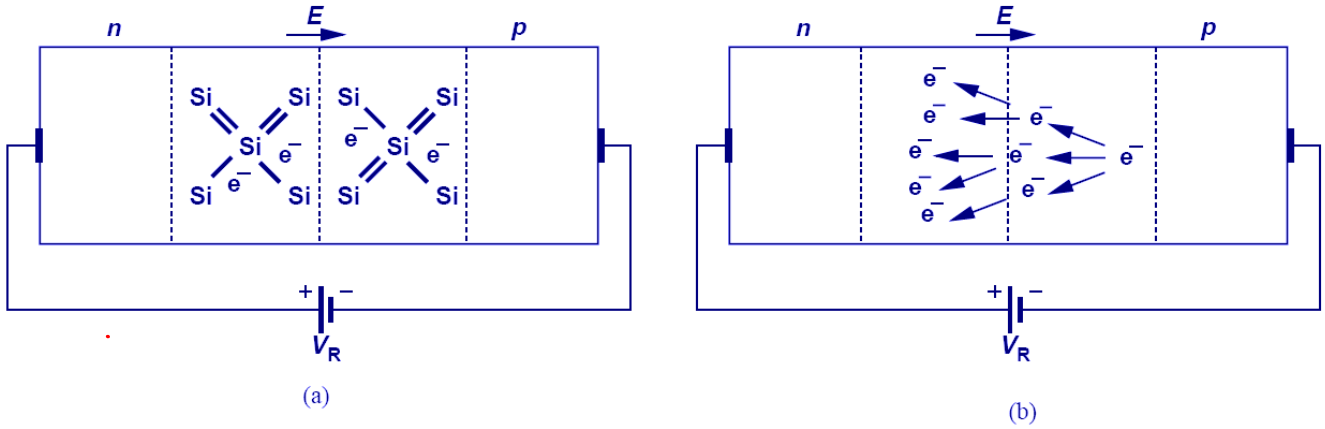
- As the reverse bias voltage increases, the electric field in the depletion region increases.
- Eventually, it can become large enough to cause the junction to break down so that a large reverse current flows:



Reverse Breakdown Mechanisms

a) ***Zener breakdown*** occurs when the electric field is sufficiently high to pull an electron out of a covalent bond (to generate an electron-hole pair).

b) ***Avalanche breakdown*** occurs when electrons and holes gain sufficient kinetic energy (due to acceleration by the E-field) in-between scattering events to cause electron-hole pair generation upon colliding with the lattice.



Tunneling effect and Zener breakdown (1)

Phenomenon of tunneling

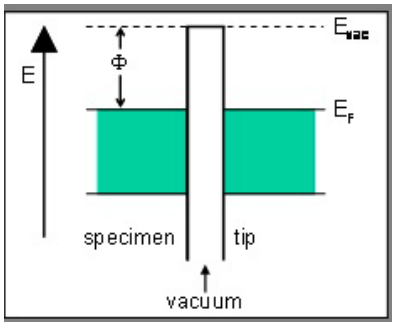
C**lassical case:** there is no chance of the particle being found beyond the barrier.

Q**uantum mechanics:** there is a **probability** that the electron can be found beyond the barrier.

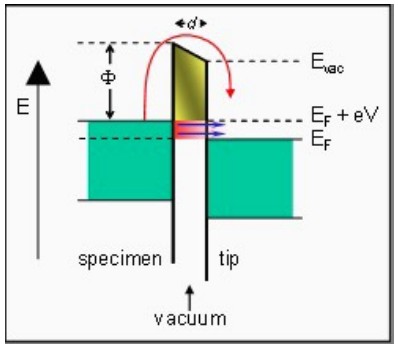
classical barrier – no transmission, only reflection

quantum barrier – part transmission, part reflection

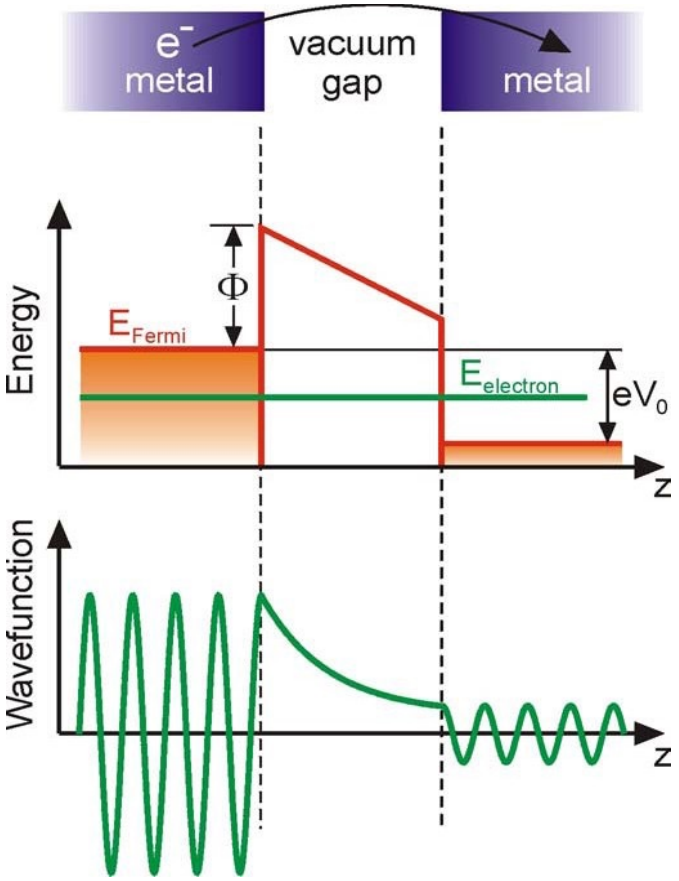
Tunneling effect and Zener breakdown (2)



When two metal surfaces are brought close to each other, there is only a narrow region of empty space left between them. On either side, the electrons occupy all states up to the Fermi energy. They need to overcome a barrier ***Φ*** to travel from tip to sample or vice versa



If the distance ***d*** between sample and tip is small enough (Å-range), electrons can 'tunnel' through the vacuum barrier. The direction of tunneling is determined by applied voltage ***V*** , which changes the energy profile as shown above

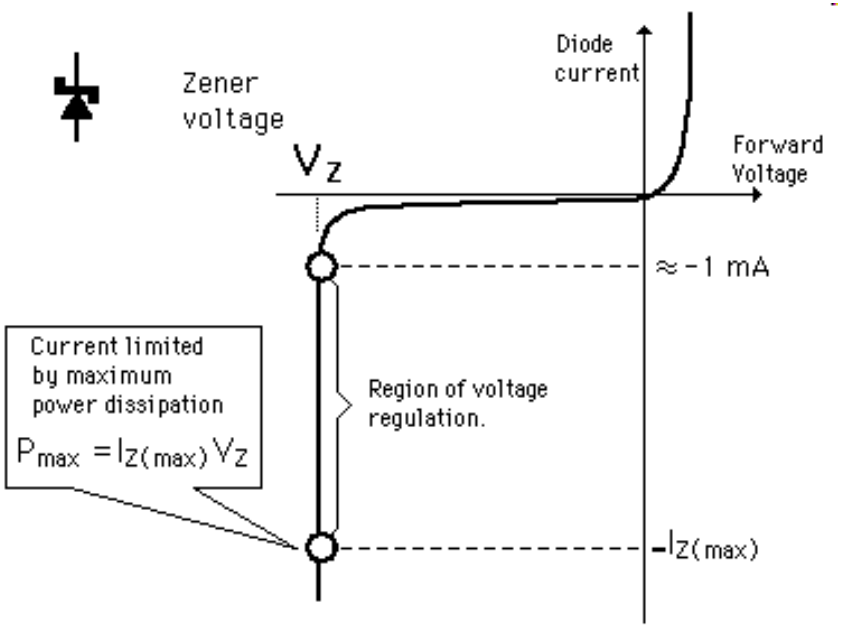


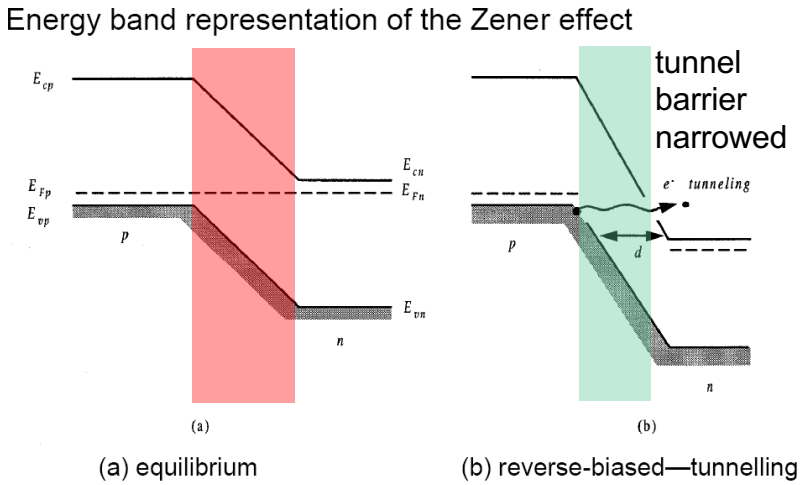
$I_{tunnel} \propto exp(-2Kd)$, d – barrier thickness

Tunneling effect and Zener breakdown (3)

• Zener breakdown occurs in heavily doped pn-junctions, which makes the depletion layer extremely thin.

• Carriers cannot accelerate enough to cause impact ionization. With the depletion layer so thin, **quantum mechanical tunneling** occurs causing current to flow.





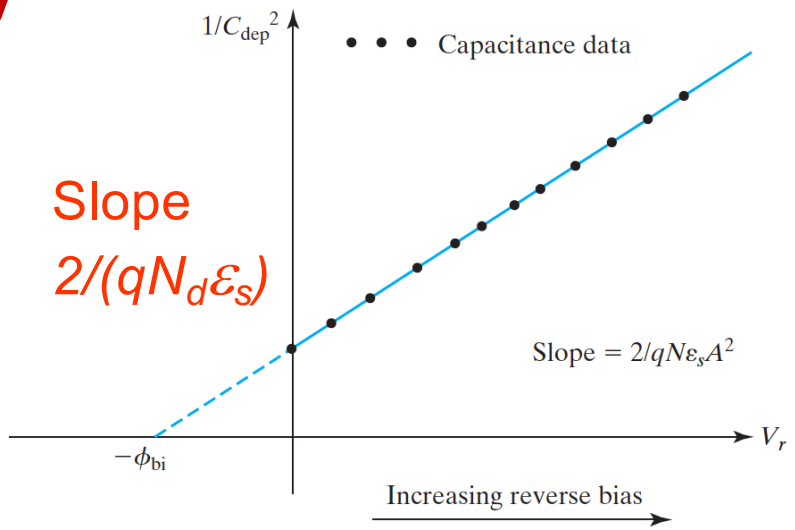
(a) equilibrium

(b) reverse-biased—tunnelling

Summary

- *pn* junction behaves like a capacitor

$$C_j(V) = \frac{\epsilon_s}{x_d(V)} = \sqrt{\frac{q\epsilon_s N_a N_d}{2(\phi_B - V)(N_a + N_d)}} = \frac{C_{jo}}{\sqrt{1 - \frac{V}{\phi_B}}}$$



- pn-junction-based *varactors*
- rectifying properties of pn-junctions
- reverse-biased pn-junction has very low saturation current and sharp reversible breakdown

$$I = I_o(\exp\frac{qV}{kT} - 1)$$