Institute of Electrical
and Microengineering
Biomedical and neuromorphic
microelectronic systems

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DIGITAL IC DESIGN
COMPLEMENTS AND *ERRATA*

This documents gathers complements of information to the course that results from issues and questions of general interest, as well as corrections to the course and exercises. Its most recent version is available for download from the Moodle web site of the course.

Thank you very much to all contributors who participate to the improvement of the course by their comments and corrections.

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1. PRESENTATION TRANSPARENCIES

1.1 LECTURE L01

The PUN equation of Slide #29 is corrected as follows (this also applied to the slide used on the video).

$$f = (\overline{w} + \overline{x})(\overline{y} + \overline{z})$$

Also, some general explanations are provided in HW01 Solution, Ex. 1.1(b).

Slide #34 presents two examples of Shannon's expansion algorithm. The initial expression is expanded with respect to variable *x* and then is expanded with respect to variable *y*. In the following, both results that are derived from applying Shannon's expansion theorem are shown to be identical to the initial expression.

The derivation with respect to variable *x* yields

$$\begin{aligned} \mathrm{f}(x,y,z) = xy + yz + xz &= x (y + yz + z) + \overline{x} (yz) \\ &= xy + xyz + xz + \overline{x}yz && (1) \\ &= y [x (1 + z)] + xz + \overline{x}yz && 1 + a = 1 \\ &= xy + xz + \overline{x}yz \end{aligned}$$

This result which is shown in the slide is further manipulated using classical Boolean algebra in order to derive the initial expression. Starting from (1)

$$\begin{aligned} & xy + xyz + xz + \overline{x}yz \\ &= xy + yz (x + \overline{x}) + xz && a + \overline{a} = 1 \\ &= xy + yz + xz \end{aligned}$$

The derivation of Shannon's expansion with respect to variable *y* follows the same principle.

$$\begin{aligned} \mathrm{f}(x,y,z) = xy + yz + xz &= y (x + z + xz) + \overline{y} (xz) \\ &= xy + yz + xyz + x\overline{y}z && (2) \\ &= x [y (1 + z)] + yz + x\overline{y}z \\ &= xy + yz + x\overline{y}z \end{aligned}$$

From (2)

$$\begin{aligned} & xy + yz + xyz + x\overline{y}z \\ &= xy + yz + xz (y + \overline{y}) \\ &= xy + yz + xz \end{aligned}$$

1.2 LECTURE L02

On slide 79 of the video, the LDD is made as an implant of n- ("n-minus" not "n-plus") meaning that the intensity of doping and thus density of dopants is "small/light" whearas n+ determines a "stong/heavy" doping.

The Damascene process is used in modern deep-submicron fabrication techniques that use copper as the metal layer. It is considered easier since the contact/via and the metal are processed in one step (one single etching required for both).

1.3 LECTURE L03B

On slide 27, following Euler path is not shown in the list of Euler paths for nMOS. z → x → y.

From the point of view of the theory of graphs, an Euler path is a trail that visits every edge one time (vertices may be visited several times). An Euler circuit, starts and end at the same vertex. Thus, z → x → y is an Euler circuit, *i.e.*, formally not an Euler path.

Still, from the point of view of VLSI, also an Euler circuit can be used to the aim of determining a suitable list of inputs. Nevertheless, if the goal of the Euler path/circuit consists of maximizing drain/source sharing, then z → x → y can not be a suitable choice. Let us consider the circuit in Figure 1.1.

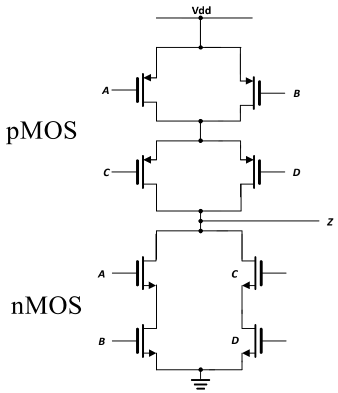

Figure 1.1: Complex function used in the study of suitable Euler paths.

Path a → c → d → b would be a suitable Euler path (circuit, actully) that is found in the PUN and PDN, thus also a valid one. Nevertheless, path a → c → d → b does not enable taking benefit of drain/source sharing of nMOSFETs A and B, that will respectively be found at each extremity of the layout.

1.4 LECTURE L03A

Cross-section and equivalent schematic on slide No. 35, and presented in part in Figure 1.2.

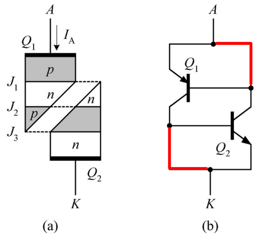

Figure 1.2: Complex function used in the study of suitable Euler paths.

The connections that appear in red in Figure 1.2(b) cannot be observed (formally) on Figure 1.2(a). The remaining cross-coupled arrangement of BJTs still suffers from latchup. These connections pertain to the biasing of the substrate and well(s). They are important in the sense that they are modeled as resistances R_{W1} and R_{S2} that should be reduced to avoid latchup.

1.5 LECTURE L07

On slide No. 45, D at logic-1 may induce the charge of node Q, that is, not the discharge.¨

On slide Nol 56, the text in the grey box should read "…. When expressing delays with respect to one single clock, then we observe that two events occur (one event while Φ_1 is high and one event while Φ_2 is high and thus while Φ_1 is low)"

On slide No. 63 of the video, the "+ t_{skew}" and "+ $t_{skew,i}$" should be replaced with "- t_{skew}" and "- $t_{skew,i}$" respectively.

2. EXERCISES

(none)