

2. Common-Source Amplifier with a Diode-Connected MOS Load

Parameters: $\mu_n C_{ox} = 278 \mu A/V^2$, $V_{TH,N} = 0.4V$, $\mu_p C_{ox} = 61 \mu A/V^2$, $|V_{TH,P}| = 0.54V$, $V_{DD} = 1.8V$

Operating Points: $V_{IN,DC} = 0.9V$, $V_{OUT,DC} = 0.9V$, $I_D = 10 \mu A$

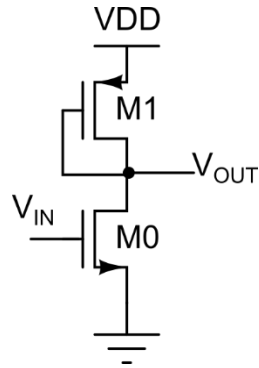
- a. To arrive at the sizing for M1, we note that

$$V_{DD} - V_{OUT,DC} = V_{SG1}$$

$$V_{SG1} = |V_{THP}| + \sqrt{\frac{2I_D}{\mu_p C_{ox} \left(\frac{W}{L}\right)_1}}$$

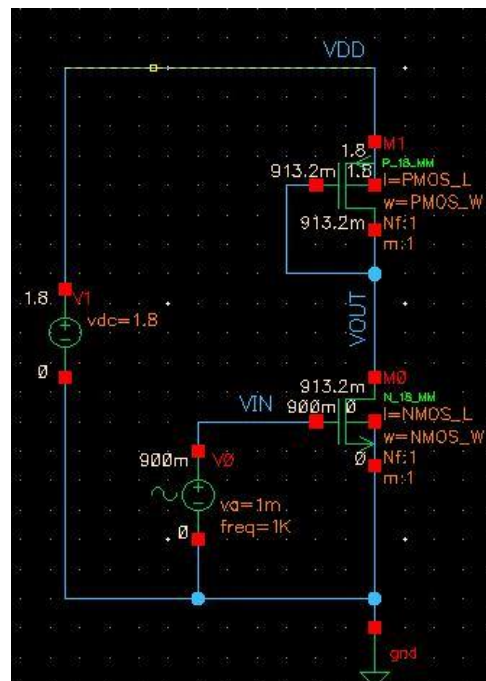
$$0.9 = 0.54 + \sqrt{\frac{2 * 10u}{61u * \left(\frac{W}{L}\right)_1}}$$

$$\left(\frac{W}{L}\right)_1 = 2.52$$



Here, we choose the length of the PMOS M1 so that $r_{o1} = r_{o0}$. For this, $L_1 \approx 580n$, and $W_1 \approx 1.47u$. We already know the sizing for the NMOS M0 from problem 1: $L_0 = 1u$ and $W_0 = 310n$.

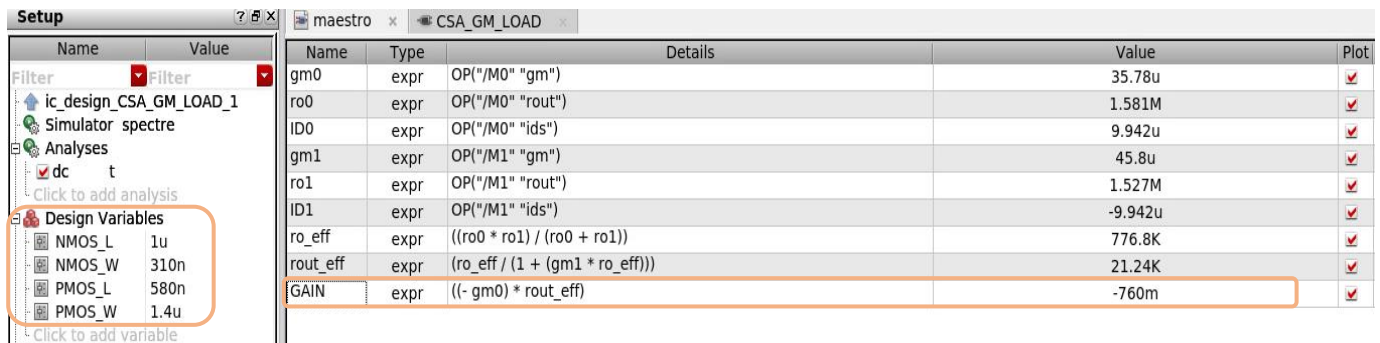
- b. Now, simulate the circuit in Cadence Virtuoso (as in Problem 1), and annotate the DC operating point. The DC operating point for the circuit is as shown below.



- c. Adjust the “PMOS_L” and “PMOS_W” parameters so that the DC operating point error is less than +/- 0.75%. For example, $L_1 = 580\text{n}$ and $W_1 = 1.4\mu$ seem to work fine for us. You can have any other value that satisfies the operating point conditions.

Now, let us add expressions for g_{m0} , g_{m1} , r_{o0} , r_{o1} (refer to problem 1 or figure below for the expressions or the easier way – do it from the ADE-Explorer Calculator), so that we can calculate the small signal gain of the circuit as,

$$A_v = -g_{m0} \cdot \left(\frac{1}{g_{m1}} \parallel r_{o0} \parallel r_{o1} \right)$$



The screenshot shows the ADE-Explorer Setup window. On the left, under 'Design Variables', the following variables are listed:

Name	Value
NMOS_L	1u
NMOS_W	310n
PMOS_L	580n
PMOS_W	1.4u

On the right, the 'maestro' window shows a table of calculated expressions:

Name	Type	Details	Value	Plot
gm0	expr	OP("/M0" "gm")	35.78u	✓
ro0	expr	OP("/M0" "rout")	1.581M	✓
ID0	expr	OP("/M0" "ids")	9.942u	✓
gm1	expr	OP("/M1" "gm")	45.8u	✓
ro1	expr	OP("/M1" "rout")	1.527M	✓
ID1	expr	OP("/M1" "ids")	-9.942u	✓
ro_eff	expr	((ro0 * ro1) / (ro0 + ro1))	776.8K	✓
rout_eff	expr	(ro_eff / (1 + (gm1 * ro_eff)))	21.24K	✓
GAIN	expr	((- gm0) * rout_eff)	-760m	✓

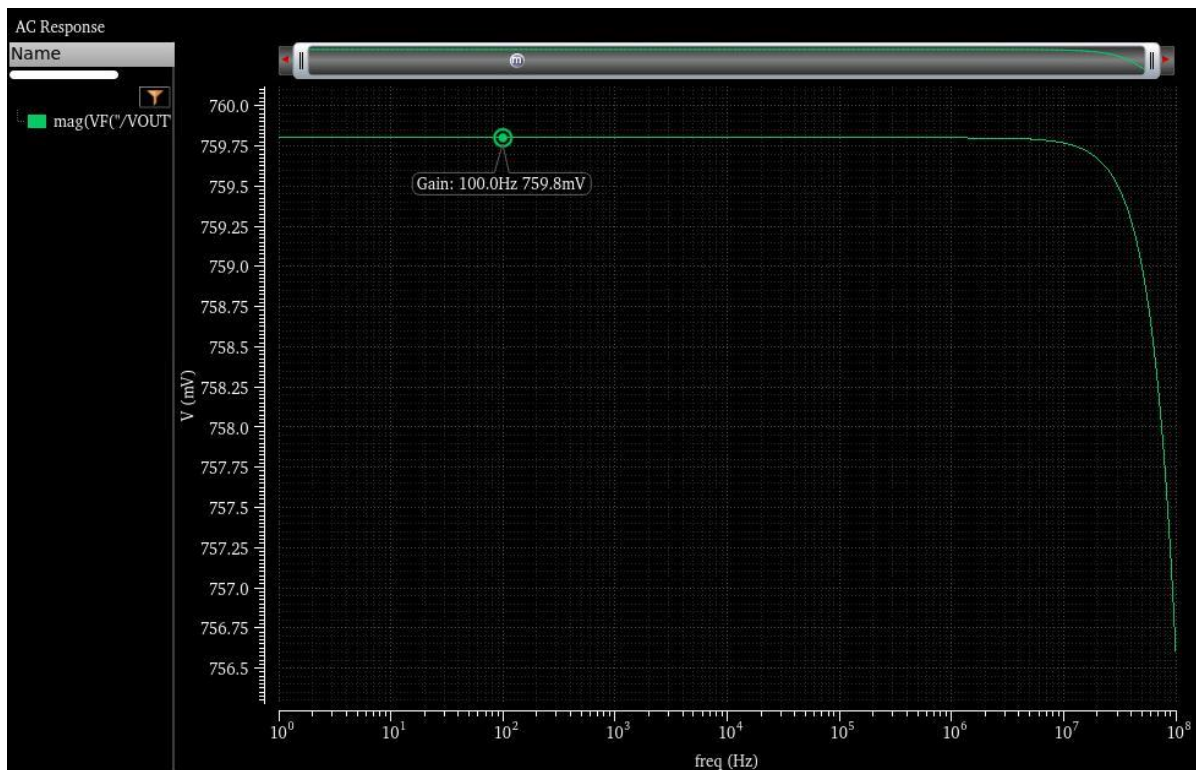
- d. To derive an expression for the voltage gain in terms of the DC operating point,

- $|A_v| = g_{m0} (1/g_{m1} \parallel r_{o0} \parallel r_{o1})$
- $|A_v| = g_{m0}/g_{m1}$ (assuming $r_{o1,2} \gg 1/g_{m1}$). Make sure this is true for you!
- $|A_v| = \frac{2I_{D1}}{|V_{IN} - V_{TH,N}|} \cdot \frac{|V_{OUT} - V_{DD} - V_{TH,P}|}{2I_{D2}}$
- $|A_v| = \frac{|V_{OUT} - V_{DD} - V_{TH,P}|}{|V_{IN} - V_{TH,N}|}$

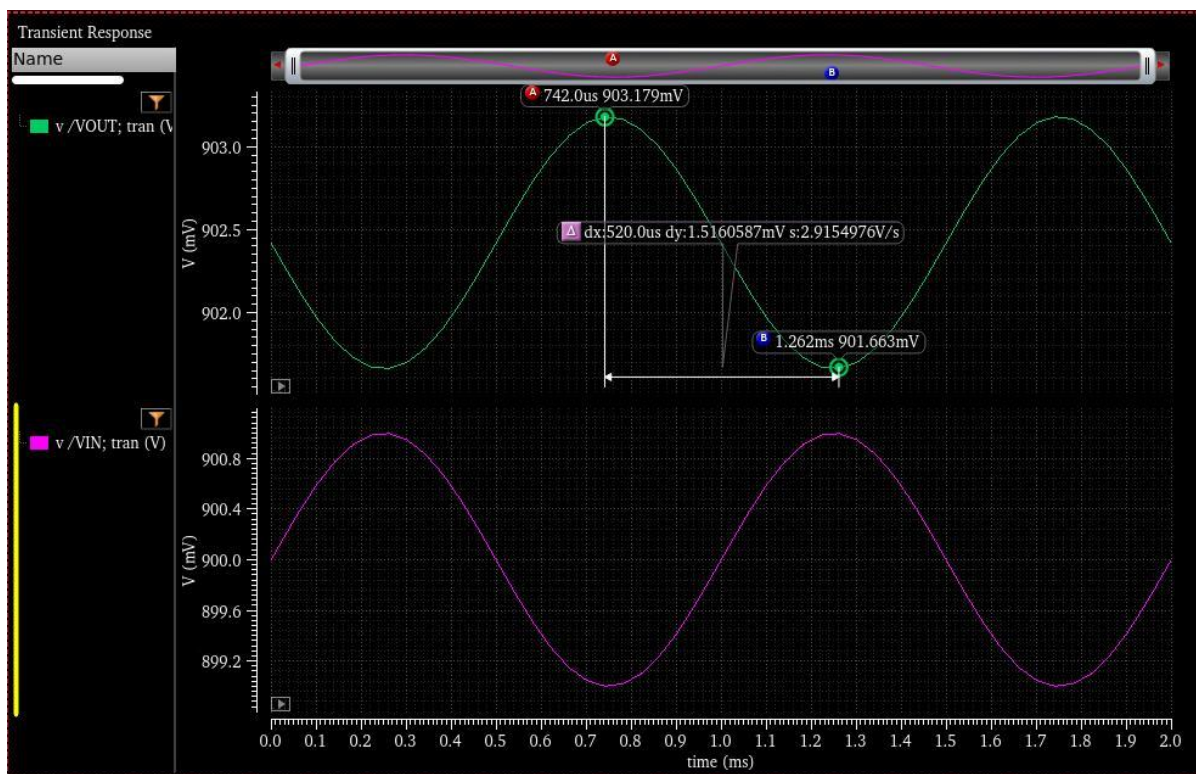


This shows that, like in the case of a resistive load, the voltage gain is determined once the input and output common modes are fixed. After all, a PMOS diode connected stage is a resistor!

- e. Now, perform the ac simulation and determine the small-signal gain (please refer to problem 1 on how to setup the ac simulation). From the plot, we see that the AC gain closely matches our calculated gain value “GAIN”.



- f. Now, perform the transient simulation and determine the gain (again, please refer to problem 1 to setup the transient simulation)



- g. Repeat the procedure for the new operating conditions: $V_{IN,DC} = 0.9V$, $V_{OUT,DC} = 0.6V$, $I_D = 10\mu A$. But, before you begin to do so, ask yourself:



- Based on the analysis in 2 (d), do you expect the gain to increase or decrease?
- Calculate the expected value of gain
- Now, verify the same using simulation



3. Common-Drain (aka Source Follower) Stage

Parameters: $\mu_n C_{ox} = 278 \mu A/V^2$, $V_{TH, N} = 0.4V$, $V_{DD} = 1.8V$

Operating Points: $V_{IN, DC} = 0.9V$, $V_{OUT, DC} = 0.4V$, $I_D = 1 \mu A$, $L = 1 \mu m$

- a. To calculate the value of the resistor R, we note that

$$V_{OUT, DC} = I_D \cdot R$$

$$R = \frac{0.4}{1 \mu} = 400 K\Omega$$

To arrive at the sizing for M0, we note that

$$V_{GS0} = V_{IN, DC} - V_{OUT, DC}$$

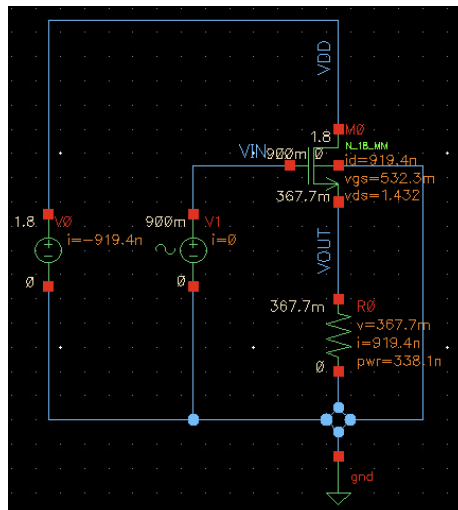
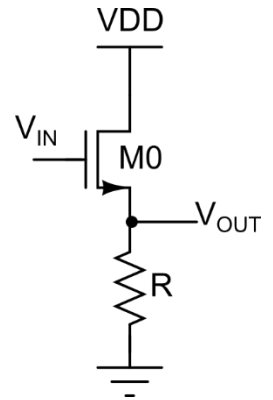
$$V_{GS0} = V_{THN} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}}$$

$$0.5 = 0.4 + \sqrt{\frac{2 * 1 \mu}{278 \mu * \left(\frac{W}{L}\right)_1}}$$

$$\left(\frac{W}{L}\right)_1 = 0.72$$

As $L_0 = 1 \mu m$, $W_0 = 720 nm$

- b. Now simulate the circuit in Cadence Virtuoso (as in Problem 1) and annotate the DC operating point. The DC operating point for the circuit is shown below.



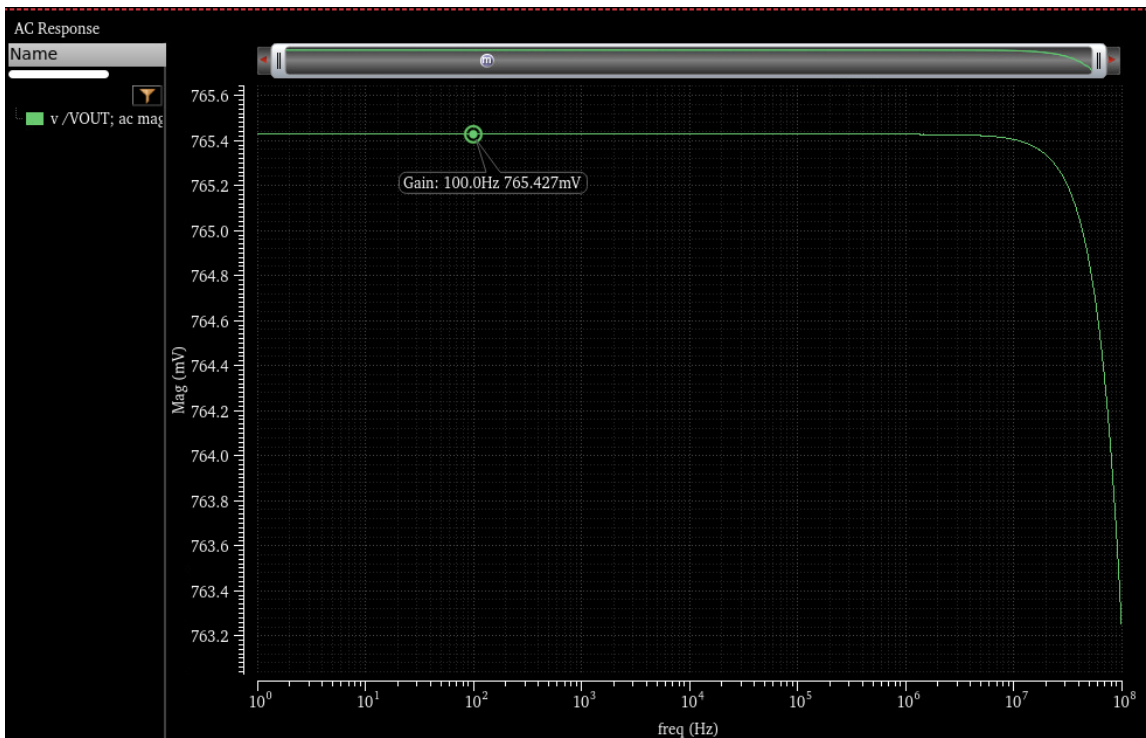
- c. Adjust the “NMOS_W” parameter so that the error is within +/- 0.75%. For example, $W_0 = 1.35\mu$ seems to work fine for us.
- d. The small signal gain for the source follower can be written as (please refer to the course slides – Lecture 5, Page 17 for the expression),

$$A_v = -g_{m0} \cdot \frac{R}{1 + (g_{m0} + g_{mb0}) \cdot R}$$

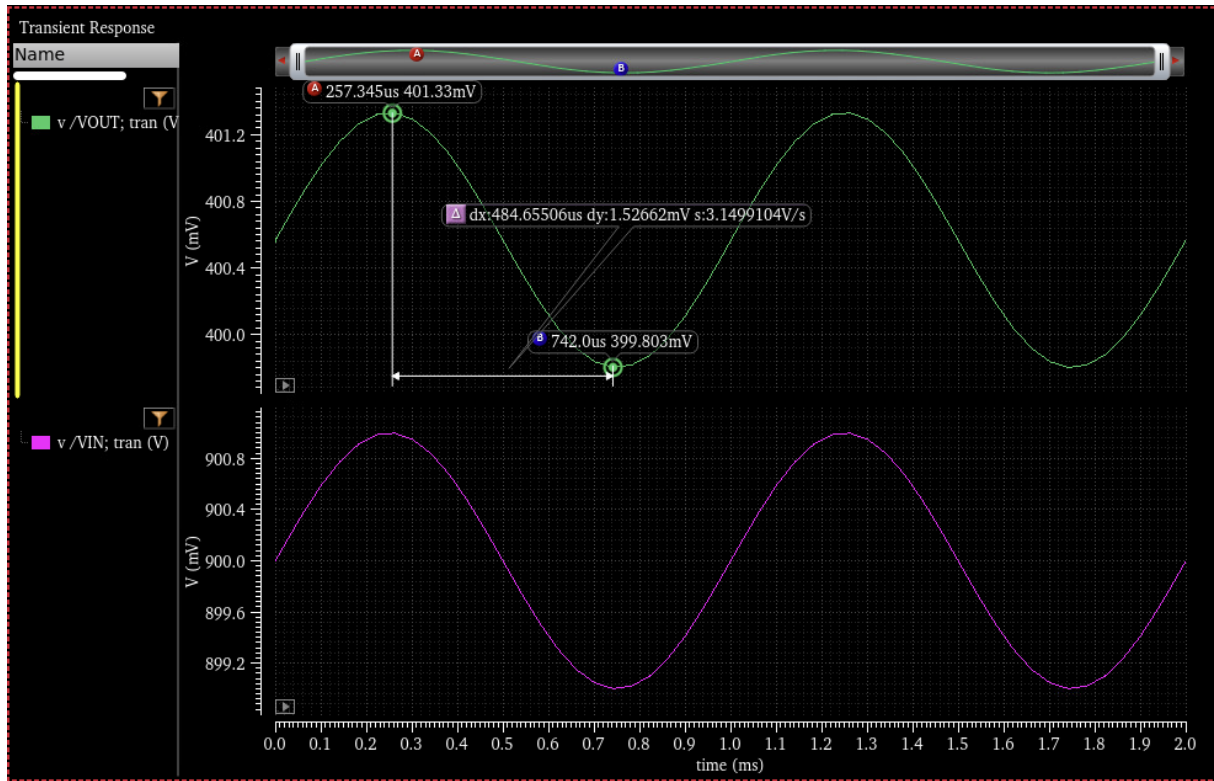
We need to add expressions for gm, gmb, R, and GAIN in the **Output Setup** palette of the ADE-Explorer as shown below.

Name	Value	Name	Type	Details	Value	Plot
Filter	Filter	id	expr	OP("/M0" "id")	1.001u	<input checked="" type="checkbox"/>
ic_design_SF_RLOAD_1		gm	expr	OP("/M0" "gm")	18.76u	<input checked="" type="checkbox"/>
Simulator spectre		gmb	expr	OP("/M0" "gmb")	3.025u	<input checked="" type="checkbox"/>
Analyses		R	expr	VAR("R")	400K	<input checked="" type="checkbox"/>
dc	t	GAIN	expr	((gm * R) / (1 + ((gm + gmb) * R)))	772.5m	<input checked="" type="checkbox"/>
Click to add analysis						
Design Variables						
NMOS_L	1u					
NMOS_W	1.35u					
R	400K					

- e. Now, perform the ac simulation and determine the gain (please refer to problem 1 on how to setup the ac simulation). From the plot, we see that the AC gain closely matches our calculated gain value “GAIN” (we attribute the resulting error to ignoring r_o in our gain calculation)



- f. Now, perform the transient simulation and determine the gain (again, please refer to problem 1 to setup the transient simulation)



- g. You can derive an expression for the output impedance of the source follower in terms of g_m , g_{mb} , r_o , and R (if in doubt, please refer to the course slides – Lecture 5, Page 22)

$$R_{out} = \frac{1}{g_m + g_{mb}} \parallel r_o \parallel R$$

Add the above expression for R_{out} along with the other expressions in the **Output Setup** palette in ADE-Explorer.

Setup

Name

Value

Filter

Filter

ic_design_SF_RLOAD_1

Simulator spectre

Analyses

tran0 2m

ac1 100M 100 Logarithm...

dc t

Click to add analysis

Design Variables

NMOS_L1u

NMOS_W1.35u

R400K

maestro

SF_RLOAD

Name

Type

Details

Value

Plot

id

expr

OP("/M0" "id")

1.001u

gm

expr

OP("/M0" "gm")

18.76u

gmb

expr

OP("/M0" "gmb")

3.025u

R

expr

VAR("R")

400K

GAIN

expr

$((gm * R) / (1 + ((gm + gmb) * R)))$

772.5m

ro

expr

OP("/M0" "rout")

4.443M

Zm_eff

expr

$(1 / (gm + gmb))$

45.9K

R_eff

expr

$((ro * R) / (ro + R))$

367K

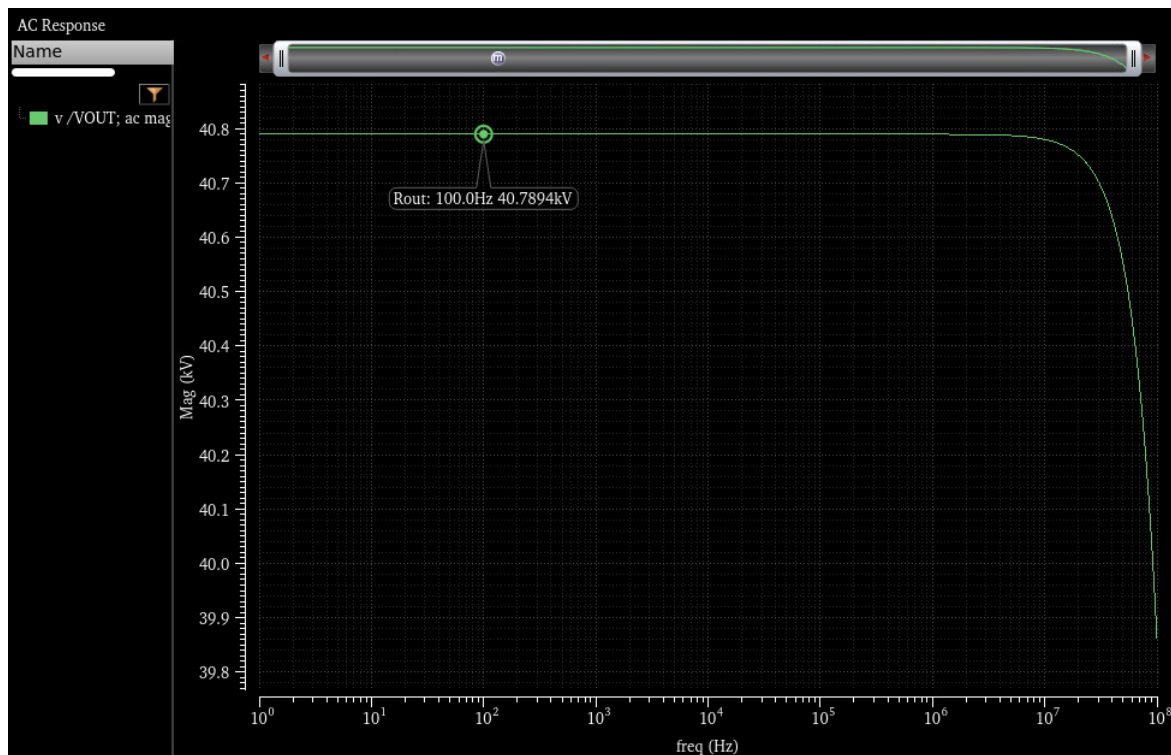
Rout

expr

$((Zm_eff * R_eff) / (Zm_eff + R_eff))$

40.79K

- h. As described in the problem statement, set the AC magnitude of the input voltage source V_0 to 0, and add a current source I_1 (with the AC magnitude set to 1) between the output “VOUT” and ground. Now, run the ac simulation and plot VOUT (as mentioned in the problem, we are measuring the output impedance R_{out} as $V_{OUT} = I_1 \cdot R_{out}$ and $I_1 = 1$)



As we can see from the plot, the calculated R_{out} very closely matches the simulated value for the small-signal output impedance.

- i. Repeat the procedure for the new operating conditions: $V_{IN, DC} = 0.9V$, $V_{OUT, DC} = 0.4V$, $I_D = 10\mu A$. But, before you begin to do so, ask yourself:



- Do you expect the gain to increase or decrease?
- Do you expect the output impedance to increase or decrease?
- Now, simulate and verify

