Lecture 4

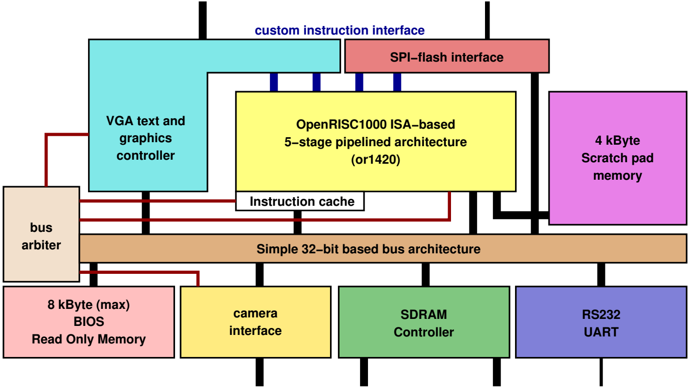
Embedded system design

Timing closure

CS476 - ESD
March 11, 2024

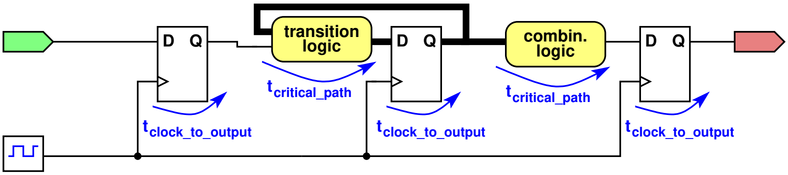
Dr. Theo Kluter
EPFL

Introduction



- Once we finished our architectural choices, we have to get the system running at the required frequency.
- We have to go into a phase which is called *timing closure*.
- To fully understand the timing closure we have first to go into some details of the final ASIC to be able to understand what is going on.

Remember: RTL design



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- Hence all our circuits look like the simplified circuit above, where all flipflops are connected to the same clock source (throughout our chip).

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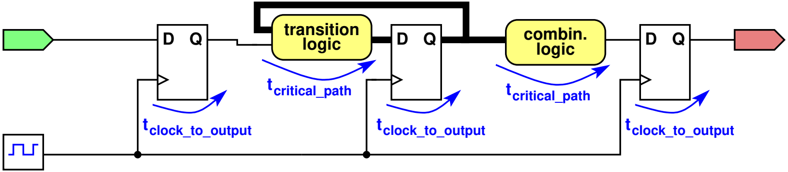

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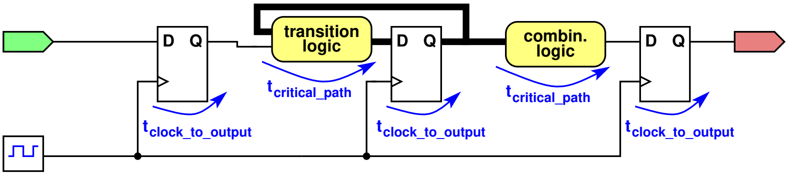

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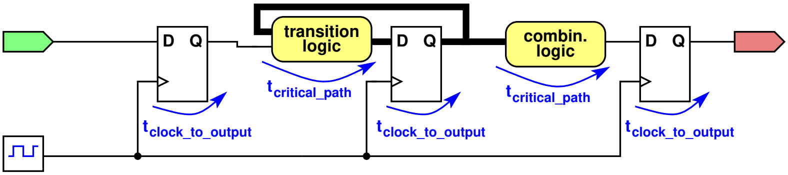

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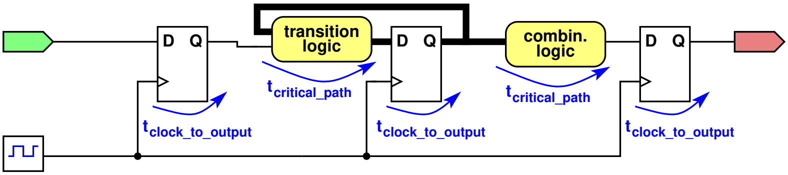

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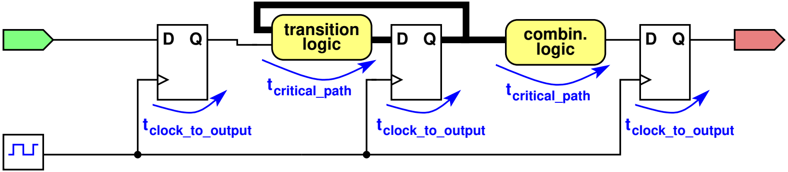

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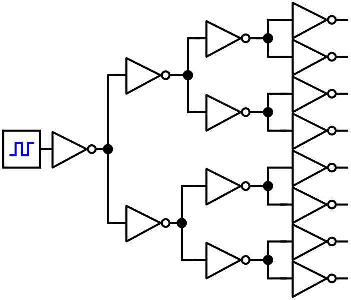
- The one thing that we did not consider yet is the question: *What happens with the clock line?*
- Just putting a wire over the whole chip probably will not work as:
  1. The clock line would have a big capacitive load.
  2. The RTL-design method assumes that the rising edge of the clock arrives at all flipflops at the same time.

Avoiding big capacitive load



- Let's look into the first point: reducing the big capacitive load:
- Using a binary tree of inverters will reduce the load on each output, however, what is the result of this operation?

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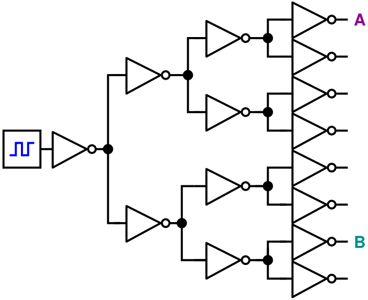

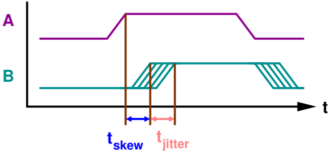

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- We also will have a jitter.

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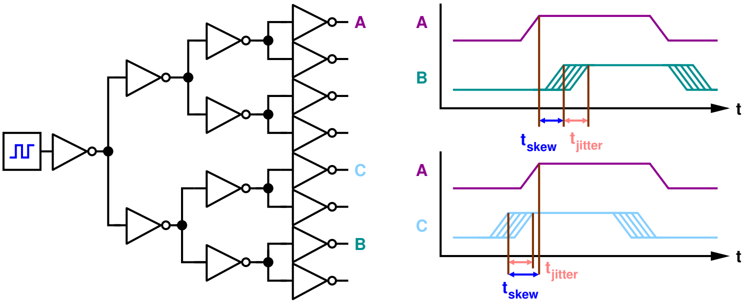

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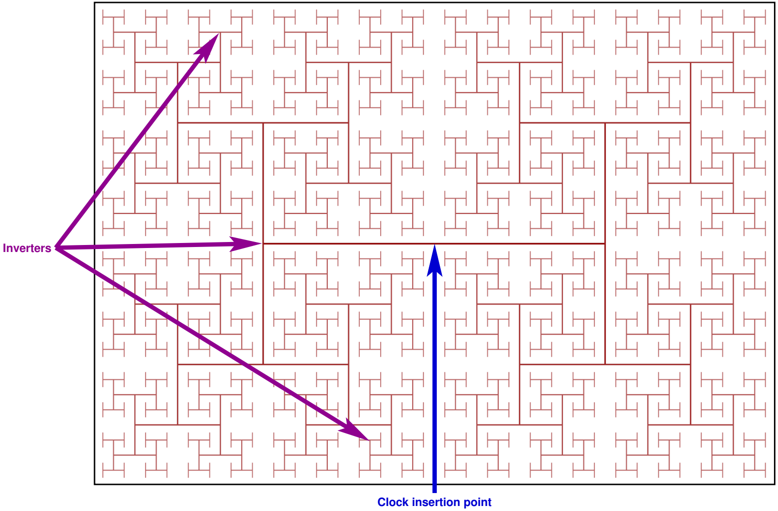
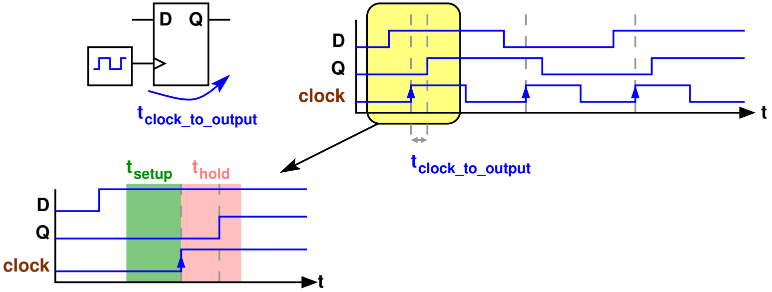
- We also will have a jitter.
- Note that we can also have a negative skew that reduces the influence of the jitter.

Reducing jitter and skew



- One of the methods is to make a *clock tree* in form of a H-tree.
- However, we still have a clock-uncertainty of approx. $2 \cdot t_{skew} + t_{jitter}$.

Remember: Setup and hold



- Remember: a real flipflop has a setup and hold time in which the D-input needs to be kept stable (otherwise the flipflop goes into meta stable state).

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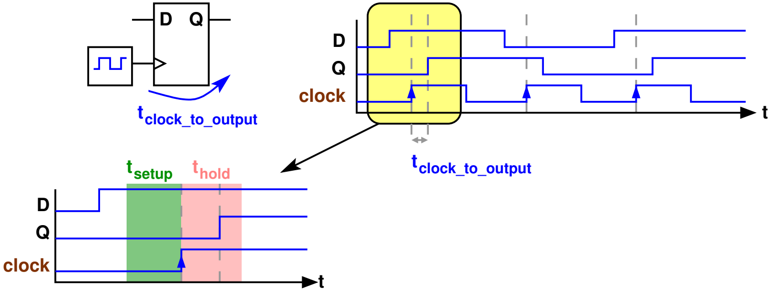
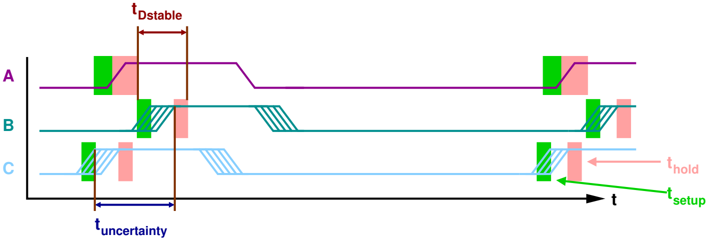


- Remember: a real flipflop has a setup and hold time in which the D-input needs to be kept stable (otherwise the flipflop goes into meta stable state).
- So which kind of situation we now can have in the real-world taking into account the *clock tree*:
  1. The path is too fast (race-condition).
  2. The path is too slow (frequency cannot be met).

Race condition



- Putting it all together gives us the above timing diagram.

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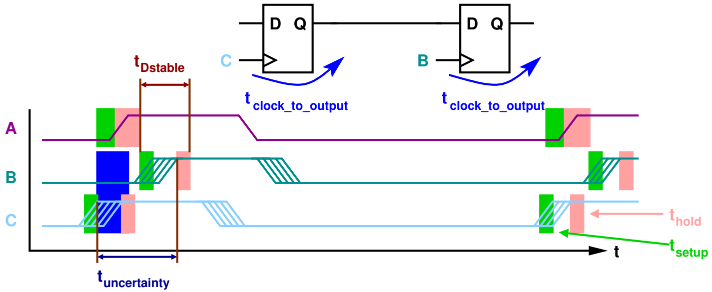

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- Let's take as example a shift-register, there are now two situation that can happen:
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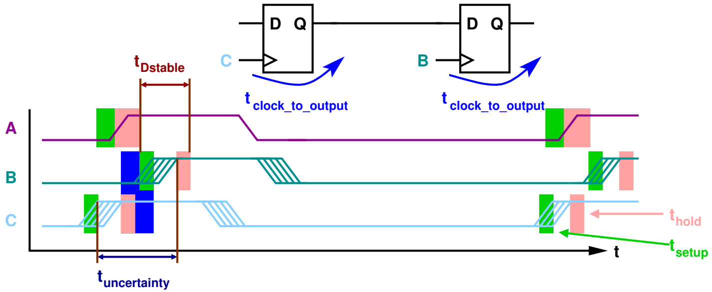

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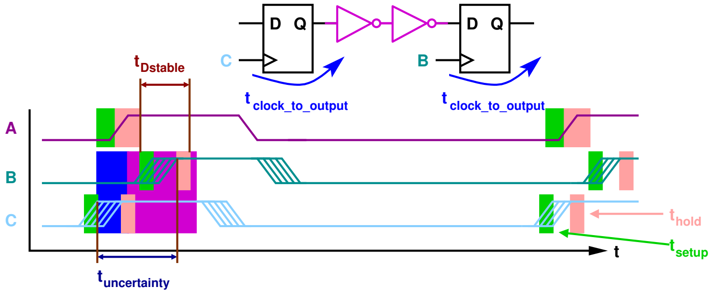

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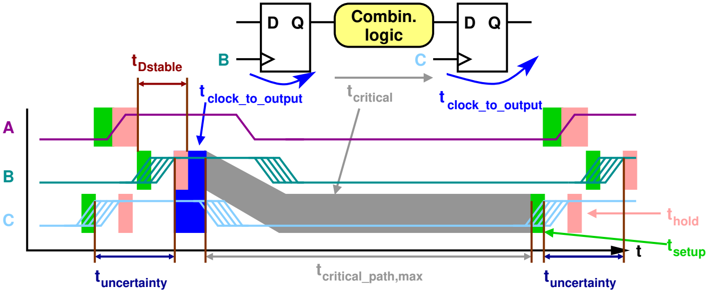
- This problem can be solved by inserting a delay between the flipflops `C` and `B`. Fortunately this is done for us by the synthesis and/or P&R-tools.

Timing not met



- The other situation is shown above (hence $t_{p,clock} = t_{clock\_to\_output} + t_{critical,max} + t_{setup} + t_{uncertainty}$).
- We know that during the critical path time we may have hazards on the D-input of flipflop C, and that the correct value is available after $t_{critical\_path}$.

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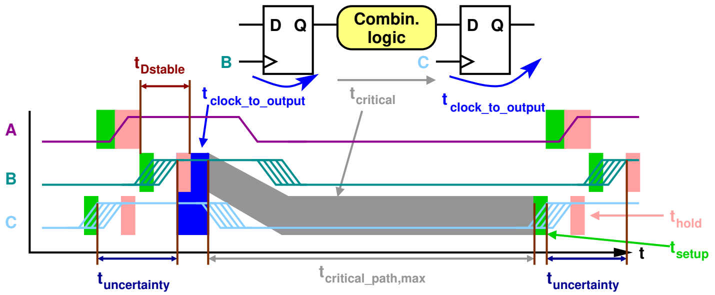

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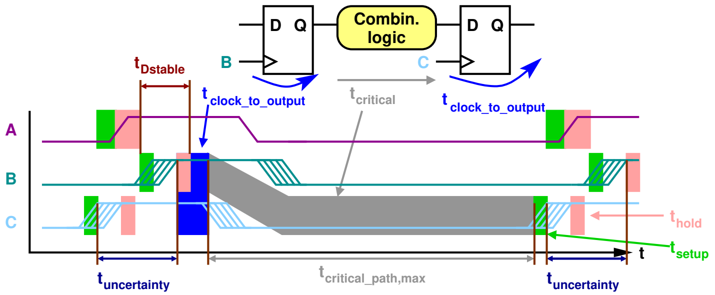

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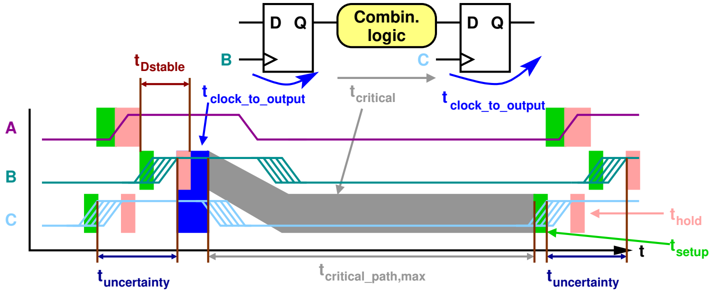
- Timing is not met when there exists at least one combinational logic path with a $t_{critical\_path} > t_{critical\_path,max}$.

Timing closure



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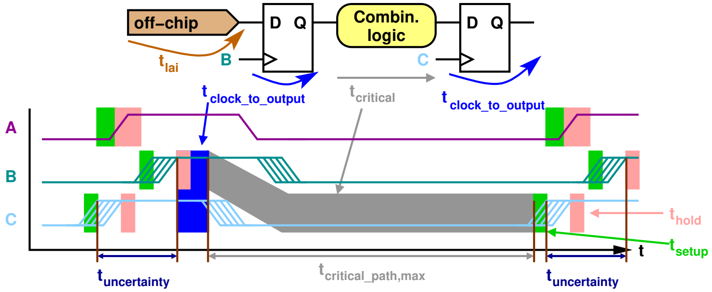

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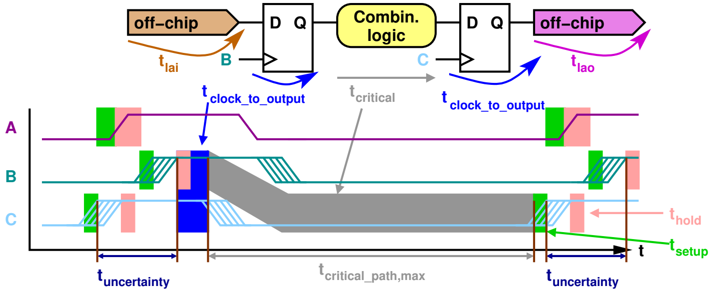

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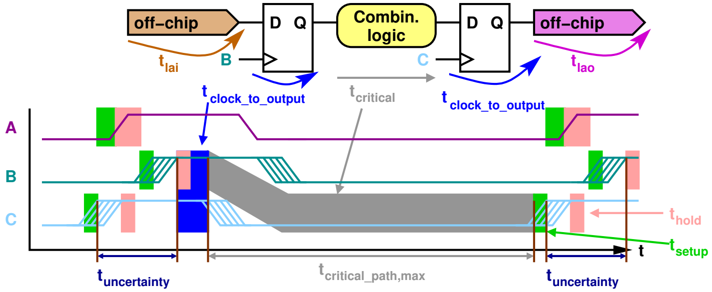

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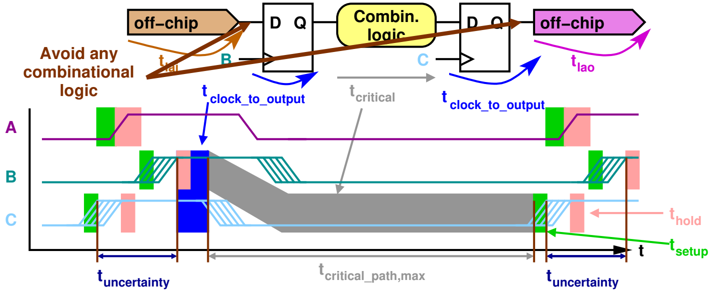
- These two numbers depend on the chips connected to this one and are in general more difficult to determine.

Timing closure off-chip



- The later aspect is “easily” solved by not using any combinational logic between the input(s) and the fist flipflop(s) and no combinational logic between the last flipflop(s) and the output(s).
- This has the advantage that you do not have any hazards outside of your chip (good thing!).

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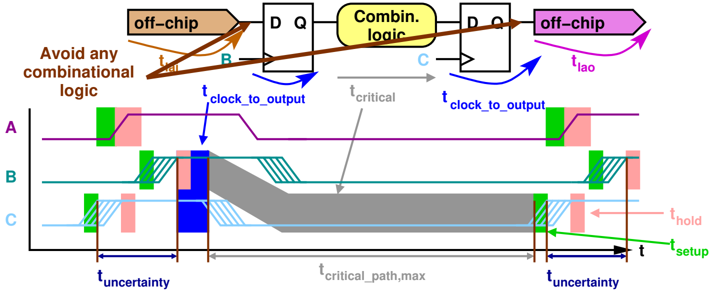

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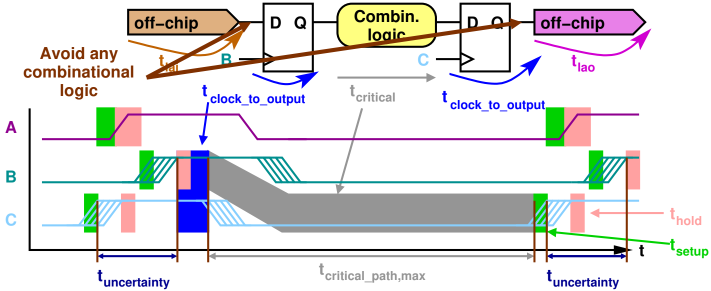

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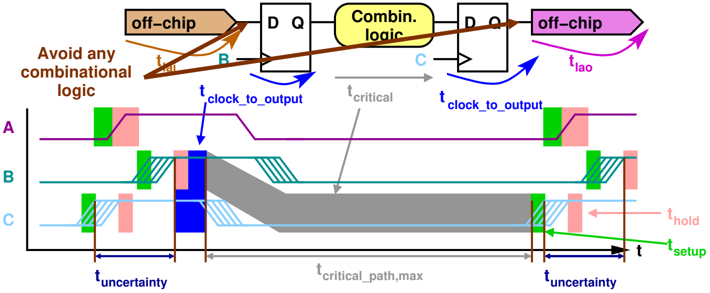

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- Note: even your internal delays due to the clock-tree may impose problems.....

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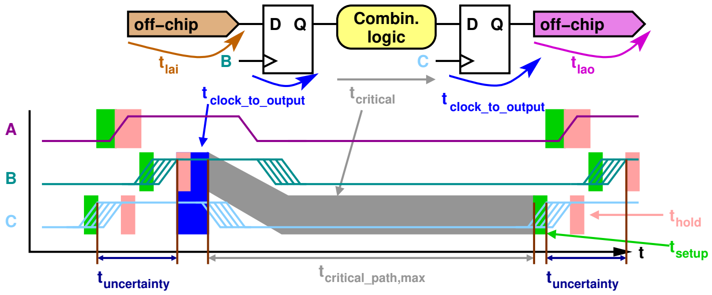
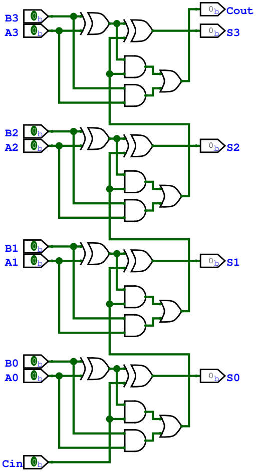


- The on-chip aspect has some methods that you can use, but be aware, the synthesis tool might be more “intelligent” than you are (compare the compiler for a programming language).
- These methods are more for things that the synthesizer does not know about (for example what does your program do):
  - Fined-grain paralyzing.
  - Multi-cycling.
  - Pipelining.

Speeding-up your circuit



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- Assume that this adder is in the critical path.

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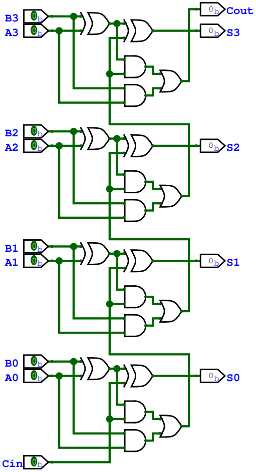

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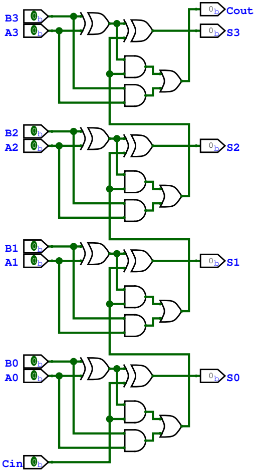

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- So what can we do to speed-up this circuit, there are basically three methods:
  - Trading-off bigger area/energy consumption against speed.

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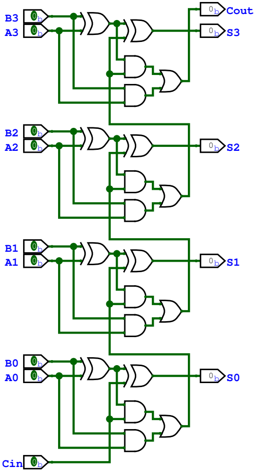

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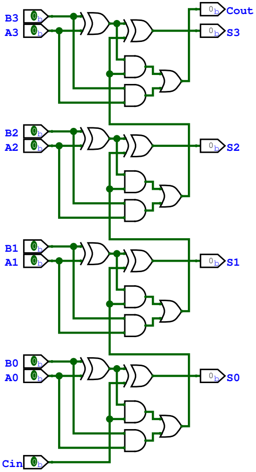

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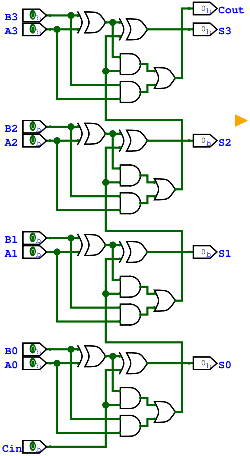
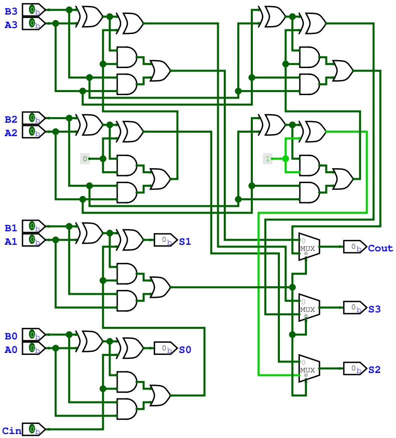
  - Trading-off bigger area/energy consumption against speed.
  - Trading-off speed against area/energy consumption.
  - Trading-off latency against speed.

Fined-grain paralyzing



- In this method we cut the circuit (critical path) in 2 (or more) parts.



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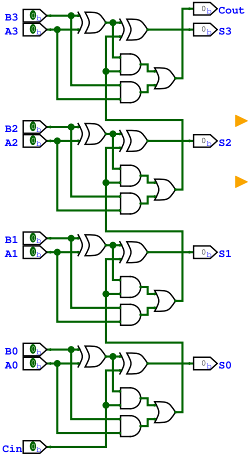

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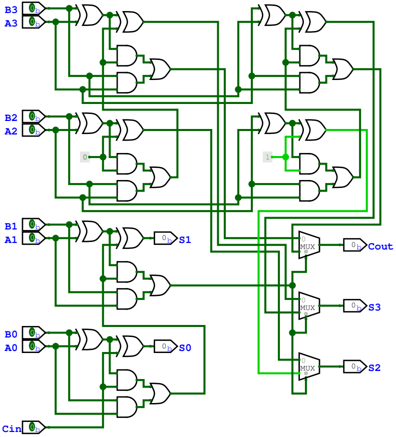

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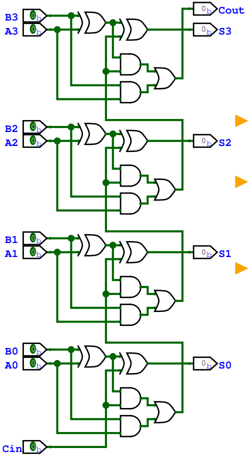

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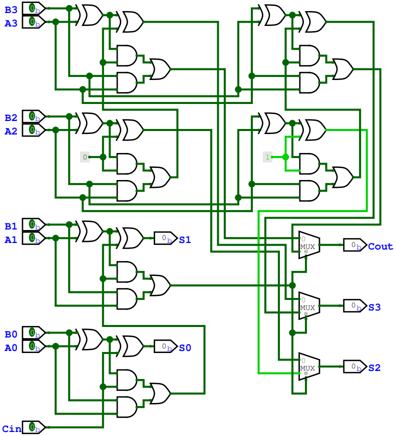
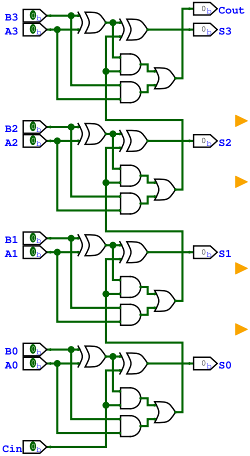
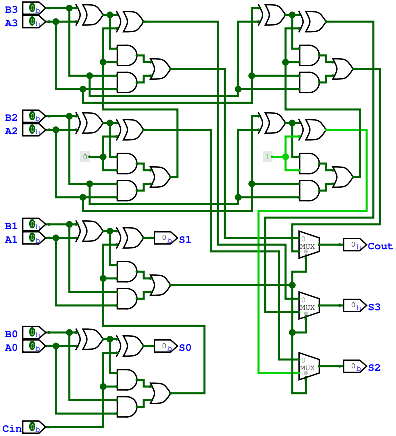
- Finally the real carry selects the correct result.



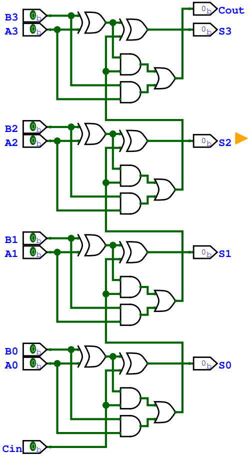
Fined-grain paralyzing



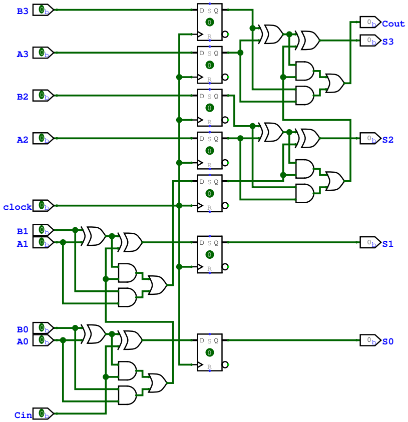
- In this method we cut the circuit (critical path) in 2 (or more) parts.
- The above part is duplicated and calculates the two answers depending the result of the carry.
- Finally the real carry selects the correct result.
- We now have a *carry select adder (CSA)* that is almost twice as fast.



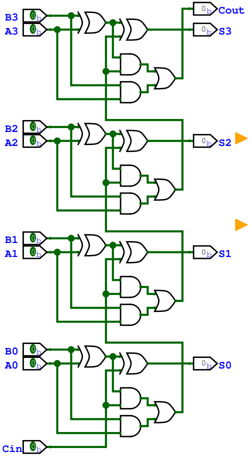
Pipelining



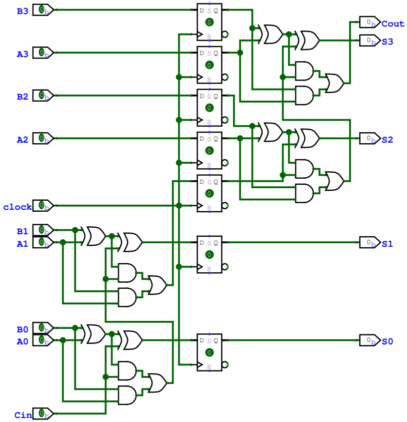
In this method we divide the critical path in 2 (or more) parts and place a row of flipflops between the parts.



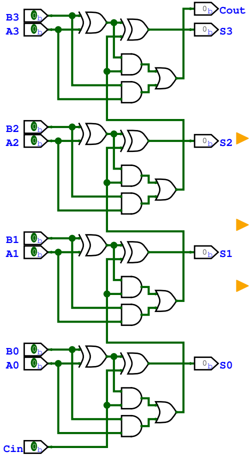
Pipelining



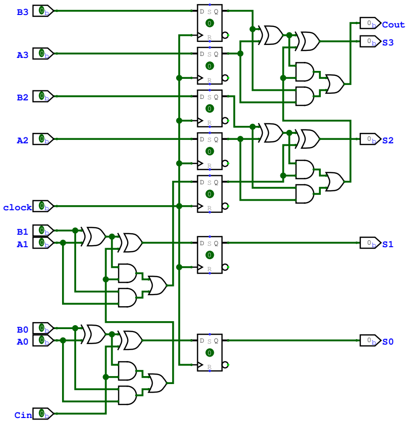
- In this method we divide the critical path in 2 (or more) parts and place a row of flipflops between the parts.
- The advantage is that we can do a calculation each cycle.



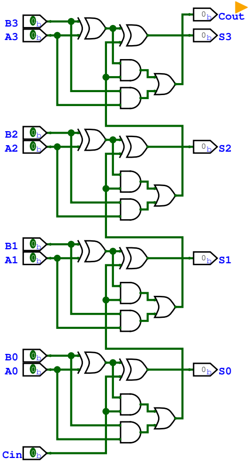
Pipelining



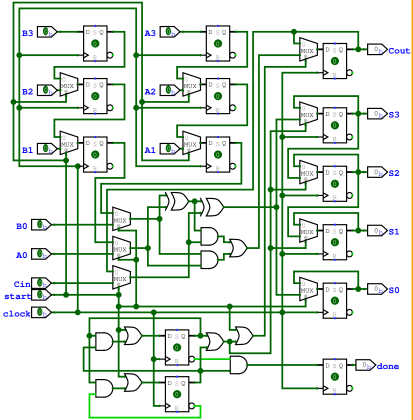
- In this method we divide the critical path in 2 (or more) parts and place a row of flipflops between the parts.
- The advantage is that we can do a calculation each cycle.
- However, we introduce a latency. This could cause problems in case of a feed-back loop.



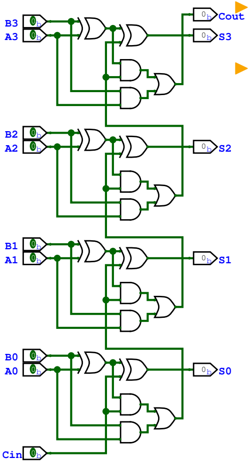
Multi-cycling



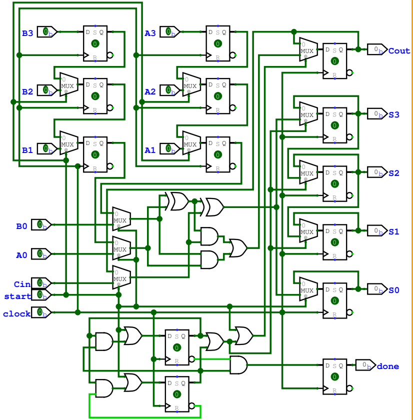
In this method we calculate at each cycle one bit.



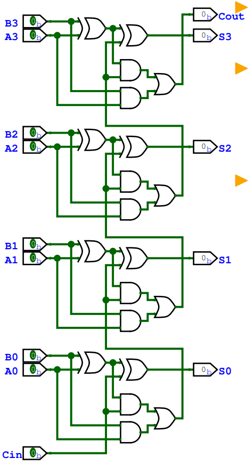
Multi-cycling



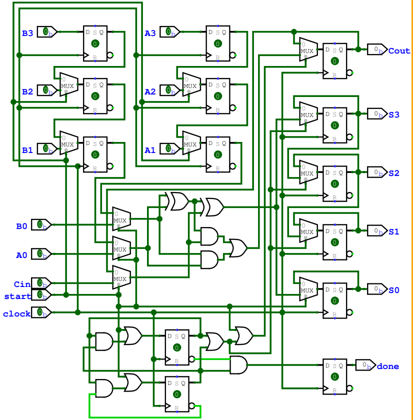
- In this method we calculate at each cycle one bit.
- Of course this has an impact on the performance, as now the addition takes 4 cycles instead of a single cycle.



Multi-cycling



- In this method we calculate at each cycle one bit.
- Of course this has an impact on the performance, as now the addition takes 4 cycles instead of a single cycle.
- But think of the alternative, slowing down all the other functions as we need to reduce the maximum frequency of the CPU.



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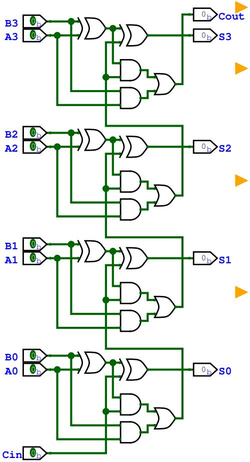

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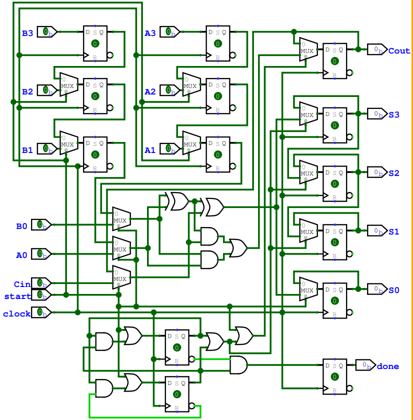
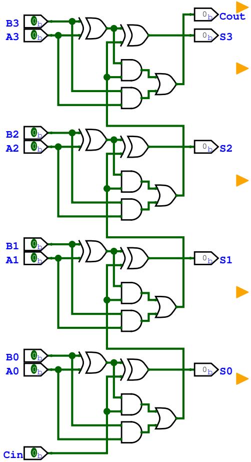
- Very often we perform a *radix-N* multi-cycle operation where at each cycle N-bits are determined.



Multi-cycling



- In this method we calculate at each cycle one bit.
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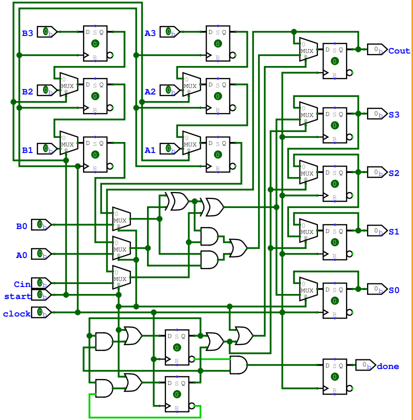
- But think of the alternative, slowing down all the other functions as we need to reduce the maximum frequency of the CPU.
- Very often we perform a *radix-N* multi-cycle operation where at each cycle N-bits are determined.
- Of course, when `A` and `B` are guaranteed to be constant between `start` and `done`, we can replace the input shift-registers by a multiplexer.



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Conclusion

- We have seen the details that determine the maximum speed with which we can safely operate a circuit.
- We also have visited three methods how to speed-up a critical path.
- Each of these methods makes a trade-off between area, energy consumption, complexity and speed.
- It depends on the requirements which of these methods can be applied to a given hot-spot.