EPFL

CS-476:
Embedded System Design

Practical work 1

Simulation, testbenches and FIFO

Version:
1.0

Contents

1 Simulation

We are going to simulate with Icarus Verilog. The documentation can be found here. To perform this first exercise download the counter with it's testbench from moodle. There are some steps to follow to simulate:

1. execute:
   `iverilog -s counterTestBench -o testbench counter.v counter_tb.v`
   in a terminal. the option `-s` defines the toplevel, and `-o` the name of the simulation executable.
2. perform the simulation by:
   `./testbench`
   This will generate a file called `counterSignals.vcd`.
3. Now we can observe the timing-diagram by:
   `gtkwave counterSignals.vcd`
   This will open a graphical window. The user manual of gtkwave can be found here.

Look at the timing diagram and try to match it with the given testbench. These programms we are going to use a lot during this course, so make sure that you understand the flow.

2 Exercise

Now that you are familiar with the simulation process we are going to implement a FIFO-buffer. The inputs, outputs, and parameters are given by:

```
module fifo #(parameter nrOfEntries = 16,
              parameter bitWidth = 32)
             (input wire                  clock,
                                          reset,
                                          push,
                                          pop,
              input wire [bitWidth-1:0]   pushData,
              output wire                 full,
                                          empty,
              output wire [bitWidth-1:0]  popData);
endmodule
```

2.1 Task1

Write the complete verilog code that realizes the correct functionality of the fifo. Hint: the verilog function `$clog2(N)` determines $\left\lceil \frac{ln(N)}{ln(2)} \right\rceil$. You will require 2 counters, an SSRAM and some glue logic.

2.2 Task2

Write a simple testbench for the FIFO and simulate the FIFO with it's testbench.