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A cryo-CMOS chip that integrates silicon quantum dots and multiplexed dispersive readout electronics

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As quantum computers grow in complexity, the technology will have to evolve from large distributed systems to compact integrated solutions. Spin qubits in silicon quantum dots are thought to offer good scalability because both spin-carrying quantum dots and support complementary metal–oxide–semiconductor (CMOS) electronics can, in principle, be monolithically integrated on a single chip. However, monolithically integrated quantum–classical hybrid circuits based on industry-standard CMOS technology remain limited. Here we report a millikelvin integrated circuit fabricated using 40 nm CMOS technology that integrates silicon quantum-dot arrays with support electronics in an architecture that allows the array to be efficiently addressed and read. The architecture contains integrated microwave lumped-element resonators for dispersive sensing of the charge state of the quantum dots, mediated via digital transistors in a column–row-addressing distribution. With the chip, we demonstrate combined time- and frequency-division multiplexing, which scales sublinearly the resources as well as footprint required for readout.

Quantum computing could be used to solve computational problems more efficiently than classical computers[1], but constructing the necessary quantum hardware[2,3] is a considerable technological challenge. Single electron spins isolated in silicon quantum dots (QDs) are a promising solid-state system to create such hardware: recent demonstrations of long coherence times[4], high-fidelity spin readout[5], and one- and two-qubit gates[6–8] fulfil the basic requirements to build a quantum computer approaching fault-tolerant thresholds[9]. Silicon QDs are typically fabricated using custom processes[4,10], but recent works have suggested that they can be manufactured at scale using industry-compatible[11] or even industry-standard processes[12,13].

Different blueprints of large-scale quantum computers in silicon have been developed[14–16], and the proposals share a common concept: (1) metal–oxide–semiconductor (MOS)-based QD arrays to host the qubits and (2) digital and analogue classical electronics for control and readout[17]. Full system integration would lead to a reduced footprint, ease of signal synchronization, reduced latency and minimized inter-chip wiring[18,19]. However, the ultimate level of possible integration is still uncertain, given the reduced availability of cooling power at millikelvin temperatures for typical classical electronics. Exploring the limits of integration[20,21] is, hence, critical to creating a full-fledged solid-state quantum processor.

For silicon, one approach has been to operate qubits at elevated temperatures (~1.2 K)[22,23] to enable larger cooling power budgets for classical electronics[24]; however, so far, this has come at the cost of reduced fidelity and/or coherence times. Alternatively, integrated circuits (ICs) that operate at millikelvin temperatures have been produced for control[25], readout[26] or signal multiplexing[27–29], and single devices have been used for time-multiplexed readout[30]; however, these circuits have not been fully integrated with quantum devices.

In this Article, we report an IC fabricated using an industrial 40 nm complementary metal–oxide–semiconductor (CMOS) technology that enables resource-efficient and scalable multiplexed microwave readout of a non-interacting array of silicon QDs, all operating at millikelvin temperatures in the same monolithic chip. Individual QDs can be addressed using a row–column random-access architecture with digital transistors, allowing a quadratic reduction in the number of required inputs. The readout is performed using gate-based microwave reflectometry[31]—a technique readily compatible with industrial CMOS technology—the core elements of which are fully integrated on our chip. Finally, we demonstrate combined time- and frequency-domain multiplexing, thus enabling a sublinear scaling of the number of readout resonators per QD (hence minimizing the circuit footprint), as well as preserving a degree of parallel readout, ideal for quantum error correction (QEC). Our circuit could be scaled up by replicating its basic building blocks to create a large-scale readout platform.

Fully integrated DRAM-like readout matrix architecture

Our quantum–classical readout interface has been designed and fabricated in an industrial 40 nm bulk CMOS technology. Figure 1a,b presents the chip micrograph and its schematic, respectively (Methods explains the chip design and Extended Data Table 1 lists the circuit component values). The modular architecture consists of a 3×3 array of nine identical cells, arranged in a row–column random-access configuration similar to a dynamic random-access memory (DRAM). Each cell contains a silicon QD device, that is, Q_{ij} ($i,j=1, 2, 3$), implemented as a MOS transistor. Furthermore,

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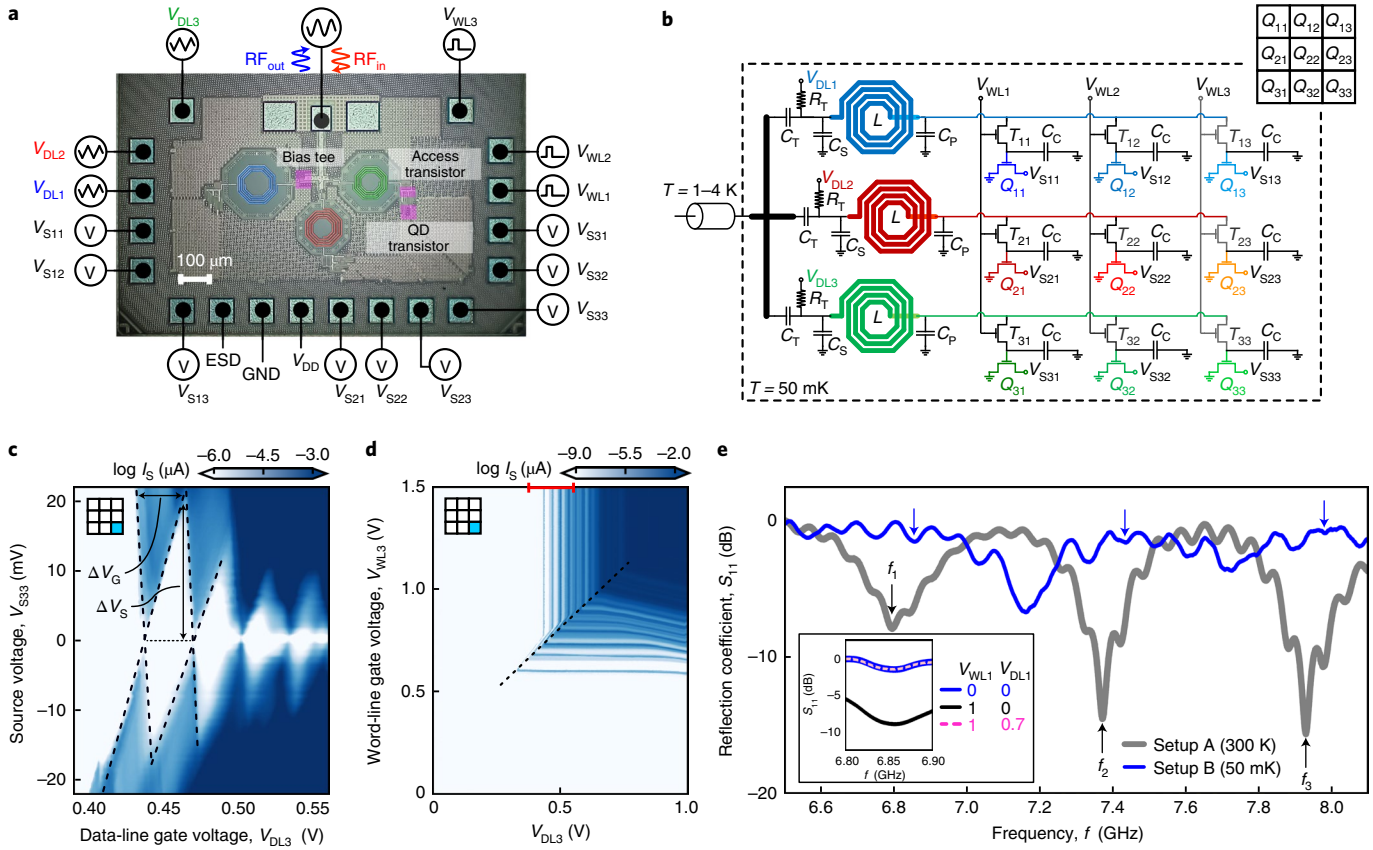

Fig. 1 | Fully integrated cryogenic CMOS quantum–classical matrix. a, Micrograph of the IC, with the corresponding control signals. ESD, electro-static discharge protection; GND, ground; V_{DD}, power supply. **b**, Schematic of the cryogenic CMOS readout matrix consisting of three integrated *LC* resonators (Resonator$_1$ (blue), Resonator$_2$ (red) and Resonator$_3$ (green)), access transistors T_{ij} and QD transistors Q_{ij}, word-lines V_{WLj}, data-lines V_{DLi}, source voltages V_{Sij}, bias tees R_T–C_T and storage capacitors C_C. Inset: a 3 × 3 grid representing the 3 × 3 QD transistor array. **c**, Coulomb diamonds at $V_{WL3} = 1.5$ V with V_{DL3} ranging from 0.39 to 0.56 V, as marked by the red line in **d**. **d**, Stability diagram as a function of V_{WL3} and V_{DL3} with $V_{S33} = 0.01$ V. **e**, Frequency spectrum of the multi-resonator for Setup A at 300 K and Setup B at 50 mK, showing the three resonant frequencies. Setup A: direct measurement with a vector network analyser (VNA) → cable → chip → cable → VNA. Setup B: the chip is placed in the dilution refrigerator, and connected via VNA → attenuator → cable → circulator → chip → circulator → low-noise amplifiers → cable → VNA (Methods and Extended Data Fig. 1 describe the experimental setup). The resonant frequencies are found to be $f_1 = 6.810$ GHz, $f_2 = 7.374$ GHz and $f_3 = 7.941$ GHz for Resonator$_1$, Resonator$_2$ and Resonator$_3$, respectively, at 300 K. The black and blue arrows indicate the resonant frequencies at 300 K and 50 mK, respectively. Inset: zoomed-in view of Resonator$_1$ at 50 mK for different V_{WL1} and V_{DL1} values.

the gate of each quantum device is connected to the source of an access MOS transistor (channel width $W = 15$ μm; channel length $L = 40$ nm), allowing conditional access, and to a storage capacitor (200 fF), storing the voltage at the gate of the quantum device. The access transistors in column j are controlled by the same word-line signal V_{WLj}. The cells in row i are connected to the shared data-line signal V_{DLi} (providing a bias voltage to control the QDs through an on-chip bias tee) as well as to the inductor–capacitor (*LC*) resonator Resonator$_i$ to perform microwave reflectometry readout[32,33]. When applying the data-line voltage V_{DLi} and the word-line voltage V_{WLj}, the quantum device Q_{ij} is accessed, and its charge state can be read out via Resonator$_i$. We also included independent source voltages V_{Sij} to perform a full electrical characterization of the individual QD devices in the quantum regime.

This architecture reduces the resources needed for the control and readout of N quantum devices from N to just $2\sqrt{N}$ lines and $\sqrt{N}$ resonators, respectively, substantially decreasing the circuit complexity of current paradigms.

Quantum–classical circuits in industrial CMOS

The QD devices are designed as minimum-size ($W = 120$ nm; $L = 40$ nm) nMOS transistors to minimize the channel volume. The devices have a low threshold voltage V_{th} and they are implemented as single-gate planar npn transistors in a deep n well, to isolate them from substrate noise. When we cool these devices down to 50 mK and apply a positive V_{DLi} voltage ($\sim V_{th}$) with high V_{WLj}, single electrons are trapped in the small area under the gate at the oxide–silicon interface, that is, few-electron QDs[34] are formed, which are observed at low V_{Sij} (Fig. 1c).

Here we measure the source–drain current I_S as a function of the V_{DLi} and V_{Sij} voltages for the QD transistor Q_{33} and we observe Coulomb diamonds. From this plot, a charging energy $E_c = e \times \Delta V_S = 21.4$ meV (e is the electron charge) can be extracted, which enables electron trapping even at 4.2 K as $E_c \gg k_B T$ (k_B and T are the Boltzmann constant and temperature, respectively). At 50 mK, all the nine devices in the matrix exhibit Coulomb-blockade oscillations (Supplementary Section 1, Supplementary Figs. 1 and 2 and Supplementary Table 1 show a QD variability study).

In Fig. 1d, we demonstrate the functionality of the access transistor–QD cell and highlight the allowed and forbidden regions for readout. When $V_{WL3} - V_{DL3} < 0.277$ V, the access-transistor channel resistance R_{acc} becomes comparable to the QD-transistor gate leakage resistance R_G; therefore, the effective equilibrium gate voltage for the QD transistor $V_{DL,eff} = (V_{DL} \times R_G)/(R_{acc} + R_G)$ is reduced.

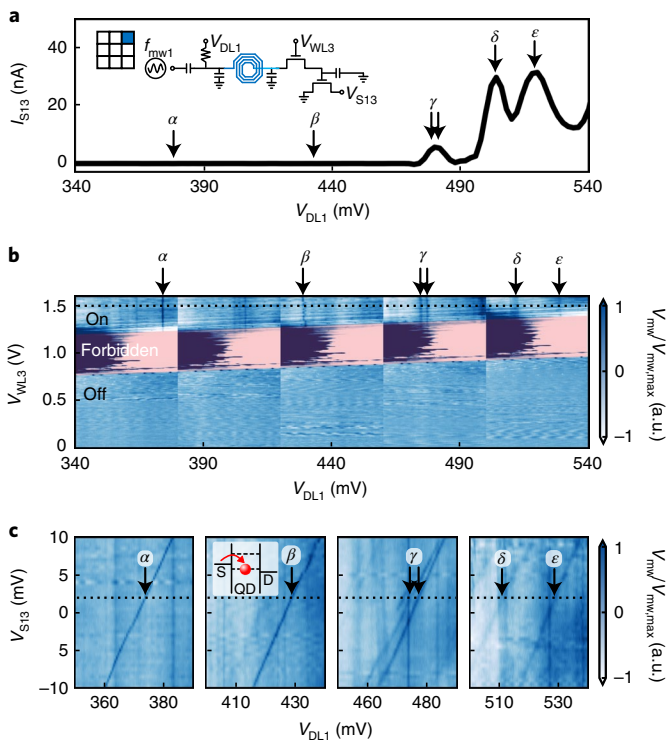

Fig. 2 | Integrated gate-based reflectometry. a, Direct current transport measurement for device Q_{13}: I_{S13} as a function of V_{DL1}. Inset: circuit diagram of a single cell. **b**, Normalized microwave reflected voltage as a function of V_{WL3} and V_{DL1} at $V_{S13}=2$ mV. This diagram is the union of five individual measurements as a function of V_{WL3} and V_{DL1}, resulting in the repetitive blue/pink pattern in the forbidden region. **c**, Microwave-reflectometry stability diagrams as a function of V_{S13} and V_{DL1} for the Coulomb peaks α, β, γ, δ and ε at $V_{WL3}=1.5$ V. Inset: energy diagram of the source–QD transition, generating signal β. S, source; D, drain. The dotted line in **b** corresponds to the dotted lines in **c**. The measurements are performed at 50 mK, and the carrier frequency is $f_{mw1}=6.877$ GHz.

Then, the QD can be decoupled from the data line (Supplementary Section 2 and Supplementary Fig. 3 show a voltage retention study). However, when $V_{WL3}-V_{DL3}$ is far higher than this threshold (above the dashed black line in Fig. 1d), then $V_{DL,eff}\approx V_{DL}$, and Coulomb-blockade oscillations are observed as a function of V_{DL3}.

This demonstrates the realization of a quantum–classical IC in industrial bulk CMOS technology at 50 mK.

Microwave frequency characterization

We designed the resonators Resonator$_i$ to have different resonant frequencies f_i to enable frequency-selective readout over the corresponding rows. Figure 1e shows the frequency spectrum for the integrated *LC* resonators (Methods and Extended Data Fig. 1 describe the experimental setup). At 300 K, the reflection coefficient S_{11} (Fig. 1e, grey trace) presents three minima at the resonant frequencies of $f_1=6.810$ GHz, $f_2=7.374$ GHz and $f_3=7.941$ GHz (Supplementary Section 3, Supplementary Fig. 4 and Supplementary Table 2 provide the resonator characterization at 300 K). At 50 mK, when all the V_{WLj} values are set to 0 V, the spectrum shows a high mismatch (Fig. 1e, blue trace), whereas by turning on, for example, column voltage V_{WL1}, all the access transistors on that column turn on, modifying the total impedance of the system and hence the reflected power (Fig. 1e (inset), black trace). The resonators were designed to match the high impedance of the gate of the QD device to the 50 Ω microwave input when the access transistors are on, allowing maximum power transfer and enhanced sensitivity[35]. To demonstrate the frequency selectivity of the readout, we then increase the data-line voltage V_{DL1} to turn off the access transistor T_{11} (Fig. 1e (inset), pink dashed line). Only when T_{11} is switched off, the reflected power at f_1 returns to its original value. At 50 mK, the probing frequencies are identified as $f_1=6.872$ GHz, $f_2=7.420$ GHz and $f_3=7.951$ GHz (Supplementary Section 4 and Supplementary Fig. 5 provide the resonator characterization at 50 mK).

Frequency-multiplexing interfaces have been previously reported[26]; however, typically, readout frequencies below 1 GHz have been used[31]. More recently, silicon QDs were interfaced with microwave resonators in the 6–8 GHz range to explore coherent spin–photon interactions[36,37]. Although these resonators enabled a fast state readout[38], hybrid manufacturing was necessary. Here the resonators and QDs are co-integrated in the same industrial CMOS process. Alternatively, the use of integrated active inductors has been proposed for readout[39], but with limited noise performance.

Operating at a higher readout frequency has several advantages. First, it reduces the footprint of the inductors—the largest elements of the architecture. Furthermore, the quality (Q) factor of the resonator, critical for the sensitivity of the technique[40], is higher for smaller inductors used at higher frequencies. Our Q factors are modest ($Q<100$), compared with superconductor-based resonators, but show the state-of-the-art of what can be achieved with industrial CMOS. Finally, the sensitivity of gate-based dispersive readout resonators is higher at higher frequencies[41].

Gate-based dispersive readout

We use resonators as sensors to perform integrated gate-based dispersive readout of the QD charge states. The resonators produce an oscillatory voltage on the gate of the QDs, which results in the cyclic tunnelling of electrons to and from the electronic reservoirs[42]. This can be represented by an equivalent capacitance that modifies the impedance of the resonator, producing a change in the reflected voltage (V_{mw}).

To benchmark the method, we perform d.c. transport measurements (Fig. 2a) for device Q_{13}, and observe the Coulomb peaks γ, δ and ε. We compare these results with those measured via reflectometry in the same V_{DLi} region (Fig. 2b), while exploring the dependence of the signal with the state of the access transistor. At low $V_{WL3}-V_{DL1}<(0.786-0.340)$ V, the access transistor is highly resistive and the microwave signal is highly attenuated (off region). At intermediate $V_{WL3}-V_{DL1}$ values, the access transistor is in the depletion region and the oscillatory voltage at the transistor input produces changes in the capacitance that are picked up as large changes in the reflected signal (forbidden region). Finally, at high $V_{WL3}-V_{DL1}>(1.278-0.340)$ V, the access transistor presents a low-resistance state and the microwave signal can travel through (on region), exciting cyclic tunnelling in the QD, which manifests as regions of enhanced V_{mw}. Besides the same transitions as in Fig. 2a, two additional peaks, namely, α and β, are observed. These are the results of cyclic tunnelling to one of the electron reservoirs only (as opposed to current, which requires sizable tunnel rates to both source and drain). This highlights the efficiency of gate-based sensing in detecting electronic transitions even if the QDs are offset from the centre of the channel and present low tunnel rates to one ohmic contact. To provide further evidence of the nature of these transitions, we present individual V_{Sij}–V_{DLi} maps (Fig. 2c). The dependence on V_S suggests that peaks α and β originate from cyclic tunnelling to the source. A lineshape analysis (Methods, Extended Data Fig. 2 and Extended Data Table 2 show the data analysis) from the data in Fig. 2c reveals a signal-to-noise ratio (SNR) of 28.7 in 400 ms of integration time and a tunnel rate to the source of 48.3 GHz for the peak α. These measurements represent the demonstration of fully integrated conditional gate-based readout of QDs implemented in an industrial CMOS technology.

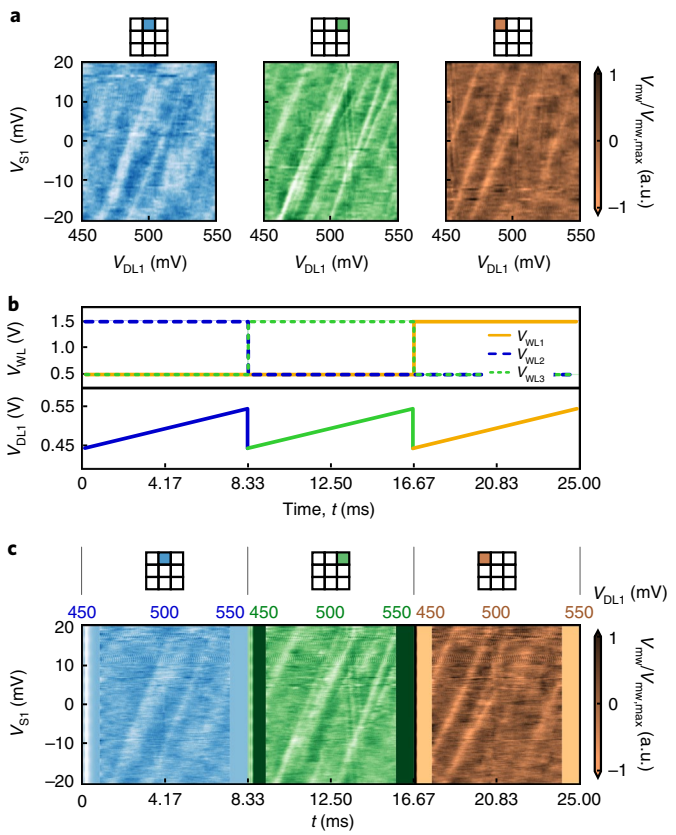

Fig. 3 | Integrated time-multiplexed readout. a, Individual gate-based reflectometry measurements for quantum devices Q_{12} (blue), Q_{13} (green) and Q_{11} (gold) with reflectometry signals V_{mw} as a function of V_{S1} and V_{DL1}. **b**, Sequences of V_{WLj} and V_{DL1} for time-domain multiplexing reflectometry sensing of Q_{12}, Q_{13} and Q_{11}. V_{WL2} (blue), V_{WL3} (green) and V_{WL1} (gold) follow a square wave between 1.5 and 0.5 V in time t. V_{DL1} follows a ramping wave synchronized to V_{WLj} in the time domain. **c**, Stability diagrams as a function of V_{S1} and time t for $Q_{12} \rightarrow Q_{13} \rightarrow Q_{11}$ corresponding to the time-domain sequences of V_{WLj} and V_{DL1} in **b**. In **a** and **c**, the source voltage is $V_{S1} = V_{S1j} = V_{S11} = V_{S12} = V_{S13}$ and the carrier frequency is $f_{mw1} = 6.872$ GHz. Measurements are performed at 50 mK. The data presented in **c** are processed by using the data processing method described in Methods and Extended Data Fig. 3.

Time-multiplexed readout

We then perform time-multiplexed reflectometry measurements of QD devices in the same row, by addressing them at the frequency of the shared resonator and activating the corresponding columns, one after the other. We choose Resonator$_1$ with carrier frequency $f_{mw1} = 6.872$ GHz and use the 1×3 QD array $[Q_{1j}]$.

We first measure the charge stability diagrams for each individual Q_{1j} (Fig. 3a), when the corresponding access transistor is active. We use such data as the control set; then, we perform the dynamic characterization in time-domain multiplexing and compare the results. The dynamic voltage sequence consists of a digital high V_{WLj} voltage ($V_{WLj}^{High} = 1.5$ V) applied to the cell to be read, whereas the other two cells are set at low V_{WLj} voltages ($V_{WLj}^{Low} = 0.5$ V). The digital values are selected according to the on–off regions shown in Fig. 2b. During that period, we simultaneously apply a voltage ramp to data-line V_{DL1} to acquire data from the Q_{1j} of the corresponding cell. We then sequentially raise the V_{WLj} voltage of the next cell, whereas the other two are kept low. The full sequence is illustrated in Fig. 3b, where we first measure Q_{12} followed by Q_{13} and Q_{11}. Finally, we repeat the full sequence as we step the V_{S1j} voltages to acquire the charge stability maps shown in Fig. 3c (Methods and Extended Data Fig. 3 describe the data processing). The match between the control set and dynamic measurements indicates the success of the protocol.

We note that time-domain multiplexing does not necessarily require sequential addressing, but it can be performed in a random-access manner similar to DRAM architectures. These results represent fully integrated time-multiplexed reflectometry measurements of silicon QDs and demonstrate an important reduction in the analogue infrastructure required for the readout of quantum circuits, since multiple devices can be read by a single resonator.

Frequency-multiplexed readout

Once time multiplexing (addressing columns) in reflectometry has been demonstrated, using the second degree of freedom in the matrix, we demonstrate frequency multiplexing (addressing rows). For this experiment, we use Resonator$_2$ at $f_{mw2} = 7.419$ GHz with Resonator$_1$ at $f_{mw1} = 6.873$ GHz to perform a parallel readout of two independent QDs on different rows (addressable at different frequencies). As shown in Fig. 4a (up to 8.33 ms), word-line voltage V_{WL2} is kept high to activate column 2, whereas both V_{DL1} and V_{DL2} are ramped up to activate rows 1 and 2. As a result, a 2×1 parallel set of Coulomb peak transitions from Q_{12} and Q_{22} is obtained (Fig. 4b, up to 8.33 ms).

A parallel readout reduces the overall integration time to read large quantum circuits by clustering the readout of a number of devices in the same time step. This feature is of particular relevance to QEC sequences, such as the surface code, which requires continuous qubit readout at scale[9]. These results demonstrate the fully integrated frequency-multiplexed gate-based readout of silicon QDs on a single chip and in the 6-8 GHz range.

Time- and frequency-multiplexed readout

Finally, we combine time- and frequency-domain multiplexing. Resonator$_1$ and Resonator$_2$ are used simultaneously for sensing the sub-arrays $[Q_{12}, Q_{13}]$ and $[Q_{22}, Q_{23}]$, respectively. Similarly to the time-domain multiplexing readout, a sequence of square waves $V_{WL2} \rightarrow V_{WL3} \rightarrow V_{WL2} \rightarrow V_{WL3}$ is applied to the word-lines, as shown in Fig. 4a, to selectively read out the transistors in different columns. Simultaneous arbitrary waves in V_{DL1} and V_{DL2} synchronized to V_{WL2} and V_{WL3}, as shown in Fig. 4a, are applied to read out two parallel rows. The result is a 2×2 matrix of Coulomb maps from the addressed QDs (Fig. 4b). The results presented here demonstrate the combination of time- and frequency-multiplexed gate-based readout for silicon QDs, in a fully integrated platform, with a scalable architecture.

Conclusions

We have reported a cryogenic IC fabricated using industrial 40 nm CMOS technology that co-integrates important elements required in a silicon-based quantum computer: silicon QDs, digital addressing and multiplexed analogue readout electronics. Our results probe the limits of monolithic integration using commercial CMOS technology without any customization and provide a route to scalable, integrated silicon quantum processors.

Qubit operation should be possible for such QDs even in the few-electron regime[43]. Single-qubit control could be achieved by embedding the IC in a three-dimensional cavity to perform electron spin resonance conditionally controlled by Stark shifts[44]. Two-qubit gates will require bringing the cells in close proximity to enable spin-exchange interaction. This would require a shorter gate pitch or smaller technology node.

Dispersive spin readout schemes based on Pauli spin blockade would also require two QDs placed in close proximity to allow spin-dependent tunnelling between the QDs. Current industrial design rules for this process set the gate pitch limit to 120 nm; therefore, some process customization will be required to bring it down to

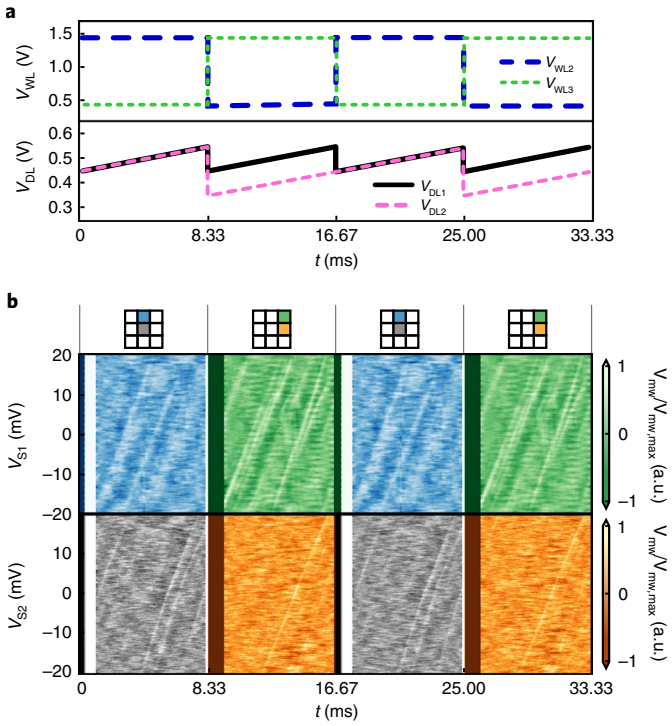

Fig. 4 | Integrated time- and frequency-multiplexed readout. a, Sequence of V_{WLi} and V_{DLi} to perform time- and frequency-multiplexed reflectometry sensing using the 2 × 2 sub-matrix [[Q_{12}, Q_{13}], [Q_{22}, Q_{23}]]. V_{WL2} (blue) and V_{WL3} (green) follow a square wave between 1.5 and 0.5 V, whereas V_{WL1} = 0 V. V_{DL1} and V_{DL2} follow a ramping wave synchronized to V_{WL2} and V_{WL3} in the time domain. **b**, Stability diagrams as a function of V_{Si} and time t for QD devices Q_{12} (blue) → Q_{13} (green) → Q_{12} → Q_{13} addressed through Resonator$_1$ in time sequence and those for Q_{22} (grey) → Q_{23} (orange) → Q_{22} → Q_{23} simultaneously addressed through Resonator$_2$. Here the source voltages are $V_{S1} = V_{S12} = V_{S13}$, $V_{S2} = V_{S22} = V_{S23}$, and the carrier frequencies are f_{mw1} = 6.873 GHz and f_{mw2} = 7.419 GHz for Resonator$_1$ and Resonator$_2$, respectively. The measurements are performed at 50 mK.

~70 nm to achieve sizable tunnel coupling[45]. Moreover, the readout SNR could be improved by lowering the tunnel rates while maintaining them larger than the probing frequency, by increasing the Q factor of the inductors using industry-compatible superconductors (TiN)[46] and by using travelling-wave or Josephson parametric amplification[47]. These improvements could reduce the minimum integration time by a factor of 100 or more, to bring it below the coherence time of the qubits[4]—a necessity for error-correction protocols (Supplementary Section 5 and Supplementary Fig. 6 provide a calculation of the expected power consumption of the architecture as a function of readout time and number of qubits for different scenarios).

Our work focuses on the full integration of quantum devices and classical electronics on a single chip operating at millikelvin temperatures with a limited power budget. In comparison to previous work[20], we demonstrate dispersive readout rather than direct electrical transport measurements, which provides a more scalable readout mechanism. Alternatively, it is also possible to separate the quantum devices from the readout/control electronics[48–50] and envision larger circuit complexity at ~3 K, where the higher power consumption of such microwave transceivers (~100 mW) can be handled. In the future, these two approaches could be combined, leaving only the quantum–classical interface to the millikelvin stage and performing the other readout/control functions at higher temperatures.

Methods

Chip design and implementation. The chip architecture was designed and simulated using Cadence Virtuoso, an industry-standard design tool for IC design and implementation. The initial design of QD transistors, access transistors and passive elements, such as inductors, capacitors and resistors in the resonators and bias tees, was based on existing device models at 300 K provided in the process design kit (PDK) of the 40 nm CMOS foundry. Subsequently, cryogenic models[51,52] have been used to establish a more predictive circuit design at temperatures of 1–4 K, based on modified compact models for transistors, adjusted lumped-element equivalent models for resistors, capacitors and inductors, and electromagnetic (EM) simulations with a modified cryogenic substrate for custom microwave signal lines and connections. This allowed to provide a closer prediction of the chip performance at 50 mK, given that no established models exist for cryogenic circuit design at 1–4 K, let alone deep-cryogenic temperatures of 50 mK. The final simulations of chip operation and performance have been executed using Cadence Virtuoso with such custom-modified cryogenic models and Keysight ADS Momentum (an industry-standard three-dimensional planar EM solver) for the EM simulations of the whole chip, including all the microwave lines, resonators, input ground–signal–ground (GSG) pads, bond wires and external printed-circuit-board (PCB) substrate, using modified material properties for cryogenic operation. The physical layout was also implemented with Cadence Virtuoso, whereas physical design verification in terms of design rule check (DRC) and layout versus schematic (LVS) was performed using Mentor Graphics Calibre. The chip was finally fabricated by a standard very-large-scale integration (VLSI) manufacturing process in 40 nm technology on a multi-project wafer (MPW) without any custom modification. The values of the circuit components (Fig. 1b) are listed in Extended Data Table 1.

Experimental setup. All the measurements reported at 50 mK were performed in an Oxford Instruments Triton 200 dilution refrigerator. The designed chip was glued to a PCB and wire-bonded to a microwave transmission line on board. The device under test (DUT) was placed on the sample stage of the dilution refrigerator. D.c. measurements were performed using filtered constantan twisted pairs in the dilution refrigerator connected to a room-temperature parameter analyser HP 4156A, and/or a source measure unit (SMU) Keithley 2400, used to apply and measure the voltages and currents of the source, gate and drain. The gate d.c. voltages were alternatively applied using voltage sources HP 3245A and Keysight 33500B. Reflectometry measurements were performed with a modified setup, including a discrete cryogenic circulator (QuinStar QCY-G0400801) placed at the mixing chamber plate of the dilution refrigerator and a discrete cryogenic amplifier (Low Noise Factory LNF-LNC4_8C) placed on a higher temperature stage (~3 K). A vector network analyser (Rohde & Schwarz ZVA 24) has been used to measure the frequency spectrum. To perform gate-based reflectometry measurements, externally, additional low-noise amplifiers (Pasternack PE1524 and/or PE1522) and an in-phase/quadrature (I/Q) mixer (Marki IQ-0618MXP) have been used at room temperature to perform signal demodulation. Microwave sources (Anritsu 3692B and 3694C) were employed to provide the local oscillator (LO) signal for the excitation of resonators and downconversion in a homodyne scheme, and an oscilloscope (Teledyne LeCroy HDO4054A) was used to acquire the intermediate-frequency (IF) signals after they were amplified by low-noise pre-amplifiers (Stanford Research Systems SR560). For time multiplexing, arbitrary waveform generators (Keysight 33500B) were used to generate the square-wave and ramp signal sequences used for V_{WLi} and V_{DLi}, respectively. Finally, for (time- and) frequency-multiplexed measurements, two microwave signal sources have been used at room temperature with a power combiner (Pasternack PE2068) to generate multiplexed single-tone microwave probing signals towards the DUT and two I/Q mixers have been used to separately demodulate the two tones by using the same microwave sources as LOs, respectively. The obtained signals have been simultaneously acquired by the oscilloscope. The complete setup is shown in Extended Data Fig. 1.

Data analysis. The signal-to-noise ratio can be derived from the reflectometry signal V_{mw}, as shown in Extended Data Fig. 2a, according to SNR = A/σ = 28.7, where A is the Coulomb-blockade peak amplitude and σ is the standard deviation of noise signals. To extract the amplitude, we use a Lorentzian fit corresponding to the expected lineshape for lifetime broadened transitions[42]:

$$V_{mw} \propto \frac{h\gamma}{(h\gamma)^2 + (e\alpha(V_{DL1} - V_{DL1,offset}))^2}, \quad (1)$$

where h is the Planck constant, γ is the tunnel rate, α is the lever arm or gate-coupling factor and $V_{DL1,offset}$ is the data-line voltage at which the source and QD Fermi levels align. We compare the individual device measurement and the time-domain multiplexing measurement in Extended Data Fig. 2b,c, respectively, and show a benchmark in Extended Data Table 2. Furthermore, we estimate the minimum integration time (defined as the time to reach SNR = 1) from the bandwidth of the measurement and the number of averages. The source-QD tunnel rate is estimated, too. These results are also shown in Extended Data Table 2.

Data processing. The time- (and frequency-)multiplexed readout data presented in this paper are processed data, and the data processing applied to them can be described as follows. To selectively address different columns in the QD transistor array, square waves are applied to the word lines when performing time-domain multiplexing readout. However, the rapid switches in the word-line voltages create large backgrounds that mask the reflectometry signals, as shown in Extended Data Fig. 3a. Hence, we use polynomial fits to the data as backgrounds. After subtracting the backgrounds from the original data (Extended Data Fig. 3b), the Coulomb-blockade peaks are revealed and are consistent with the individual reflectometry measurement for transistors Q_{12}, Q_{13} and Q_{11} (Fig. 3a).

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

A.R., M.F.G.-Z. and E.C. conceived the architecture and devised the experiments. A.R. and Y.P. designed the chip with inputs from E.C. and M.F.G.-Z. T.-Y.Y., J.M., M.F.G.-Z. and A.R. performed the experiments and analysed the results. A.R., T.-Y.Y. and M.F.G.-Z. wrote the manuscript with inputs from all the co-authors. M.F.G.-Z. and E.C. supervised all the experiments.

Competing interests

M.F.G.-Z. is employed by Quantum Motion Technologies, a start-up focusing on building a silicon-based quantum computer. All other authors declare no competing interests.

Additional information

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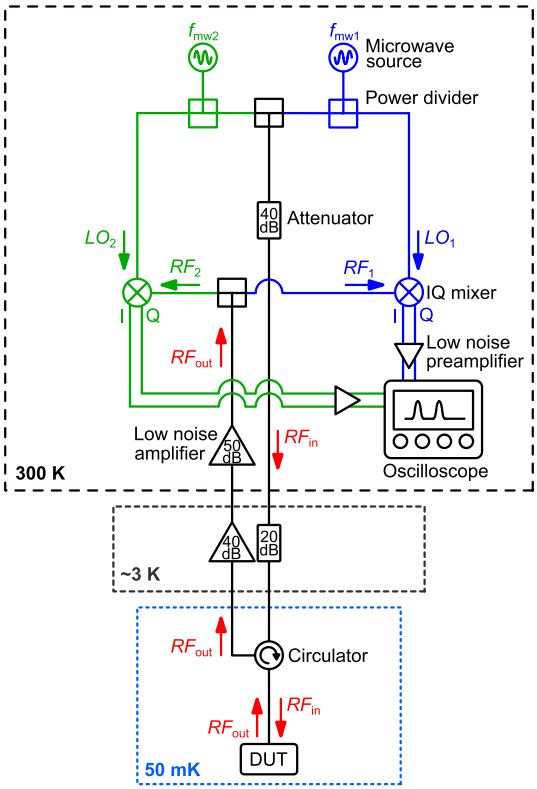
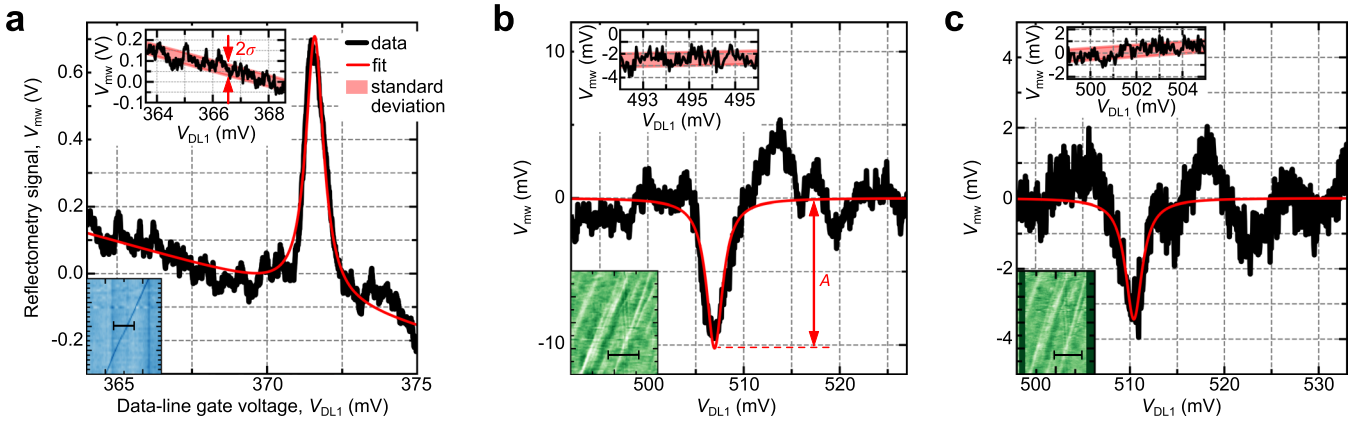
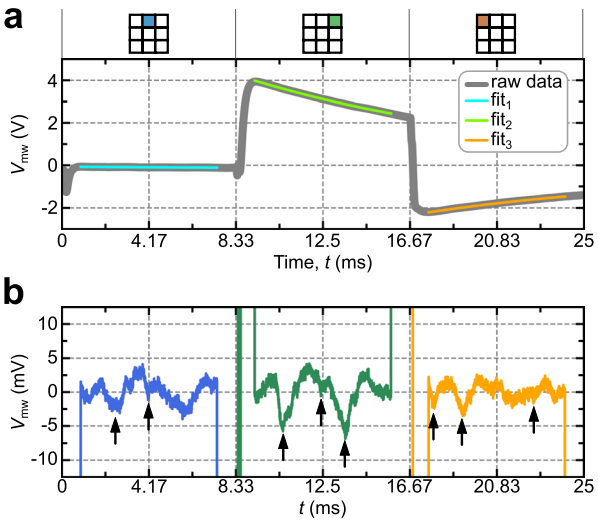


Extended Data Fig. 1 | Experimental measurement setup. Dilution refrigerator measurement setup for the time- and frequency-multiplexed gate-based readout experiment. The DUT is placed at 50 mK on the sample stage of the dilution refrigerator. A cryogenic circulator is placed at the mixing chamber plate and a low-noise amplifier and attenuators are placed at intermediate cryogenic temperatures (~3 K). At room temperature, two microwave signal sources are power-combined to generate two multiplexed single-tone probing signals f_{mw1} and f_{mw2}, and two I/Q mixers are used to demodulate the reflected signals RF_1 and RF_2 at the two frequencies, by using the microwave sources as respective local oscillators LO_1 and LO_2. An oscilloscope acquires the I/Q outputs for each of the two tones.



Extended Data Fig. 2 | Signal-to-noise ratio analysis. a, Trace of reflectometry signal V_{mw} as a function of V_{DL1} from an individual measurement of quantum device Q_{13}, corresponding to the black line section in the bottom left inset (left panel in Fig. 2c). The red curve is a Lorentzian fit to the experimental data. Top left inset: zoom-in of the background noise. σ is the standard deviation of noise signals. **b**, Trace of V_{mw} as a function of V_{DL1} for Q_{13} from an individual device measurement (middle panel in Fig. 3a). A is the Coulomb peak amplitude from the fit. **c**, Trace of V_{mw} as a function of V_{DL1} for Q_{13} from the time-domain multiplexing measurement (middle panel in Fig. 3c). The measurement in **a** was performed in a different cool down thermal cycle with respect to those in **b** and **c**, while the measurements in **b** and **c** are within the same cool down.



Extended Data Fig. 3 | Data processing. a, A single sweep of reflectometry signal V_{mw} (grey curve) as a function of time t at $V_{S1} = 0$ V corresponding to Fig. 3c. The data show the reflectometry signals from Q_{12} ($t = 0$ to 8.33 ms), Q_{13} ($t = 8.33$ to 16.67 ms), and Q_{11} ($t = 16.67$ to 25 ms). The light blue, light green, and gold curves are fits to the data and are used as backgrounds for data processing. **b**, Processed reflectometry signals of Q_{12} (blue), Q_{13} (green), and Q_{11} (gold) after subtracting the background fits. The arrows indicate Coulomb-blockade peaks.

Extended Data Table 1 | Values of the circuit components

Row (i)	C_T (fF)	R_T (kΩ)	C_S (fF)	L (nH)	C_P (fF)	C_C (fF)
1	231	92	231	2.42	540	200
2	81	92	243	1.95	1450	200
3	79	92	210	1.84	1160	200

Nominal value of all the circuit components in the schematic of Fig. 1b.

Extended Data Table 2 | Benchmark of signal-to-noise ratio analysis for device Q_{13}

Parameter	Formula	Individual, Q_{13} (Fig. 2c)	Individual, Q_{13} (Fig. 3a)	Time multiplexing, Q_{13} (Fig. 3c)
Peak amplitude ($\|A\|$, mV)		783	10.2	3.44
FWHM (mV)		0.721	2.05	2.13
Noise standard deviation (σ, mV)		27.3	0.569	0.513
Signal-to-noise ratio (SNR)	A/σ	28.7	18.0	6.70
Integration time (t_{int}, ms)	400 sweeps*/ 1 kHz**	400	400	400
Minimum integration time (t_{min}, ms)	t_{int}/SNR^2	0.487	1.24	8.90
Lever arm (α, eV/V)	$\Delta V_S/\Delta V_G$¶	0.555	0.555	0.555
Tunnel rate (GHz)	$\alpha \times \mathrm{FWHM}/2h$§	48.3	137	143
R^2 (coefficient of determination)		0.941	0.622	0.486

* Number of sweeps for data integration in oscilloscope
** Low-pass filter frequency
§ Planck constant
¶ ΔV_S and ΔV_G are derived from the Coulomb diamond diagram as demonstrated in Fig. 1c.

Coulomb peak amplitude (A), peak full width at half maximum (FWHM), noise standard deviation (σ), signal-to-noise ratio (SNR), measurement integration time (t_{int}), estimated minimum integration time (t_{min}), gate lever arm (α), source-QD electron tunnel rate, and coefficient of determination of the fit (R^2) for multiple data sets.