

MICRO-435

Quantum and Nanocomputing

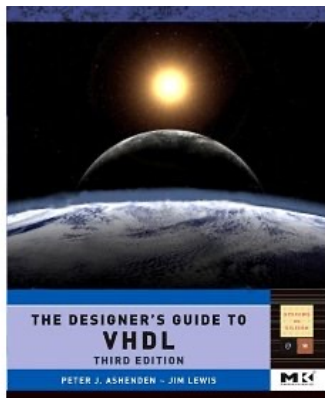
Edoardo Charbon
Mariagrazia Graziano



Daniel D. Gajski,
Principles of Digital Design, Prentice Hall, 1st Edition (1997).



Scott Hauck, André Dehon, Ed.
Reconfigurable Computing, Morgan Kaufmann, 1st Edition (2007).



Peter J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann Publishers,
1st Edition (1995)

Quantum Computing Syllabus (Week 1-7)

- Fundamentals of quantum computing
- Qubit realization & control
- **Cryo-CMOS components**
- Scalable quantum computers (Wednesday lecture)
- Quantum communication, sensing, and metrology (MICRO428/429)

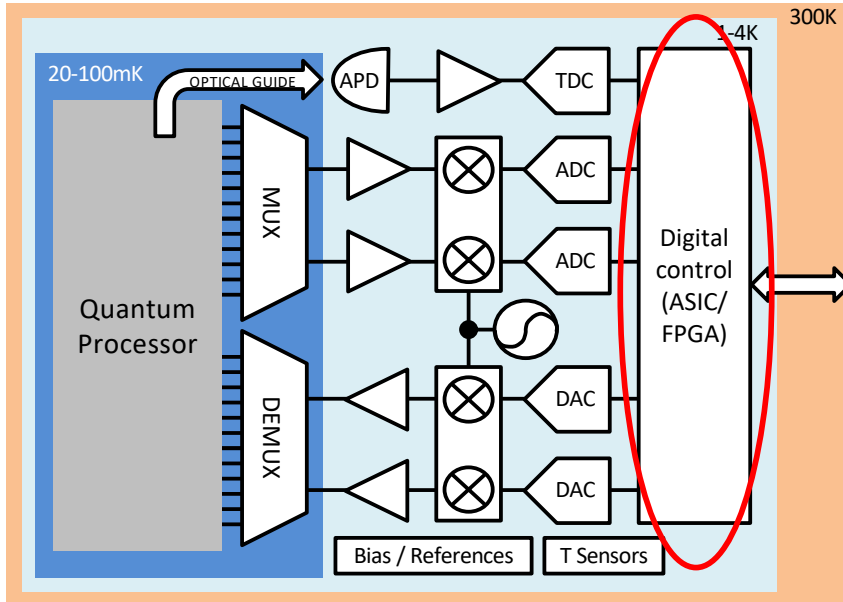
Cryo-CMOS Components (3)

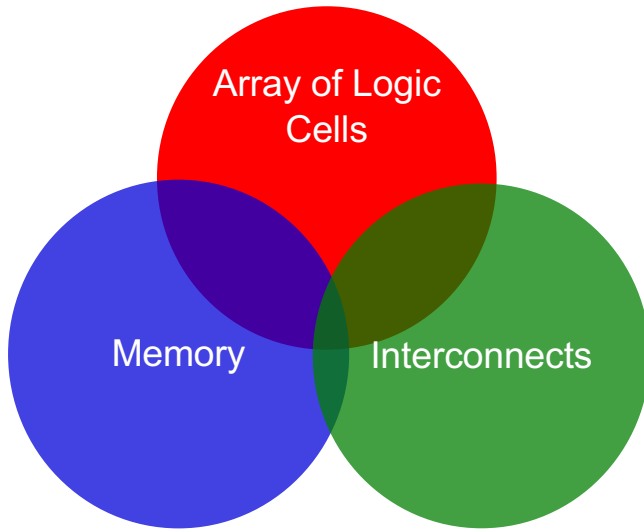
- Choosing a technology
- Cryo-CMOS modeling
- LNAs
- ADCs
- DACs
- Digital circuits in CMOS
- FPGAs
- Q&A

Acknowledgements: Fabio Sebastiano

Field-Programmable Gate Arrays (introduction)

Cryo-CMOS Quantum-Classical Interface

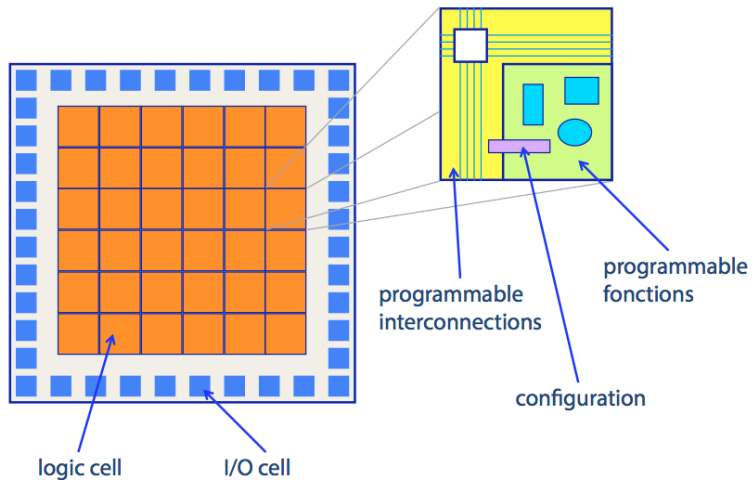




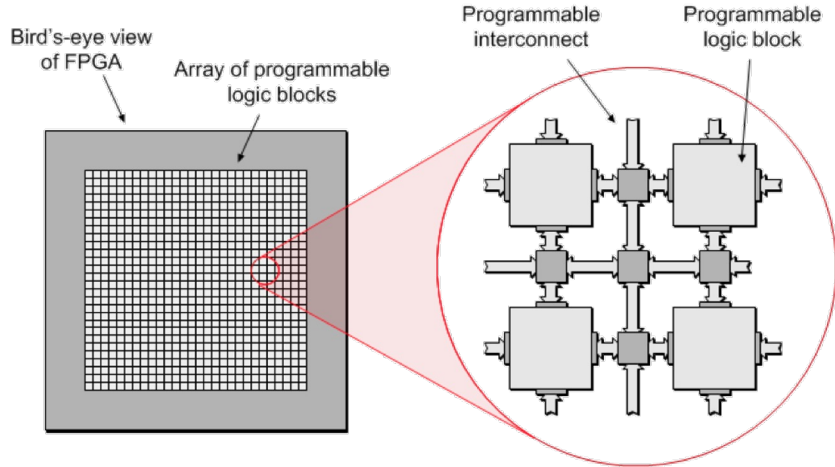
Basic Idea of FPGAs (2)

- Array of logic cells
 - Each logic cell implements a logic function
 - Logic function selected and stored
- Interconnections between logic cells
 - Programmable
 - Two types: fine grain vs. coarse grain
- Memory
 - Embedded in array
 - RAM: every logic cell contains a LUT (lookup table), accompanied by a flip-flop, and all interconnected with programmable routing pathways

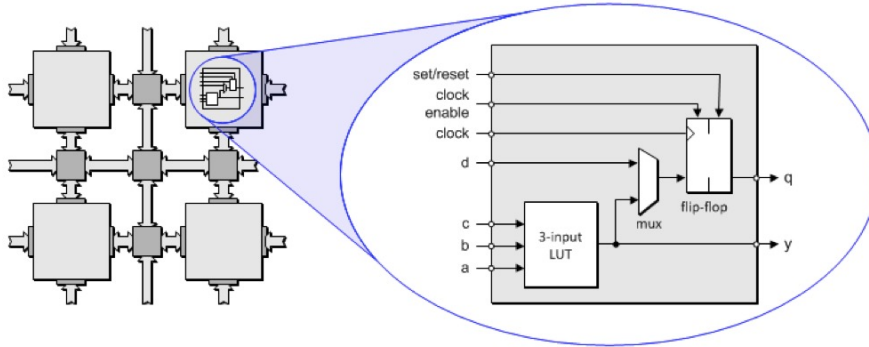
Basic Idea of FPGAs (3)



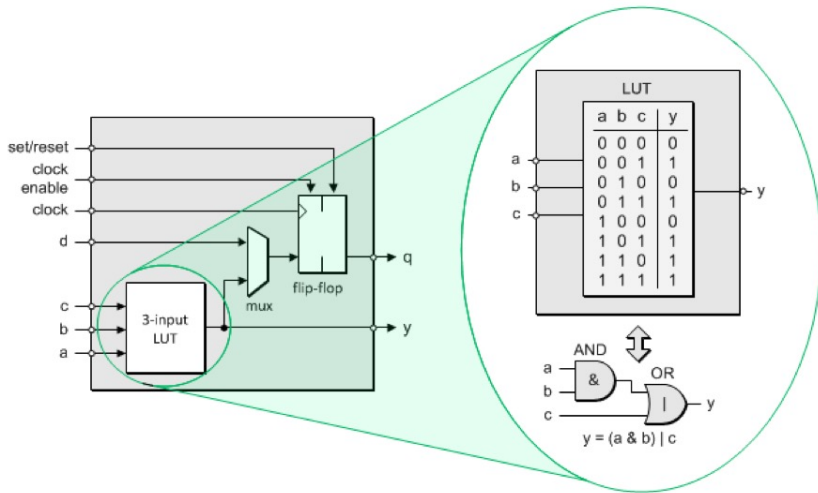
Basic Structure of FPGAs: 'Fabric'



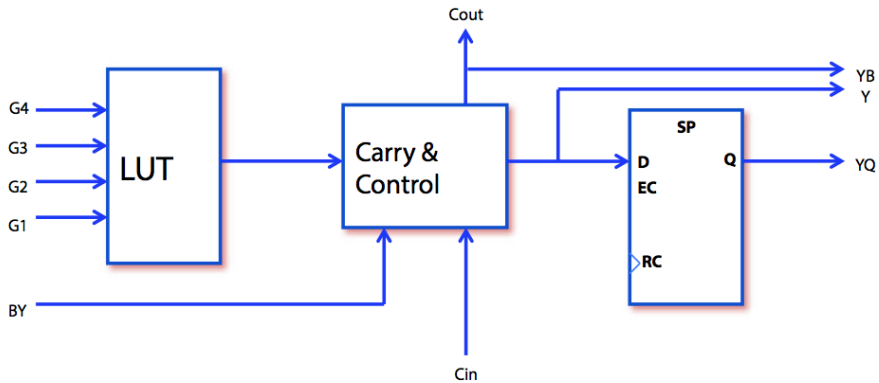
Basic Structure of FPGAs (2)

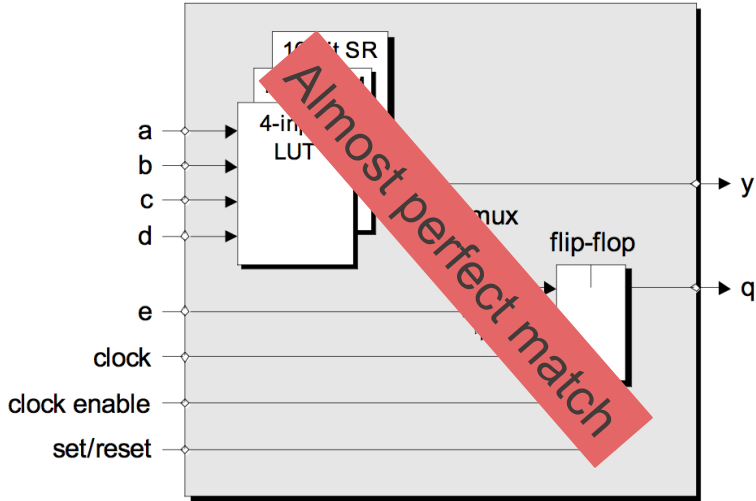


Basic Structure of FPGAs (3)

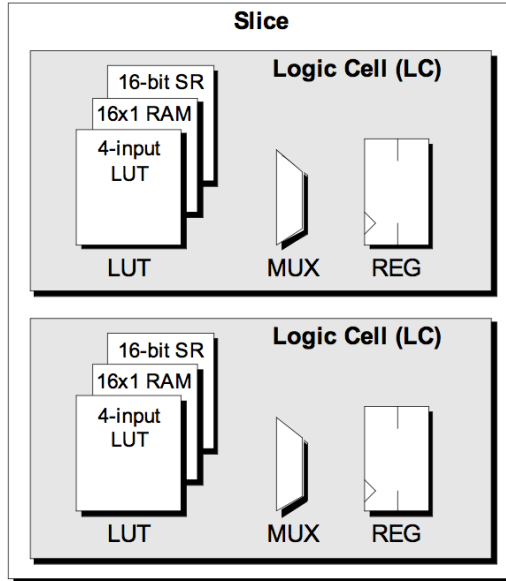


Example: Carry Logic + Latch

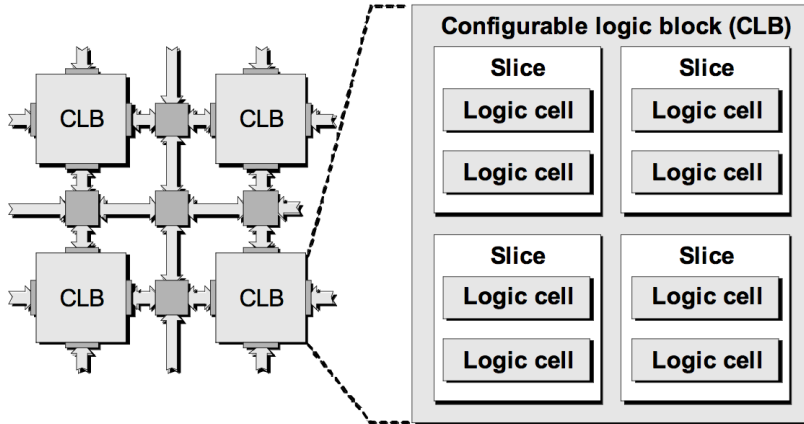


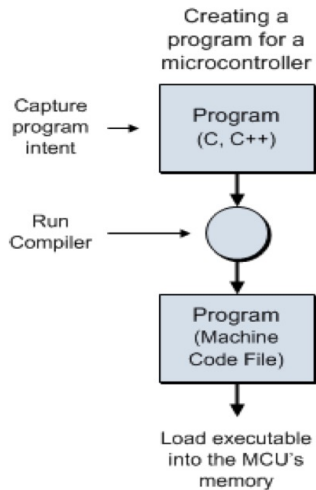


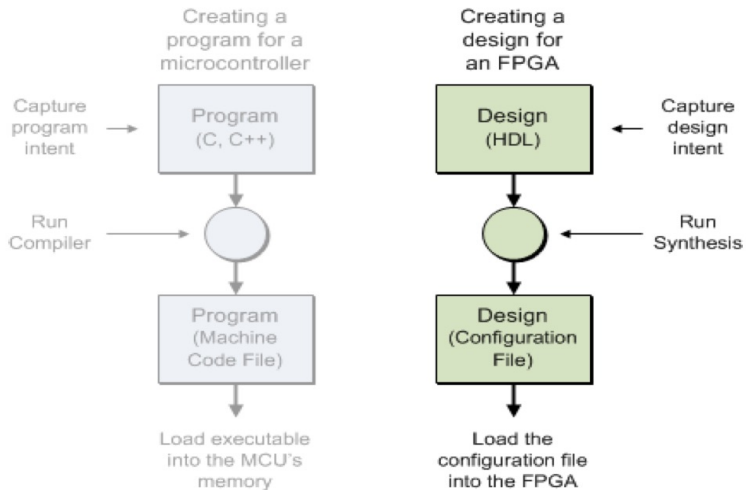
Concept of 'Slice'

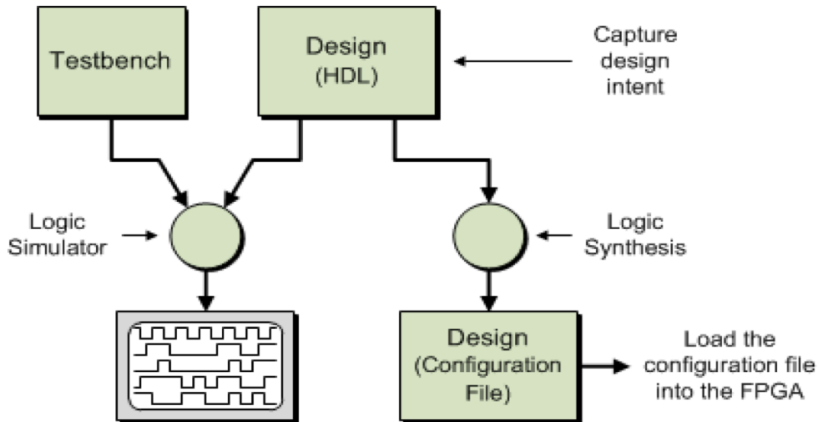


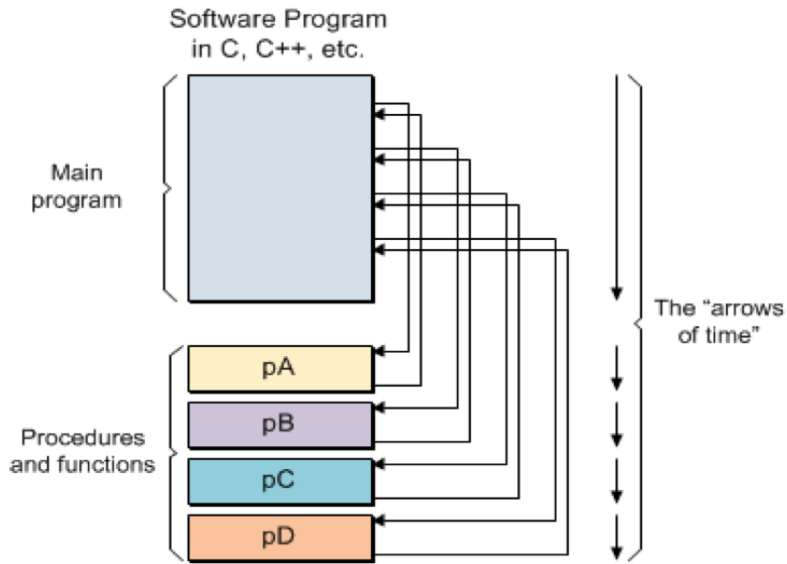
Slices in the FPGA Fabric



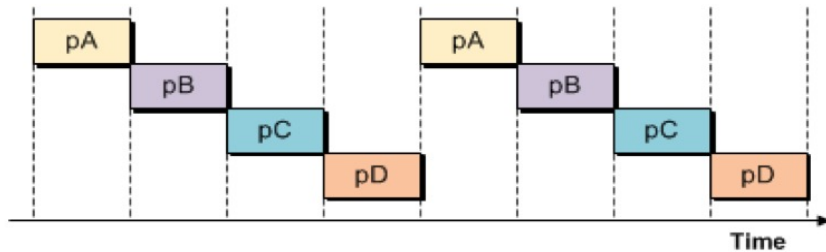


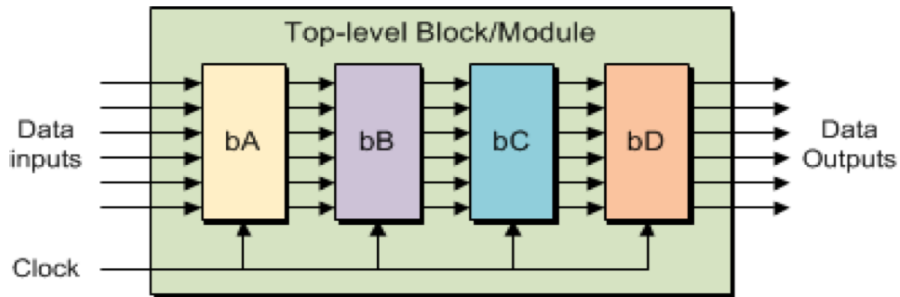






Execution Flow (Firmware)





FPGAs vs. ASIC

FPGA

Field-programmable gate array

- Reconfigurable
- Simple design flow
- High cost
- Medium performance
- High power
- Medium size

ASIC

Application Specific Integrated Circuit

- Very limited reconfigurability
- Complex design flow
- Low cost
- High performance
- Low power consumption
- Small size

CryoCMOS Hardware Technology

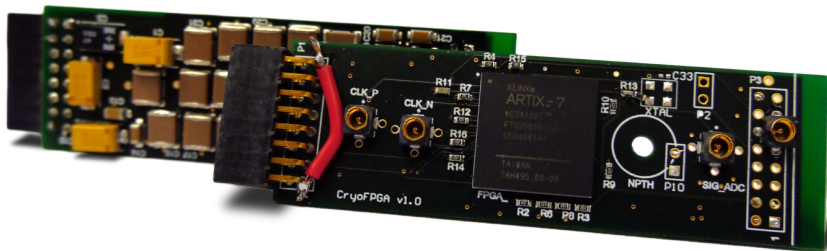
A Classical Infrastructure for a Scalable Quantum Computer

ACM Frontiers in Computing, Como 2016

Harald Homulle¹, Stefan Visser¹, Bishnu Patra¹, Giorgio Ferrari², Enrico Prati³,
Carmen G. Almudéver¹, Koen Bertels¹, Fabio Sebastiano¹, Edoardo Charbon¹

¹QuTech, Delft University of Technology, Delft, The Netherlands

²Politecnico di Milano, Milano, Italy, ³Consiglio Nazionale delle Ricerche, Milano, Italy
{h.a.r.homulle, f.sebastiano, e.charbon@tudelft.nl}

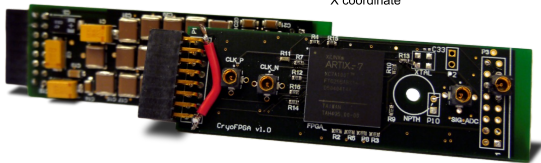
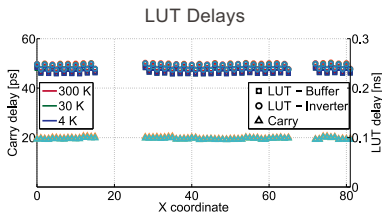
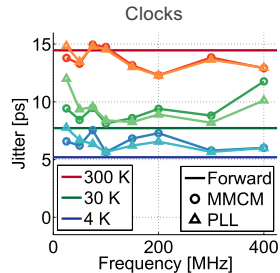
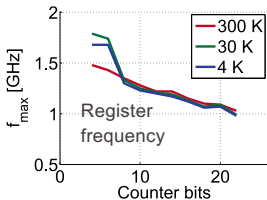
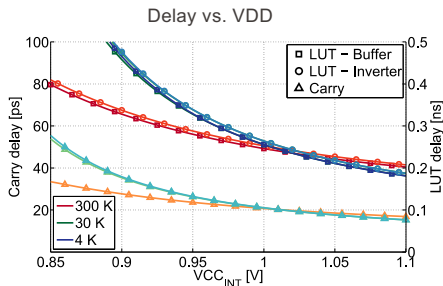


- All FPGA components are working in the cryogenic environment down to 4K
- No modifications required

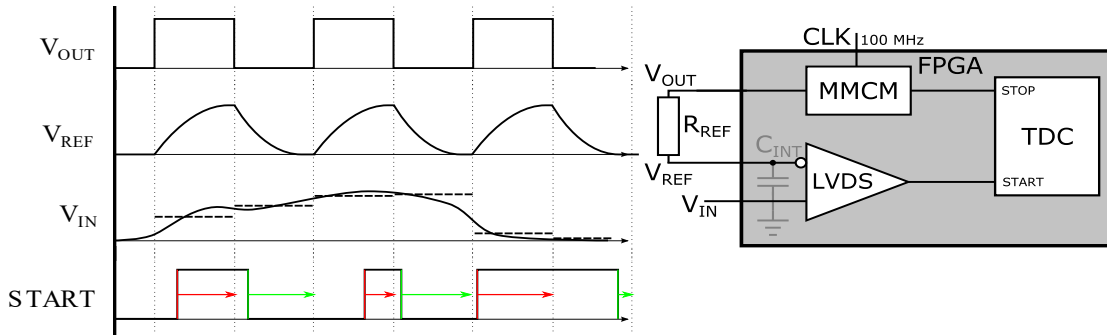
Component	Functional	Behavior
IOs	✓	
LVDS	✓	
LUTs	✓	Delay change < 5%
CARRY4	✓	Delay change < 2%
BRAM	✓	No corruption (800 kB)
MMCM	✓	Jitter reduction of roughly 20%
PLL	✓	Jitter reduction of roughly 20%
IDELAYE2	✓	Delay change of up to 30%
DSP48E1	✓	No corruption over 400 operations

FPGA Performance

Specs:
 Carry: 20 vs. 8.4 ps at 300 K
 LUTs: 238 vs 235 ps at 300 K
 Speed-up 2.4 vs 10.8% toward 300 K

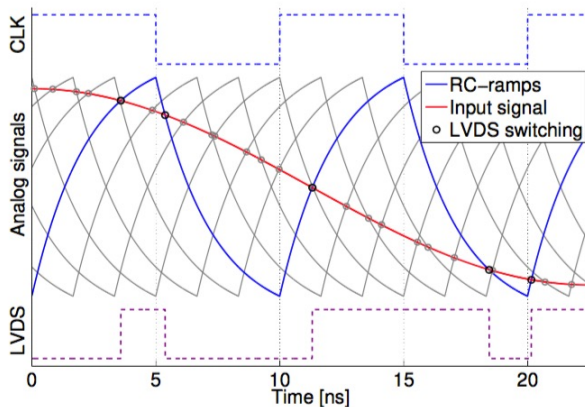


- ADC principle:
 - Conversion from voltage to time by timing cross-over of input with reference ramp
 - TDC performs time-to-code conversion
- Internal components are used, except for external resistance

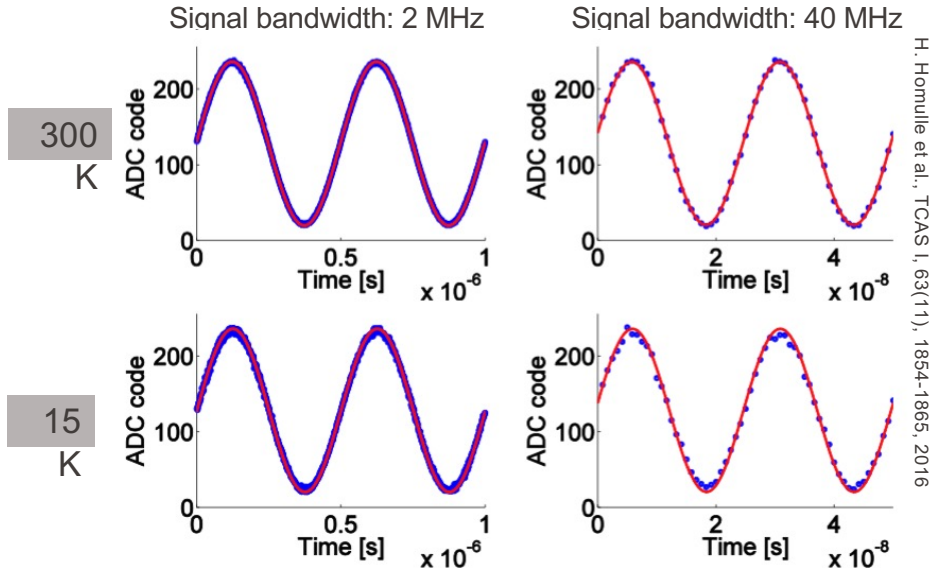


Increasing Sample Rate – Multiple Sampling

- Multiple sampling principle
 - Use n independent but synchronized converters
 - For up to 1 GSa/s \rightarrow phase interpolation

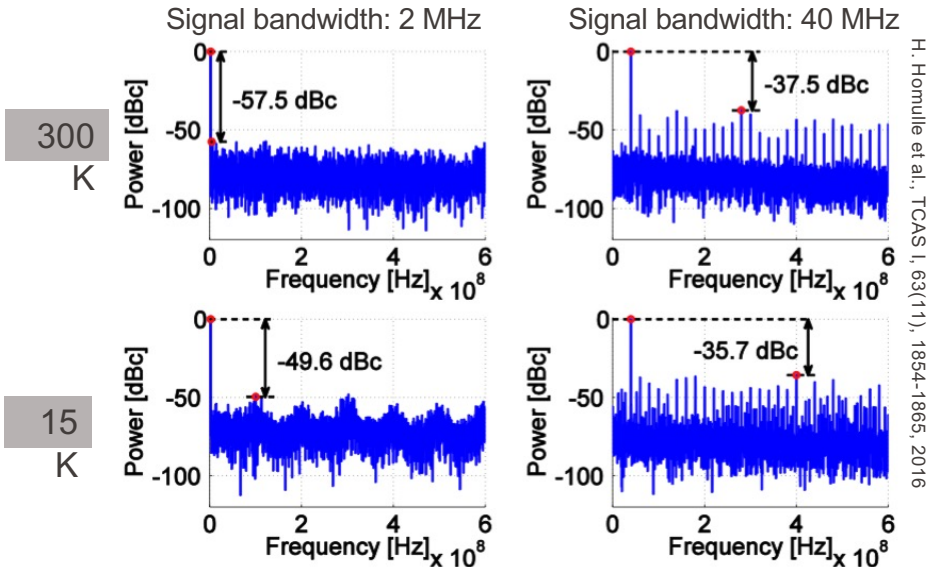


ADC on FPGA (1.2GSa/s)



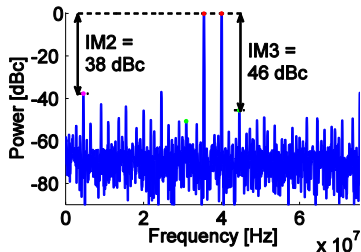
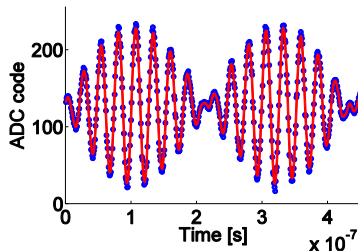
H. Homulle et al., TCAS I, 63(11), 1854-1865, 2016

ADC on FPGA (1.2GSa/s)



Distortion (IM2, IM3)

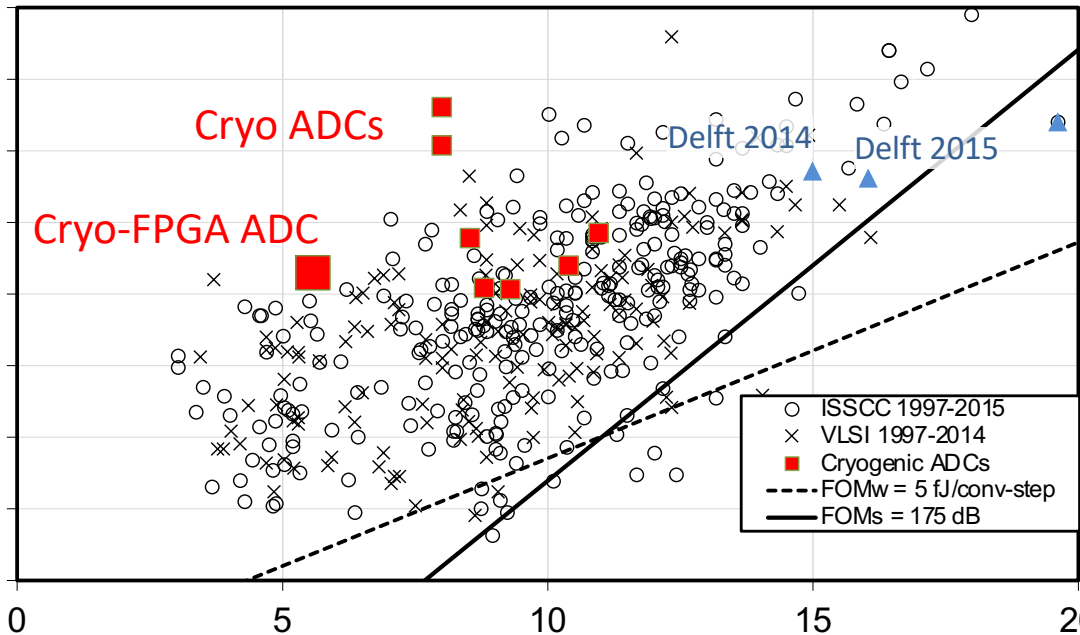
- Two tones: $\approx 36 / 41$ MHz
 - IM2 = 38 dB
 - IM3 = 46 dB
- Many secondary harmonics
- Interference with 100 MHz (sampling tone)



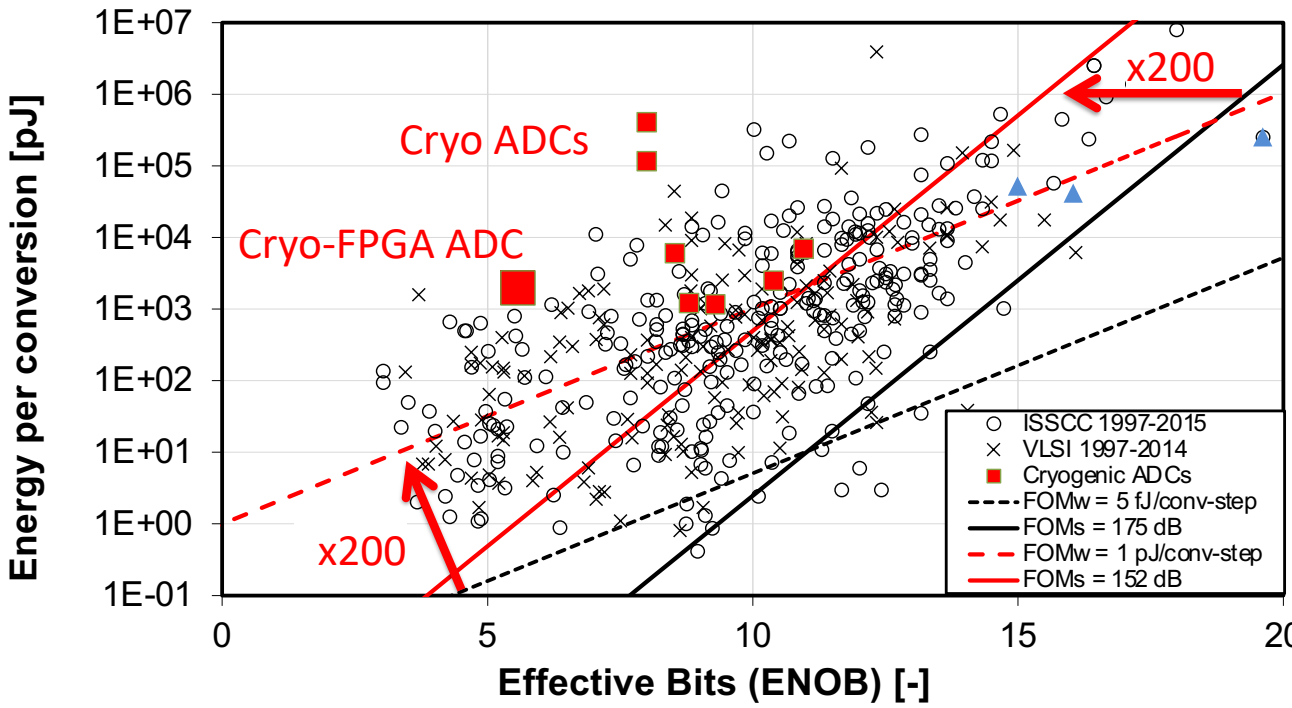
$$\text{SNDR} = 6.02 \text{ ENOB} + 1.76, \text{ FOMw} = \text{Energy} / 2^{\text{ENOB}}, \text{ FOMs} = \text{SNDR} - 10 \log_{10} 2 \text{ Energy}$$

Energy per conversion [pJ]

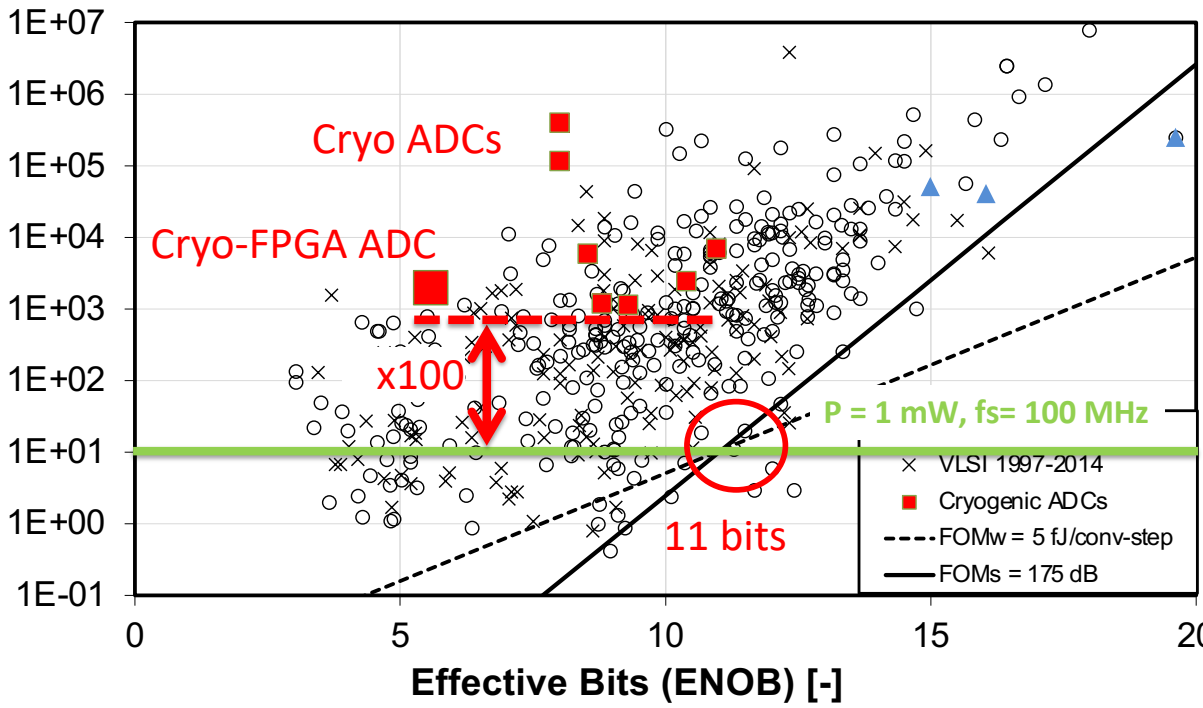
1E+07
1E+06
1E+05
1E+04
1E+03
1E+02
1E+01
1E+00
1E-01



Murrmann - "ADC performance summary"



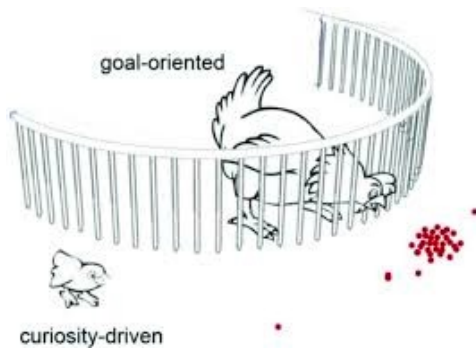
Energy per conversion [pJ]



Effective Bits (ENOB) [-]

- x VLSI 1997-2014
- Cryogenic ADCs
- - - FOMw = 5 fJ/conv-step
- FOMs = 175 dB

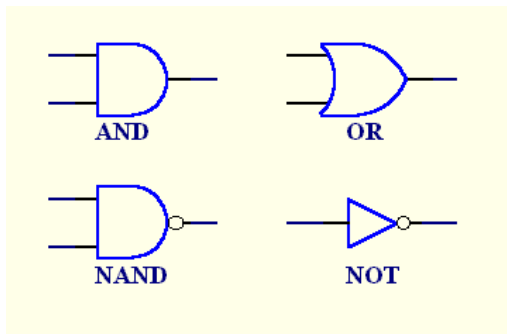
Thank you



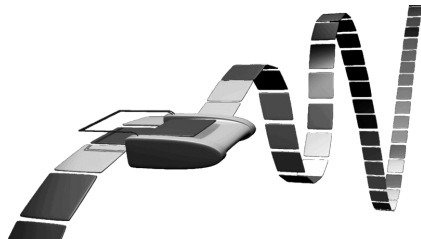
T. Haensch

Appendix:
Classical/Computer Engineering
Integrated Circuits

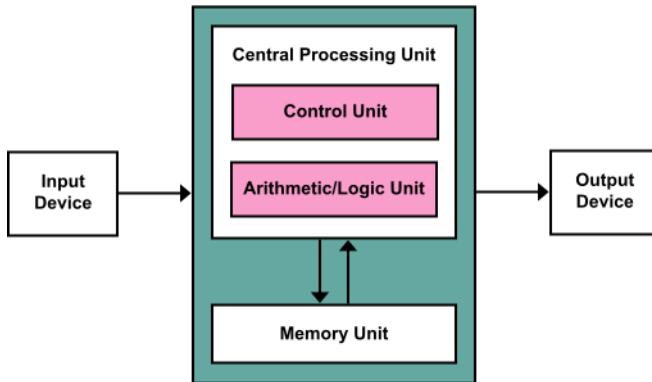
- Boolean logic
- Boolean algebra becomes the algebra of choice (Victor Shestakov & Claude Shannon – 1935-1937)
- Logic gates are invented



- Abstract model of a machine capable of executing classical algorithms
- Infinite tape with symbols that can be read or written in sequence according to a set of rules – the algorithm
- With this model, Turing falsified Hilbert's Decision Problem (1928)
- Theoretical Computer science is born!



The Von Neumann essence



- Instructions are read from memory
- Data are read from and written to memory
- ALU performs operations on data
- Operation is controlled by the control unit

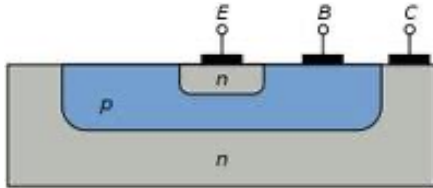
Source: Wikipedia

The microprocessor (μP) is a multipurpose, programmable device that accepts digital data as input, processes it according to instructions stored in its memory, and provides results as output.

Source: Wikipedia

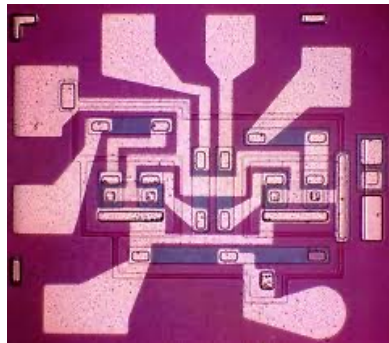
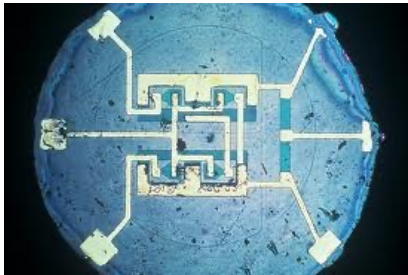
Technical background: planar process

- The planar process enables the integration of high density of transistors on the same substrate (1958)
- Moore's Law (1963): transistor density doubles every 1.5-2 years



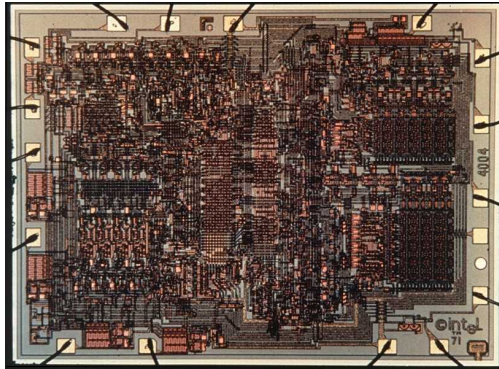
The first integrated circuits (ICs)

- First integrated circuit (Noyce – 1961)
- First commercial IC by Fairchild (1963)



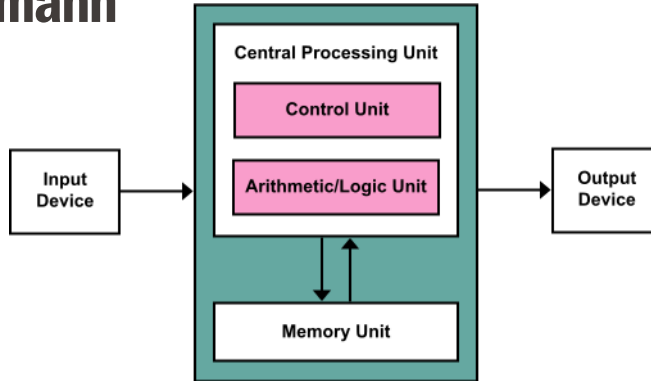
The first microprocessor

- Intel 4004 (F. Faggin, design / M. Hoff, architecture – 1971)
 - 4b CPU
 - 94k ops per second
 - 0.5W
- MCS-4 (4001-4) family
- Intel 8008
 - 8b CPU
 - 16kB addressable RAM
- Birth of the computers of IV generation

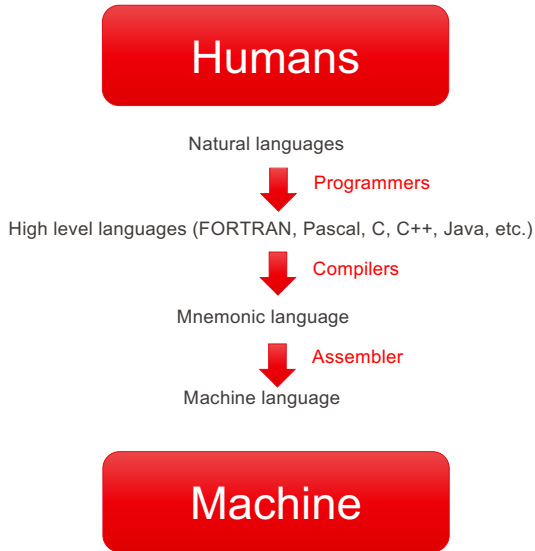


Basic μ P architectures:

Von Neumann

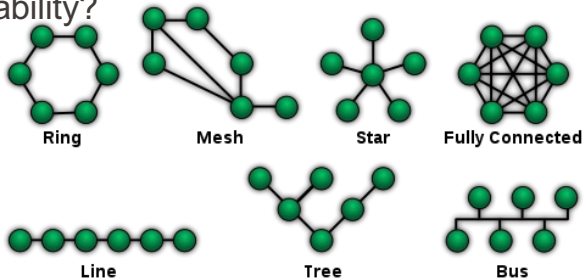


Source: Wikipedia



- Emerging in the early 2000s
- Developed to continue the doubling of computational power without increasing clock frequency – use of parallelism
- Conventional languages used (parallelism is implemented at compiler level)
- Examples
 - 2 cores [AMD Phenom II X2](#), [Intel Core Duo](#)
 - 8 cores [Intel Xeon E7-2820](#), [AMD FX-8350](#)
 - 10-cores (e.g. [Intel Xeon E7-2850](#))

- Fraction of parallelizable code (Amdahl's Law)
- Network topology
- Compiler
- Reconfigurability?



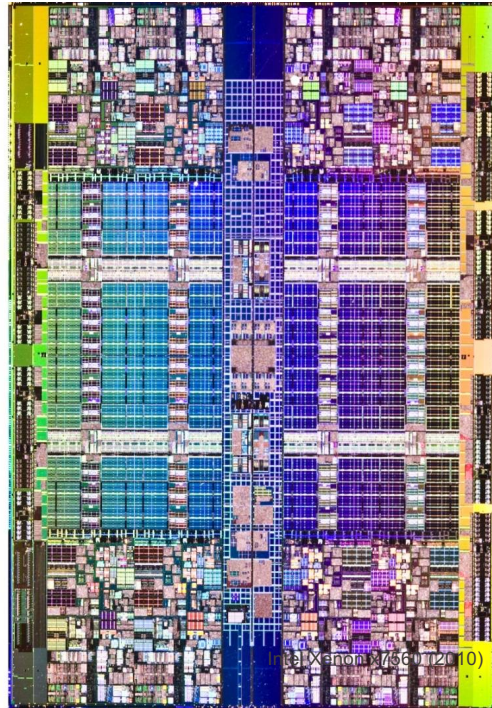
- Superscalar
 - One instruction → one operation
 - Out-of-order execution, branch prediction, speculative execution
 - Hardware is complex
- VLIW (very large instruction word)
 - One instruction → multiple operations
 - Instruction level parallelism (ILP)
 - Hardware is simple, compiler makes decisions (complex)
- Vector processing
 - Instructions operating on one-dim arrays of data
 - Heavily used in supercomputers in 1970s-90s
 - Effective in highly specialized (numerical) algorithms

- SIMD (single instruction multiple data)
 - Exploits data level parallelism
 - Used in image and audio processing
- Multithreading
 - Partitioning of code in threads executed in parallel

- VLIW (very long instruction word)
- RISC (reduced instruction set computer)
- CISC (complex instruction set computer)

- 1970s: 4004 – the first integrated device
- 1980s: CISC vs. RISC, parallel computing schemes
- 1990s: ARM architecture (RISC) emerges - the Pentium architecture (VLIW) supported by Intel-Microsoft survives
- 2000s: the demise of the DEC Alpha (RISC) in favor of less performing CPUs but better marketing
- 2000s-2010s: multi-cores, GPUs, multithreading, reconfigurable logic, open-source processors

IR Drop calculation



- CPU is just a component, more functionality present
 - Micro-electromechanical systems (MEMS)
 - Peripherals, analog circuits
 - Radiofrequency links
 - Wifi enabled
- Embedded systems
 - Highly automated design
 - Design-for-manufacturability
 - Built-in test
 - Built-in security



Trends (1): mobile computing

- The PC/Mac – smartphone boundary is fading
- Miniaturization and style takes over with rock-solid operating systems and apps



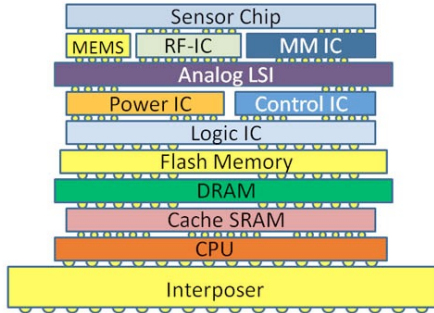
Apple's MacBook Air

Trends (2): infrastructure computing

- Datacenters emerge as bulk infrastructure to contemporary e-commerce
- Server-farms take over supercomputing – demise of Cray (2000s)
- Cloud computing – internet based server-farms

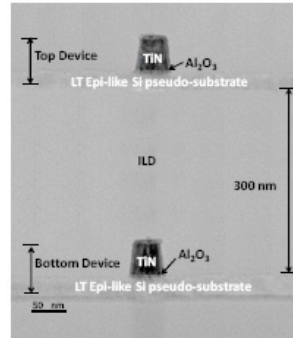


Trends (3): 3D integration



Hybrid approach

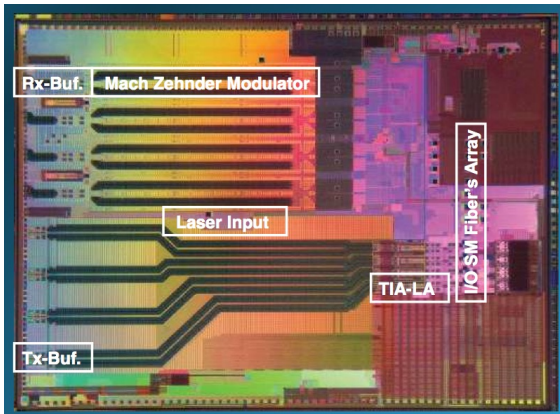
(Source: SRC Center of Excellence
Georgia Tech)



True 3D approach

(National Nano Device Lab,
Taiwan) – IEDM 2013

- Promise:
 - 40Gb/s per pad
 - Lower noise
 - Lower complexity
- Challenges:
 - Hybrid integration
 - Light generation



Source: Luxtera