MICRO-435 Quantum and Nanocomputing

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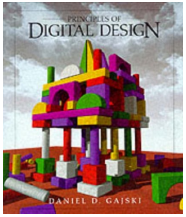
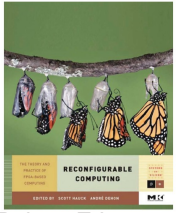
Reference books

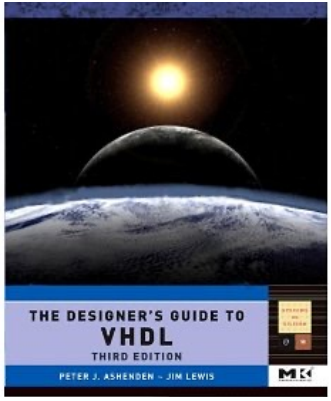


Daniel D. Gajski,
Principles of Digital Design, Prentice Hall, 1st Edition (1997).



Scott Hauck, André Dehon, Ed.
Reconfigurable Computing, Morgan Kaufmann, 1st Edition (2007).

Also recommended



Peter J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann Publishers,

1st Edition (1995)

Quantum Computing Syllabus (Week 1-7)

- Fundamentals of quantum computing
- Qubit realization & control
- **Cryo-CMOS components**
- Scalable quantum computers
- Quantum communication, sensing, and metrology

Cryo-CMOS Components (2)

- Choosing a technology
- Cryo-CMOS modeling
- LNAs
- ADCs (part I)
- ADCs (part II)
- DACs
- Digital circuits in CMOS

Acknowledgements: Fabio Sebastiano

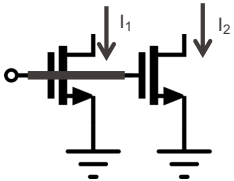
EPFL

Analog-to-Digital Converters (Part II)

Digression: Mismatch

- Mismatch = difference between 2 devices that are designed to be identical
- Systematic mismatch (reproducible from die-to-die)
  - Electrical biasing difference, mechanical stress, edge effects, temperature gradients
- Random mismatch
  - Due to microscopic effects (random dopant fluctuations), local mobility fluctuations, polysilicon and oxide granularity, oxide charges, ...)
  - Statistically characterized

Mismatch (2)

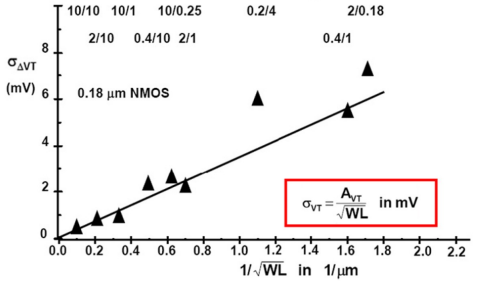


$$\Delta I = I_1 - I_2$$

ΔI is normally distributed with

$$\frac{\sigma_{\Delta I}}{I} = \frac{A}{\sqrt{WL}}$$, W width, L length

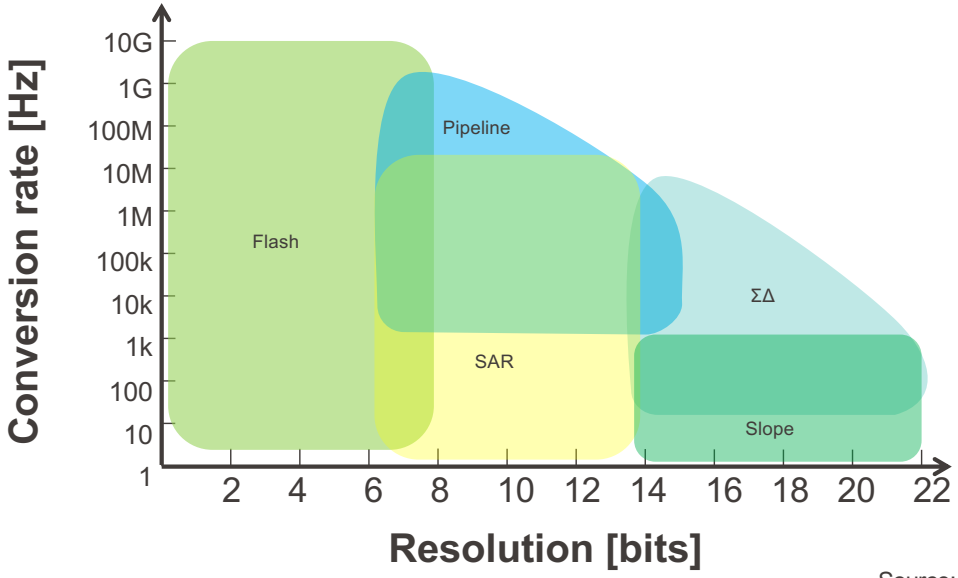
Example: std deviation of threshold voltage



[Courtesy: Pelgrom, *Analog to Digital Conversion*]

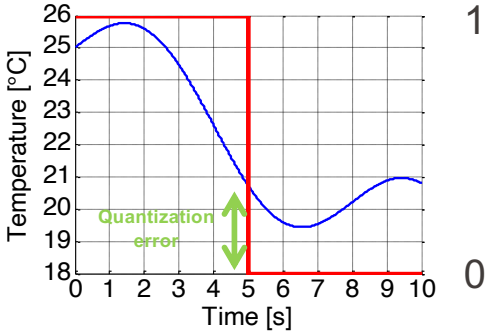
- Mismatch minimized by increasing area (*WL*)
- Better matching ⇒ large area
  - ⇒ higher cost
  - ⇒ larger parasitic capacitance ⇒ slower behavior/larger power
- Aspect ratio (*W*/*L*) *usually* determines electrical behavior, not area (*WL*)
  - Exception: for capacitors $C \propto WL$
- Minimum achievable mismatch depends on technology
  - Typically below ~10-12 bits in integrated circuits

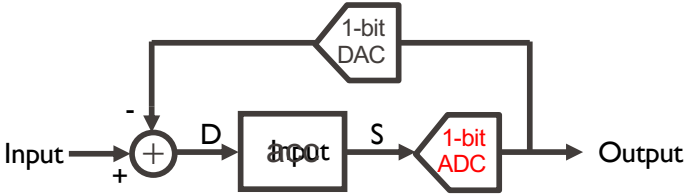
ADC Architectures



Source: Pelgrom 2006

Basic Idea of a Sigma-Delta ADC

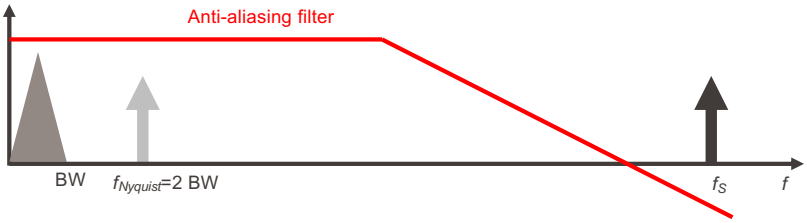




Why This Type of ADC?

- 1-bit ADCs
  - ⇒ Very simple robust circuits
- Run for many cycles
  - ⇒ longer time or ***faster execution***
- Modern IC technologies
  - Very fast circuits (GHz microprocessors)
  - Exploit speed ***and*** use simple circuits
- ***Fast simple circuit "better" than complex slow circuit***
- Typical applications: low-error/high-resolution
  - Instrumentation, sensors, audio

The Advantage of Oversampling

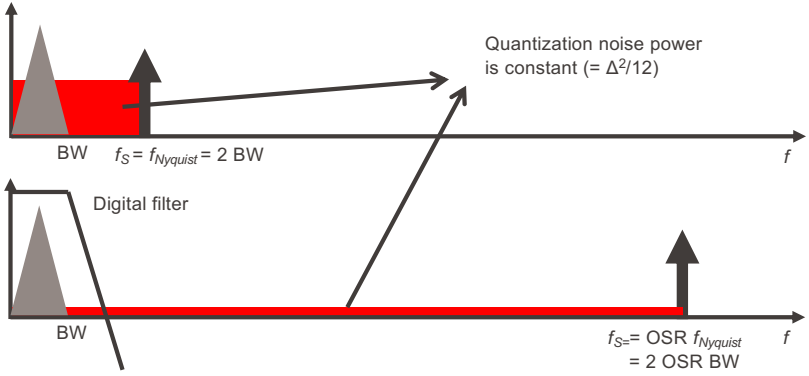


- Sampling at much higher rate than Nyquist rate
- Oversampling ratio

$$OSR = \frac{f_s}{f_{Nyquist}} = \frac{f_s}{2BW}$$

- Relax requirements on anti-aliasing filter
- **Quantization noise shaping**

Quantization Noise

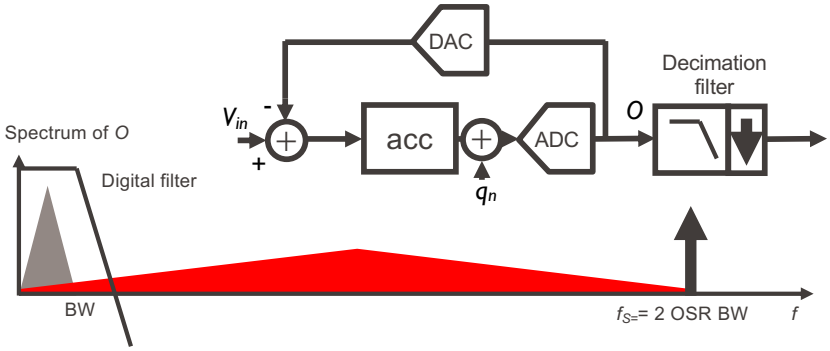


- Quantization noise is spread over a wider bandwidth
- Total quantization noise is lower ***in the signal bandwidth***
- Signal-to-Quantization-Noise-Ratio (SQNR) improves:

$$SQNR_{oversampled,dB} = SQNR_{Nyquist} + 10\log_{10} OSR$$

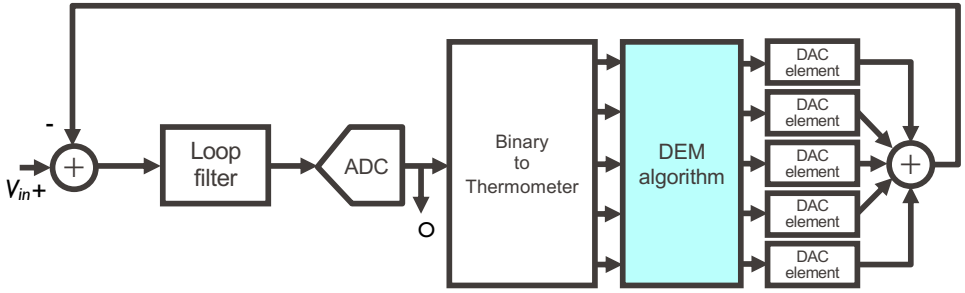
- **It requires digital filtering**

Noise Shaping in ΣΔ (or ΔΣ) ADC



- Accumulator is a low-pass filter (a.k.a. loop filter)
- Quantization noise (q_n) is attenuated by loop filter
- Quantization noise is shaped
- Even lower noise than just oversampling

Dynamic Element Matching (DEM)

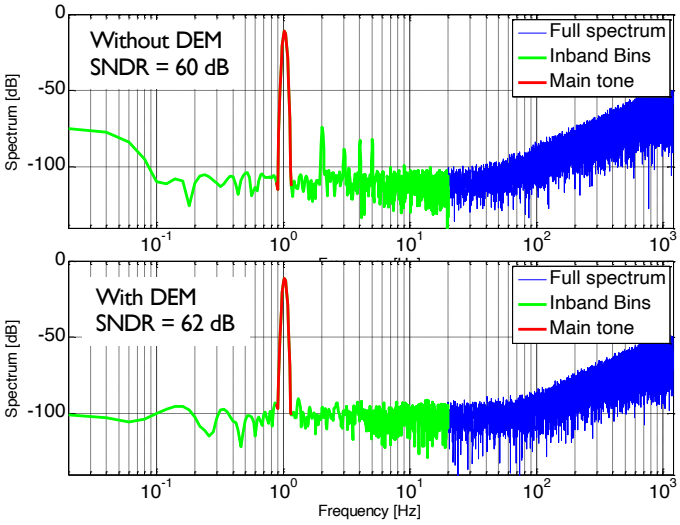


DAC elements

Cycle	No DEM	DEM
1	1 2 3 4	1 2 3 4
2	1 2 3 4	2 4 6 7
3	1 2 3 4	1 3 5 6

- DEM average mismatch over multiple cycles

DEM – Randomizing Algorithm



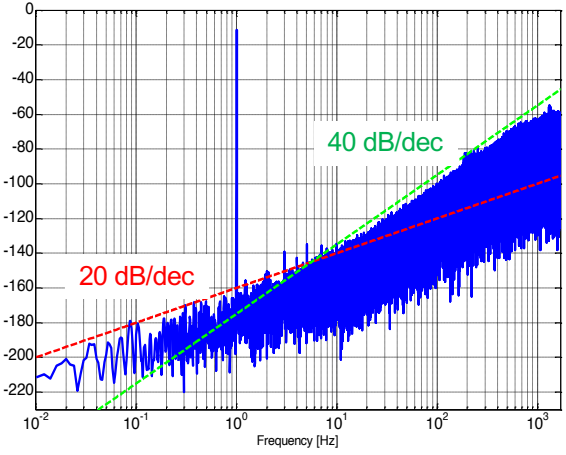
- Distortion energy spread over BW
- SNDR ~ equal but better SFDR

Other DEM algorithm

Example of 8-level
Data-Weighted Averaging (DWA)

Cycle	DAC	DAC elements
1	2	
2	2	
3	5	
4	2	
5	3	
6	4	

Resulting spectrum
(with DAC mismatch)



- Other DEM algorithms gives mismatch-error shaping

Oversampled ADC vs. Nyquist ADC

Oversampled ADC

- Simplified anti-aliasing filter
- Requires cascaded digital filter (decimation filter)
- Low distortion
- Limited in bandwidth
- Very high resolution
- Higher speed (OSR) for higher resolution

Nyquist ADC

- Requires anti-aliasing filter
- Digital signal readily available
- Higher distortion
- High speed
- Moderate resolution
- Higher complexity for higher resolution

Figures of Merit (FoM)

- Walden FoM

$$FoMw = \frac{P}{f_s 2^{ENOB}}$$

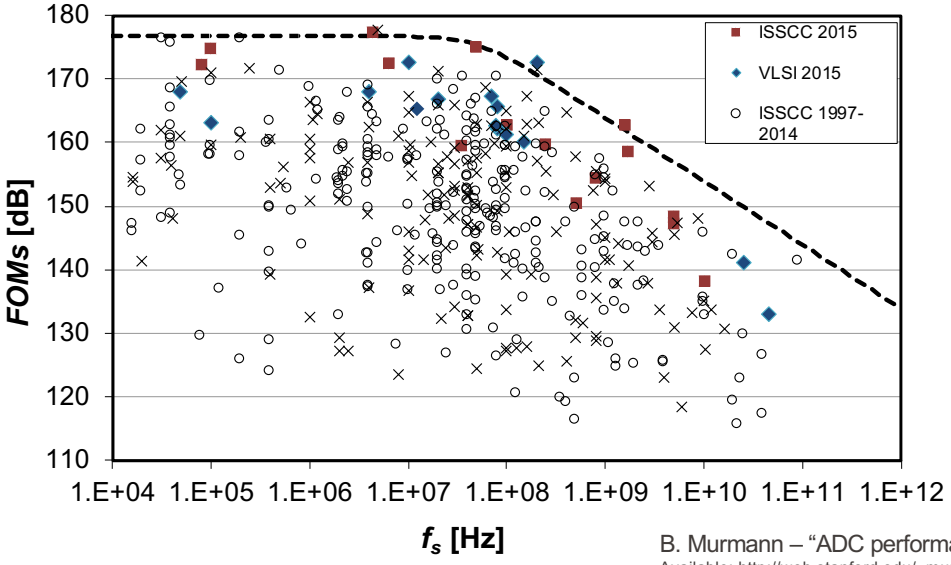
  - Good if power is proportional to the number of levels (2^{ENOB})
  - For ADCs limited by quantization-noise

- Schreier FoM

$$FoMs = SNDR_{dB} + 10\log_{10}\frac{f_s}{2P} = 10\log_{10} 3\frac{2^{2(ENOB-1)} f_s}{P}$$

  - Good if power is proportional to the square of the number of levels (2^{2ENOB})
  - For ADCs limited by thermal-noise

Figure of Merit (FoM)



B. Murmann – "ADC performance summary",
Available: http://web.stanford.edu/~murmann/adcsurvey.html

SNDR = 6.02 ENOB + 1.76, FOMw=Energy/2^{ENOB}, FOMs = SNDR - 10 $\log_{10}$ 2 Energy

Figure of Merit (2)

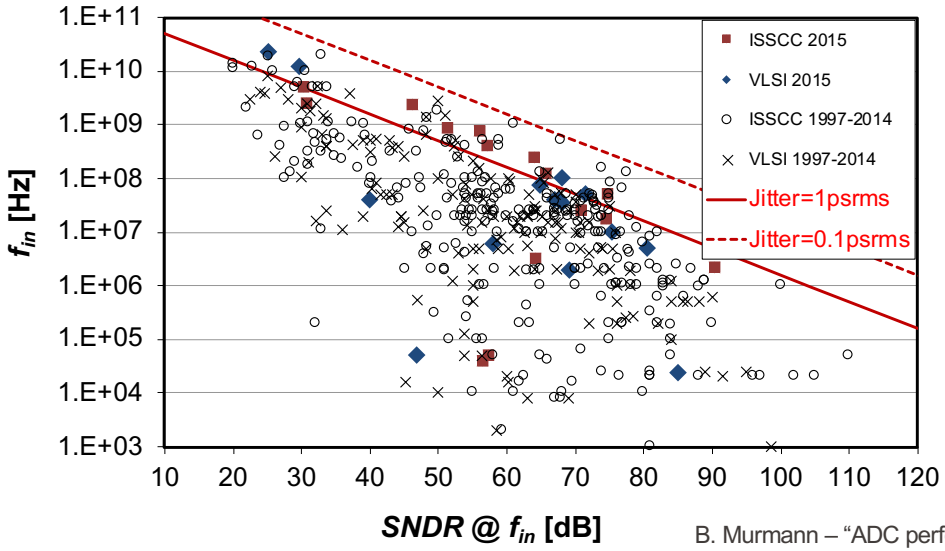


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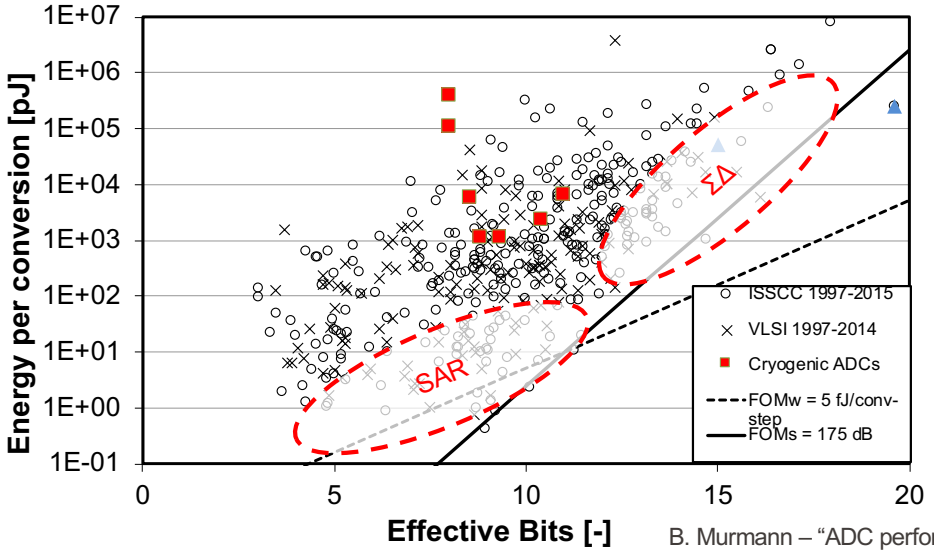
Figure of Merit (3)

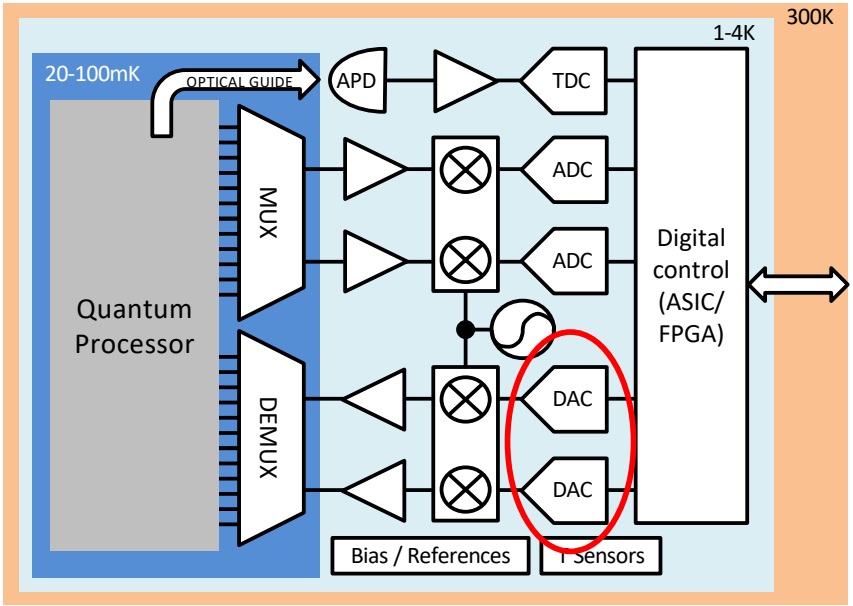


B. Murmann – "ADC performance summary",
Available: http://web.stanford.edu/~murmann/adcsurvey.html

SNDR = 6.02 ENOB + 1.76, FOMw=Energy/2^{ENOB}, FOMs = SNDR - 10 $\log_{10}$ 2 Energy

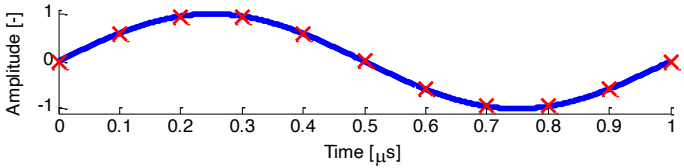
Digital-to-Analog Converters (DACs)

Cryo-CMOS Quantum-Classical Interface

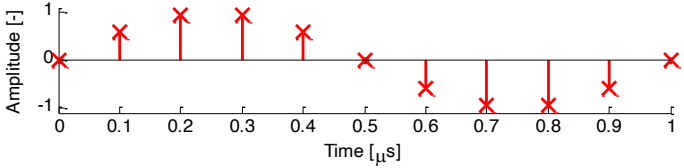


Digital-to-Analog Conversion

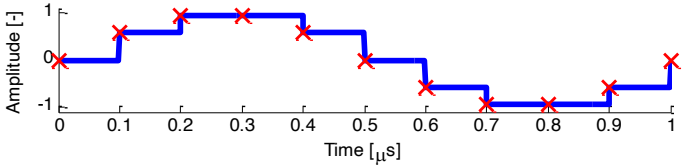
Sampling



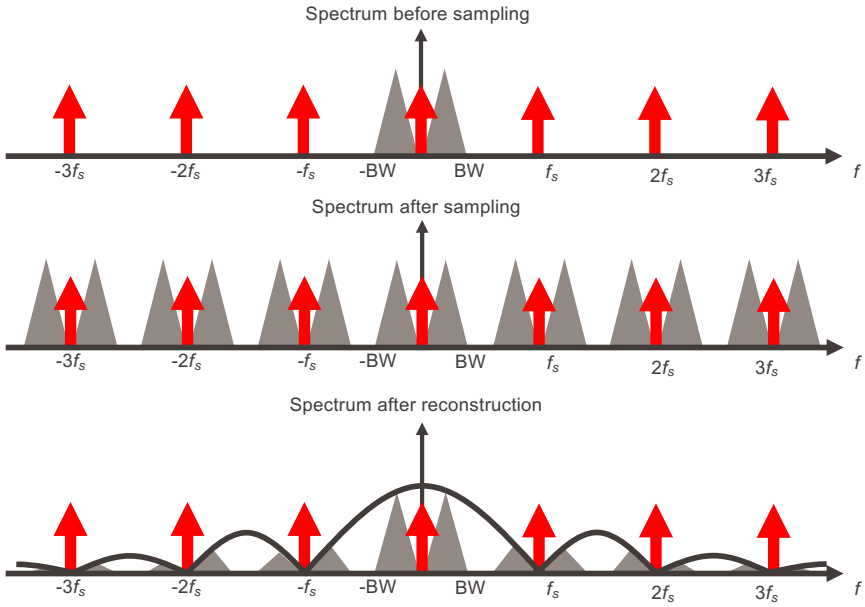
Digital domain



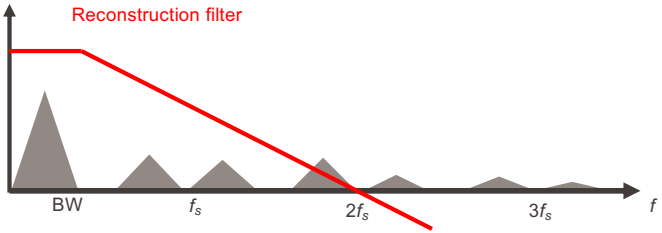
After Digital-to-Analog conversion



Digital-to-Analog Conversion



Reconstruction Filter



$$sinc(x) = \frac{sin\,(x)}{x}$$

- Non-idealities
  - In-band $sinc(x)$ distortion
  - Replicas around harmonics
- **Need for reconstruction filter**
- Filter requirements can be relaxed by:
  - Oversampling
  - In-band pre-distortion

Basic DAC Architectures

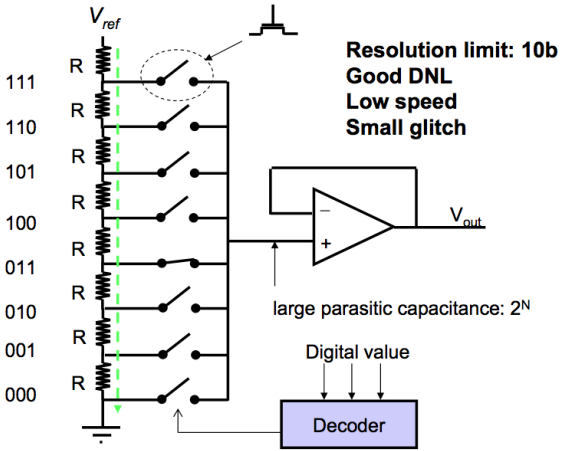
- Resistive based
- Capacitive based
- Current based

- Nyquist DAC / oversampled DAC

- Linear coded / Binary coded

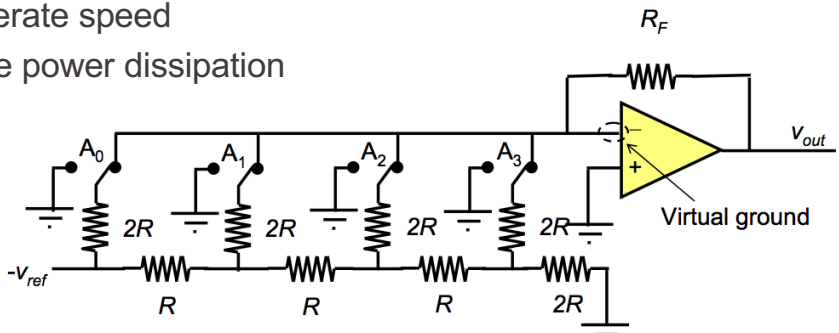
Resistor string DAC

- Small DNL
- Large area at high resolution



R-2R based DAC

- Large DNL
- Small area at high resolution
- Moderate speed
- Large power dissipation



$$v_{out} = R_F\left(I_r \cdot A_0 + \frac{I_r}{2} \cdot A_1 + \frac{I_r}{2^2} \cdot A_1 + \frac{I_r}{2^3} \cdot A_1\right)$$

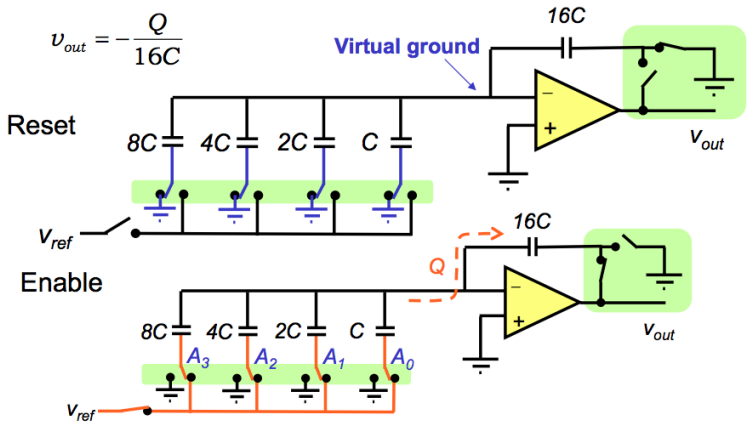
$$I_r = \frac{v_{ref}}{2R}$$

Capacitor Array DAC

- Low power
- No sample and hold required

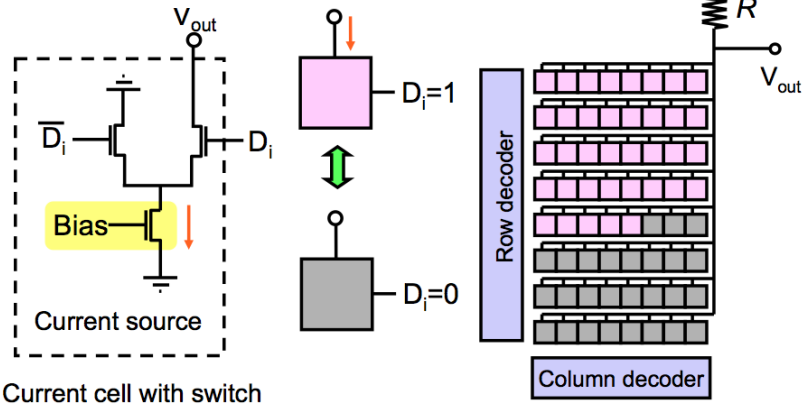
$$Q = v_{ref}\left[C \cdot A_0 + 2C \cdot A_1 + 4C \cdot A_2 + 8C \cdot A_3\right] \qquad A_i = 0 \text{ or } 1$$

$$v_{out} = -\frac{Q}{16C}$$

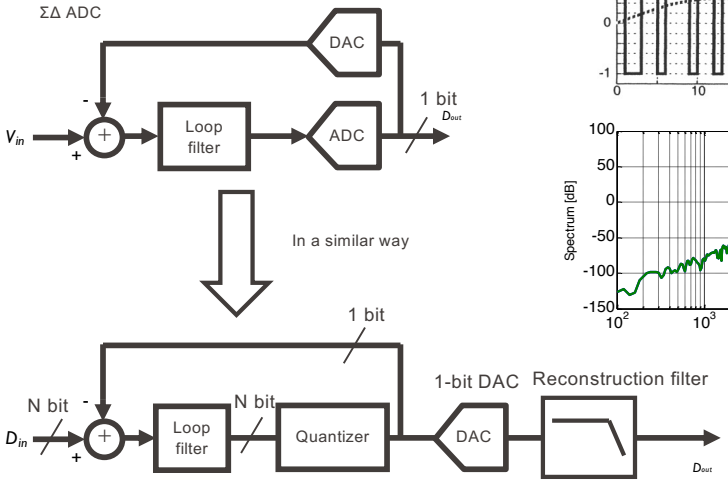


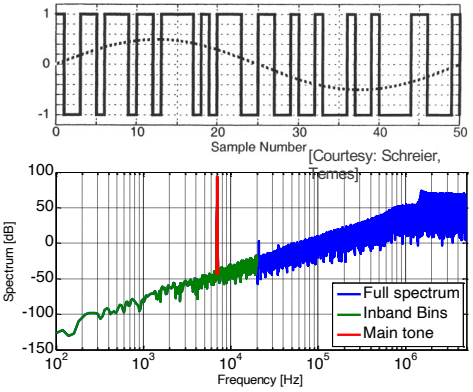
Current Steering DAC

- High speed (1GHz)
- Large area
- Moderate resolution
- Small DNL



Oversampled DAC





- Similar advantages of ΣΔ ADC:
  - High linearity
  - Simple
  - Trade-off between amplitude resolution and time resolution

Characterizing a DAC

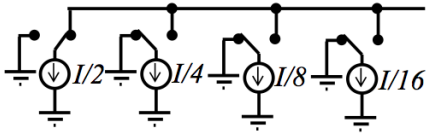
- Sampling frequency
- Number of quantization levels (bits)
- Static performance
  - Differential non-linearity (DNL)
  - Integral non-linearity (INL)
  - Monotonicity
- Dynamic performance
  - SNR, SFDR, THD, SNDR, ENOB
  - Sampling Jitter

- **Additional: glitch**

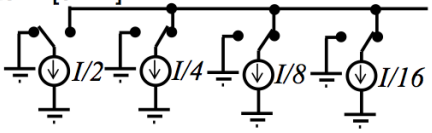
Same as ADCs

Glitch

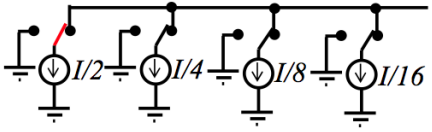
State 1: [1000]=8



State 2: [0111]=7



Intermediate: [1111]=15

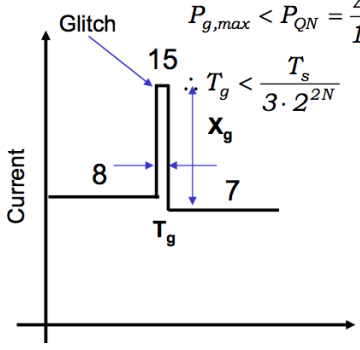


Caused by overlapping of signals
This appears within a few psec,
However, energy is not negligible.
Glitch causes the distortion of signal

$$P_{g,max} = 2^{2N-2} \cdot \Delta^2 \cdot \frac{T_g}{T_s}$$

$$P_{g,max} < P_{QN} = \frac{\Delta^2}{12}$$

$$\therefore T_g < \frac{T_s}{3 \cdot 2^{2N}}$$

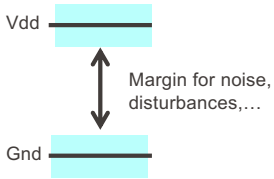


Digital Circuits in CMOS

Digital Logic

- Electronic devices are analog

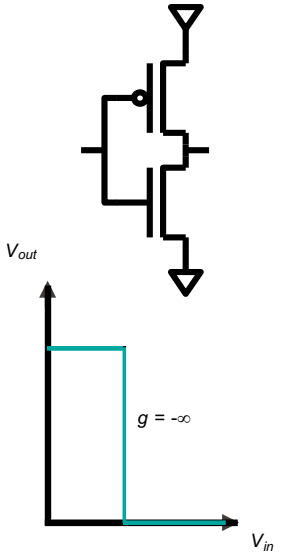
- Why digital processing?
  - Represent information using discrete levels
  - Drastically reduce the probability of errors



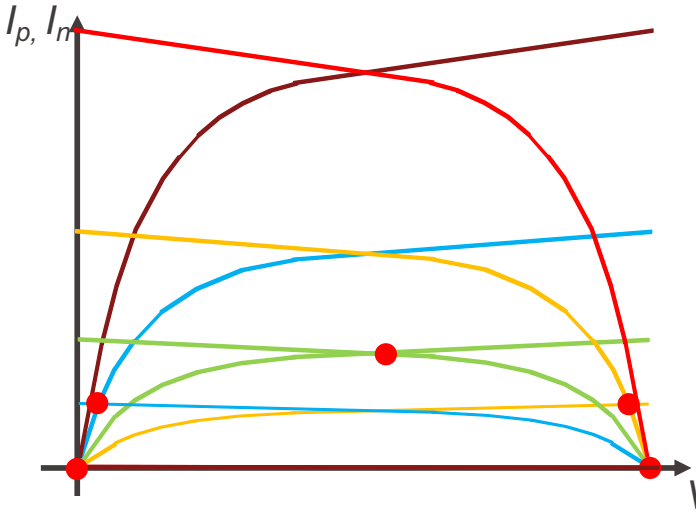
- Why CMOS for digital?
  - Any logic function can be implemented with switches
  - CMOS transistors are just very good switches

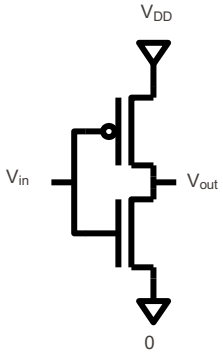
Static CMOS Circuits: the Inverter

- Basic inverter belongs to class of static circuits
  - Output always connected to either V_{DD} or V_{SS}
- Not ideal but:
  - Rail to rail voltage swing
  - Ratio less design
  - Low output impedance
  - Extremely high input impedance
  - No static power dissipation
  - Good noise properties/margins

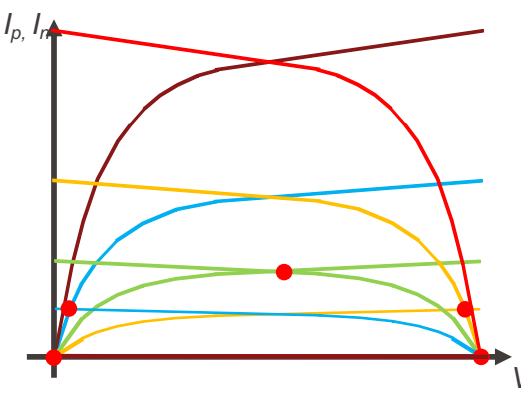


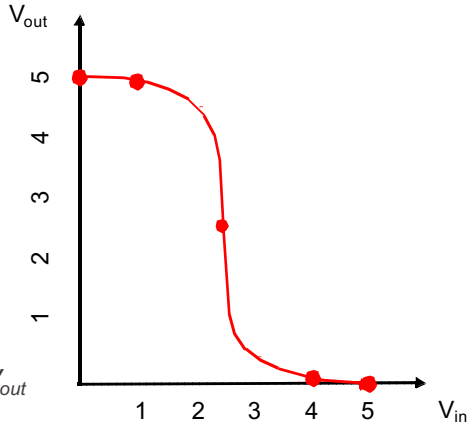
CMOS Inverter Load Characteristics



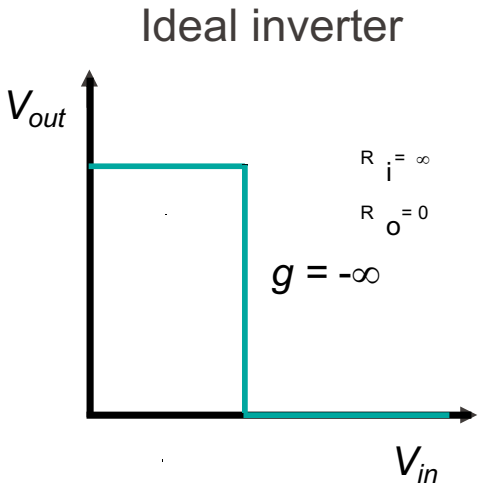


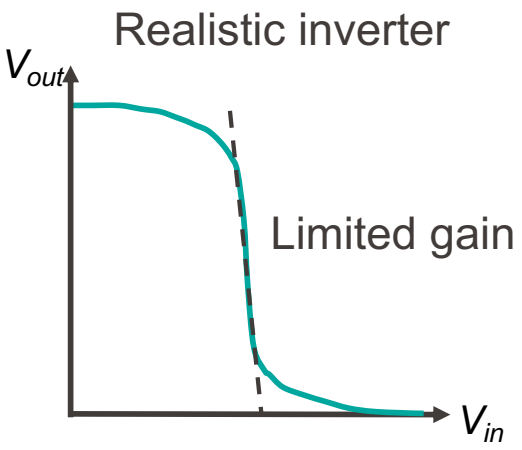
CMOS Inverter VTC



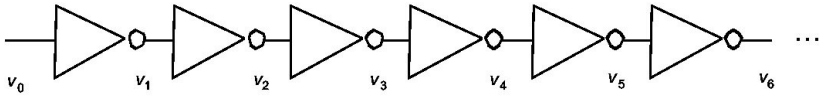


Inverter Non-Idealities

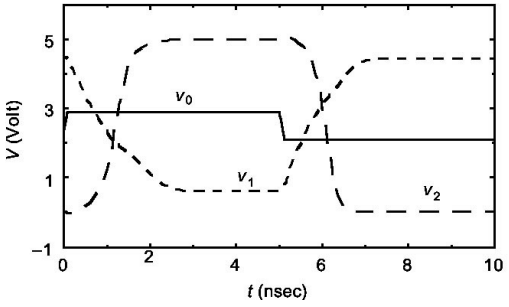


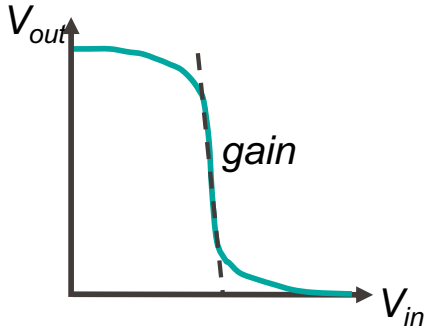


The Regenerative Property



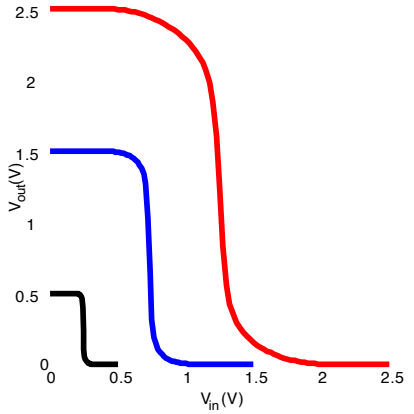
A chain of inverters

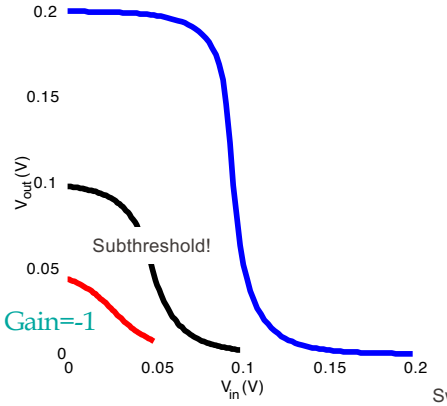




- Regenerative property
  - Ability to regenerate a weak signal in a chain of gates
- Requires |gain| > 1

Gain as a Function of VDD

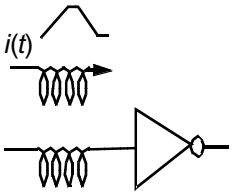




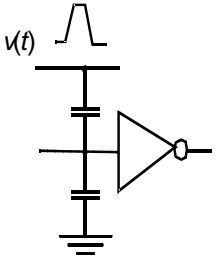
Swanson, JSSC 1972

- Inverter can work at supply voltage too low for turning transistor on, but gain deteriorates
- |Gain| should be > 1 for regeneration ⇒ V_{DDmin} > 4…8 kT/q

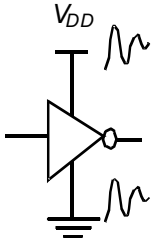
Noise in Digital Integrated Circuits



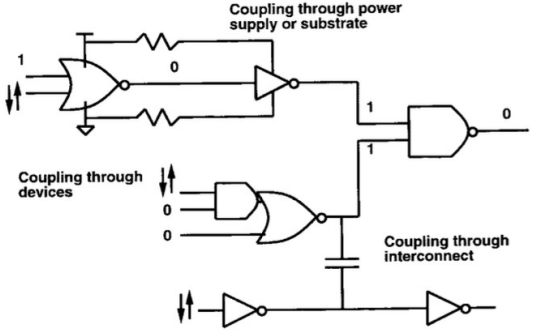
(a) Inductive coupling



(b) Capacitive coupling

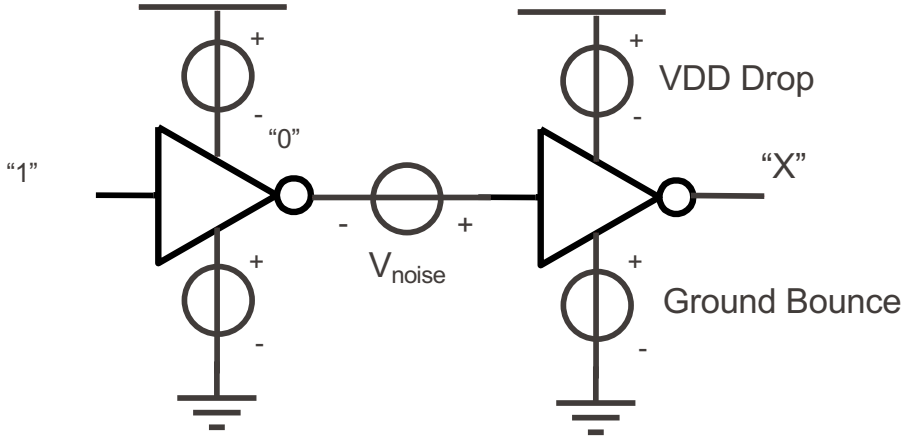


(c) Power and ground noise

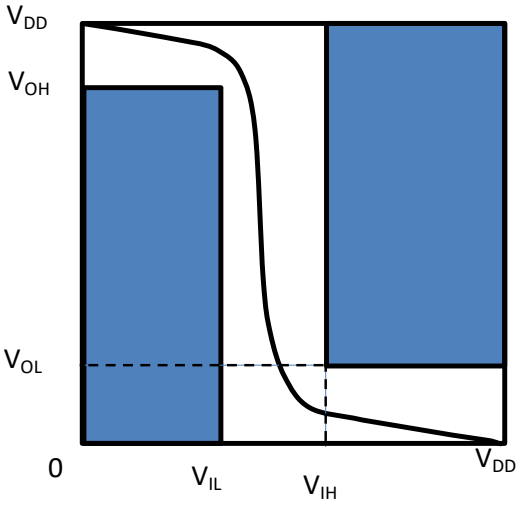


Shepard, IEEE TCAD, 1999

Noise in Digital Circuits ICs (2)

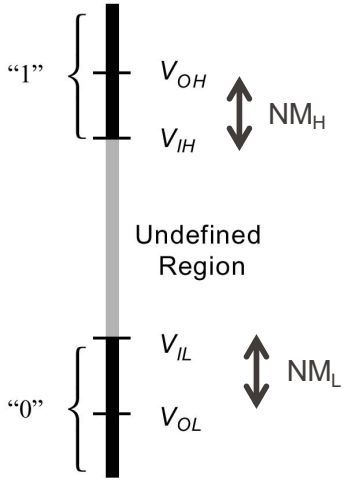


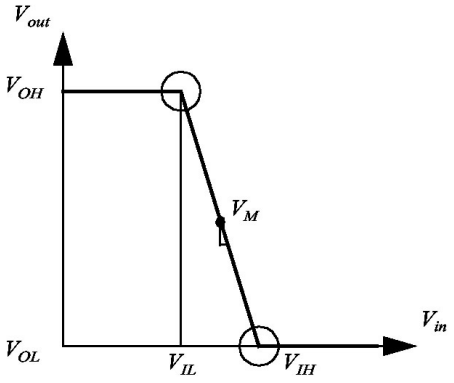
Noise Margins



- V_{OL} = Output Low Voltage
- V_{IL} = Input Low Voltage
- V_{OH}, V_{IH} = …

Noise Margins

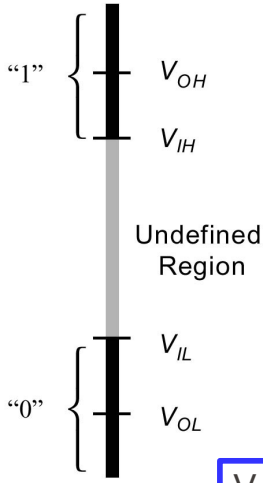


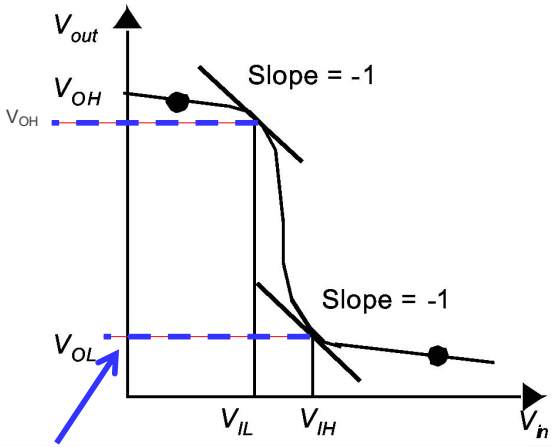


V_{OL} = Output Low Voltage
V_{IL} = Input Low Voltage
V_{OH}, V_{IH} = …

$NM_H = V_{OH} - V_{IH}$ = High Noise Margin
$NM_L = V_{IL} - V_{OL}$ = Low Noise Margin

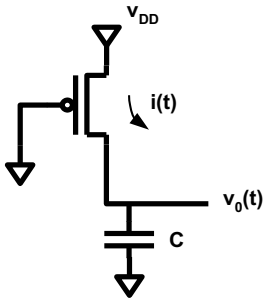
Noise Margins for Realistic Gates

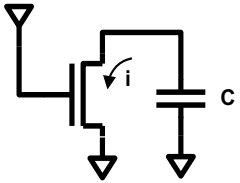




V_{OL} V_{OH} V_{IL} V_{IH} typically defined at slope = -1
(dots on curve is alternative/ambiguous choice

Power in digital CMOS – Dynamic Power



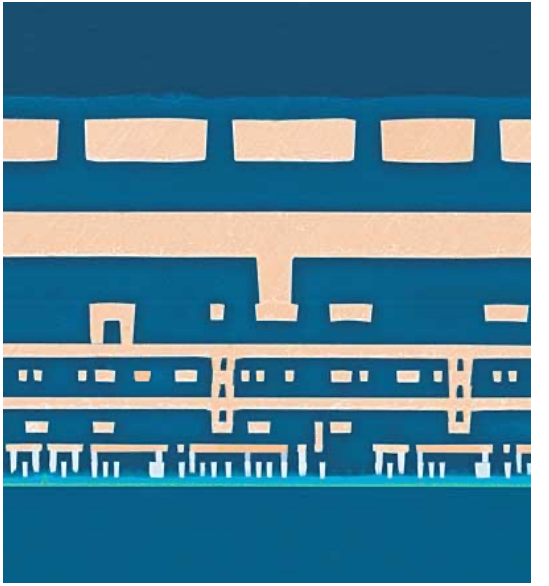


- $E_{Vdd} = \int_0^{+\infty} i(t) V_{dd}\, dt = = CV_{dd} \cdot V_{dd} = CV_{dd}^2$
- $E_{cap} = \frac{1}{2} CV_{dd}^2$
- $E_{PMOS} = \frac{1}{2} CV_{dd}^2$

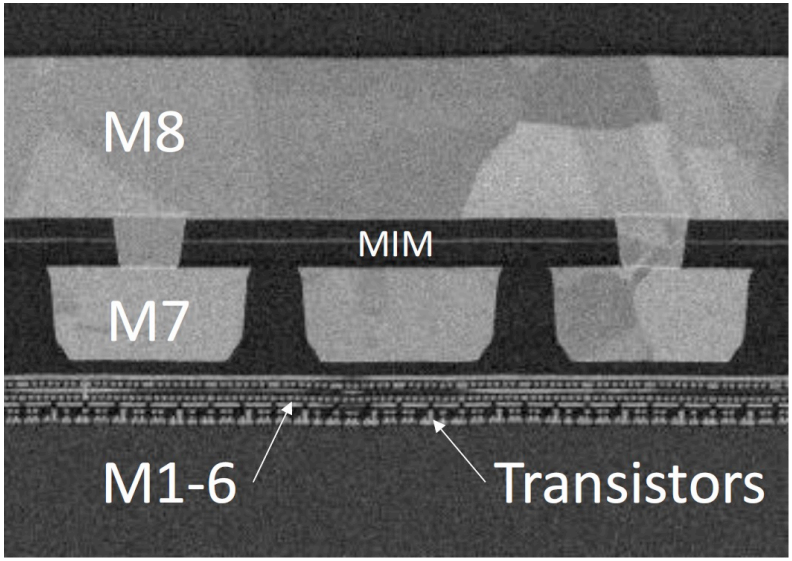
- $E_{cap} = \frac{1}{2} CV_{dd}^2$
- $E_{NMOS} = \frac{1}{2} CV_{dd}^2$
- $E_{tot} = CV_{dd}^2$

CMOS Dynamic Power Dissipation

- $Power = \frac{E_{tot}}{T} = E_{tot} f = C V_{dd}^2 f$
- Independent of transistor on-resistance
- Reduced as follows:
  - Frequency ⇒ slowing the operation rate
  - V_{dd} ⇒ but reduce noise margin
  - C ⇒ smaller devices, i.e. more advanced (scaled) process

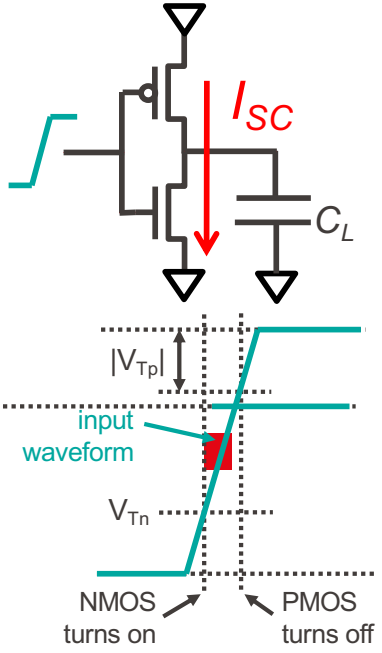


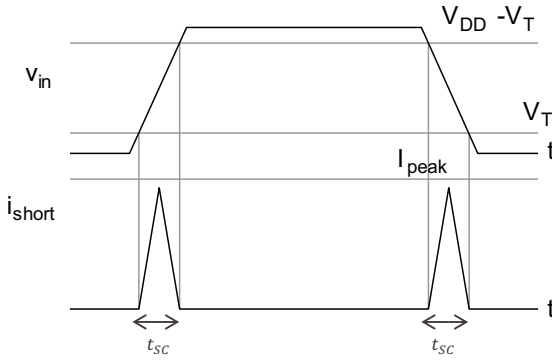
Intel 22-nm CMOS Process



Sell et al., IEDM 2017

Short Circuit Current



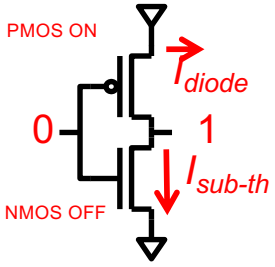


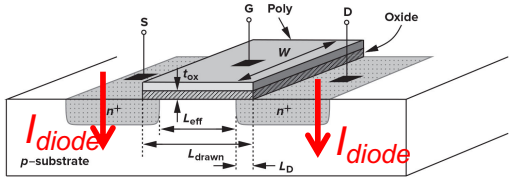
$$P_{SC} = t_{sc} V_{DD} I_{peak} f$$

$$t_{SC} = \frac{V_{DD} - 2V_T}{V_{DD}} t_S$$

- I_{peak} depends on loading C_L:
- Faster gate ⇒ more short-circ. current

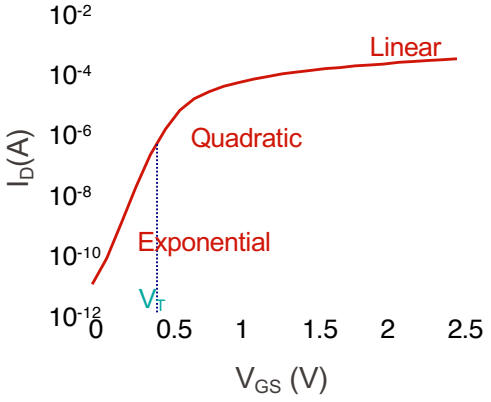
Leakage and Sub-Threshold Current



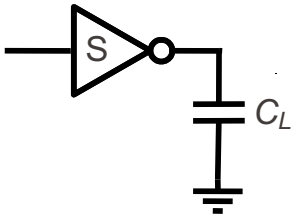


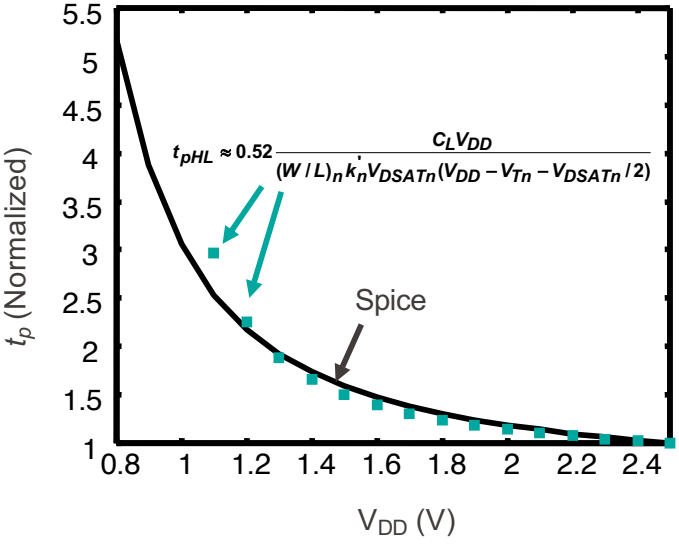
- Leakage current of reverse-biased S/D junctions
- Sub-threshold current of MOS devices (parasitic bip. dev.)
- Increases with higher T, V_{DD}, V_{DS}
- Leakage during static operation

⇒ **No zero static power**



Delay of Digital Gates



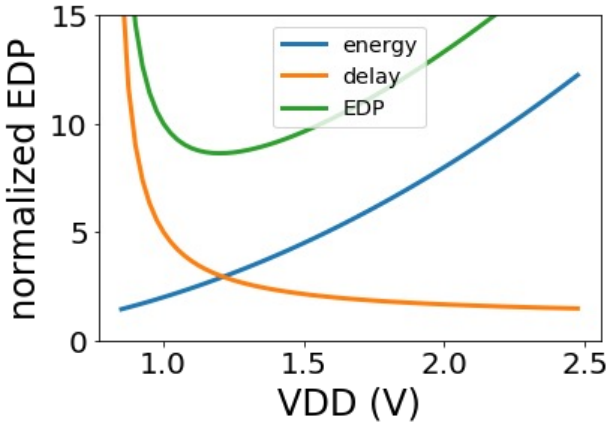


Energy Delay Tradeoff

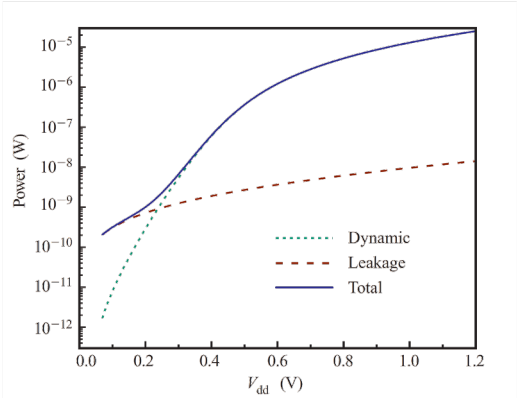
$$E_{dyn} = CV_{DD}^2$$

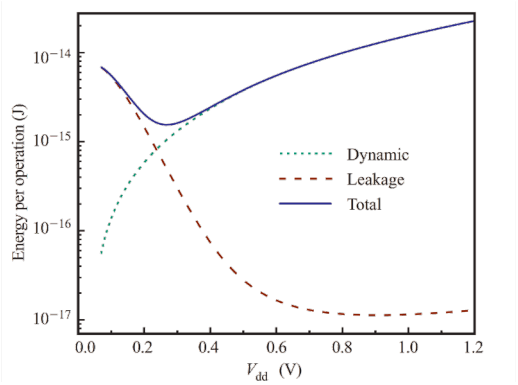
$$t_p = \frac{\alpha C V_{DD}}{V_{DD} - V_{TE}}$$

$$EDP = \frac{\alpha C^2 V_{DD}^3}{V_{DD} - V_{TE}}$$



Scaling VDD

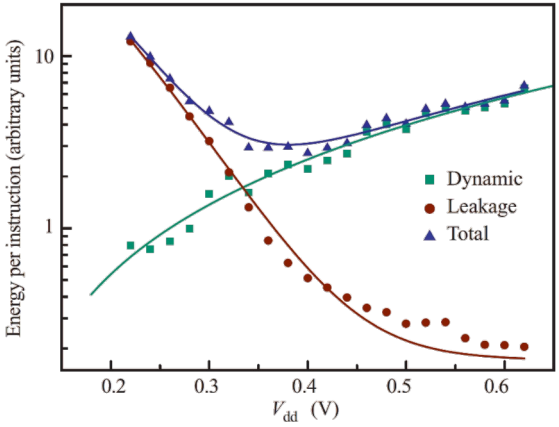




- Lower VDD ⇒ slower gates ⇒ longer operation
  ⇒ leakage energy increase
- Minimum energy typically at low frequency

Hanson et al., IBM J. Res. & Dev., July/Sep. 2006

Scaling VDD (2)

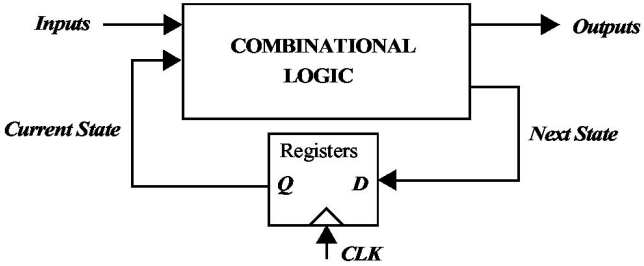


- Measured energy per operation for an 8-bit microprocessor in 130-nm CMOS technology

Hanson et al., IBM J. Res. & Dev., July/Sep. 2006

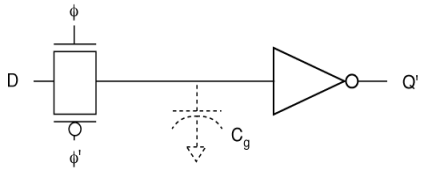
Sequential Circuits

- Combinational circuit: all digital function can be implemented
- To implement any algorithm: need for memory ⇒ sequential circuit
- Sequential circuits require ordered computation
- Several ways for imposing ordering
  - Synchronous (clock) → dominant design strategy
  - Asynchronous, self-timed → no good/general design tools



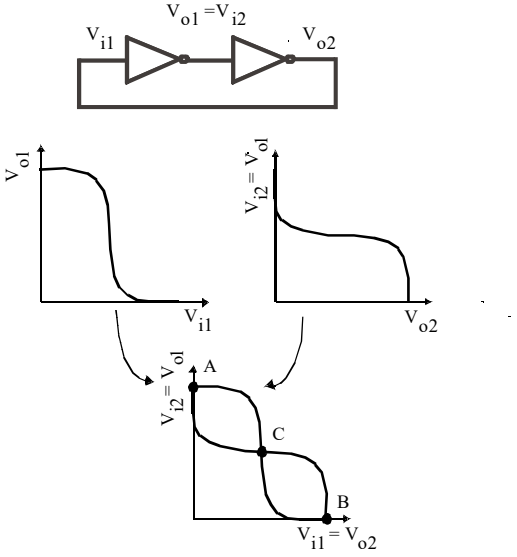
Memory Element – Latch

Dynamic latch

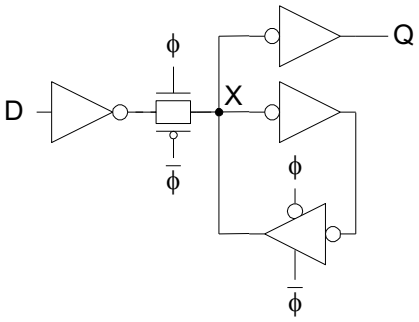


- Charge leaks away
- Not good for high T, high VDD

Static latch



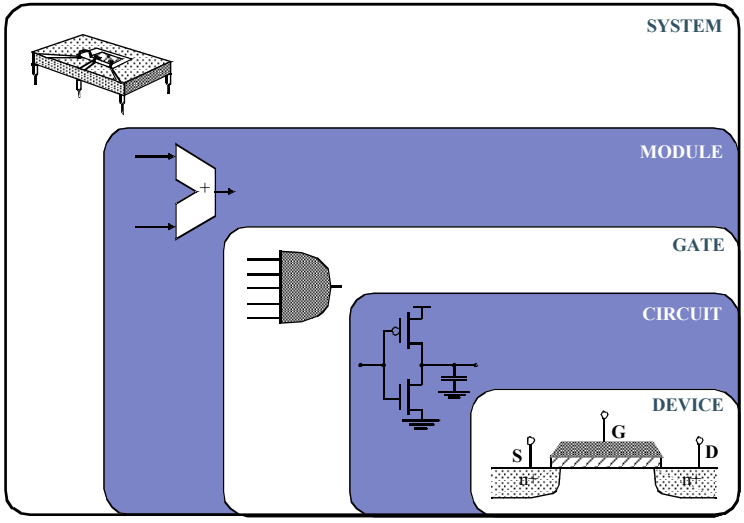
Practical Latch Design



- **Buffered input and buffered output**
- **Enable to write**
- Robust
- Widely used in standard cells

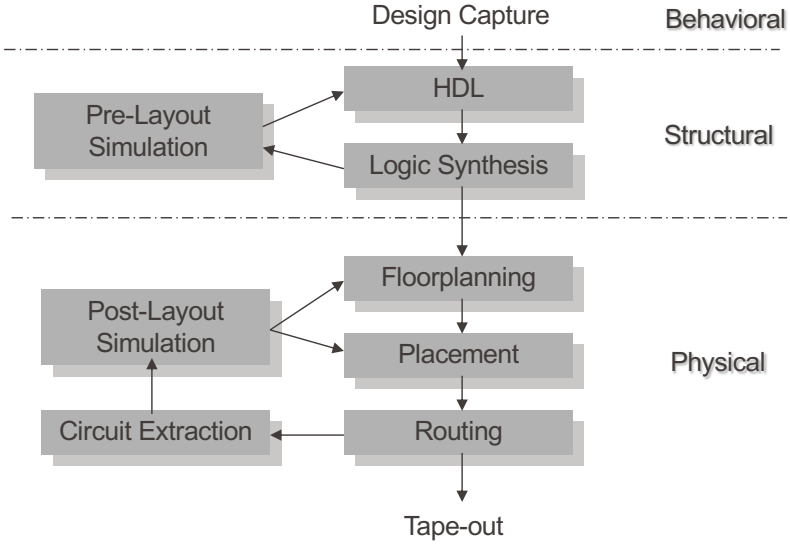
☺ No back driving
☺ Very robust (most important)
- Variant designs:
  - w/o input buffer and/or output buffer,
  - More efficient, less robust
- Safe in noise-controlled environments

Abstraction Levels



Courtesy: Jan Rabaey, UCB

Digital Design Flow



Courtesy: Jan Rabaey, UCB

Lowerbounds in Digital Design

$$V_{DD,min} \approx 2\frac{kT}{q}\ln(2) = 36\text{mV}$$

CMOS circuits operate in subthreshold wherever this equation holds

$$I_{DS} = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nv_t}}\left(1 - e^{-\frac{V_{DS}}{v_t}}\right);\ I_0 = \mu_0 C_{ox}\frac{W}{L}(n-1)v_t^2,$$

n is the sub-threshold slope (SS) factor and $v_t = kT/q$,

The net effect in sub-threshold regimes is a decrease of leakage currents by orders of magnitude, implying a significant increase in the I_{ON}/I_{OFF} ratio

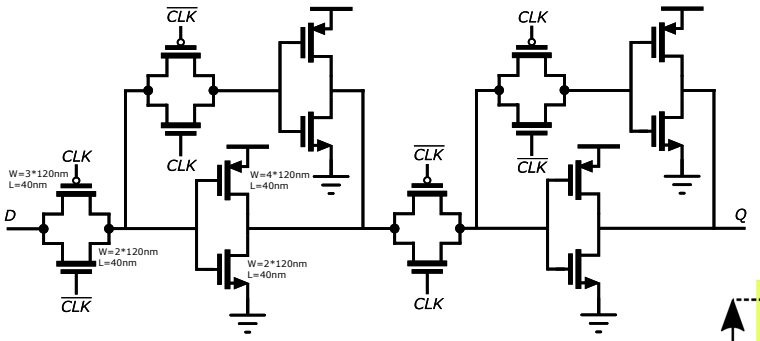
Lowerbounds in Digital Design (2)

Assuming an ideal SS factor $n = 1$, at 4.2 K, according to well established room temperature models, one could theoretically achieve $V_{DD,min} \approx 2\ln(2)v_t = 0.48\text{mV}$.

However, at 4.2 K the consensus is that *n≈34.9*. Thus, this fundamental limit is actually *VDD,min*≈ 2.47mV. Additional non-idealities include reverse short-channel effect (RSCE) and inverse narrow-width effect (INWE).

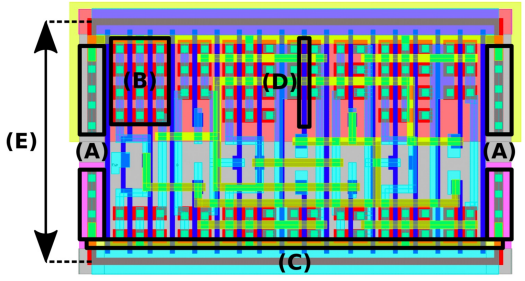
Both effects substantially modulate the threshold voltage.

Recommendations



A) create extensive substrate contacts and well-taps, so as to minimize latch-up;

B) resize the transistors, so as to reduce INWE and thus maximize V_{TH} modulation;



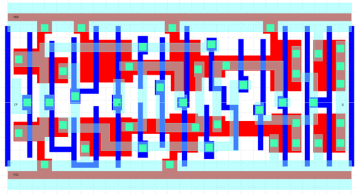
C) add secondary power rails;

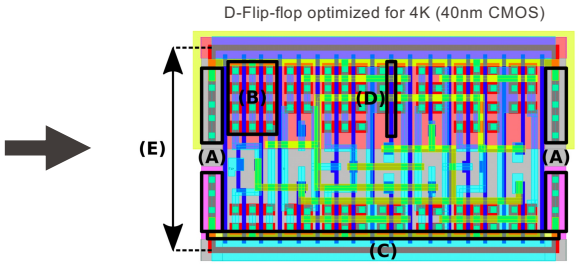
D) minimize the length of transistors;

E) when useful, make the layout aware of mismatch by increasing the overall height of the cells.

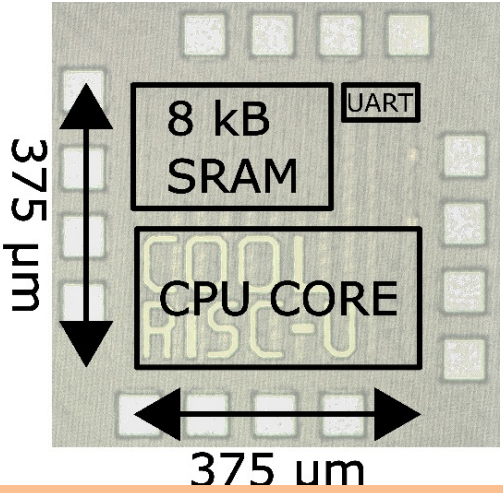
Ultra-Low Voltage Library ‘cooLib’

- Digital library optimized for 4K
- Ultra low voltage operation (100s mV)
- Sub-threshold bias of N/P MOS
- Resilient to latchup and hysteresis-free
- Several logic families (static and dynamic CMOS)
- Compatible with commercial P&R tools





RISC-V Processor

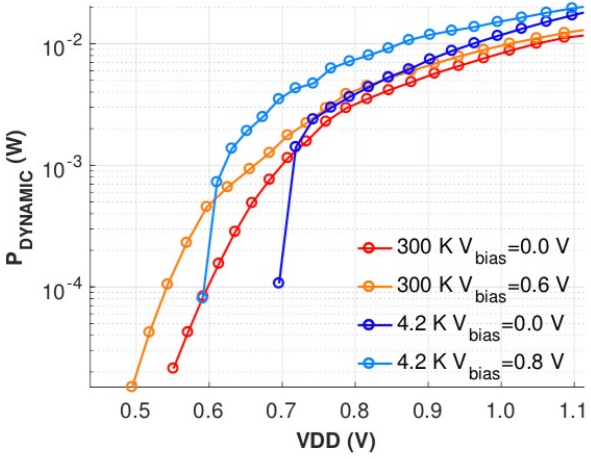


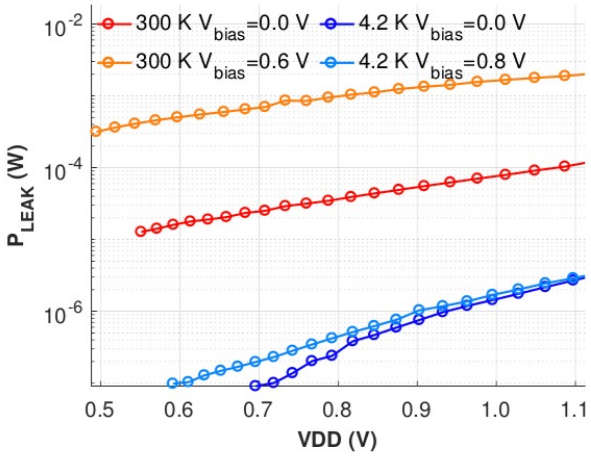
FEATURES

- RISC-V (picorv32, open-source) implemented using ‘CooLib’
- 8 Kb single-port SRAM from TSMC
- SRAM operates at nominal voltage, core at lower voltage
  - Interfacing by ‘CooLib’ level-shifters
- UART interface for serial in/output
- JTAG interface for SRAM write/read

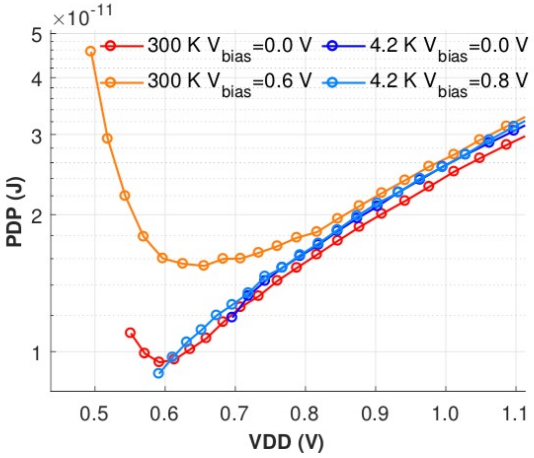
Fully functional µP operating at 4K

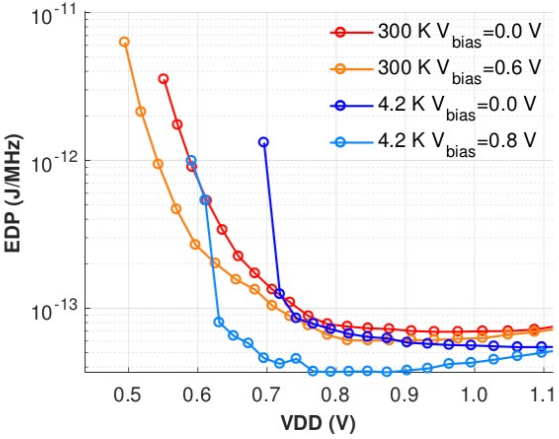
Dynamic vs. Static Power





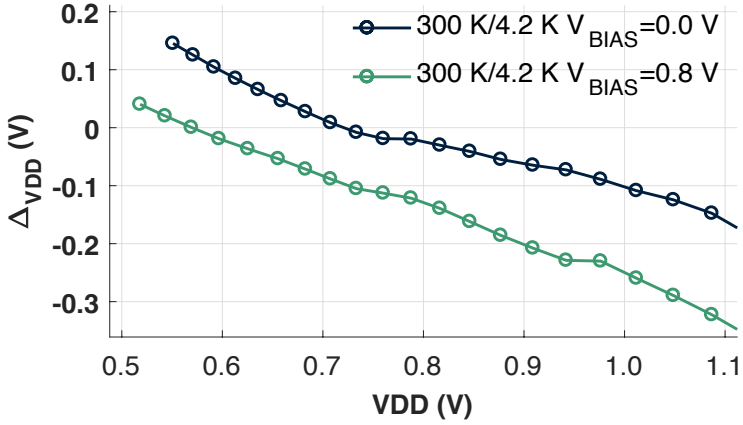
FOMs


×10^-11
5
4
3
2
1
PDP (J)
300 K V_bias=0.0 V
4.2 K V_bias=0.0 V
300 K V_bias=0.6 V
4.2 K V_bias=0.8 V
0.5
0.6
0.7
0.8
0.9
1.0
1.1
VDD (V)


10^-11
10^-12
10^-13
EDP (J/MHz)
300 K V_bias=0.0 V
300 K V_bias=0.6 V
4.2 K V_bias=0.0 V
4.2 K V_bias=0.8 V
0.5
0.6
0.7
0.8
0.9
1.0
1.1
VDD (V)

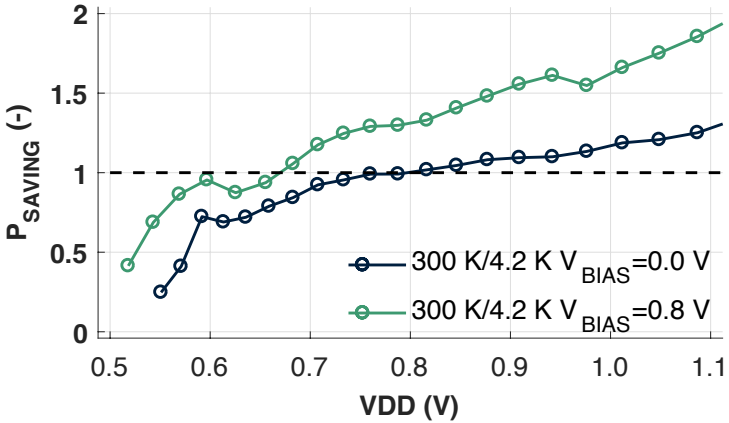
Forward Bias

- When a bias is applied to the substrate
- Δ_{VDD} required to achieved equal F_{MAX}

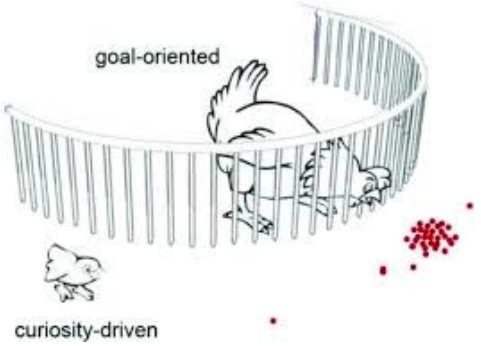


Forward Bias

- When a bias is applied to the substrate
- Average power savings for equal F_{MAX}



Thank you



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