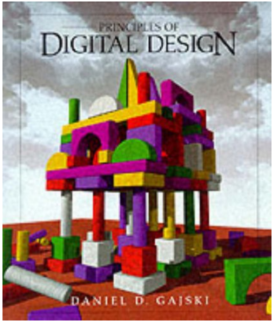
EPFL

MICRO-435 Quantum and Nanocomputing

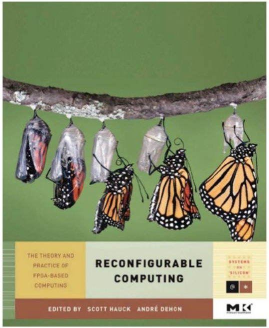
Edoardo Charbon
Mariagrazia Graziano

October 7 2025

Reference books

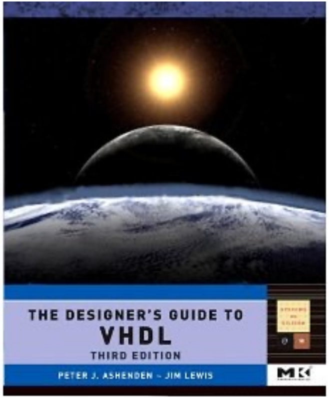


Daniel D. Gajski,
Principles of Digital Design, Prentice Hall, 1st Edition (1997).



Scott Hauck, André Dehon, Ed.
Reconfigurable Computing, Morgan Kaufmann, 1st Edition (2007).

Also recommended



Peter J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann Publishers,

1st Edition (1995)

Today

John M. Martinis

Facts

Ill. Niklas Elmehed © Nobel Prize Outreach

John M. Martinis
Nobel Prize in Physics 2025

Born: 1958

Affiliation at the time of the award: University of California, Santa Barbara, CA, USA

Prize motivation: “for the discovery of macroscopic quantum mechanical tunnelling and energy quantisation in an electric circuit”

Prize share: 1/3

To cite this section
MLA style: John M. Martinis – Facts – 2025. NobelPrize.org. Nobel Prize Outreach 2025. Tue. 7 Oct 2025. <https://www.nobelprize.org/prizes/physics/2025/martinis/facts/>

Quantum Computing Syllabus (Week 1-7)

- Fundamentals of quantum computing
- Qubit realization & control
- **Cryo-CMOS components**
- Scalable quantum computers
- Quantum communication, sensing, and metrology

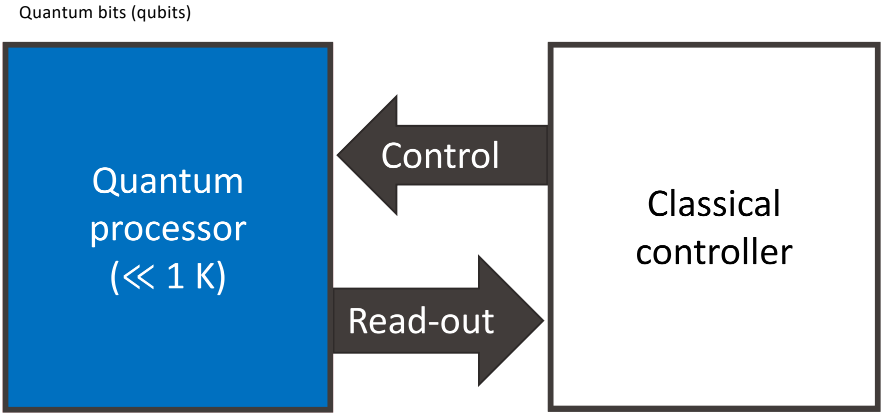
Cryo-CMOS Components

- Choosing a technology
- Cryo-CMOS modeling
- LNAs
- ADCs

Acknowledgements: Fabio Sebastiano, Marcel Pelgrom, Akira Matsuzawa

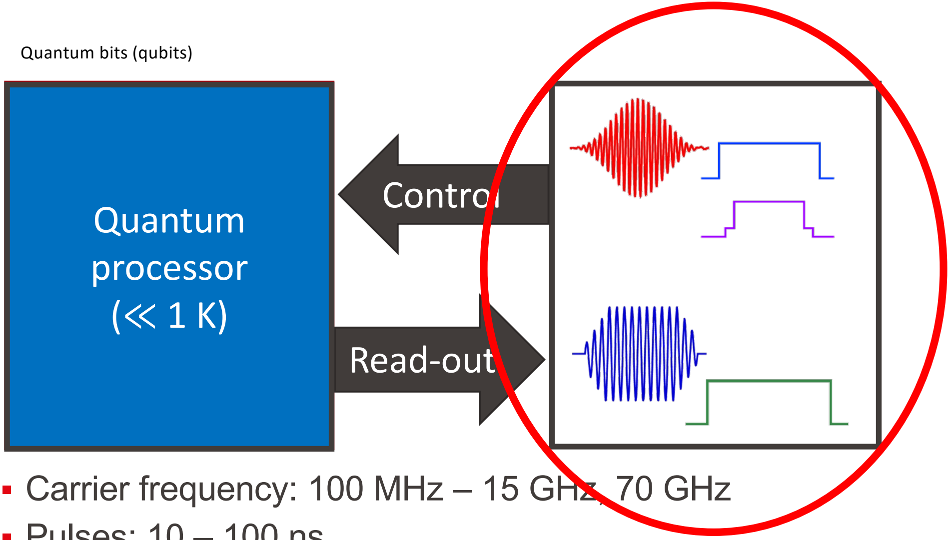
Choosing a Technology

Interfacing Qubits with Classical World



- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns

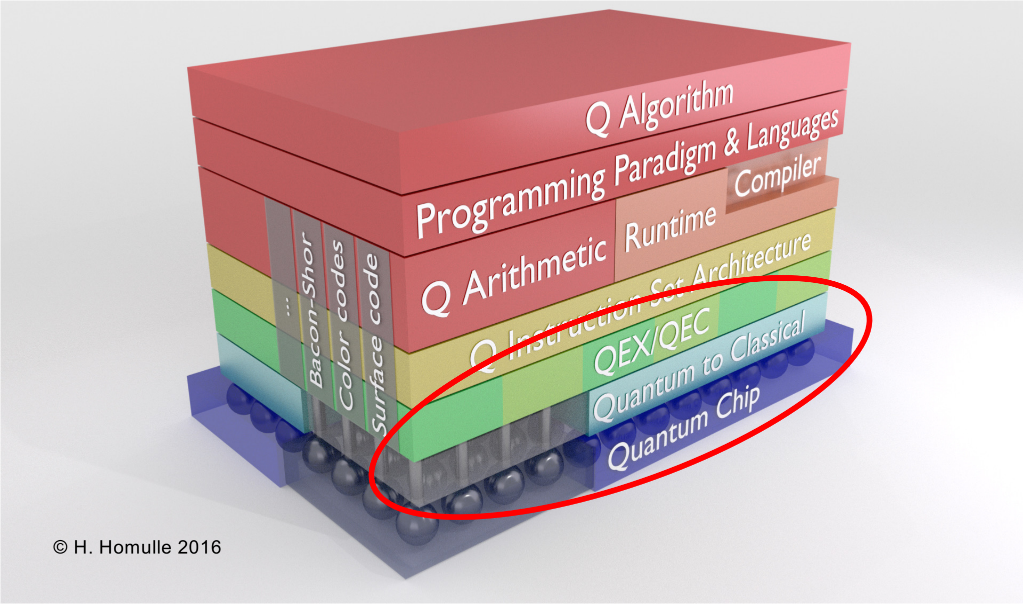
Interfacing Qubits with Classical World



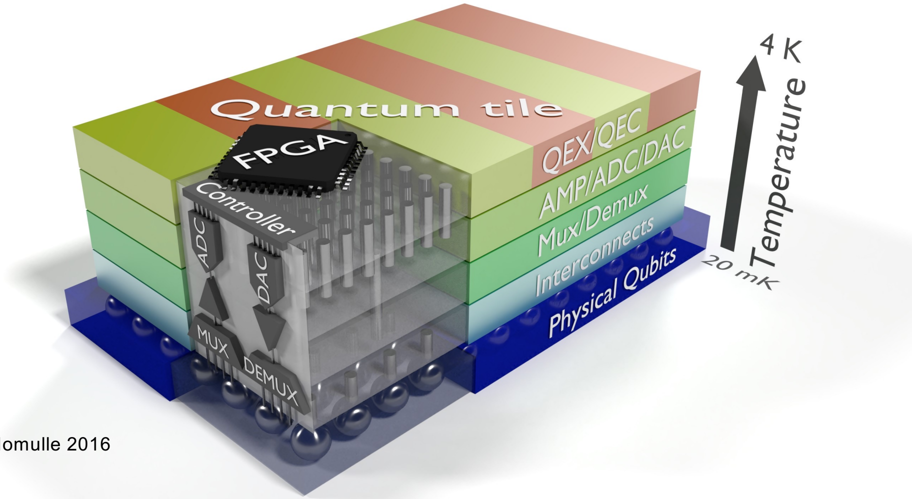
- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns
- Readout techniques for spin qubits: **ESR, EDSR**

ESR: Electron spin resonance – EDSR: Electric dipole spin resonance

Quantum Computing Stack



Quantum Computing Stack Detail



Which Technology?

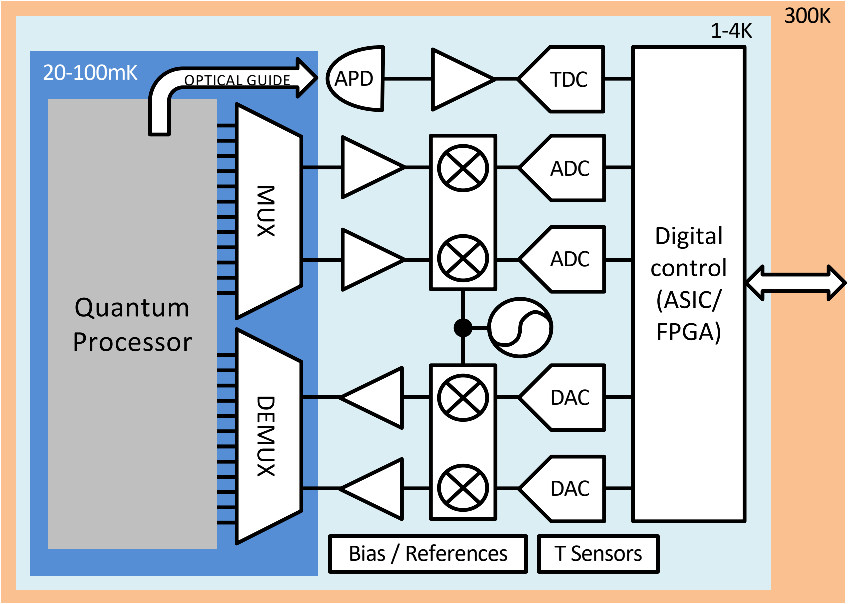
- Single-electron Transistors (SET)
- Superconducting devices (RSFQ, RQL, SQUID)
- Low-temperature semiconductors:

Device	Lowest useable temperature	Limit
Si BJT	100 K	Low gain
Ge BJT	20 K	Carrier freeze-out
SiGe HBT	4 K (or lower?)	?
Si JFET	40 K	Carrier freeze-out
III-V MESFET	4K (or lower?)	Lower freeze-out?
CMOS	4 K (30 mK ?)	?

Most used (Si JFET, III-V MESFET)

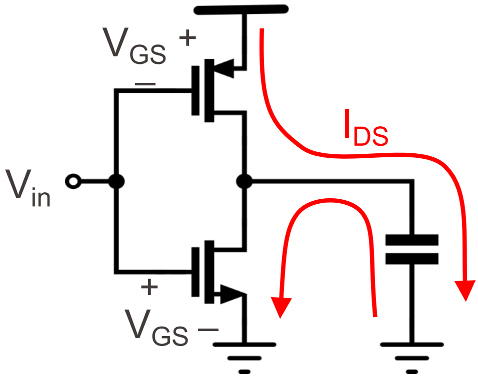
VLSI integration → CMOS

Cryo-CMOS Quantum-Classical Interface



Cryo-CMOS Modeling

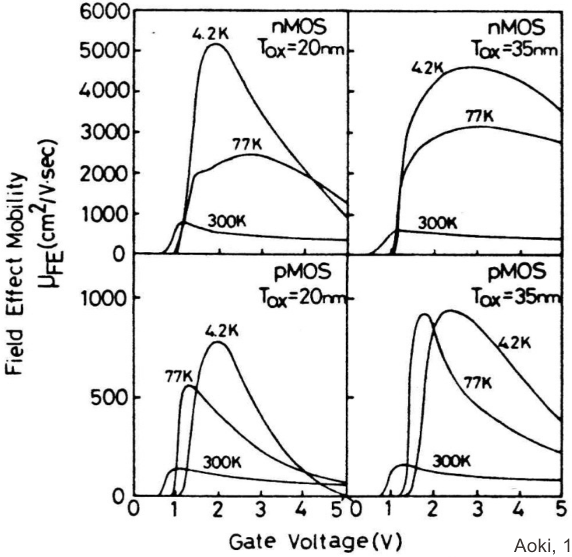
Cryo-CMOS Parameters



$$I_{DS} = \mu \cdot C_{OX} \frac{W}{2L}(V_{GS} - V_T)^2$$

- Speed depends on
  - Mobility
  - Threshold voltage
  - Parasitic resistance/capacitance

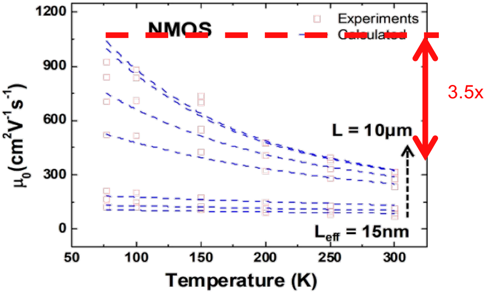
Mobility over Temperature

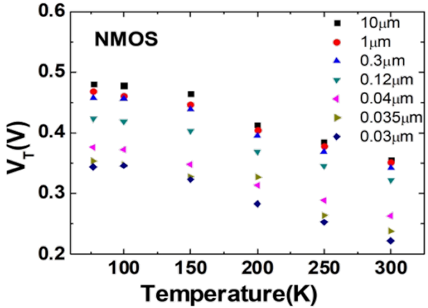


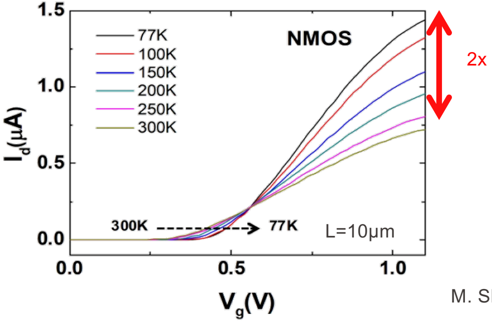
Aoki, 1987

- Mobility increases at low temperature
- It depends on the materials used in the substrate

Mobility in Modern Process (14 nm)







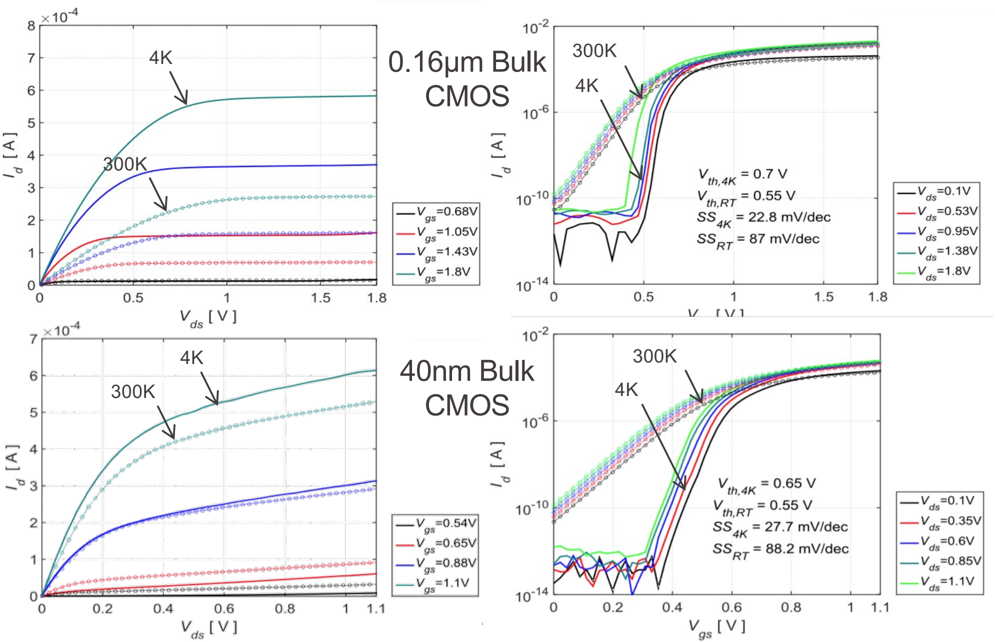
In general:

- More current, less parasitics
- Higher speed
- Lower thermal noise

M. Shin, 2014

EPFL

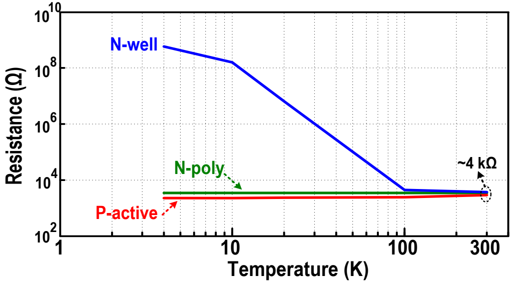
Cryo-CMOS Characterization: Transistors



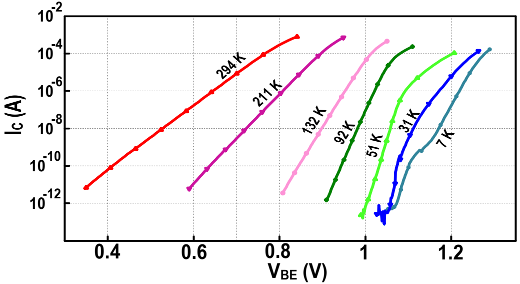
Cryo-CMOS characterization: passives

0.16µm bulk CMOS

Integrated resistor



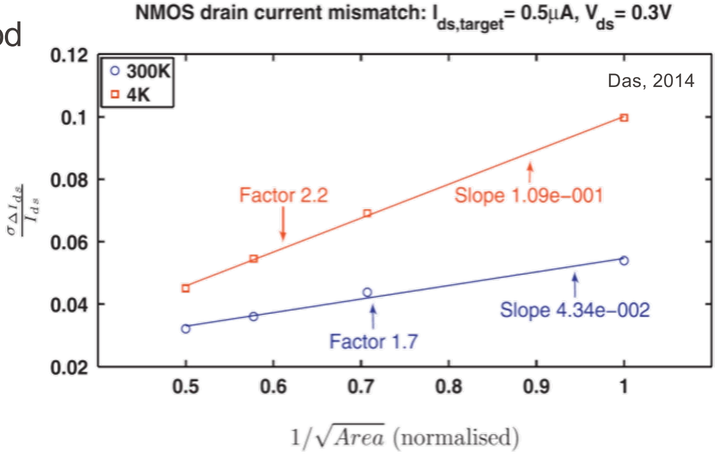
Integrated BJT



L. Song et al. IEEE Sensors 2016

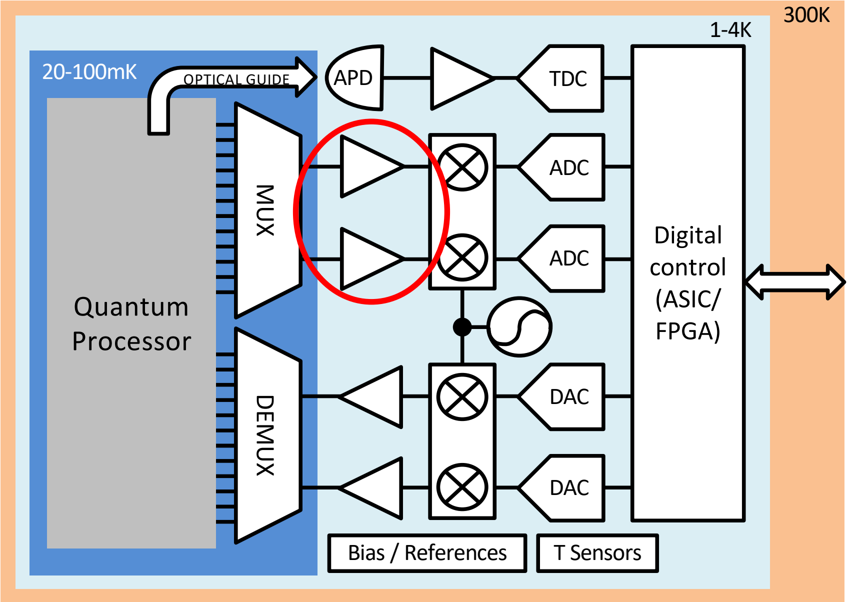
Transistor Mismatch

- Mismatch: difference between nominally equal devices
- Fundamental for ADC/DAC design
- Degradation up to 2x
- Root cause not yet understood



Low-Noise Amplifiers (LNAs)

Cryo-CMOS Quantum-Classical Interface



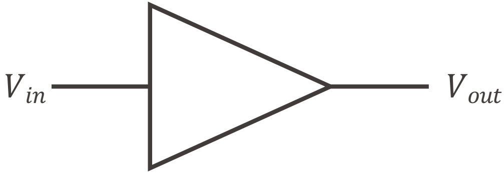
Classification of Amplifiers

- Signal amplifiers
  - Deliver small signals
- Power amplifiers
  - Deliver large signal
  - Classified based of efficiency (A, B, AB, C, D, E, …)

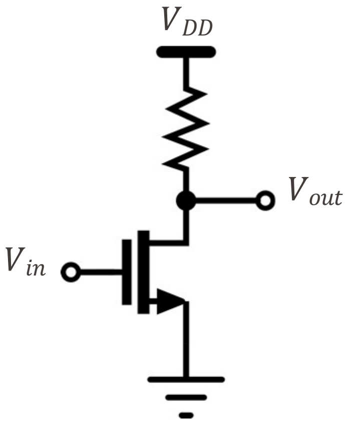
Input	Output	Amplifier type	Ideal input impedance	Ideal output impedance
I	I	Current	0	∞
I	V	Transimpedance	0	0
V	I	Transadmittance	∞	∞
V	V	Voltage	∞	0

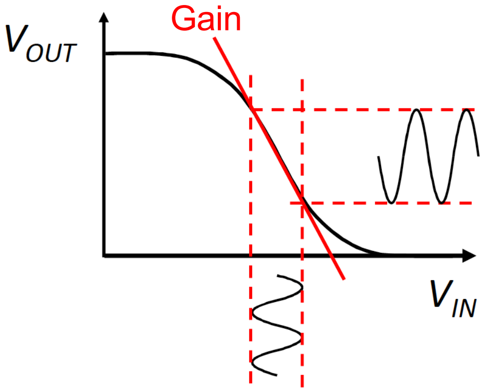
Amplifier Performance

- Gain
- Linearity
- Bandwidth
- Noise
- Immunity to interference
- Impedance matching
- Power dissipation



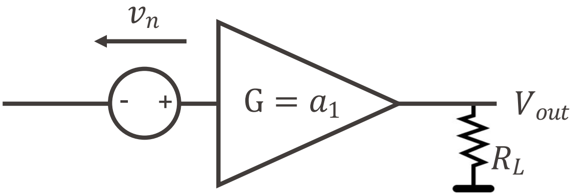
Common-source Amplifier Example





Noise in Amplifiers

- Input-referred noise (voltage) source v_n is a random process with mean $\overline{v_n} = 0$ and variance $\overline{v_n^2}$.
- This source accounts for all sources of noise in the amplifier.



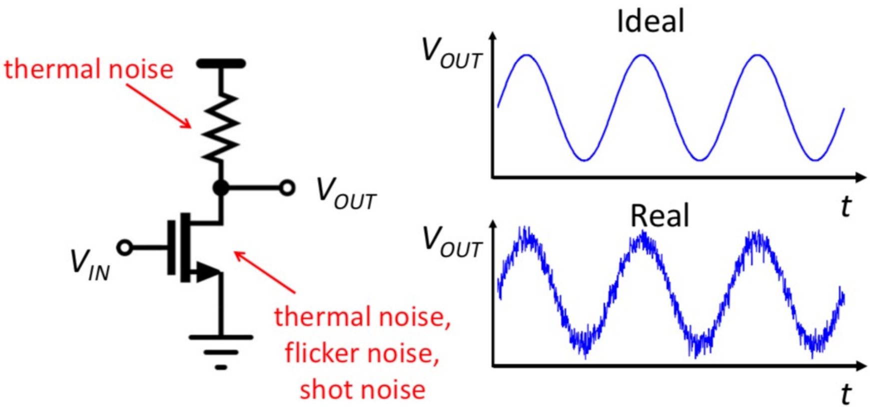
- The output noise is computed as:

$$\overline{v_{out\_n}^2} = |a_1|^2\, \overline{v_n^2}.$$

- If referred to output impedance R_L, then the noise power $P_n = \frac{|a_1|^2\, \overline{v_n^2}}{R_L}$.

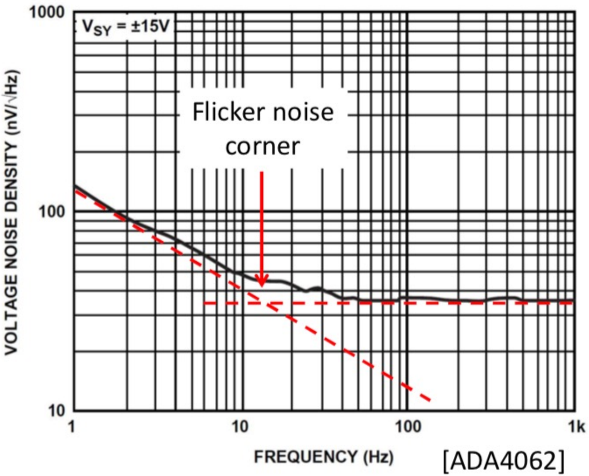
Noise in Amplifiers (2)

- Noise sources: thermal noise, shot noise, $1/f$ or flicker noise, RTS.



Noise Sources

- White noise:
  - Thermal noise (resistors, transistors)
  - Shot noise (diodes, transistors)
- Flicker or $1/f$ noise (non-idealities of fabrication).
- Random telegraph signal (traps and fabrication non-idealities).



[ADA4062]

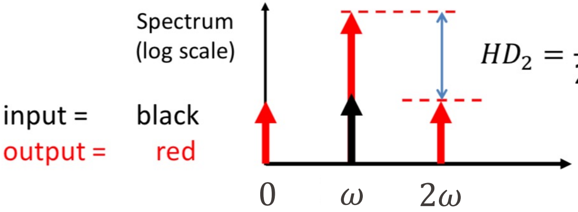
Linearity – Harmonic Distortion

- Gain may not be linear, thus output voltage is represented as:

$$V_{out} = a_0 + a_1 \cdot V_{in} + a_2 \cdot V_{in}^2 + a_3 \cdot V_{in}^3 + a_4 \cdot V_{in}^4 + \cdots$$

- Thus, if $V_{in} = A \cdot \cos\omega t$, then

$$V_{out} = a_0 + a_1 \cdot A \cdot \cos\omega t + a_2 \cdot A^2 \cdot \cos^2\omega t + a_3 \cdot A^3 \cdot \cos^3\omega t + \cdots$$
$$= a_0 + a_1 \cdot A \cdot \cos\omega t + \frac{1}{2} a_2 A^2 + \frac{1}{2} a_2 A^2 \cdot \cos 2\omega t + \cdots$$



$$HD_2 = \frac{a_2}{2a_1} A$$

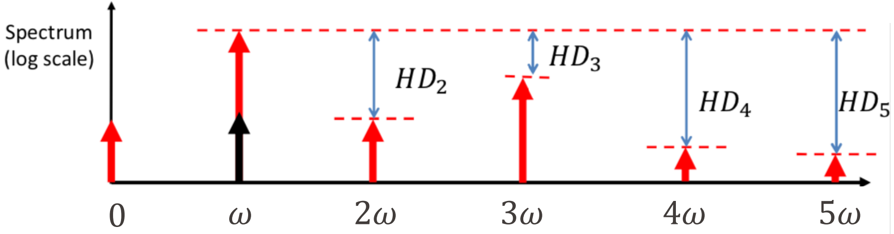
Linearity – Harmonic Distortion (2)

- Higher order distortions can be similarly computed:

$$HD_3 = \frac{a_3}{4a_1}A^2,\ \ HD_4, \dots$$

- Total harmonic distortion:

$$THD = \sqrt{\sum_i HD_i^2}$$

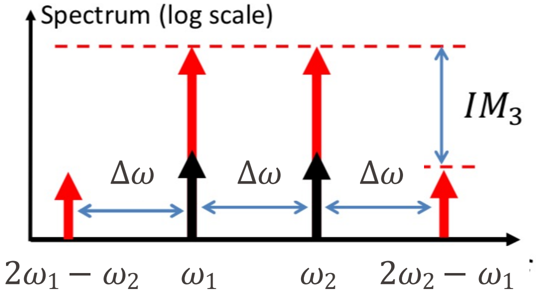


Intermodulation

- Let $V_{in} = A \cdot (\cos\omega_1 t + \cos\omega_2 t)$, then:

$$IM_3 = \frac{3a_3}{4a_1}A^2 = 3HD_3.$$

- Intermodulation creates harmonics at distances $\Delta\omega = \omega_2 - \omega_1$.

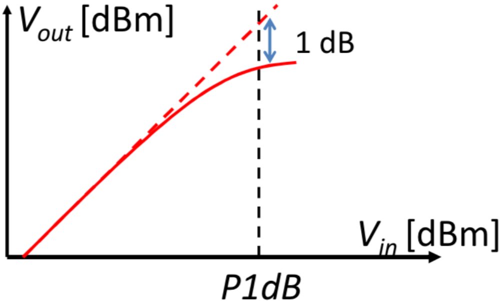


1-dB Compression Point

- Let $V_{in} = A \cdot \cos\omega_1 t$

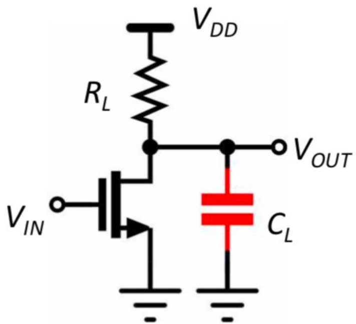
then:

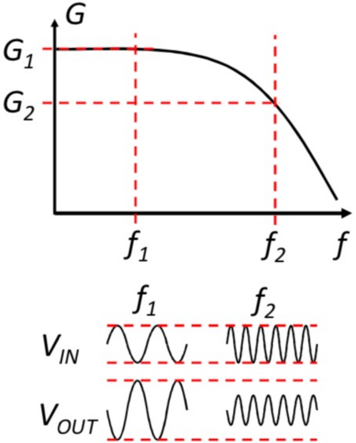
$$V_{out} = a_1 V_{in} + a_3 V_{in}^3$$
$$= \left(a_1 + \frac{3}{4} a_3 A^2\right) \cdot A \cdot \cos\omega t + \frac{a_3}{4} A^3 \cdot \cos 3\omega t$$



Bandwidth

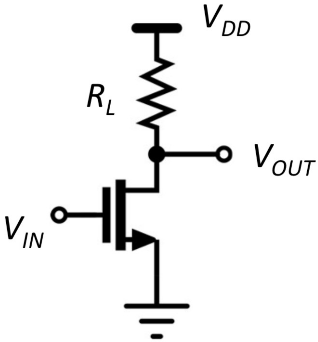
- Amplifier has frequency limits due to internal passive components.

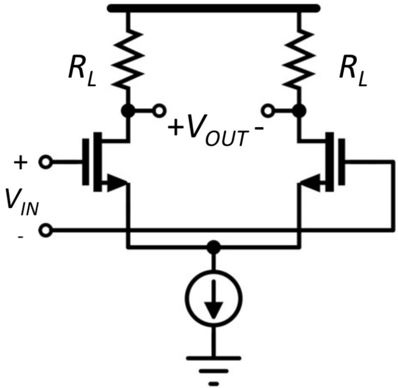


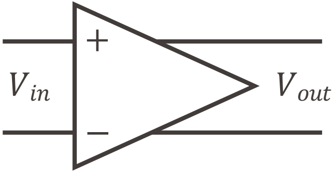


Differential Amplifiers

- Input/output characteristic = odd function
- No offset ($a_0 = 0$), no even-order distortions ($a_i = 0, HD_i = 0, i = 2,4,6, \ldots$)
- Mismatch destroys, in part, this property.

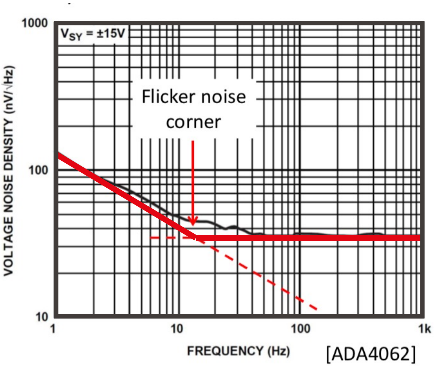


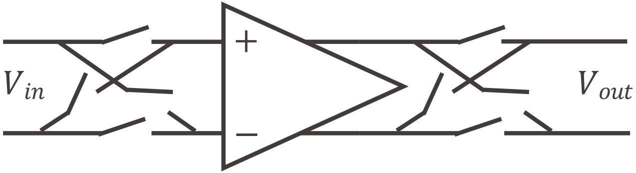


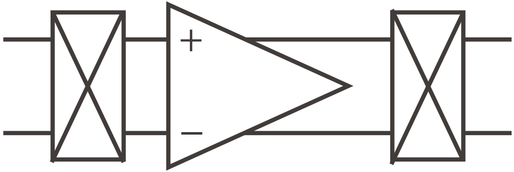


Chopper Amplifiers

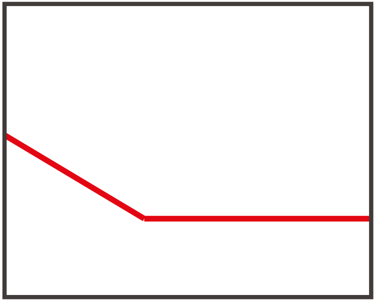
- Reduce 1/f noise
- Cancel mismatch effects (to a first approximation)



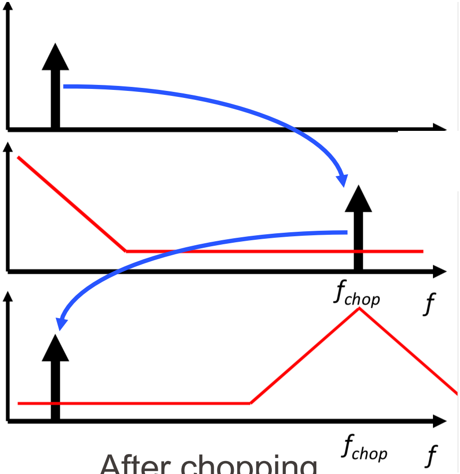




Chopper Amplifiers (2)



Before chopping

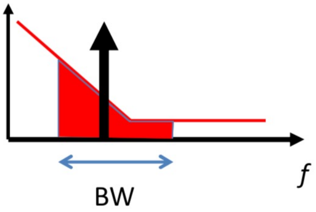


After chopping

Noise Specifications

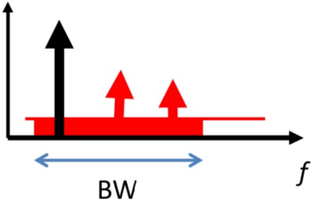
- S_{out} = signal power
- N_{out} = noise power
- Signal-to-Noise Ratio

$$SNR = \frac{S_{out}}{N_{out}}$$

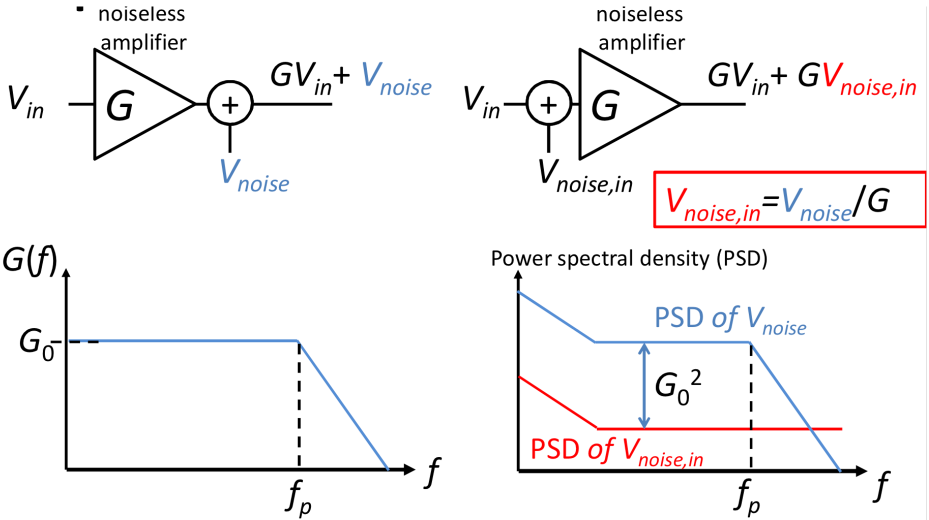


- Must be defined for a certain bandwidth BW
- If also distortion are taken into account:
  - Signal-to-Noise-and-Distortion-Ratio
  - $SNDR = \frac{S_{out}}{\sqrt{N_{out}{}^2 + S_{out}{}^2 THD^2}}$

$$= \sqrt{\frac{1}{\frac{1}{SNR^2} + THD^2}}$$

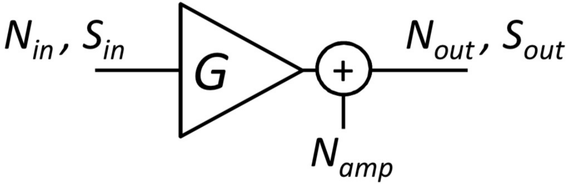


Noise Specifications (2)



- Input-referred noise ($V_{noise,in}$) is an useful tool for calculation
- But it is not really there!

Noise Specifications (3)



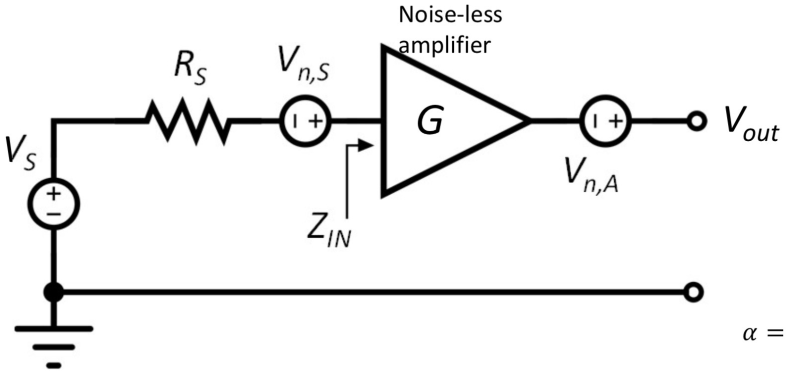
$$N_{out} = G^2 N_{in} + N_{amp}$$
$$S_{out} = G^2 S_{in}$$
$$N_{amp,in-referred} = N_{amp}/G^2$$

- Noise Figure

$$NF = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}}{S_{out}}\frac{N_{out}}{N_{in}} = \frac{1}{G}\cdot\frac{GN_{in}+N_{amp}}{N_{in}} = 1 + \frac{N_{amp}}{GN_{in}}$$

- By definition $N_{in} = 4kTR_S$, R_S= 50 Ω, T = 290 K
  - $NF = 1 + \frac{N_{amp,in-referre}}{4kTR_S}$
- *NF* is expressed in dB
- *NF* is frequency dependent

Noise Figure



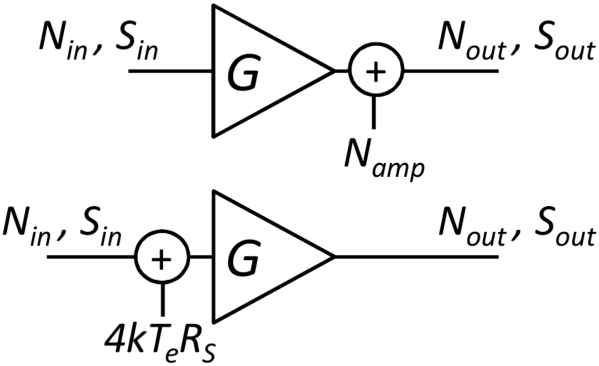
$$\alpha = \frac{Z_{IN}}{Z_{IN} + R_S}$$

- $SNR_{in} = \frac{V_S^2|\alpha|^2}{V_{n,S}^2|\alpha|^2} = \frac{V_S^2}{V_{n,S}^2}$, $SNR_{out} = \frac{V_S^2|\alpha|^2|G|^2}{V_{n,S}^2|\alpha|^2|G|^2+V_{n,A}^2}$
- $NF = \frac{SNR_{in}}{SN\ \ out} = \frac{1}{|\alpha|^2|G|^2}\frac{V_{n,S}^2|\alpha|^2|G|^2+V_{n,A}^2}{V_{n,S}^2}$

  Noise at the output

  Noise at the output due only to input noise
- **Be aware:** NF depends on source and input impedance

Noise Temperature



- T_e is temperature of resistor R_S to generate same output noise
- $NF = 1 + \frac{N_{amp,in-referre}}{4kT_0R_S} = 1 + \frac{4kT_eR_S}{4kT_0R_S} = 1 + \frac{T_e}{T_0}$
- By definition $T_0 = 290$ K
- Equivalent noise resistance is defined in analog way

Example

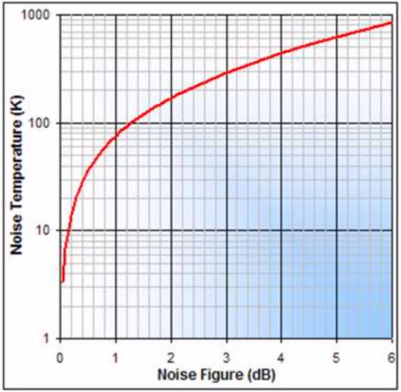
- Amplifier noise is the same as a 50 Ω resistance (input referred):
  - $V_{in,rms} = (4\ kT\ R_S\ BW)^{0.5}$

    $= 0.9\ nV_{rms}$

    @ 290 K, BW = 1 Hz
  - NF = 3 dB, T_e= 290 K, R_e = 50 Ω
- We cool down the amplifier to 4 K. Assuming the noise scale with T:
  - $V_{in,rms} = (4\ kT\ R_S\ BW)^{0.5}$

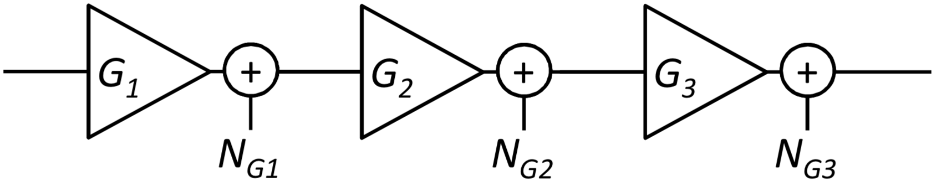
    $= 0.1\ nV_{rms}$

    @ 4 K, BW = 1 Hz
  - NF = 0.06 dB, T_e= 4 K, R_e = 0.7 Ω



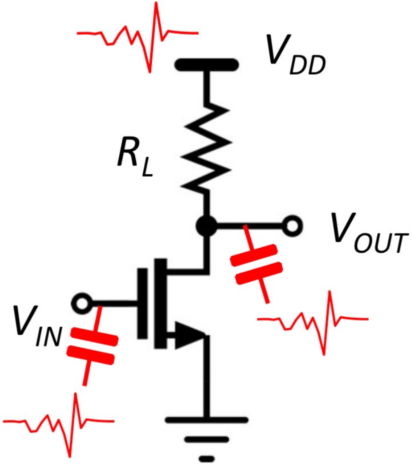
[http://www.rfcafe.com/references/calculators/noise-figure-temperature-calculator.htm]

Cascading Amplifiers



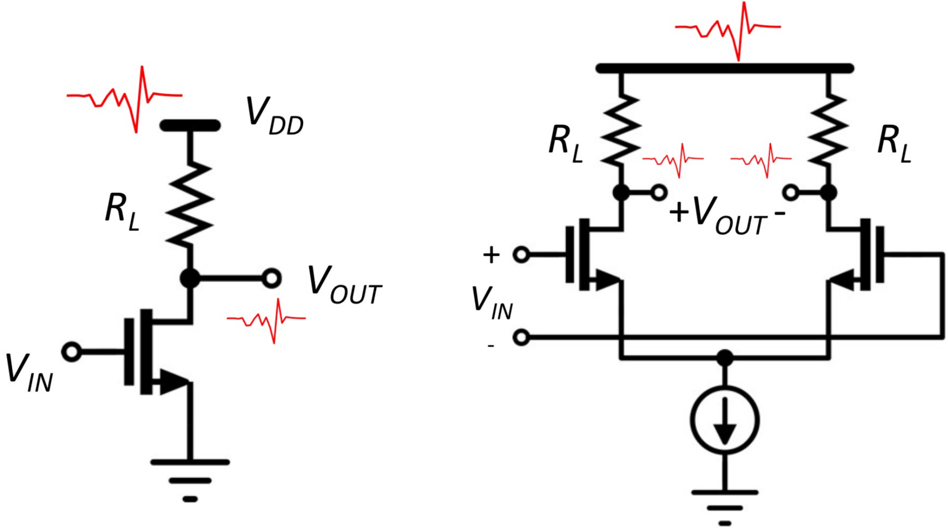
- Input-referred noise
  - $V_{noise,in} = \frac{N_{G1}}{G_1} + \frac{N_{G2}}{G_1 G_2} + \frac{N_{G3}}{G_1 G_2 G\_3} + \cdots$
- Noise Figure
  - $NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1} + \cdots$
  - "Friis" formula
  - Note: G_i is the available power gain

Immunity to External Interference



- Interference coupling through signal lines
  - Inductive coupling
  - Capacitive coupling
- Interference coupling through supplies

Immunity to External Interference (2)

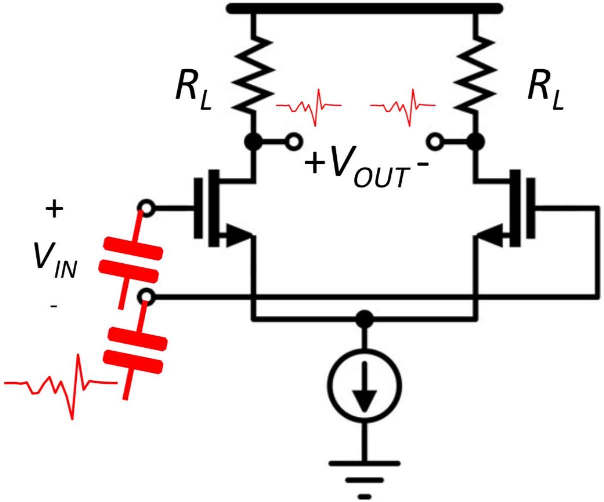


- Differential structure cancels supply noise (when perfect matching)
- Power Supply Rejection Ratio (PSRR) = 20 $\log_{10}(V_{noise,out}/V_{noise,supply})$

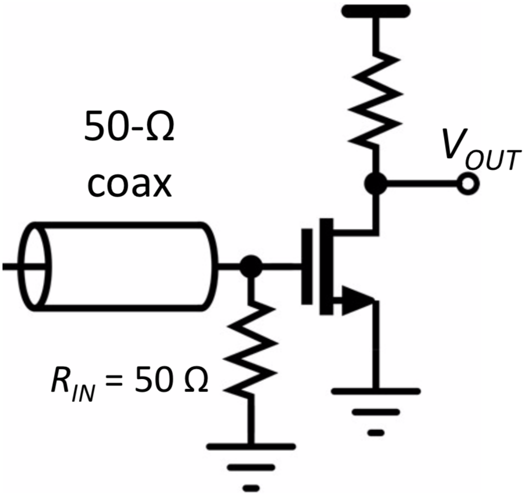
Immunity to External Interference (3)

- Differential structure cancels common-mode noise
  - (when perfect matching)
- Common-Mode Rejection Ratio

  $CMRR = V_{noise,out}/V_{noise,CM}$
- Always try to route signals differentially
  - Ex. Twisted pairs

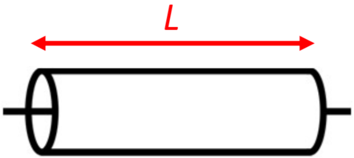


Impedance Matching



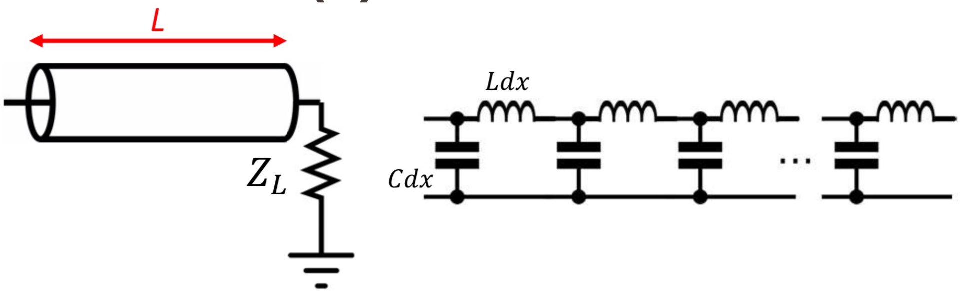
- Coaxial lines to propagate high frequency signals
  - Controlled impedance
  - Typically R_0=50 Ω
- If no input matching $R_{IN} \neq 50\ \Omega$
  - Previous stage output load depends on line length
  - Previous stage load is different than expected ⇒ malfunctioning
  - Multiple reflections ⇒ signal distortion
- Similar requirements for output impedance

Coaxial Cables



- Signal propagation time is finite
  - $v = \frac{c}{\sqrt{\epsilon_r \mu_r}}$
  - L = 1 m ⇒ typically $\Delta t = 4$ ns
- Propagation effect can be ignored if $L < \frac{\lambda}{10}$
  - L = 1 m ⇒ $\lambda = \frac{v}{f} > 0.1$ m ⇒ f < 2.25 GHz
- **Propagation effects are important at high frequency**

Coaxial Cables (2)



- Modelled as sequence of distributed LC filters
- Electrical waves can propagate in both direction
- **Characteristic impedance:** $Z_0 = \sqrt{L/C}$, typ. 50 Ω or 75 Ω
- Standing waves can form due to reflections
  - Destructive interference with reflected wave
  - If unlucky, no voltage at the receiving end
- **Reflection coefficient:** $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$

Impedance Matching

- Input matching measured by S_{11}

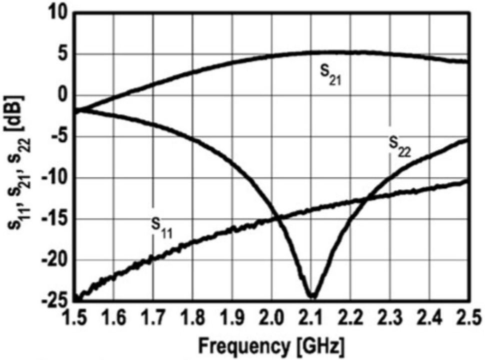
$$S_{11} = \frac{Z_{in} - R_0}{Z_{in} + R_0}$$

- Output matching measured by S_{22}

$$S_{22} = \frac{Z_{out} - R_0}{Z_{out} + R_0}$$

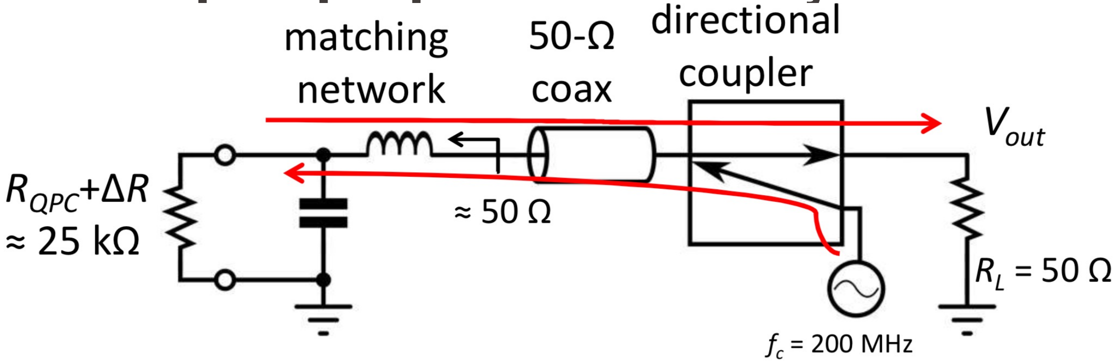
- Typical requirement

  $S_{11}, S_{22} < -10$ dB



[Jussila 2008]

Example: Spin qubit Reflectometry

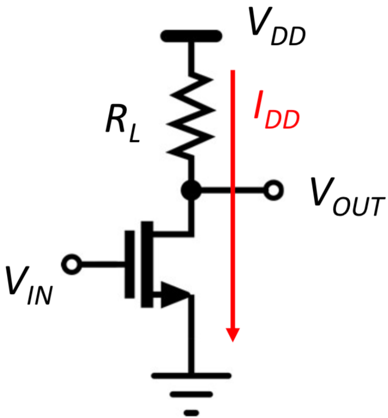


- Reflection of power also follows the same equation:

$$S_{11} = \frac{Z_{in} - R_0}{Z_{in} + R_0}$$

- Matching network adapt impedance from R_{QPC} to 50 Ω
- $\Delta R = 0 \Rightarrow$ impedance matching $\Rightarrow$ no reflected power

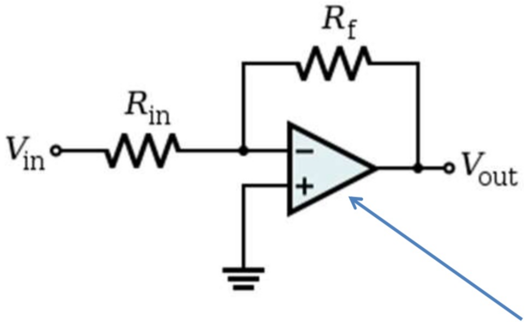
Power



- $P = V_{DD} \cdot I_{DD}$
- Typical trade-offs:
  - Gain: $G = -gm \cdot R_L \propto I_{DD}$
  - Noise: $v_{in,rms} \propto 1/I_{DD}$
  - Linearity

- For cryo electronics, power dissipated by cooling
- **Limiting factor for large scale quantum computers**

Feedback Amplifier (Inverting OpAmp)

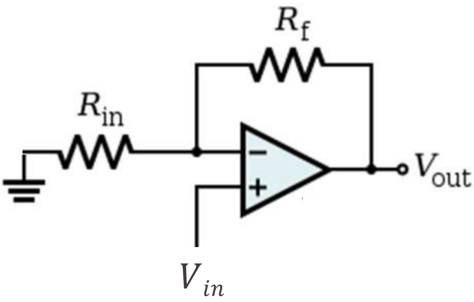


$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

Opamp = amplifier with very large DC gain and low output impedance

- Use feedback to improve
  - Well-controlled gain
  - High linearity
- But limited bandwidth

Feedback Amplifier (Non-inverting OpAmp)



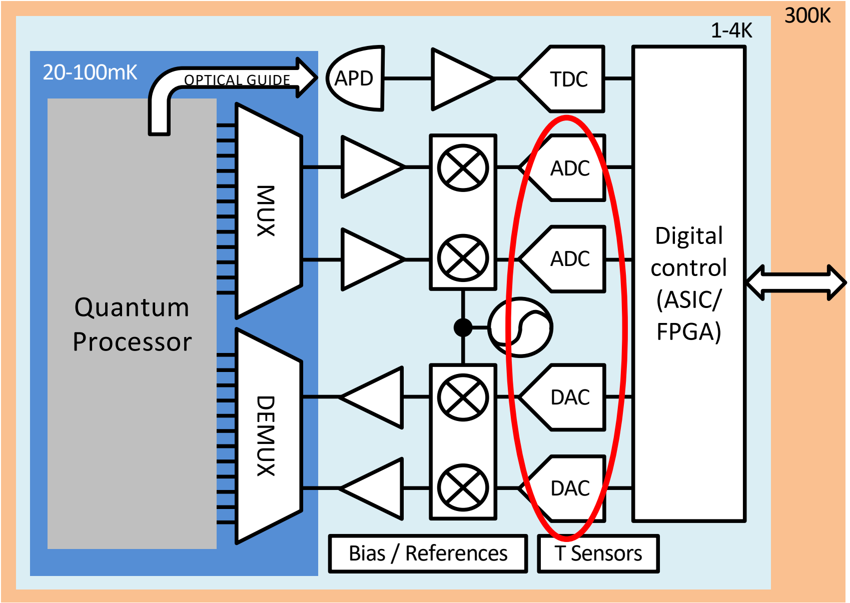
$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_{in}}$$

<u>Special case</u>: $R_{in} \to \infty\ (open\ circuit) and\ R_f \to 0$ (short), then gain = 1 (buffer)

Analog-to-Digital Converters (ADCs)
Digital-to-Analog Converters (DACs)

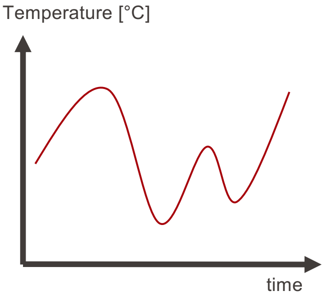
Analog-to-Digital Converters (ADCs)
Part I

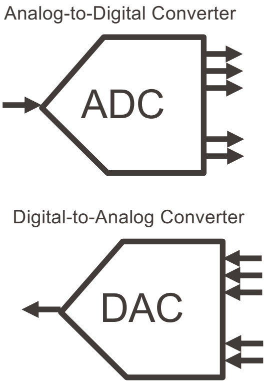
Cryo-CMOS Quantum-Classical Interface

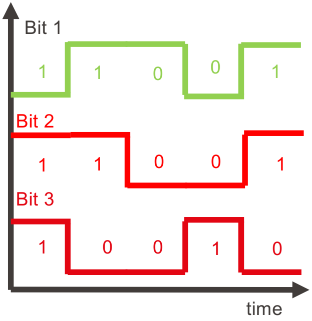


Analog vs. Digital

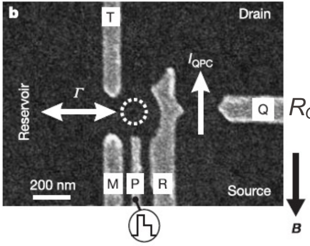
- The world is analog
  - Temperature, humidity, speed, light,… are analog!
- Computing is digital



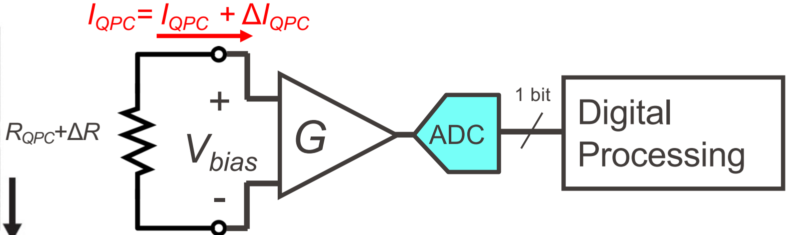




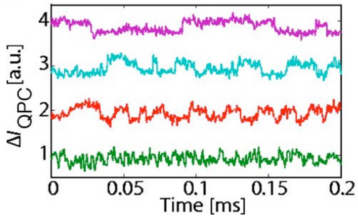
ADC Example: Spin-qubit Readout



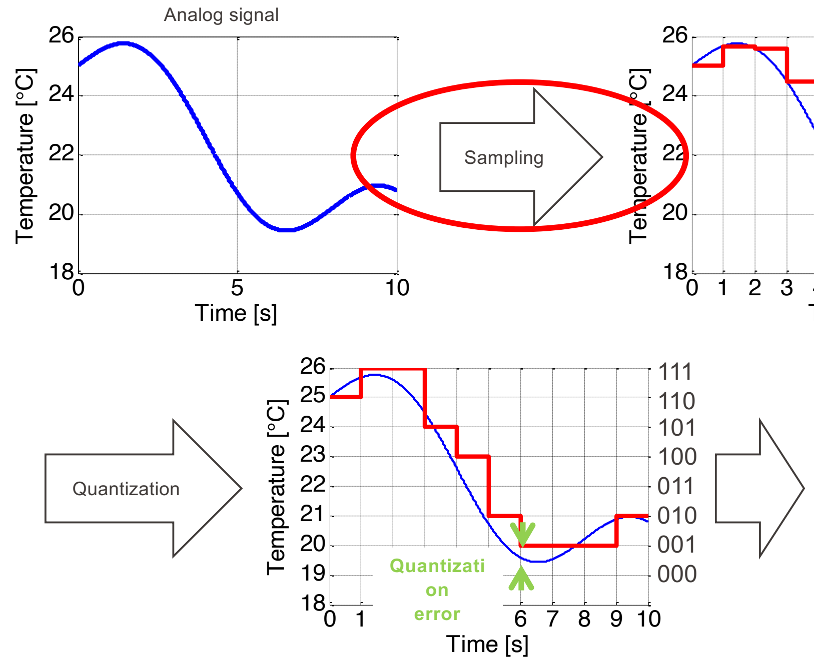
Source: I.T. Vink



- Decide if qubit is $|0\rangle$ or $1\rangle$
- **Need for 1-bit ADC**



Sampling and Quantization

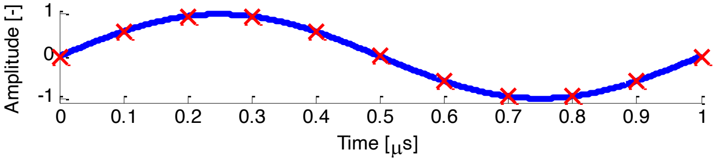


Digital signal

110, 111, 111, 101, 100, 010, 001, 001, 001, 010

3-bit ADC

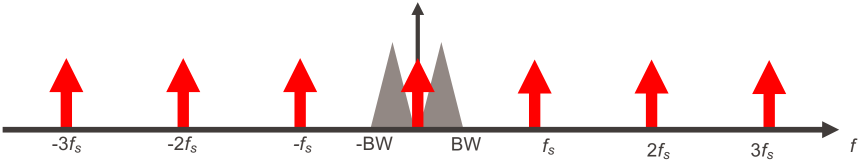
Sampling



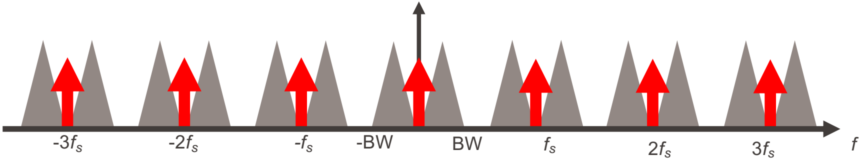
f_{in} = 1 MHz
f_s = 10 MHz

Sampling (BW < f_s/2)

Spectrum before sampling

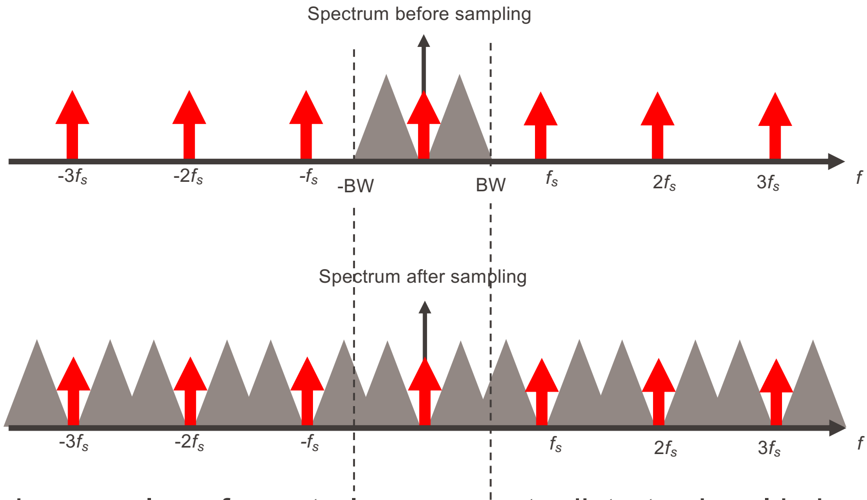


Spectrum after sampling



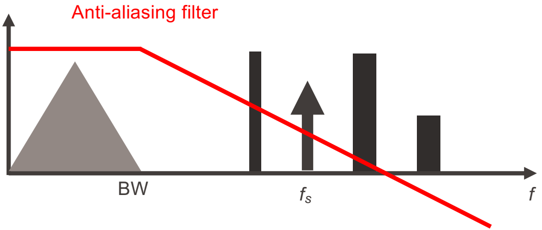
- Replica of the signal around harmonics of sampling frequency (f_s)

Sampling (BW > $f_s/2$)



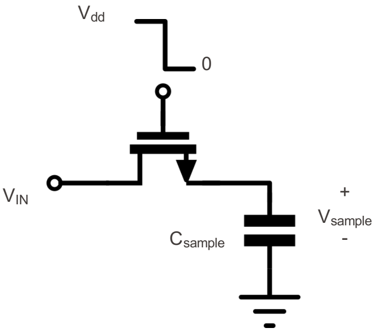
- Aliasing: overlap of spectral components distorts signal in baseband

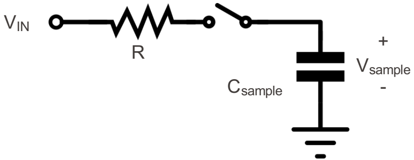
Nyquist Frequency



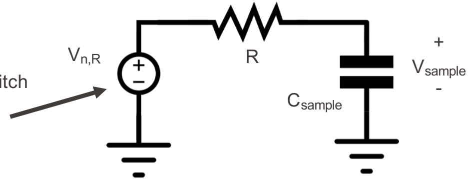
- Nyquist frequency: $f_s = 2 \cdot BW$
- Anti-aliasing filter attenuates high frequency (> $f_s/2$) components before sampling
- Beware! Also noise (always present) folds back into baseband.

Sampling Limitations – Noise

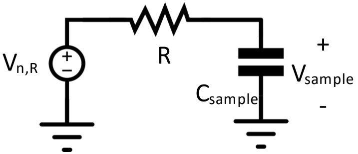


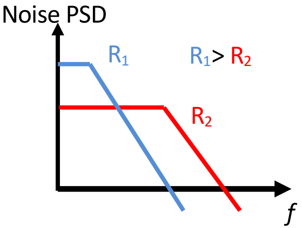


Thermal noise due to switch resistance R (4 *kTR*)



Sampling Limitations – Noise (kT/C)





$$\langle V_{sample}^2 \rangle = \int_0^{+\infty} S_{Vn,R}(f)|H(f)|^2 df = \frac{kT}{C}$$

- Lower noise ⇒ Larger cap
- Larger cap ⇒ less BW or more power
  - BW ~ gm/C and gm ~ I

C_{sample}	Noise (rms)	SNR (V_{IN}=1 V_{pp})	ENOB [see slide 31]
1 pF	64 µV	78 dB	12.6 bit
10 pF	20 µV	88 dB	14.3 bit
100 pF	6 µV	98 dB	16 bit

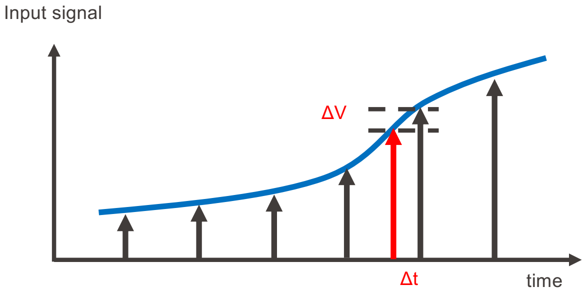
Derivation:

$$H(f) = \frac{1}{1 + j2\pi RCf}$$
$$S_{Vn,R}(f) = 4kTR$$

⇨

$$\int_0^{+\infty} S_{Vn,R}(f)|H(f)|^2 df = \int_0^{+\infty} \frac{4kTR}{1 + (2\pi RCf)^2} df$$
$$= \int_0^{+\infty} \frac{4kTR}{1 + (2\pi RCf)^2} df = \frac{4kTR}{2\pi RC} \int_0^{+\infty} \frac{1}{1 + x^2} dx$$
$$= \frac{2kT}{\pi C} \lim_{x \to +\infty} \operatorname{atan} x = \frac{kT}{C}$$

Sampling Limitations – Jitter



$$\Delta V \cong \Delta t \frac{dV}{dt}$$

- For a sine input:

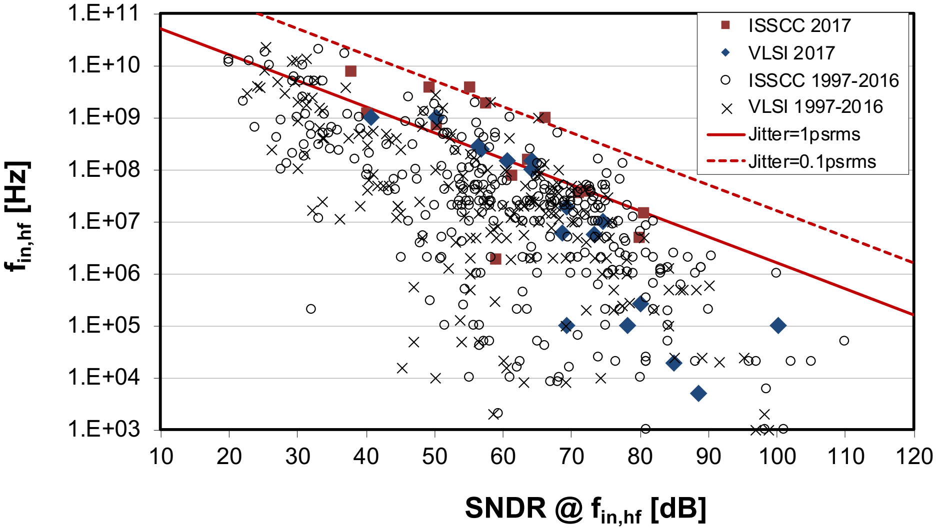
$$V = A \sin \omega t$$
$$\Delta V = \Delta t \ \omega \cos \omega t$$

- Integrating over a full sine period:

$$\sigma_V^2 = \frac{A^2}{\sqrt{2}} \sigma_t^2 \omega^2 \Rightarrow \text{SNR} = \frac{1}{\sigma_t^2 \omega^2}$$

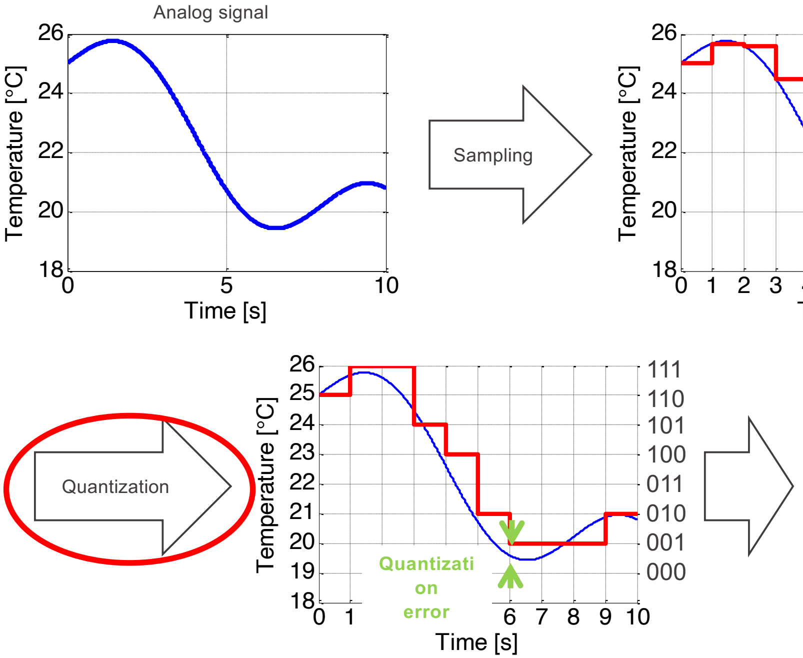
Jitter

Sampling Limitation – Jitter



B. Murmann, "ADC Performance Survey 1997-2017"

Sampling and Quantization

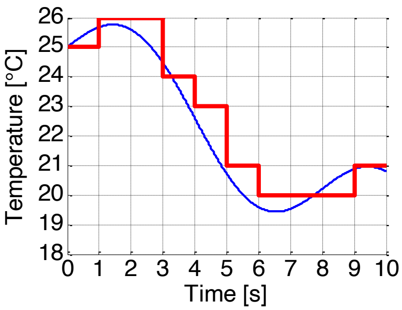


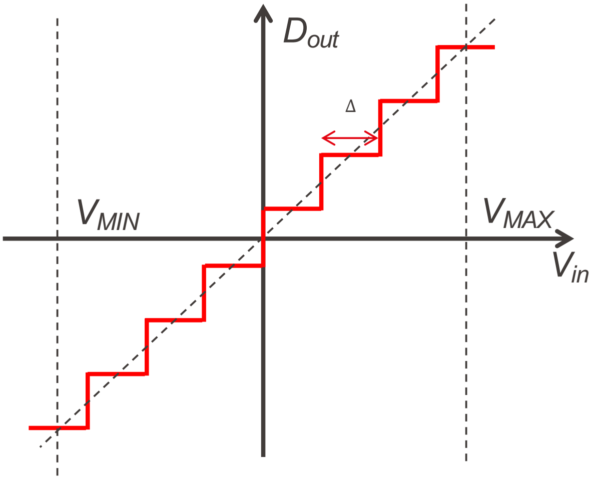
Digital signal

110, 111, 111, 101, 100, 010, 001, 001, 001, 010

3-bit ADC

Quantization





$$\Delta = \frac{V_{MAX} - V_{MIN}}{2^N - 1}$$

- Δ = quantization step, LSB (least significant bit)
- *N* = *number* of bits of the ADC

Quantization – Signal Spectrum

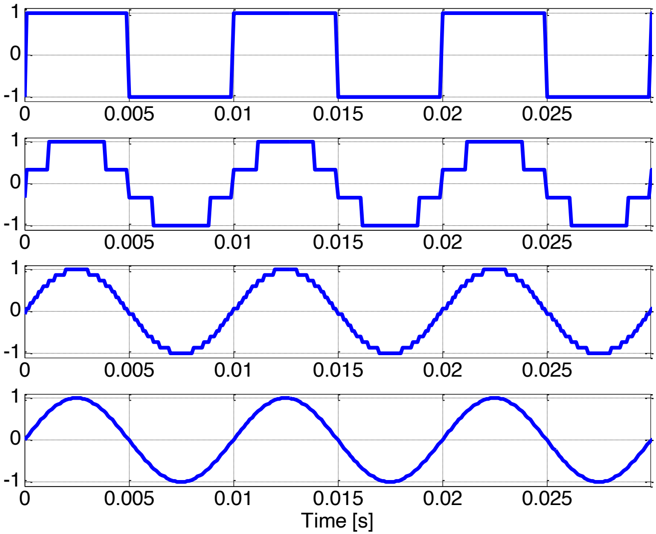
Quantizing a sinusoid at 10 kHz

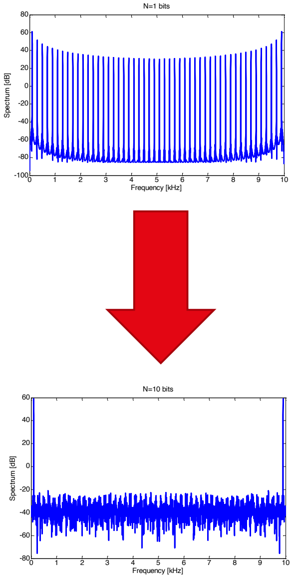
N = 1 bit

N = 2 bit

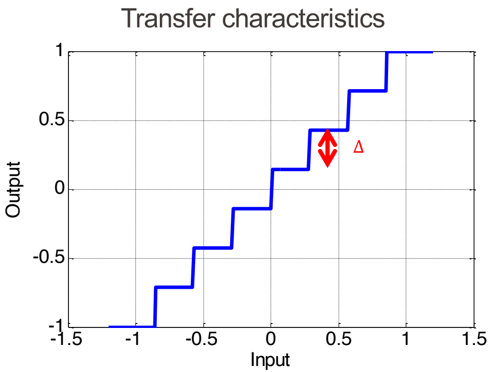
N = 4 bit

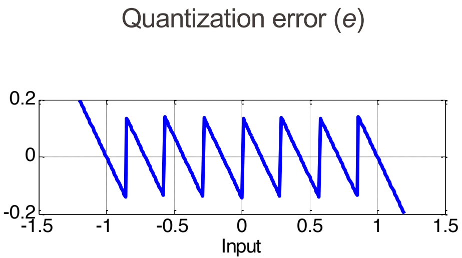
N = 8 bit





Quantization Noise





Variance of the quantization error (assuming uniform distribution):

$$P_q = \int_{-\Delta/2}^{\Delta/2} e^2 P(e)de = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} de = \frac{1}{\Delta}\frac{e^3}{3}\bigg|_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} = \frac{\Delta^2}{12}$$

Signal-to-Noise Ratio (SNR)

- For a full-scale sinusoid: $P_S = \frac{\left(\Delta 2^{N-1}\right)^2}{2}$

- Since $P_q = \frac{\Delta^2}{12}$, $\quad SNR = \frac{P_S}{P_q} = 1.5 \cdot 2^{2N}$

- In dB:

$$SNR_{dB} = 10\log_{10}\frac{P_S}{P_q} = 6.02 \cdot N + 1.76$$

$$N = \frac{SNR_{dB} - 1.76}{6.02}$$

Effective Number of Bits (ENOB)

- **Consider**
  - **Real ADC (noise, quantization noise, distortion) with given *SNDR***
  - **Ideal ADC (only quantization noise) with same *SNDR***
- **The number of bits of the ideal ADC is**

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02}$$

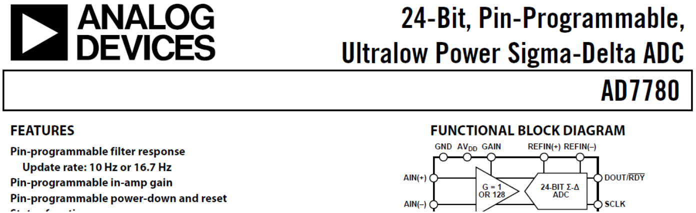
Recall for q-noise:

$$SNR = 1.5 \cdot 2^{2N}$$

$$SNR_{dB} = 6.02 \cdot N + 1.76$$

- Often *ENOB* ≠ number of (*marketing*) bits

Example:


ANALOG DEVICES

24-Bit, Pin-Programmable, Ultralow Power Sigma-Delta ADC

AD7780

FEATURES

Pin-programmable filter response

Update rate: 10 Hz or 16.7 Hz

Pin-programmable in-amp gain

Pin-programmable power-down and reset

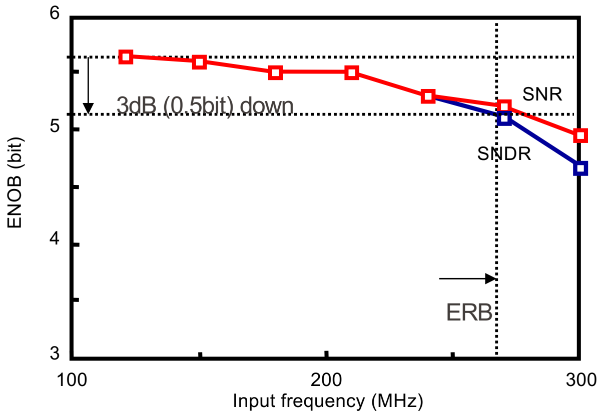
FUNCTIONAL BLOCK DIAGRAM

But:

- SNR = 130 dB
- INL > 6 bits

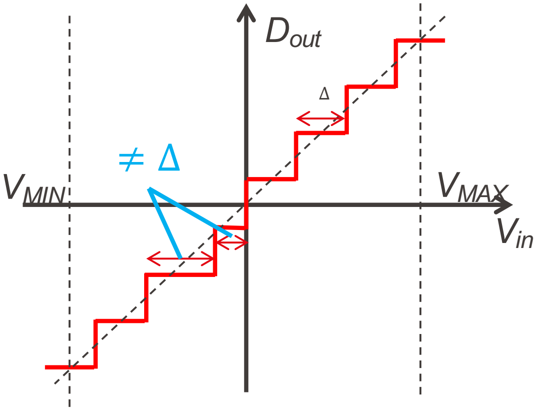
⇒ ENOB < 21 bits

Effective Resolution Bandwidth (ERB)



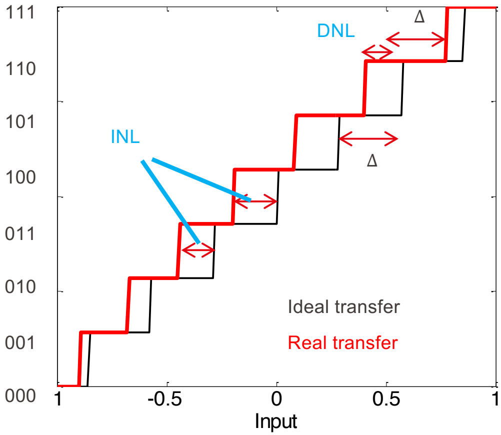
- SNDR changes with input frequency
- ERB is the bandwidth at which SNDR drops by 3 dB (0.5 bits)
- Note: we are observing variations of the input frequency, not of the sample frequency

Quantization Limitations – Matching



- Mismatch causes errors in the input/output transfer

Effect on ADC: INL, DNL

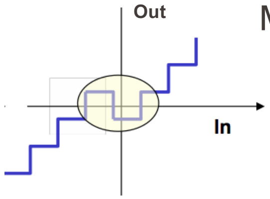


Differential non-linearity (DNL)

$$DNL[i] = INL[i] - INL[i-1]$$

Integral non-linearity (INL)

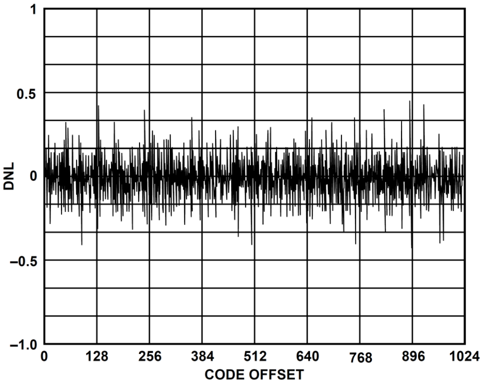
$$INL[i] = \sum_{1}^{i} DNL[j]$$



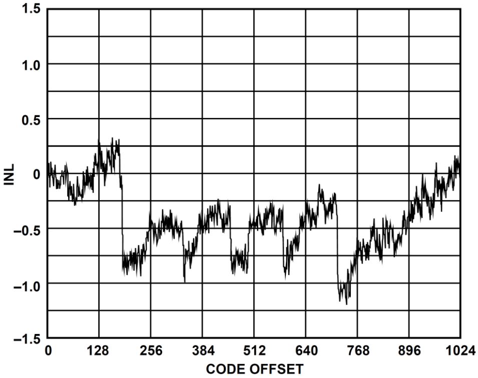
Monotonicity

Effect on ADC: INL, DNL (2)

DNL

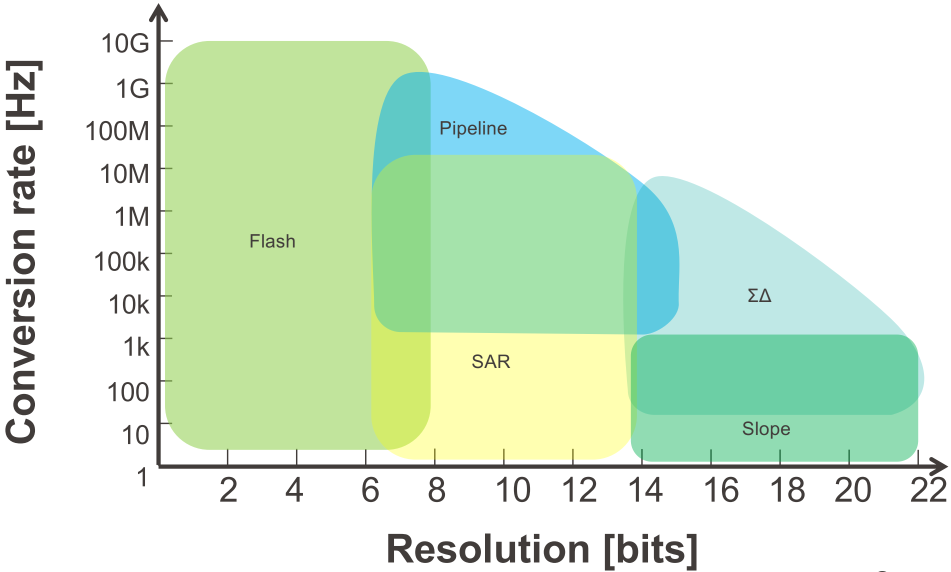


INL



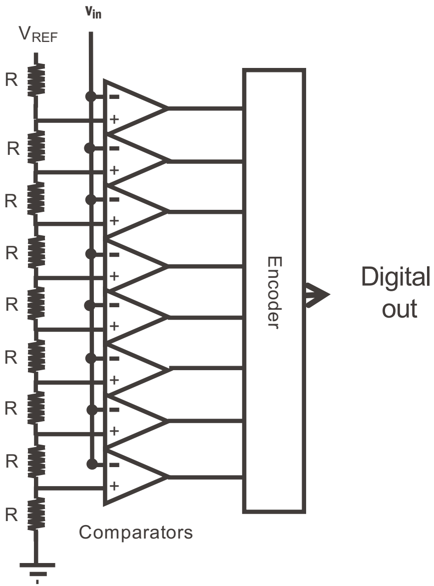
[Datasheet: AD9201]

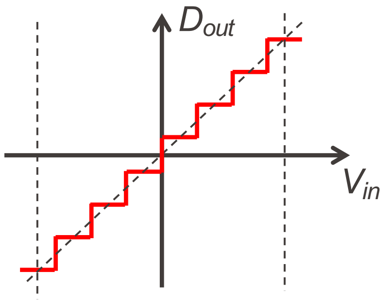
ADC Architectures



Source: Pelgrom 2006

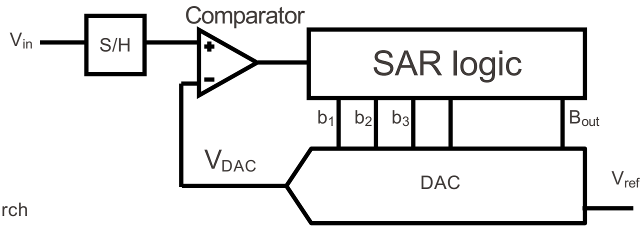
Flash ADC

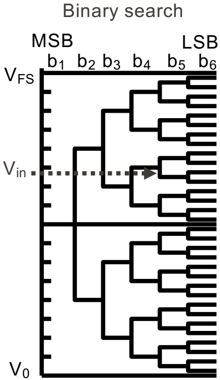


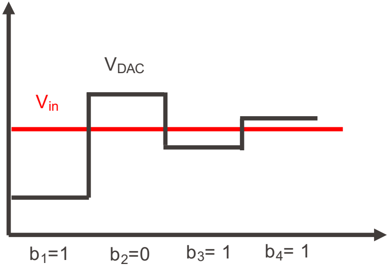


__Features:__
Low resolution (<8 bits)
High power
Ultra-high speed
Large input capacitance

Successive-approximation ADC (SAR)







Features:

Moderate resolution

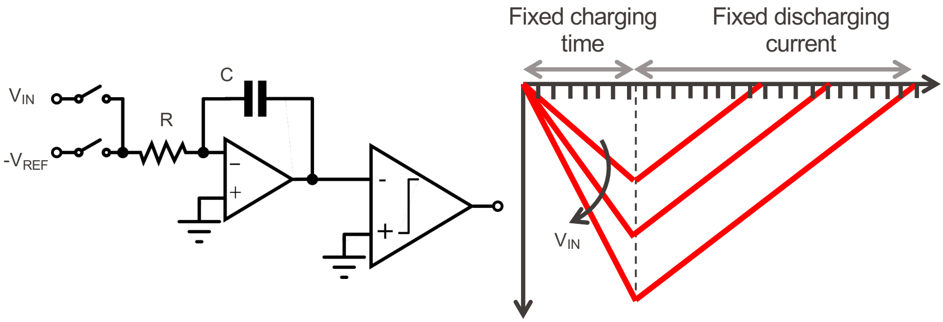
Low power

Relatively low speed

Easy calibration

Needs multi-clock

Dual-slope ADC



Features:

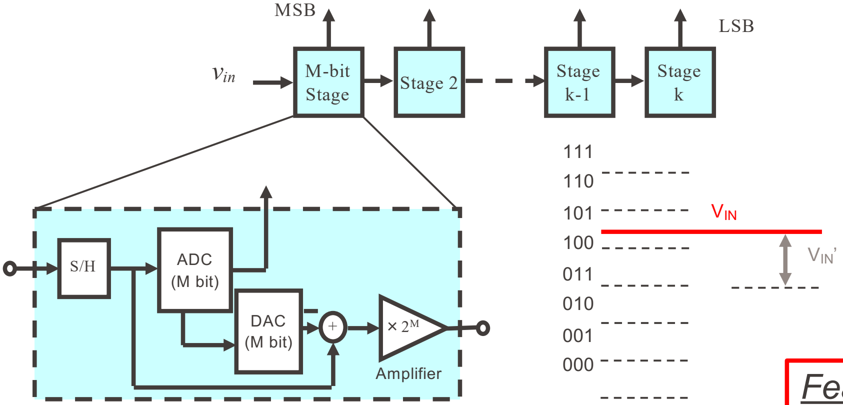
High resolution (<20b)

Low speed

Small DNL

Small area/power

Pipelined ADC

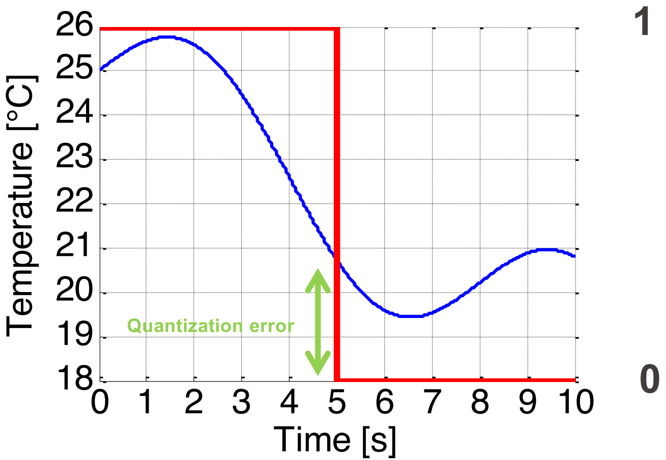


Conventional M is 1 or 1.5

- Cascaded stages contribute less noise
- Scaling of the stage

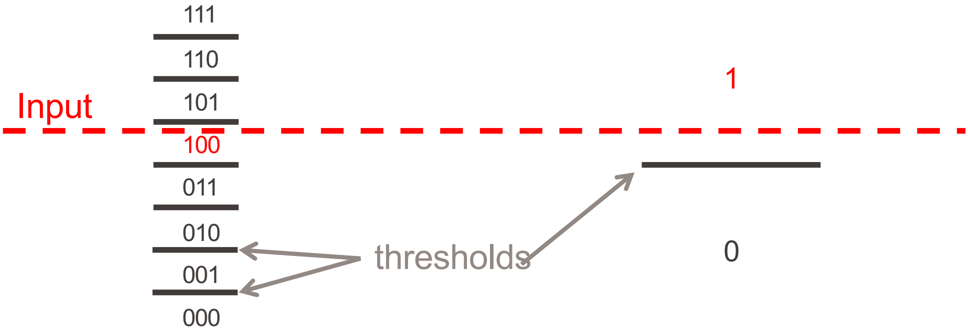
Features:
High resolution
Low power
Moderate speed

A 1-bit ADC?

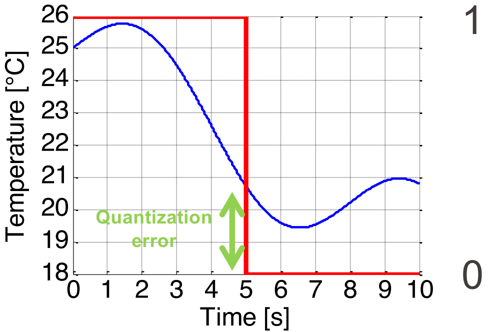

26
25
24
23
22
21
20
19
18
Temperature [°C]
0 1 2 3 4 5 6 7 8 9 10
Time [s]
Quantization error
1
0

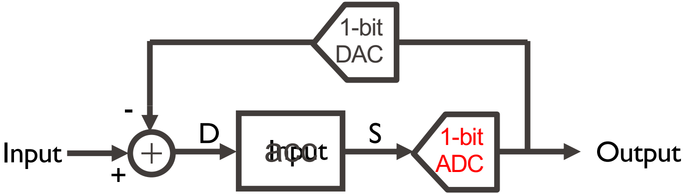
Why 1-bit ADC?

- Multi-bit ADCs
  - Many thresholds
  - Many comparisons
  - Prone to errors
  - Complex circuit
- 1-bit ADCs
  - One threshold
  - One comparison
  - Robust
  - Simple circuit

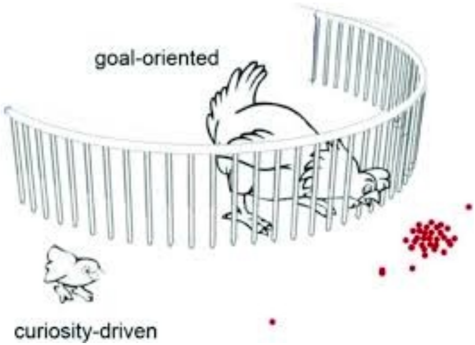


Basic Idea of a Sigma-Delta ADC





Thank you



T. Haensch