



MICRO-435
Quantum and
Nanocomputing

Edoardo Charbon
Mariagrazia Graziano

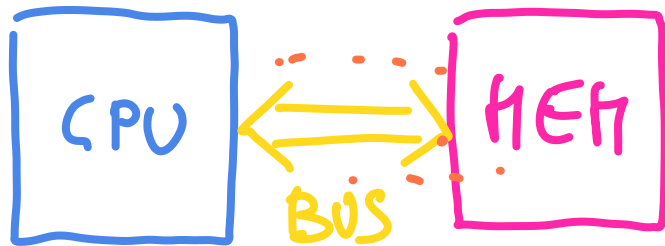
LOGIC - IN - MEMORY

MAGNETIC IMPLEMENTATION : FCN & BEYOND

OBJECTIVES

- 1) LOGIC - IN - MEMORY : GENERAL VIEW
- 2) IN PLANE NANO MAGNETIC LOGIC
→ MAGN-FCN

LIMIT OF VON-NEUMANN ARCHITECTURES



- FETCH (FROM INSTR. MEMORY)
- DECODE
- EXECUTE
 - GET DATA FROM DATA M. ←
 - EXEC. IN CPU ←
 - STORE DATA IN DATA M. ←

BUS & MEM

→ SLOW

→ POWER CONSUMING

W.R.T. CPU



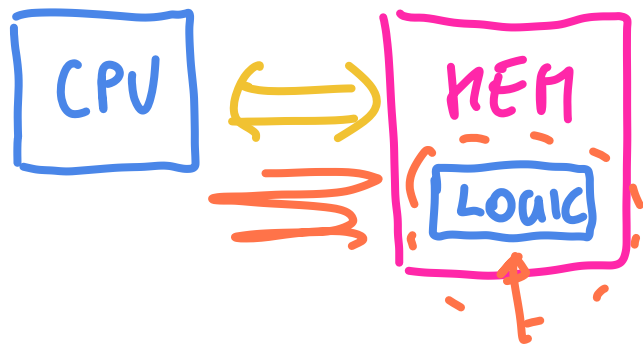
→ MEMORY BOTTLENECK
DAR K MEMORY

SOLUTIONS → MEMORY HIERARCHY (MULTIPLE LEVEL CACHING)

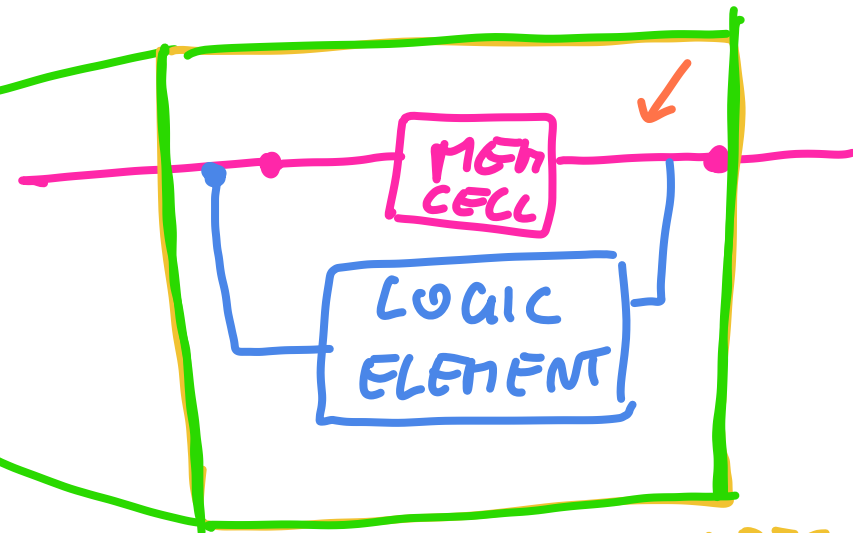
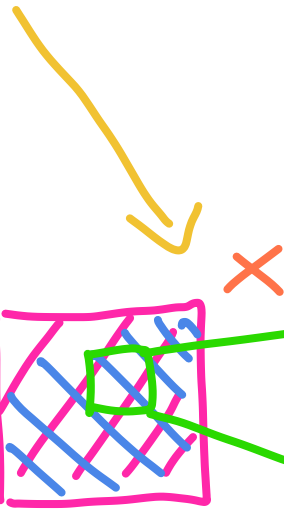
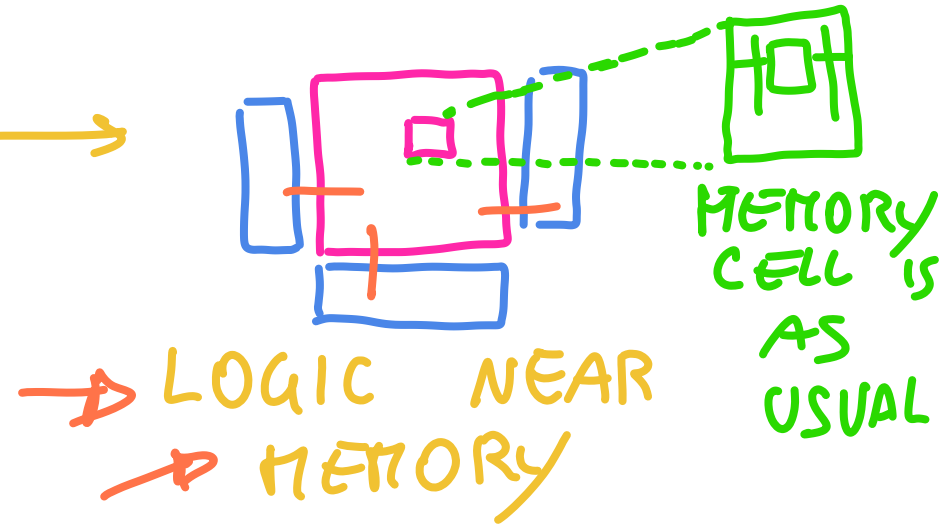
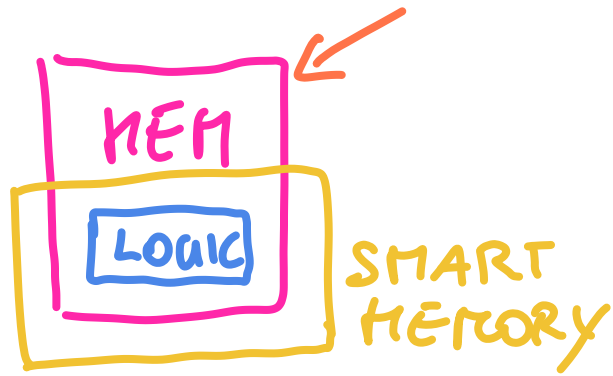
→ LOGIC-IN-MEMORY

in memory computing

processing in memory

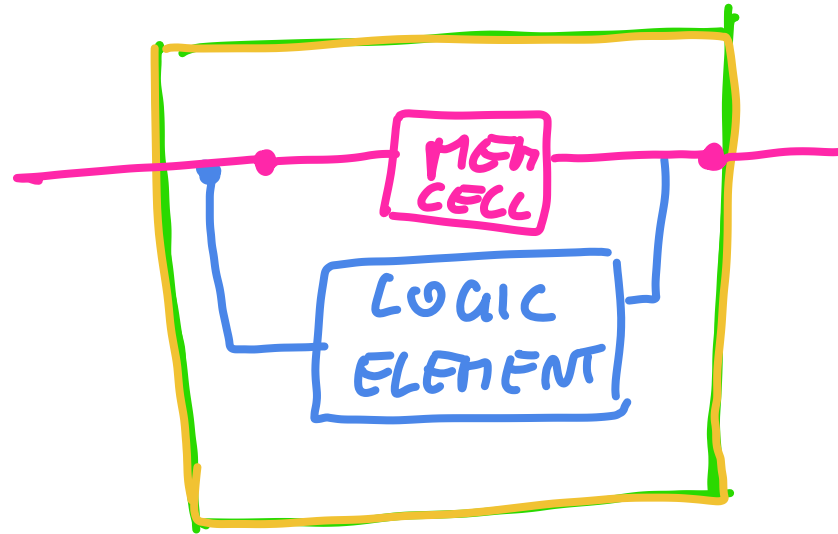


← PART OF THE PROCESSING EXECUTED IN PART OF A "SMART-MEMORY"



EACH CELL INCLUDES

- STORAGE ←
- LOGIC ←



IMPLEMENTED
USING STANDARD
TECHNOLOGY

- FEASIBLE
- NOT EFFICIENT

→ IMPLEMENTED
USING NEW
TECHNOLOGIES

- MANY UNDER
→ PRE-INDUSTRIAL STUDY
- SEVERAL AT RESEARCH
→ LEVEL

NEW TECHNOLOGIES :

- CAN BE USED FOR MEMORY ONLY
- CAN DEVELOP LOGIC AS WELL

- RERAM

- PC-RAM

- STT-RAM

- FEFET-RAM

- M-RAM

BORN AS MEMORIES



MODIFIED TO LOGIC & MEM.

I-NML

P-NML

RACETRACK

SKYRION

(SPW WAVES)

CAN BE USED AS

LOGIC WITH

INTRINSIC MEMORY

CAPABILITIES

SPINTRONICS

MAGNETIC DEVICES FOR LOGIC,
INTERCONNECT, MEMORIES,
SENSORS



MAGNETIC FCN

↳ I-NML

↳ P-NML

DOMAIN WALLS



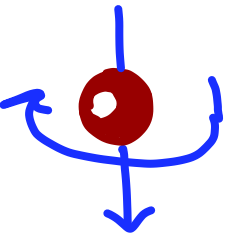
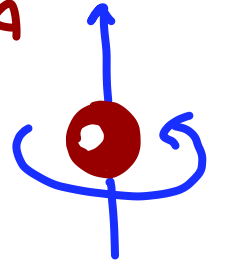
RACETRACK LOGIC & NEH

SKYRMIONS

→ NEH &
→ LOGIC

ELECTRONS HAVE A
NATURAL ROTATION

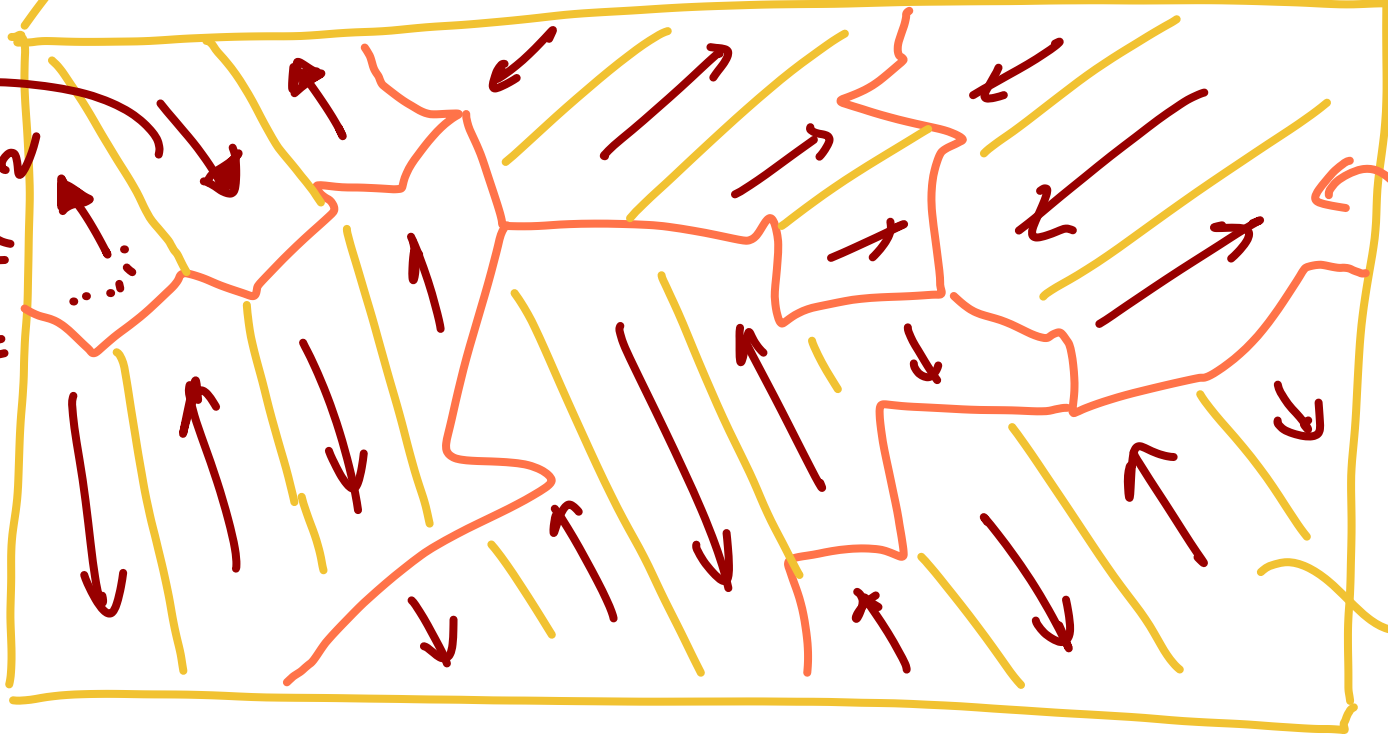
→ INTRINSIC ANGULAR
MOMENTUM
SPIN



MAGNETIC
MATERIAL



MAGNETIZATION
RESULT OF
SPIN OF
ALL
ATOMS
IN
DOMAIN



GRAINS

DOMAINS

DEFINITIONS

MAGNETIZATION

TOTAL MAGNETIC MOMENT PER UNIT VOLUME OF A MATERIAL

RESULT OF THE INTERACTION OF SPINS OF ALL ATOMS

MAGNETIC PERMEABILITY

RATIO B/W. MAGNETIZATION & APPLIED MAGNETIC FIELD

DEFINES HOW EASY THE MAGNETIC FLUX CAN INFLUENCE THE MATERIAL

MAGNETIC ANISOTROPY

TENDS TO BLOCK ATOMS SPIN ORGANIZATION
IN A SPECIFIC MAGNETIC MOMENT
(magnetization memory)

DIFFERENT DEVICES CAN HAVE
ONE OR MORE OF THEM

- MAGNETO CRISTALLINE ANISOTROPY

DEPENDS ON CRISTAL TYPE

TYPICALLY
ORIENTATION
ALONG THE
↑ LONGEST SIDE

- SHAPE ANISOTROPY

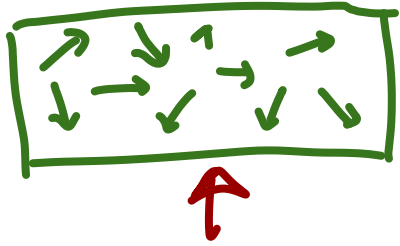
DEPENDS ON SHAPE & GEOMETRY

MAGNETIZATION ALIGN TO MINIMIZE ENERGY

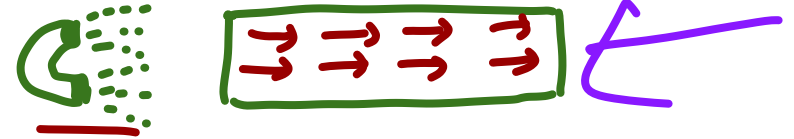
MAGNETOSTATIC

- STRESS ANISOTROPY

APPLY A MECHANICAL STRESS → CHANGES THE
LACTICE STRUCTURE → ORIENTATION OF M
CHANGES



• IF APPLY MAGNETIC FIELD



↳ ALL M. OF GRAINS ASSUME SAME DIRECTION
→ UNIFORM MAGNETIZATION

• WHEN RELEASED

↳ DIFFERENT SITUATION DEPENDS ON MAT:

• DIAMAGNETISM

• PARAMAGNETISM

• FERROMAGNETISM

• ANTIFERROMAGNETISM

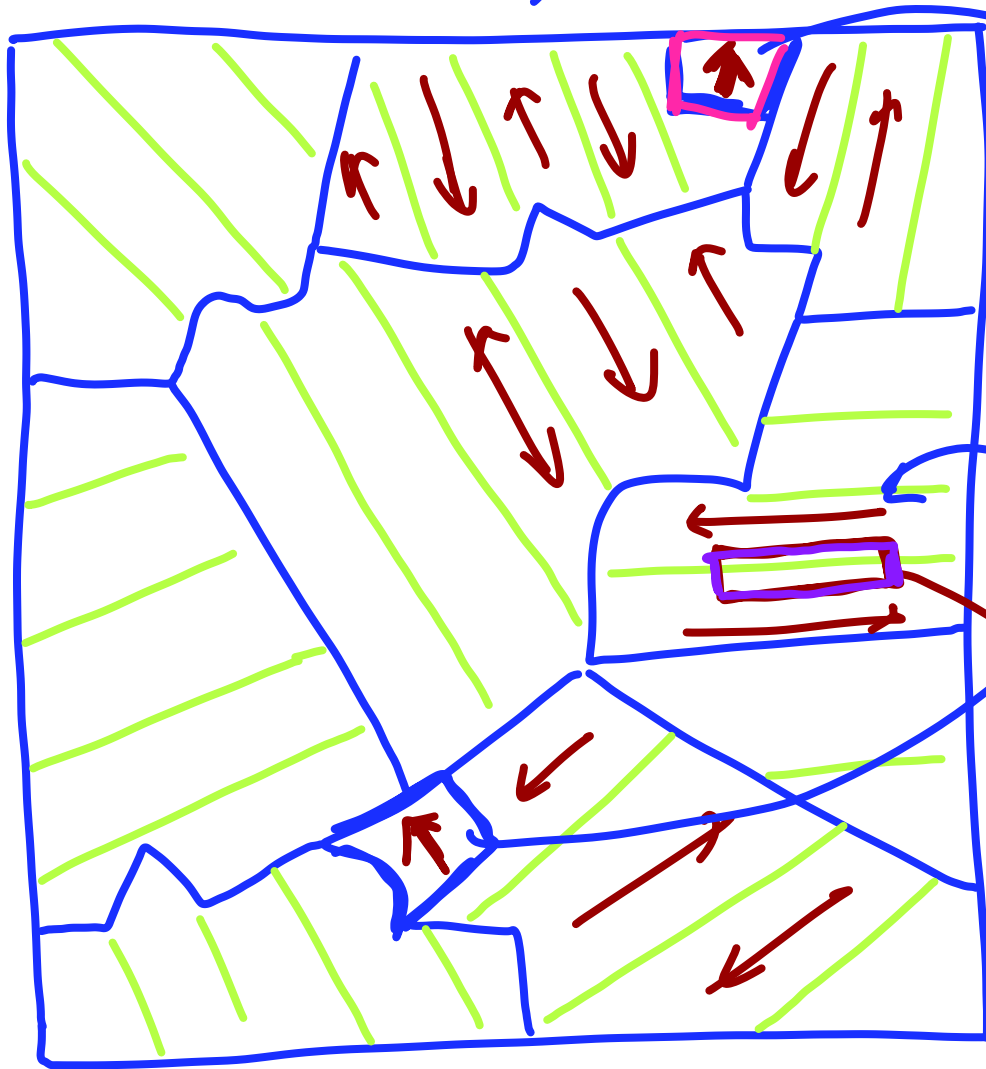
• FERRIMAGNETISM

Ⓜ

SELF SUSTAINED

SUSTAINED ALIGNMENT
OF A MAGNETIC MOMENT
ALL IN SAME DIRECTION
EVEN AFTER RELEASING
M.F.

IN A CRYSTAL



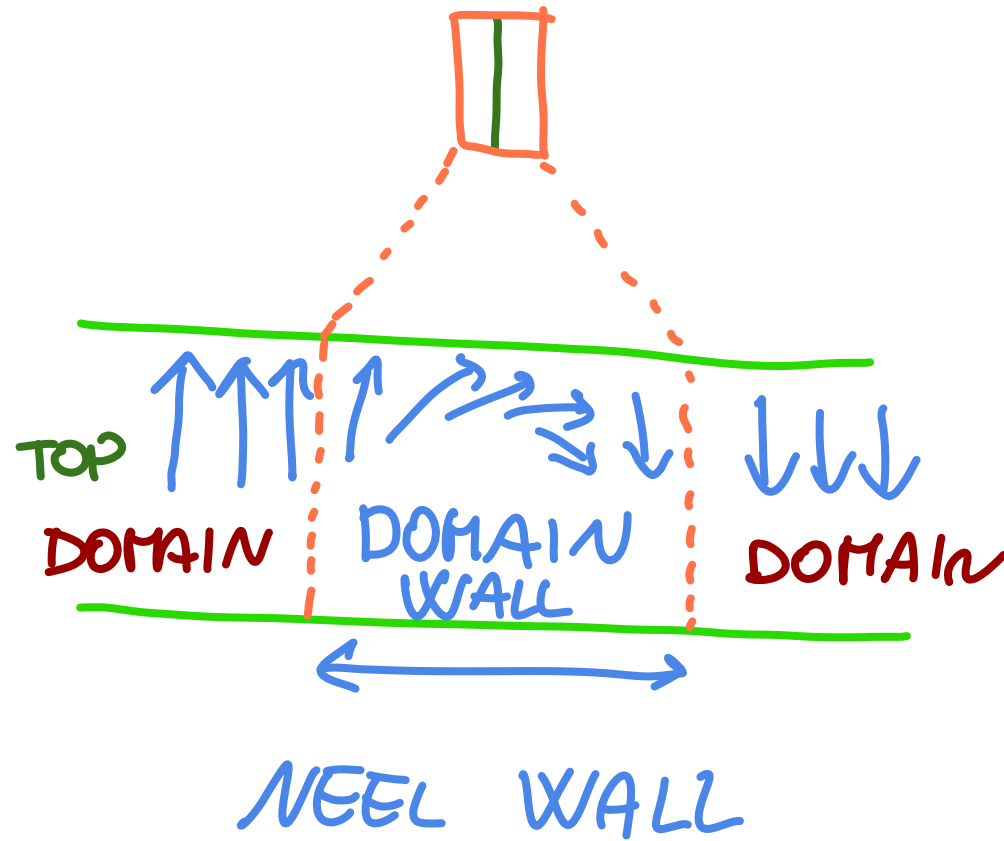
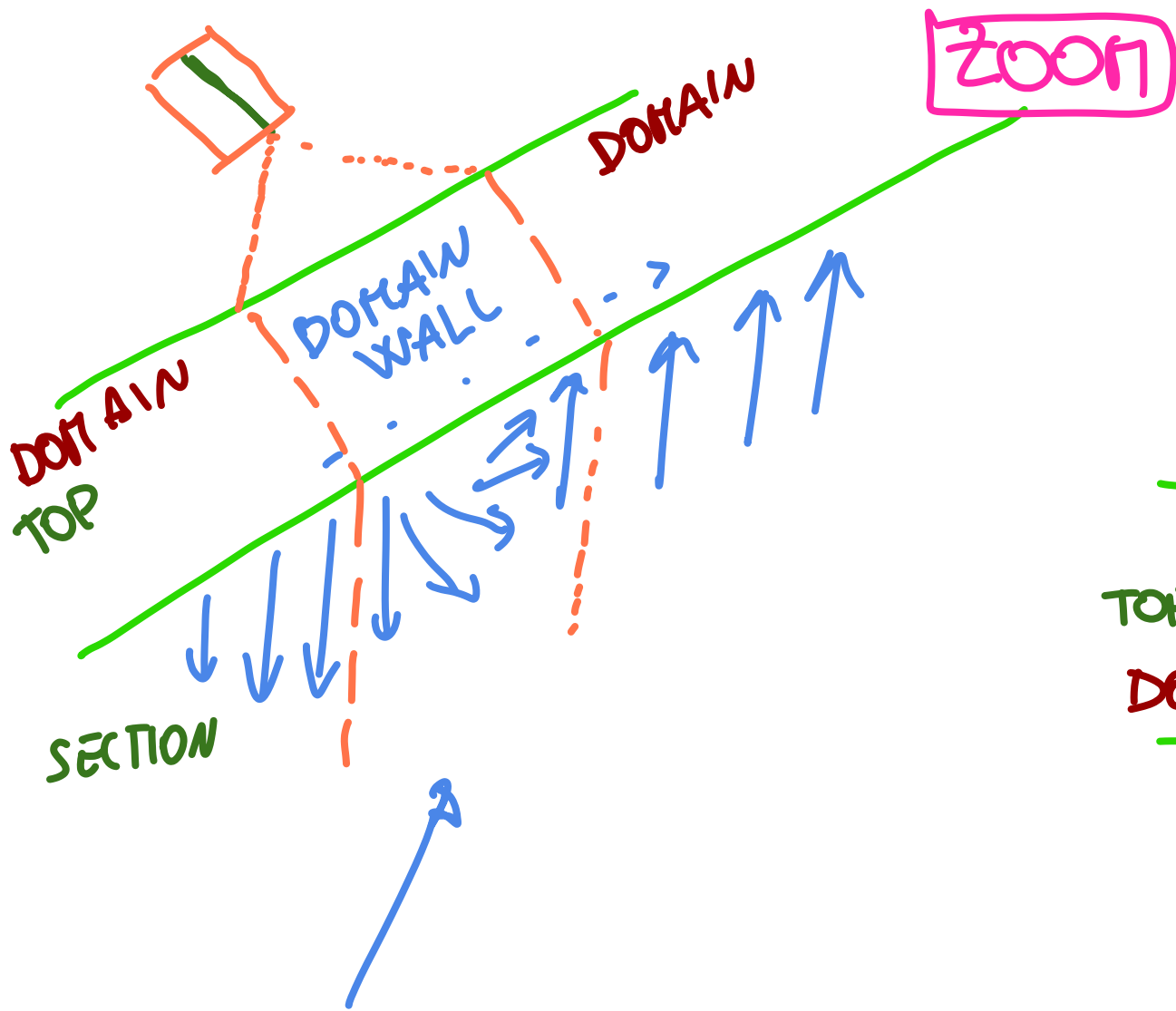
SINGLE DOMAINS

DIFFERENT
USES

MULTIDOMAIN

WHAT IN BETWEEN
DOMAINS?

2007

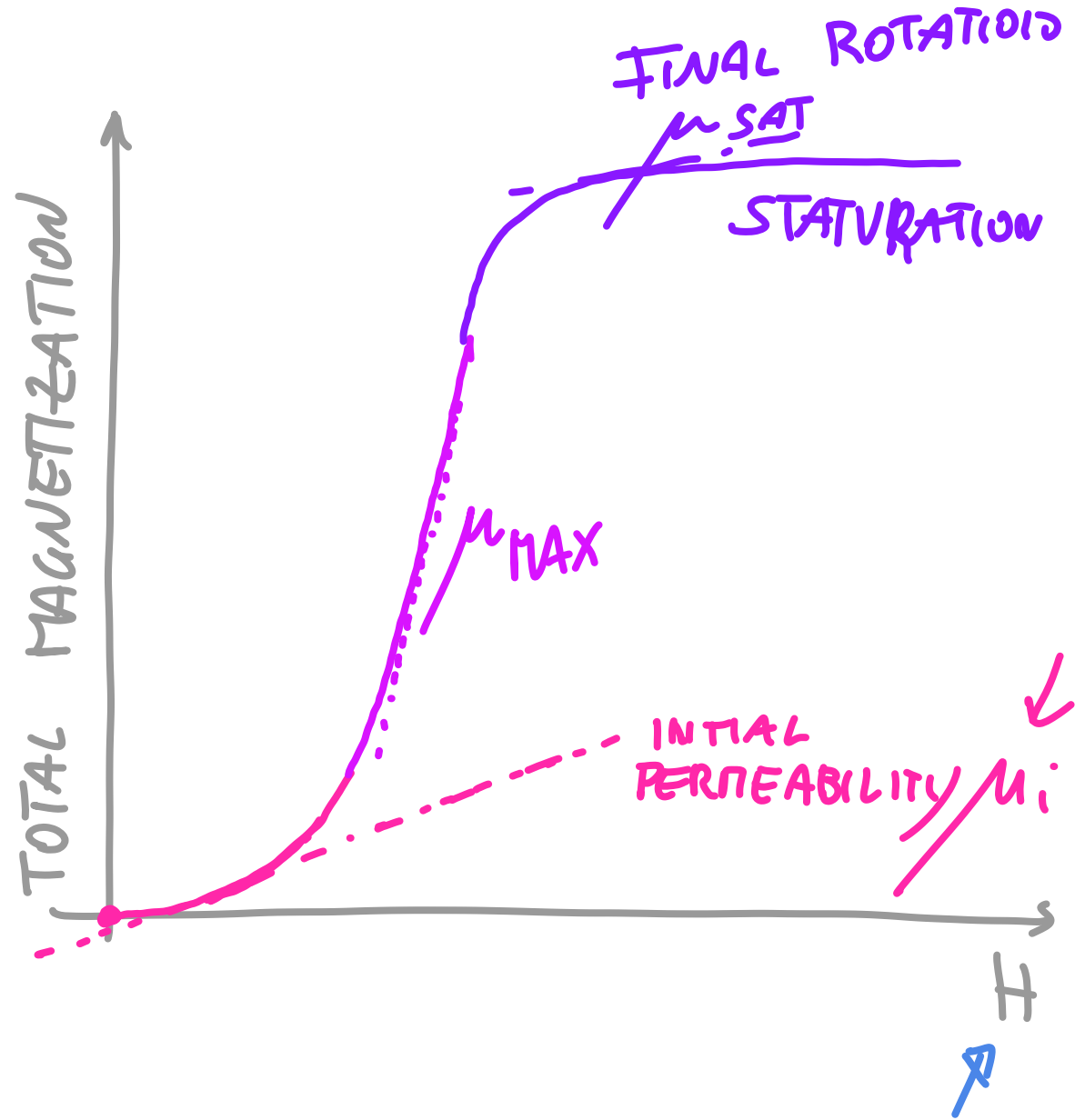


LATER WE WILL SEE
HOW THE DOMAIN WALLS
CAN "MOVE"

MULTIDOMAIN MAGNETIC MATERIAL

APPLY
MAGNETIC FIELD

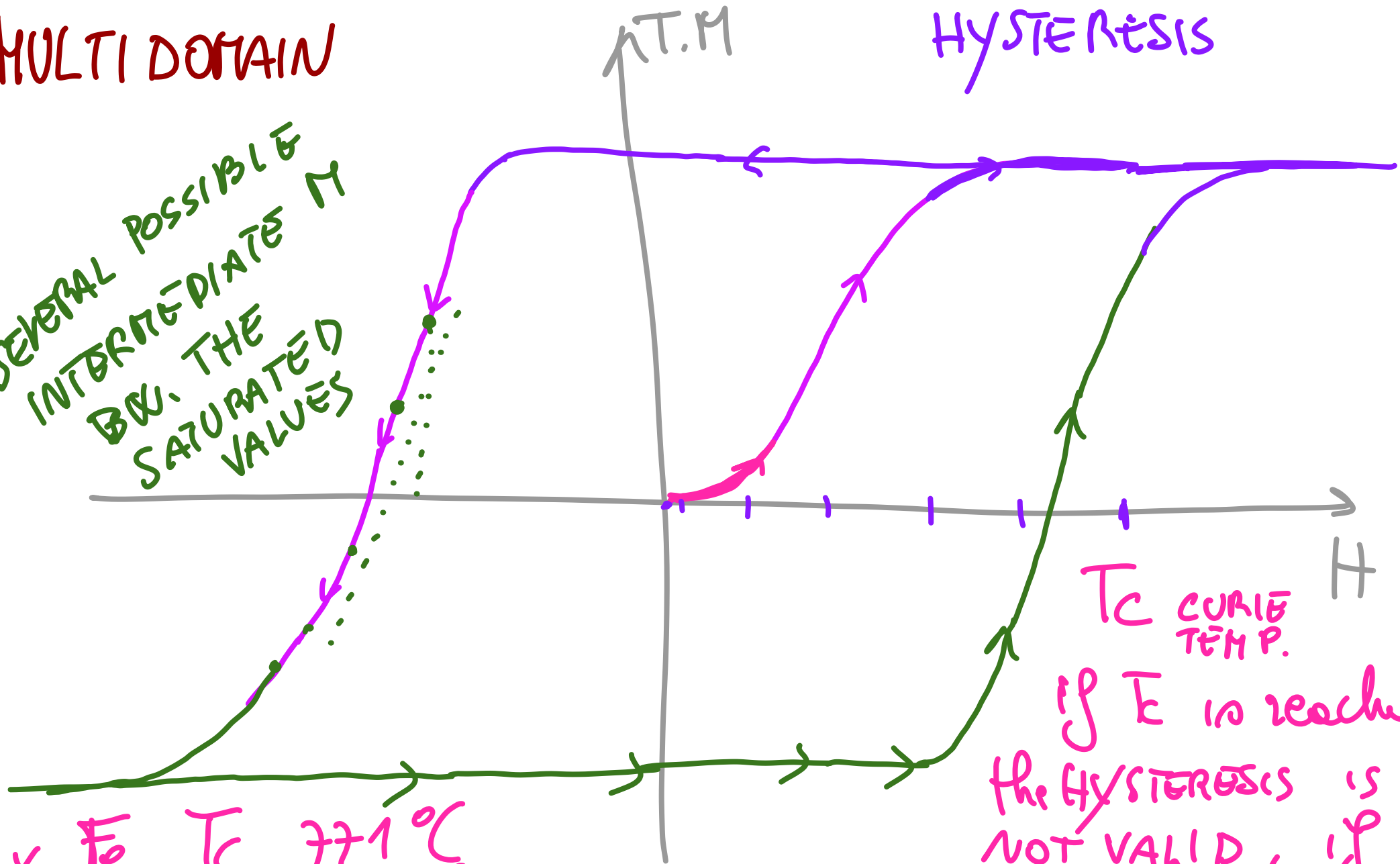
- MAGNETIZATION M INCREASES SLOWLY AT THE BEGINNING
- M INCREASES RAPIDLY
- M SATURATES



MULTI DOMAIN

HYSTERESIS

SEVERAL POSSIBLE INTERMEDIATE B.W. THE SATURATED VALUES

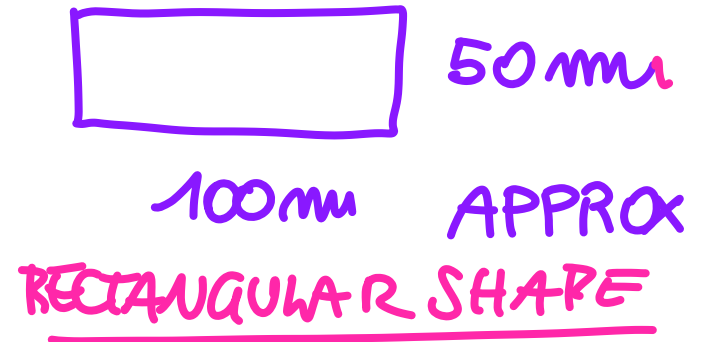


ex	Fe	T _c	771°C
	Ni	T _c	358°C
	Co	T _c	1117°C

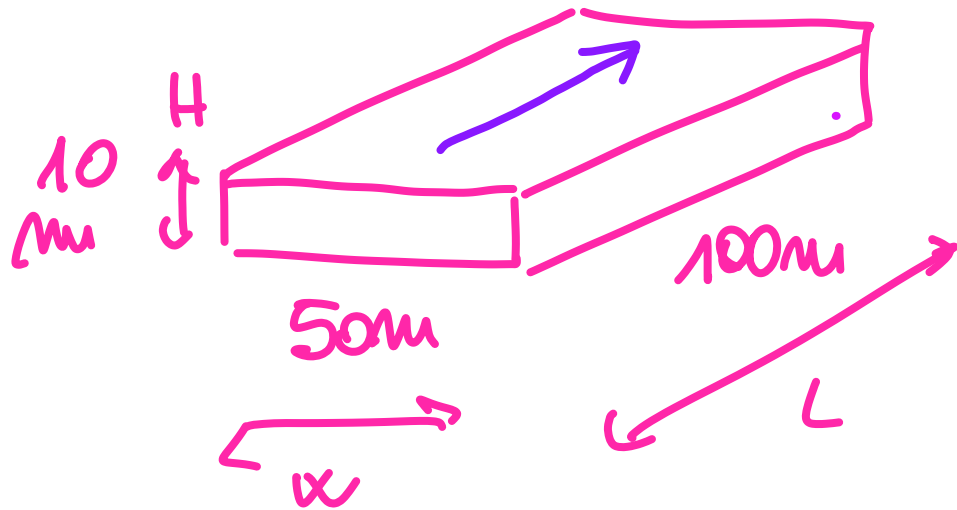
T_c CURIE TEMP.
 if T is reached the hysteresis is NOT VALID, if R.F. IS RELEASED H. IS LOST (PARAMAGNETIC)



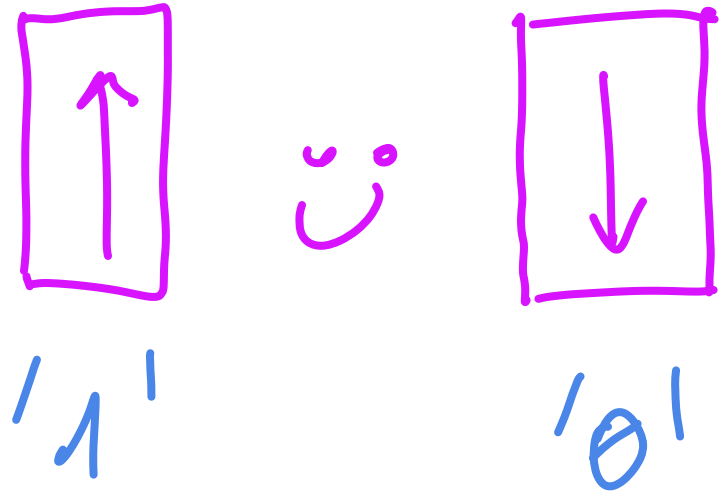
→ SQUEEZED
TO THE SIZE
OF A SINGLE
DOMAIN
~ 100mm



SINGLE DOMAIN MAGNET: DUE TO SHAPE ANISOTROPY H_c ALIGNS WITH LONGEST SIDE OF MAGNET

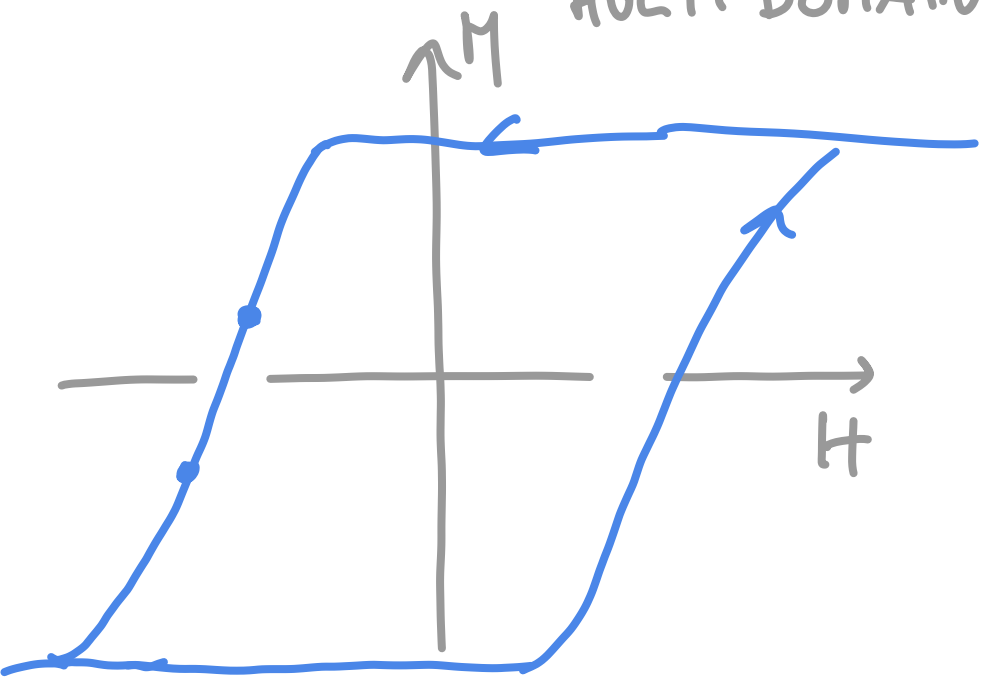


TOP VIEW

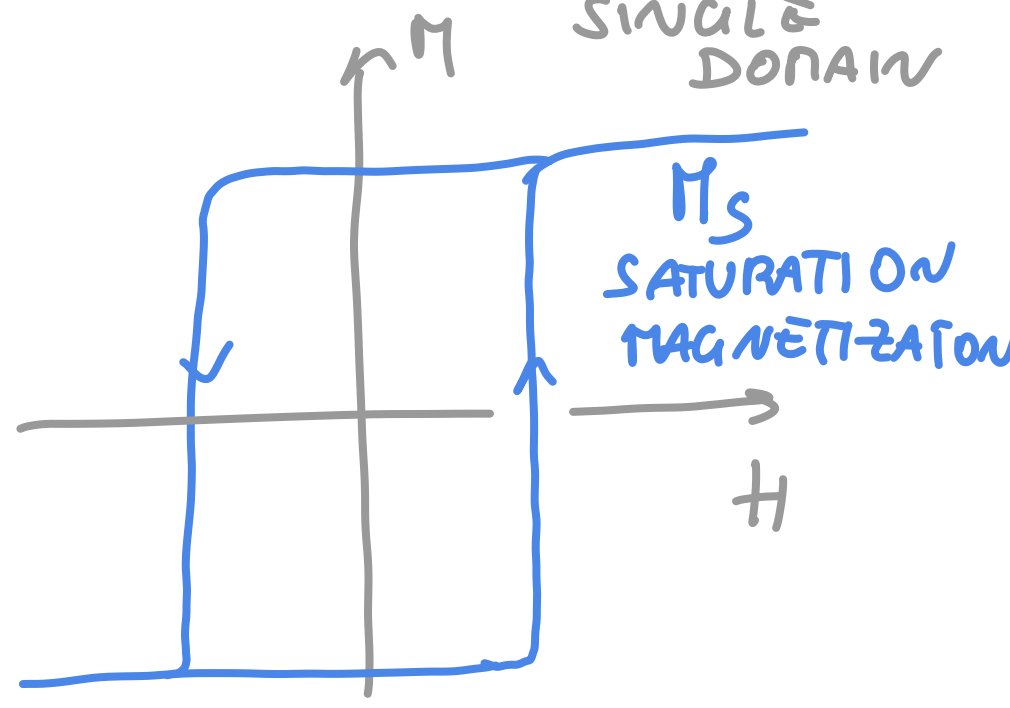


ASSOCIATE INFORMATION
TO MAGNETIZATION

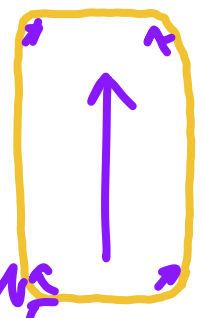
KULTI DOMAIN



SINGLE DOMAIN

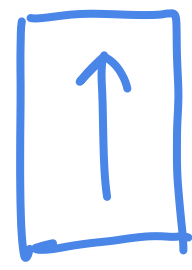


REAL
NANO
MAGNET



BUT

IN MORE
REALISTIC
CASE



SHAPE
IDEAL



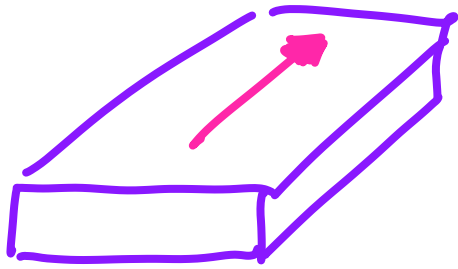
SOME DIFFERENCES

1. AT CORNERS

→ THE CENTRAL STILL PREVAILS

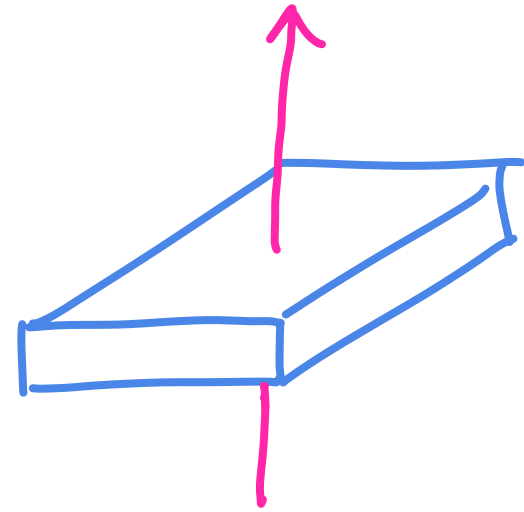
→ ∪ WORKS AS INFO STORAGE

IN-PLANE
I-NML



\vec{n} IS IN THE
PLANE OF THE
BIGGER SURFACE

OUT-OF-PLANE
P-NML



\vec{n} IS PERPENDICU-
LAR TO THE
SURFACE

MAGNETIC LOGIC

I-NMML

- a) INTRODUCTION
- b) TECHNOLOGY
- c) IMPPL PHASES & CIRCUITS

I-NML

OBJECTIVES

Q.) INTRODUCTION

Focus NOW ON

I-NML

I-NANO MAGNETIC LOGIC →

MAGNETIC FCN

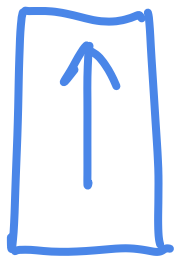
↓
HAS INTRINSIC MEMORY

COUPLING AS IN
MOL-FCN

HOW CAN THE MAGNETS INTERACT?

↳ SEE LATER

→



STABLE

WE WANT THEM TO BE STABLE



STABLE

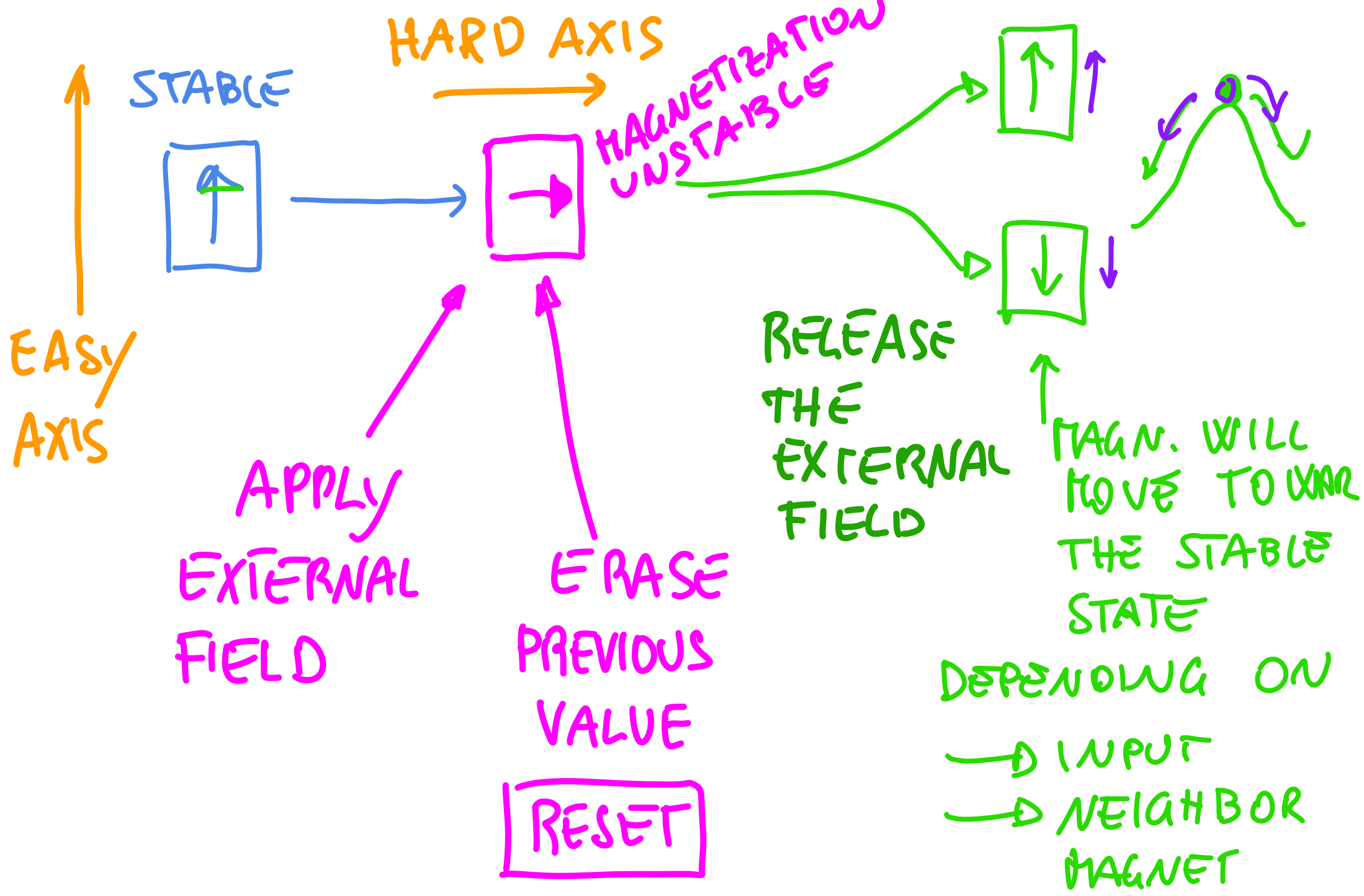
↓



PROPAG.

→

BUT WANT ALSO TO CHANGE THE N. FOR WFO

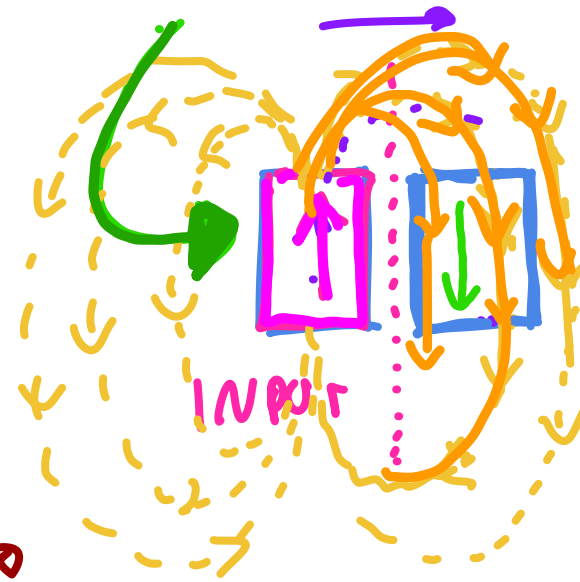
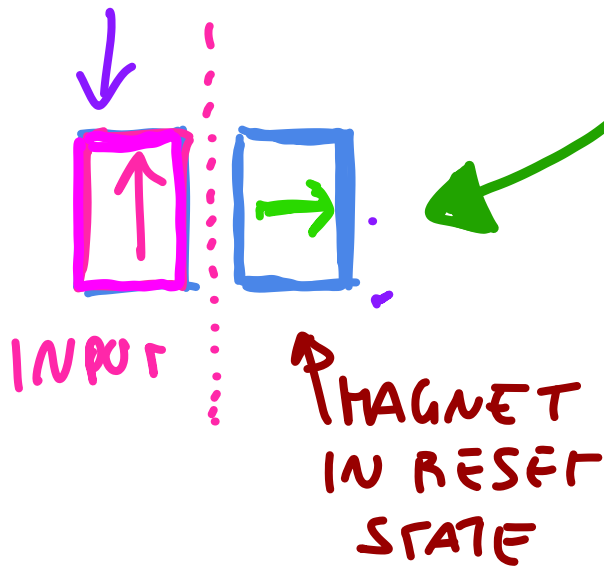


HORIZONTAL INFORMATION PROPAGATION

EXTERNAL
M.F.H

APPLIED

RELEASED



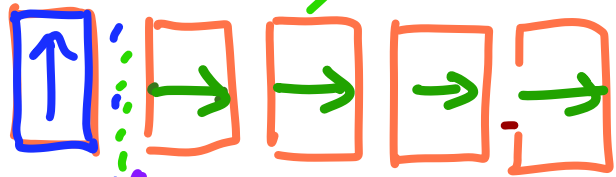
→ LANDAU-LIFSHITZ EQUATIONS (NEXT LECTURES)

→ MODEL

THE INPUT GENERATES A MAGNETIC FIELD THAT INFLUENCES THE DIRECTION OF THE MAGNETIZATION OF THE MAGNET WHEN IT EXITS FROM THE UNSTABLE RESET STATE

I-NHL WIRE

APPLY EXT. H

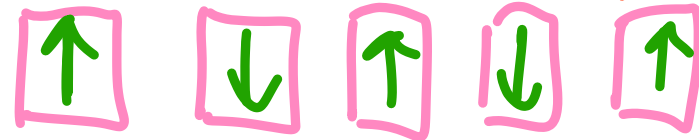


H WIRE
COUPLED VIA
LONGER AXIS

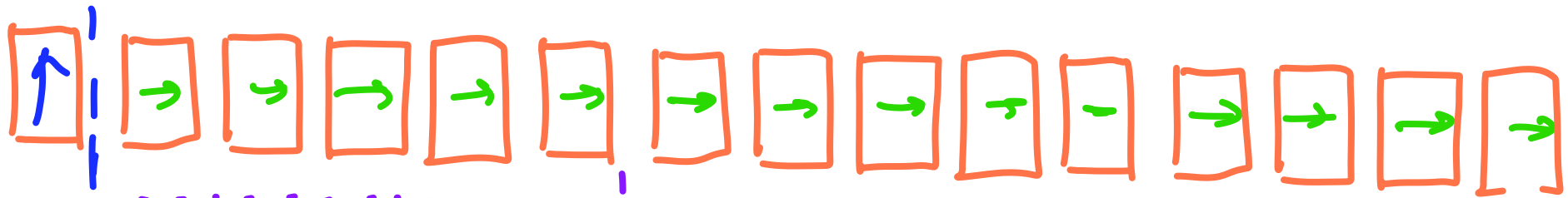
RELEASE EXT. H



ANTI FERRO MAGNETIC
COUPLING



↑
SHORT WIRE
LONG WIRE
↓

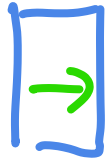


... CRASH!

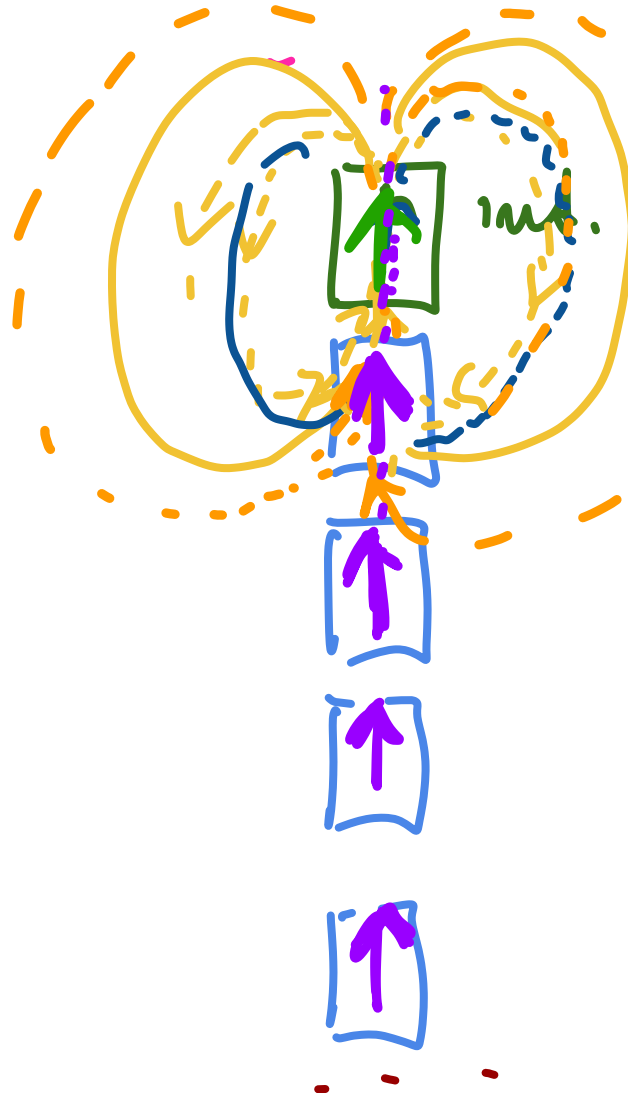
ACTS AS
INPUT

ONLY A MAXIMUM LENGTH IS ALLOWED

VERTICAL WIRE INFORMATION PROPAGATION



V. WIRE
COUPLED VIA
SHORTER AXIS



FERROMAGNETIC
COUPLING

THERE IS A
LIMIT IN THE
NUMBER OF
MAGNETS THAT
CAN BE
ALIGNED

THE TRANSFER OF INFORMATION DEPENDS ON

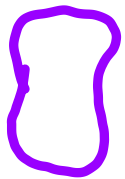
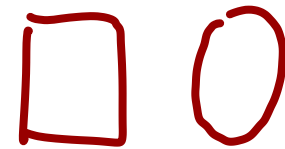
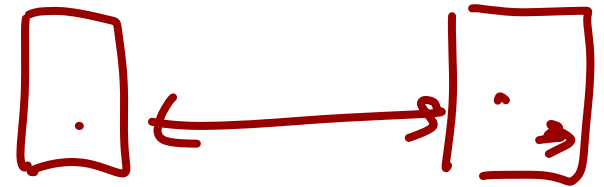
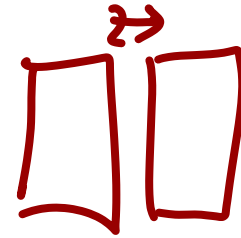
→ DISTANCE

→ TEMP.

→ INPUT, INPUT DIST.

→ SHAPES

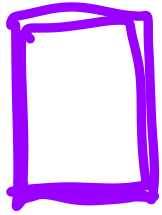
→ TECH. PARAMETERS



I-NML

IM-NML

IN PLANE MAGNETIC



PROS

CONS

→ VERY LOW POWER
(SWITCHING), NO LEAKAGE

→ INTRINSIC MEMORY

→ RAD HARD

→ CAN BE FABRICATED
WITH CURRENT TECH,
AND INTEGRATED WITH
STANDARD.

→ CLOCK GEN,
ENERGY
CONSUMING

→ INTERFACE
WITH STANDARD.

→ NOT SO NAND

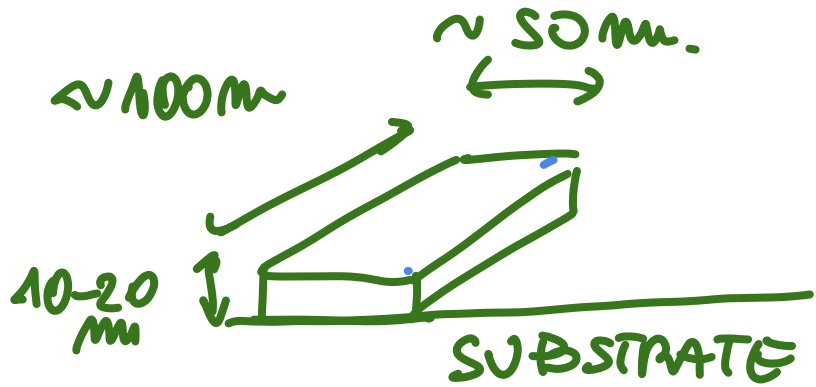
→ SLOW

I-NML

OBJECTIVES

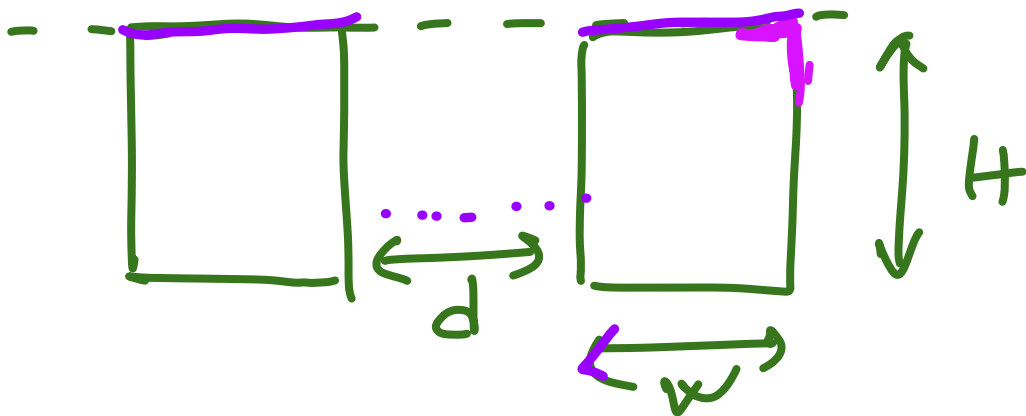
Q) TECHNOLOGY ...

NHL TECHNOLOGY



- LITHOGRAPHY EBL., FIB
- EVAPORATION OF METAL
Co, PERMALLOY

ALIGNMENT

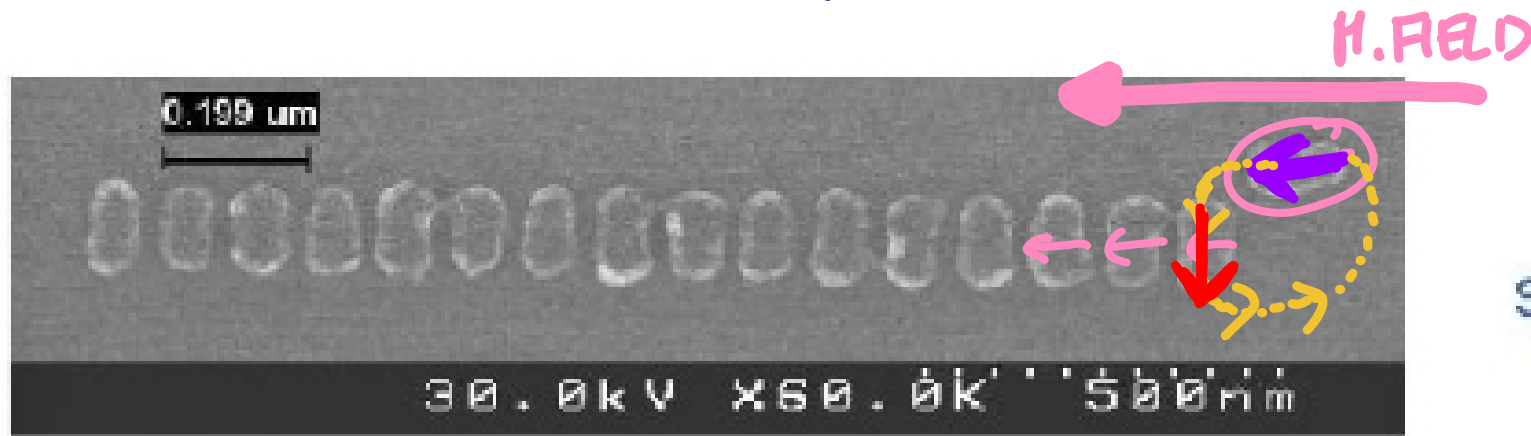


- ALIGN.
- d → H
- w

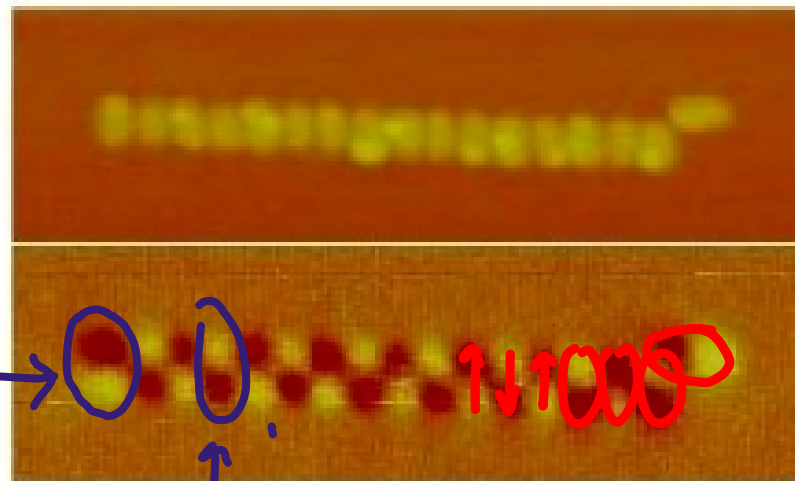
→ THICKNESS



DEMONSTRATION OF ANTIFERROMAGNETIC COUPLING IN A WIRE



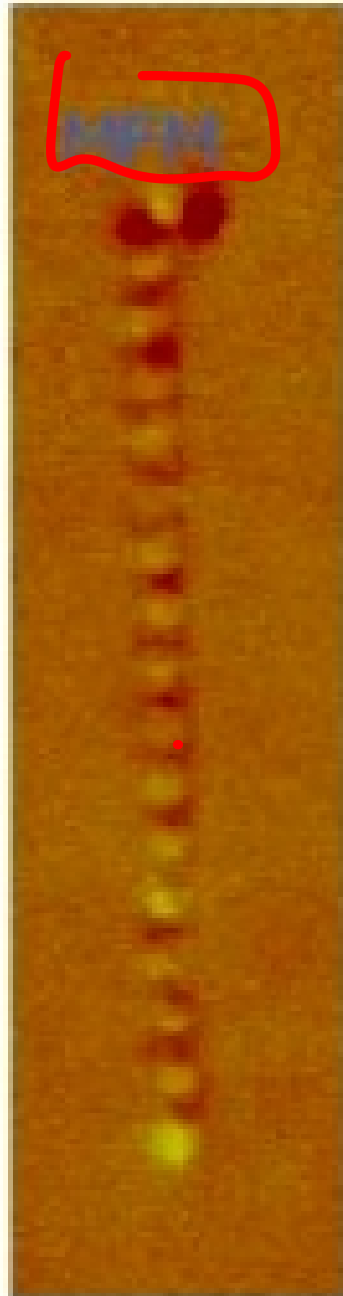
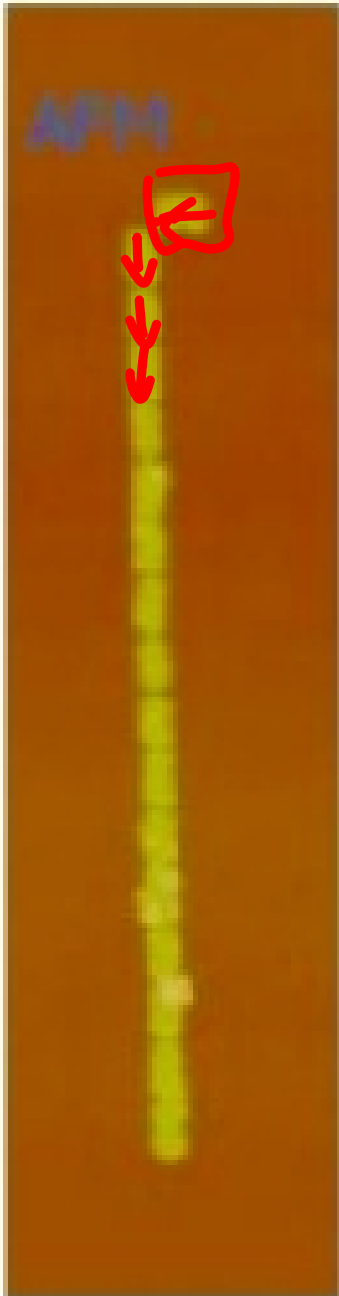
SCANNING
ELECTRO
MICROSCOPY



AFM
ATOMIC
FORCE
MICROSCOPY

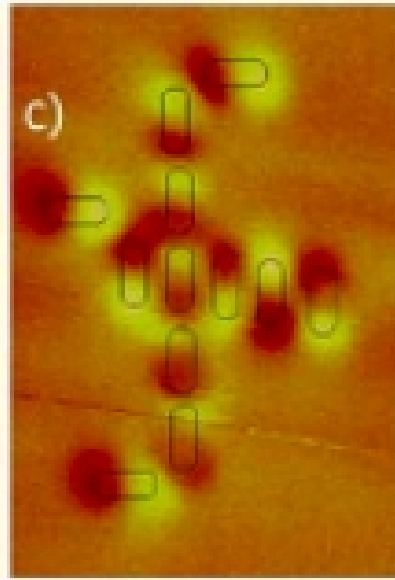
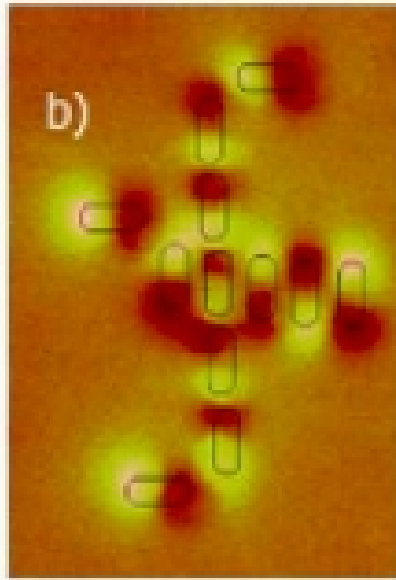
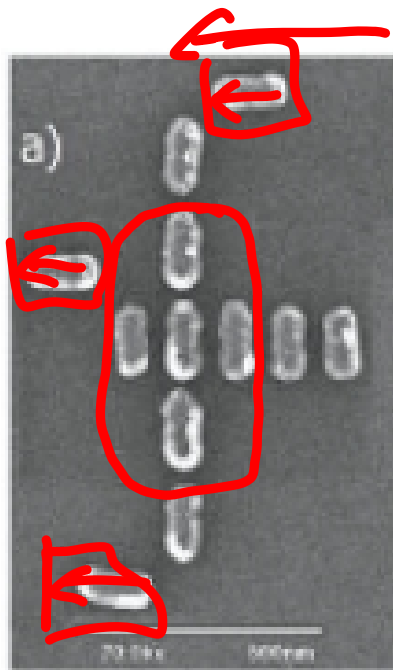
MFM
MAGNETIC
FORCE
MICROSCOPY

IN RE, POROD \rightarrow NOTRE DAME UNIVERSITY

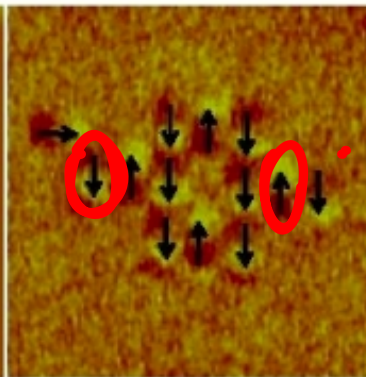
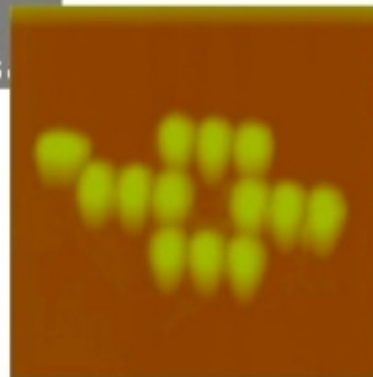
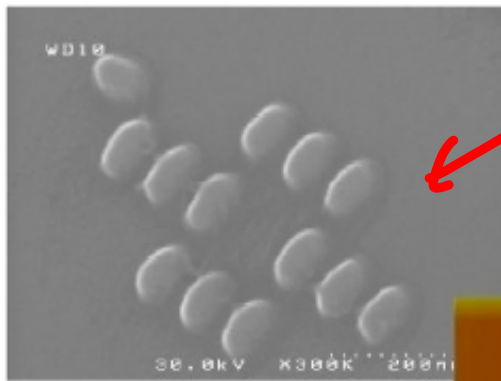


DEMONSTRATION
OF A
FERROMAGNETIC
COUPLING

IN RE, POROD NOTRE DANÉ U.



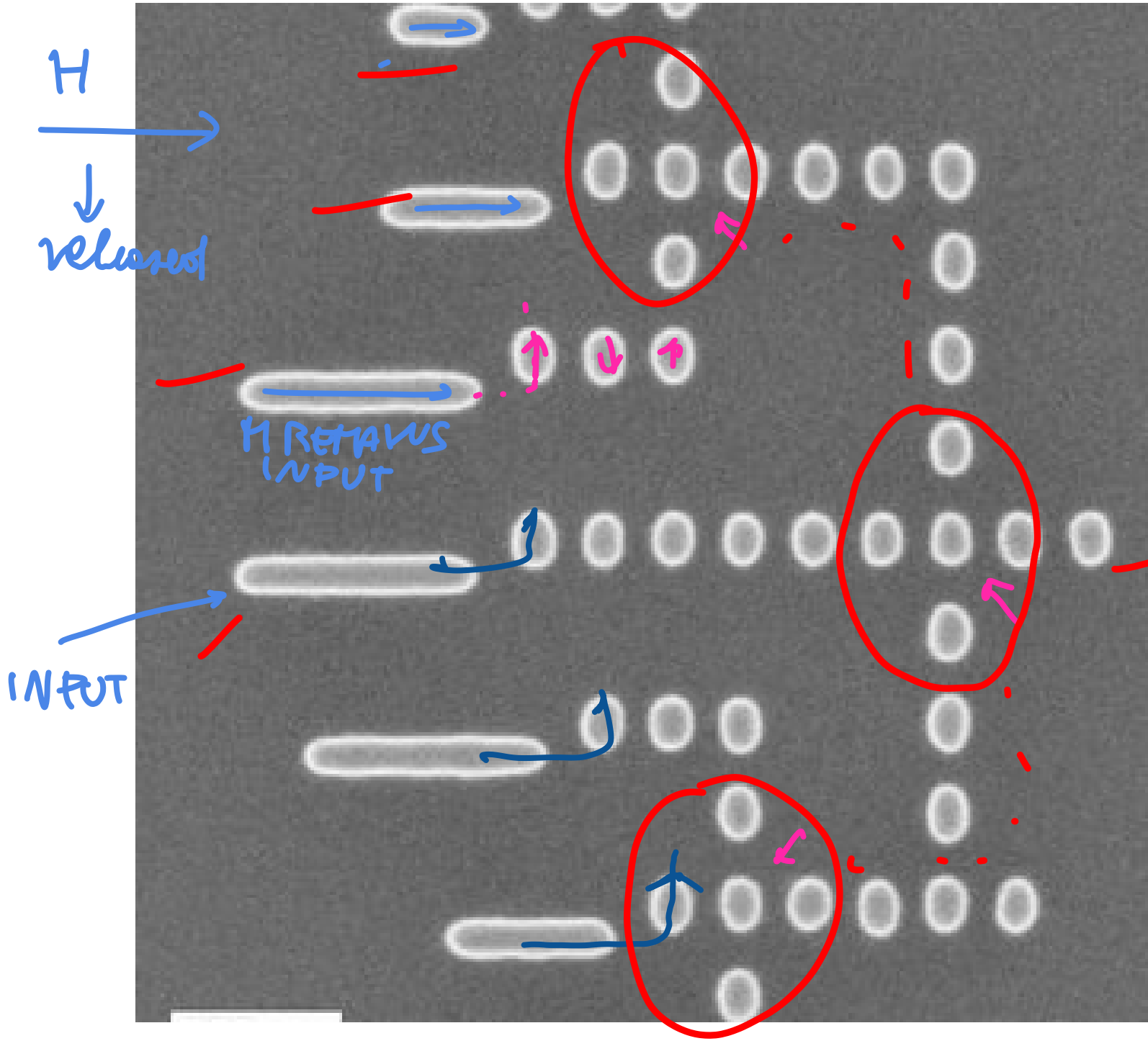
DEMONSTRATION
OF A MAJORITY
VOTER



DEMONSTRATION
OF AN INVERTER

INRE, PORD

NOTRE DAME UNIVERSITY



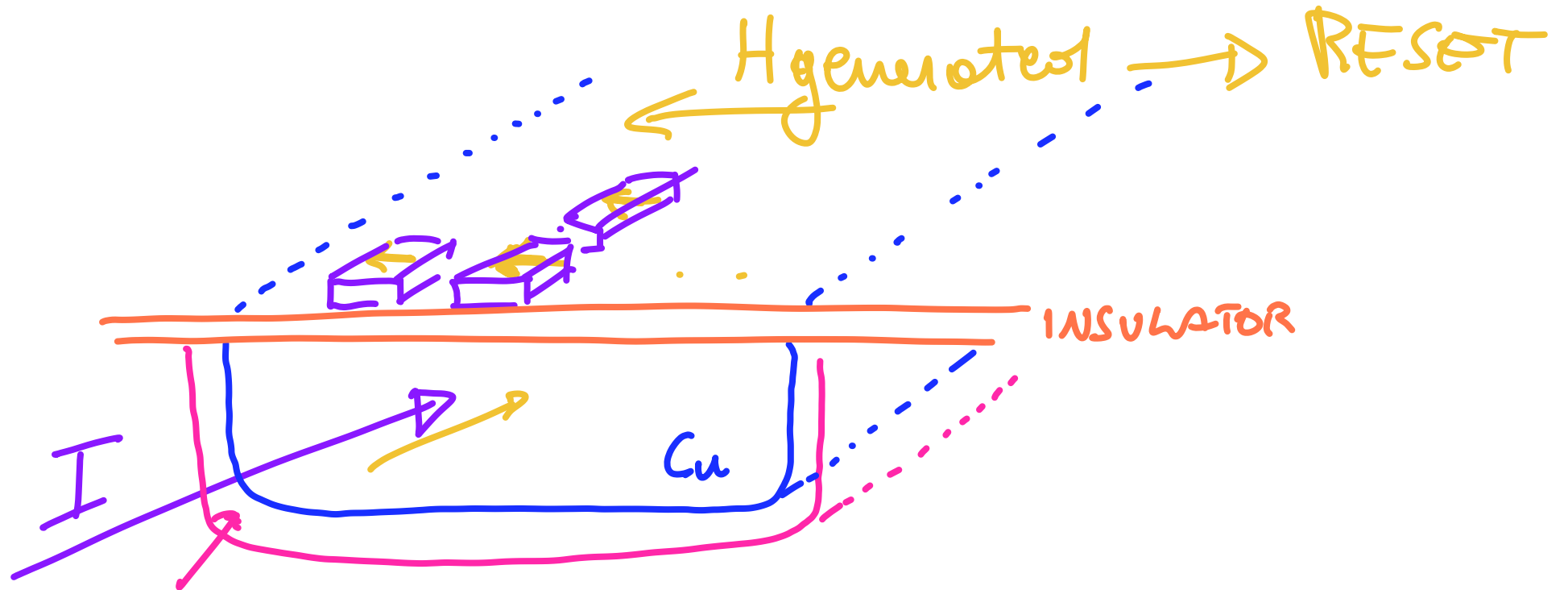
DÉMONSTRATION OF A FULL ADDER

IN RE, POND NOTRE DANÉ U.

EXTERNAL "ENABLE" or "CLOCK"
HOWTO

AND IMPACT
ON CIRCUITS

EXTERNAL MAGNETIC FIELD FOR RESET

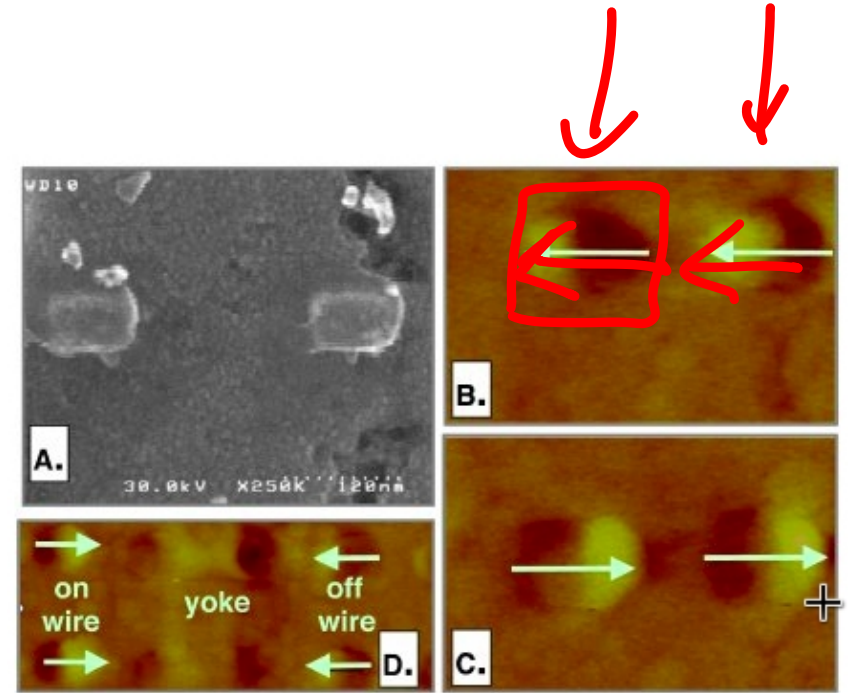
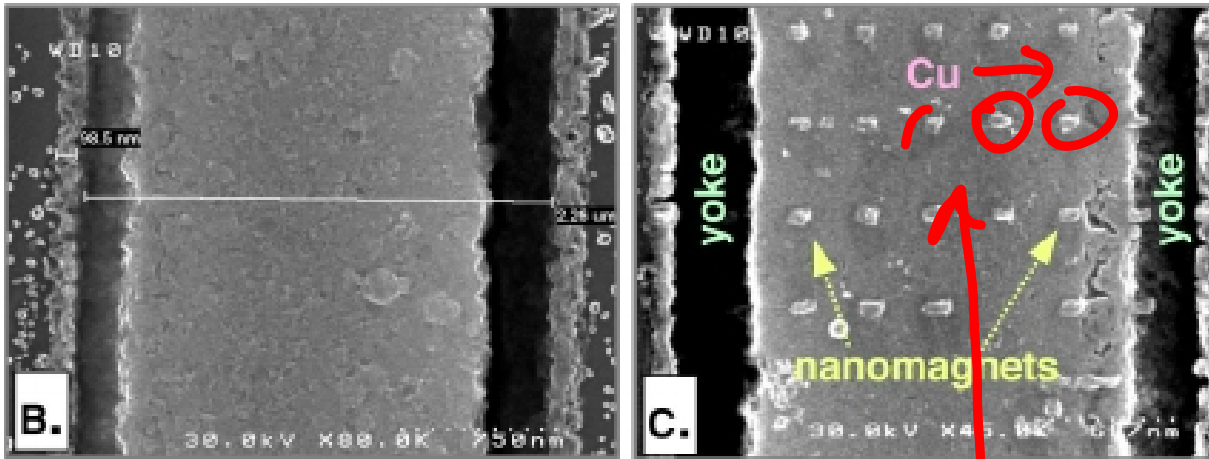
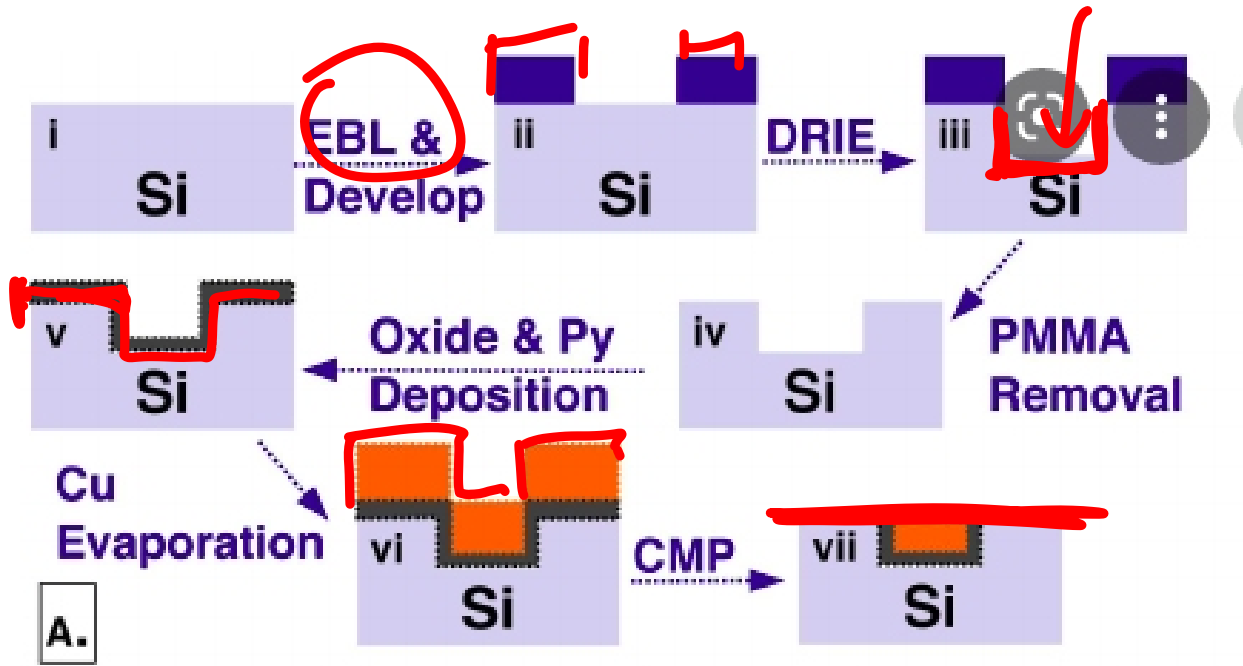


FERRITE JOKE

HEMPHASIZES
THE MAGN. FIELD FOR RESET

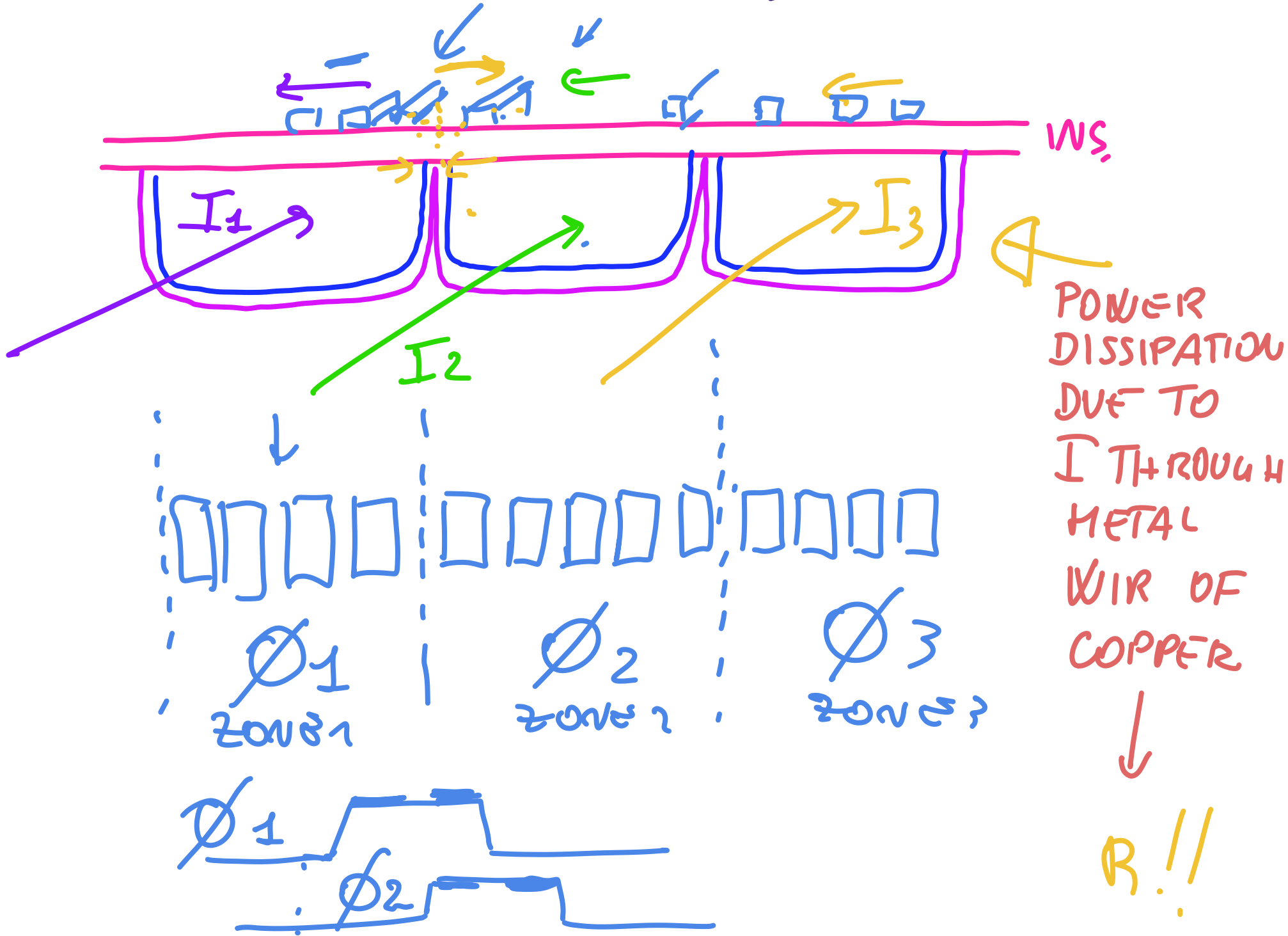
(SMALLER CURRENT!)

CLOCK - RESET FABRICATION & DEMONSTRATION

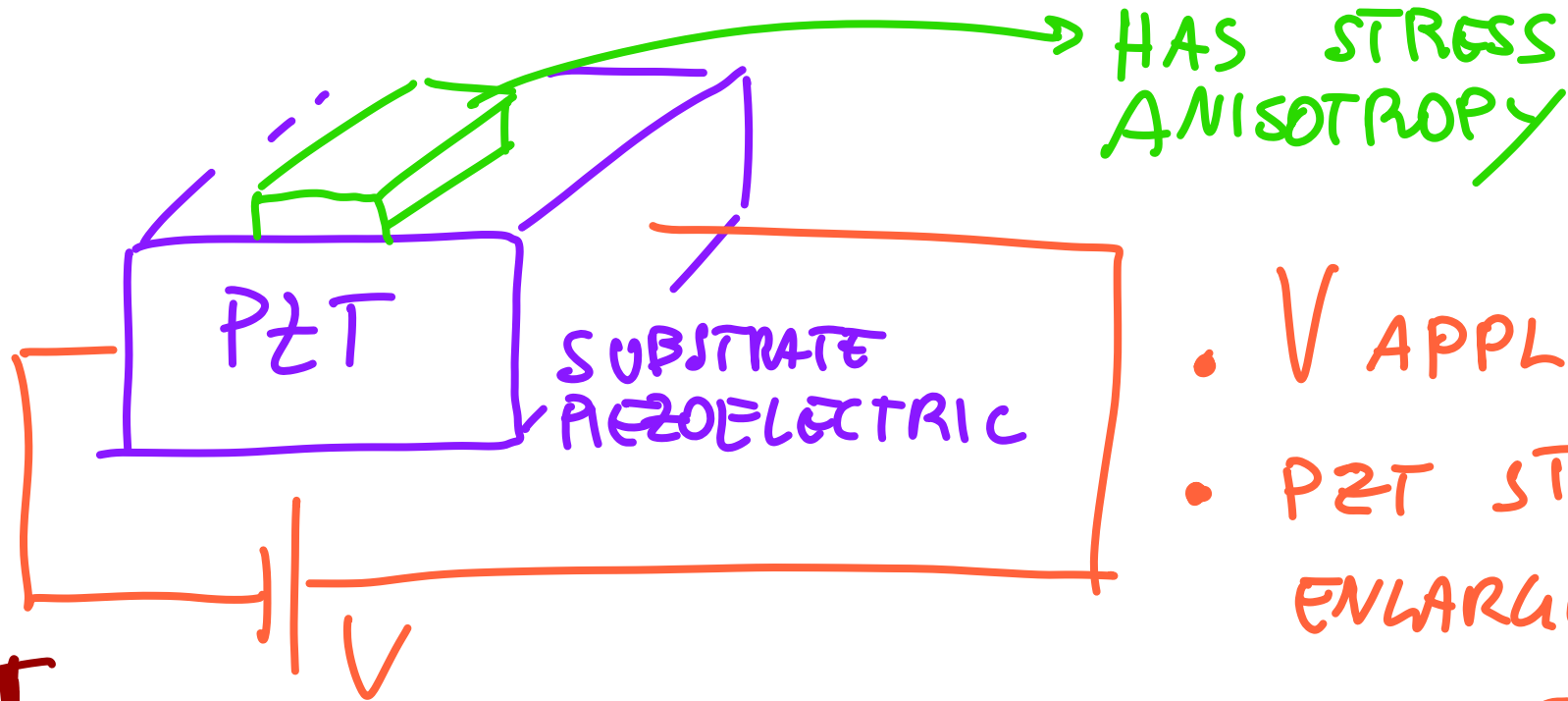


DRIE: DEEP REACTION ION ETCHING

MULTIPLE PHASES



ANOTHER WAY TO APPLY CR

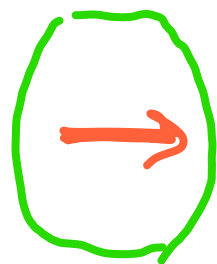


- V APPLIED
- PZT STRESSED ENLARGED
- MAGNETIC MATERIAL CHANGES DUE TO STRESS ANISOTROPY

NO I ,
SMALL
POWER
DISSIPATION



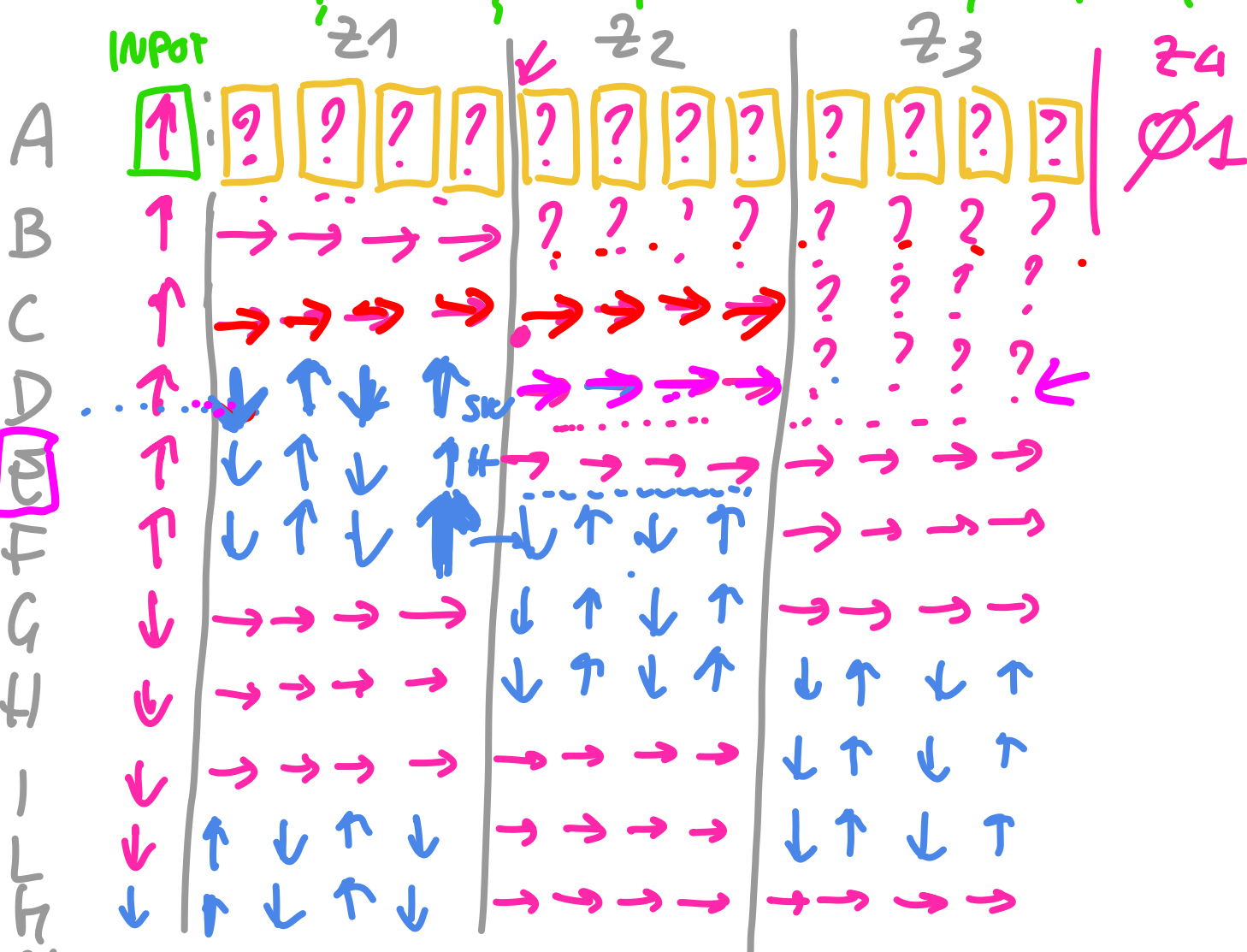
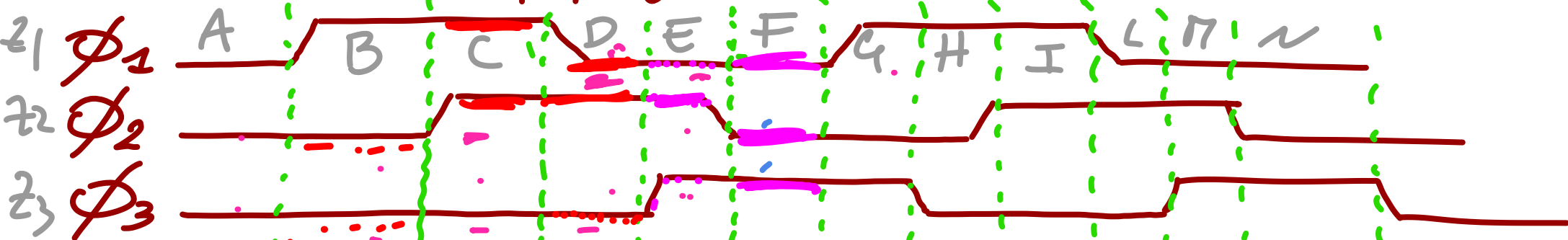
V NOT
APPLIED



V IS
APPLIED

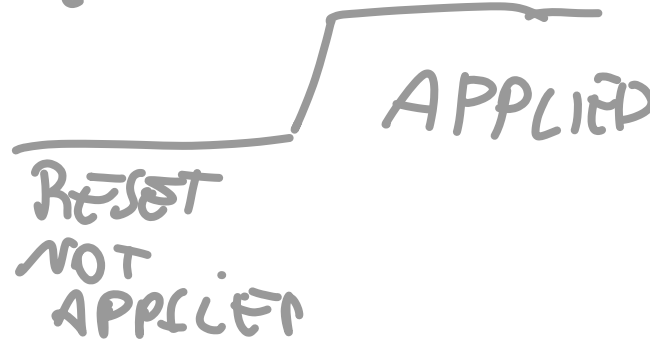
MAGNETIZATION CHANGES
ORIENTATION \rightarrow RESET

CLOCK PHASES FOR I-NML



3 ZONES
A, D, C, N. EACH

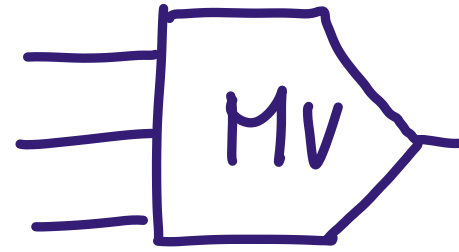
TIME



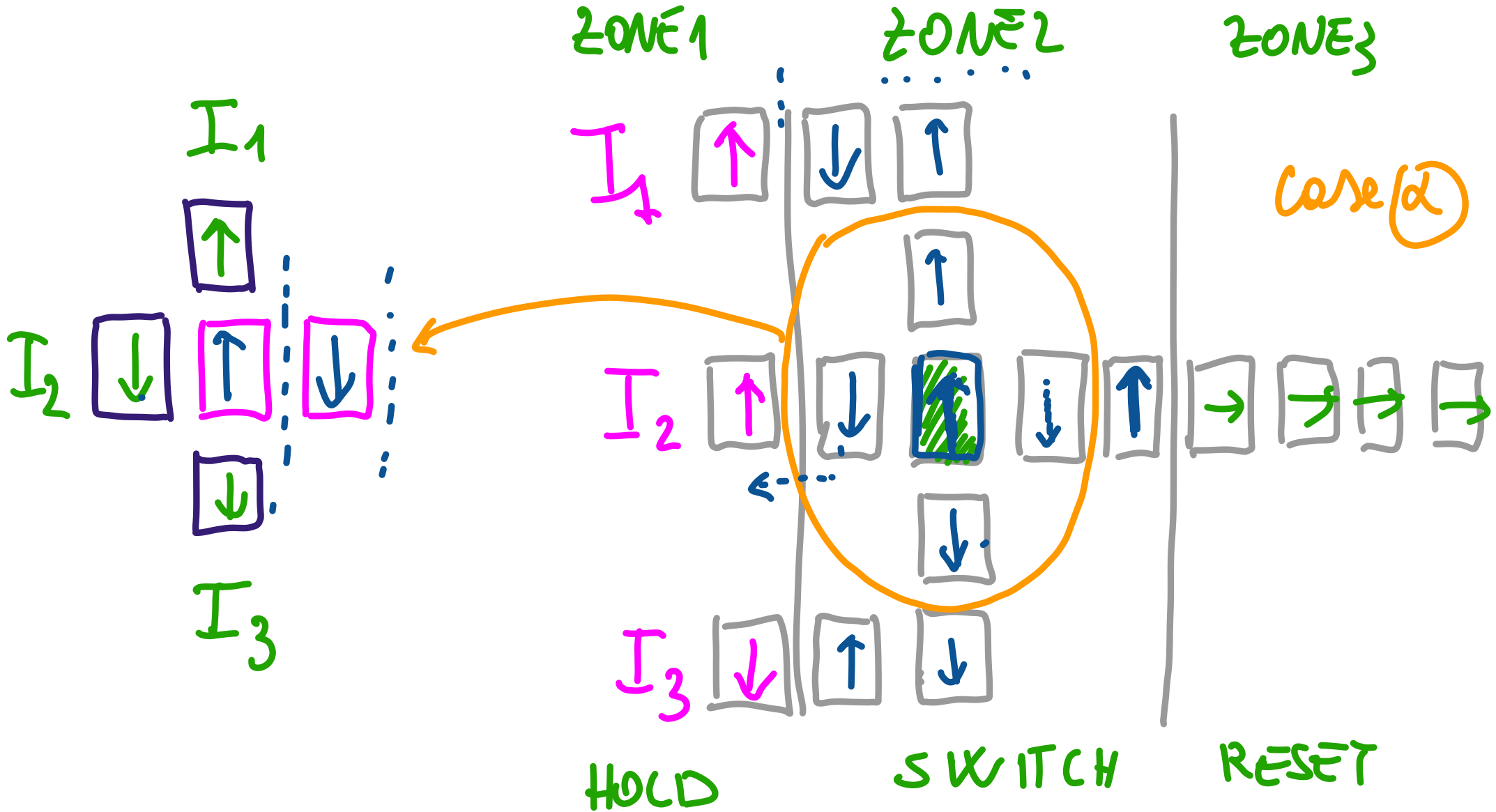
I-NHL

CIRCUITS & PHASES

LOGIC GATES



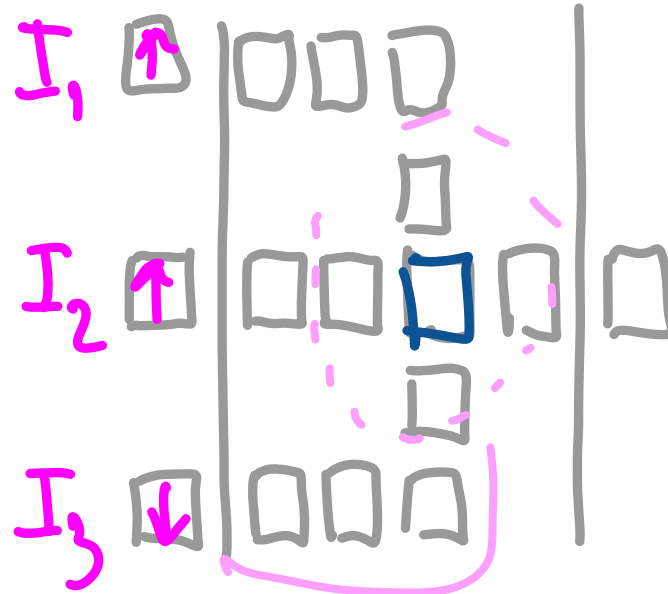
MAJORITY
VOTER



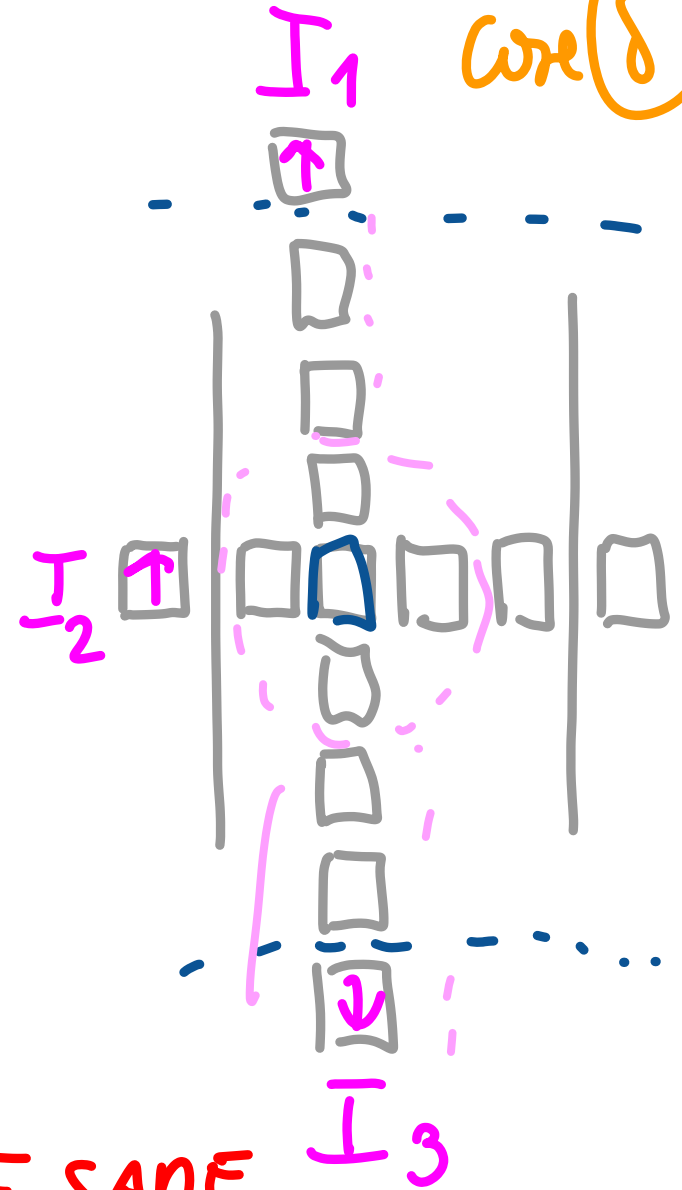
Case β



Case γ



Case δ

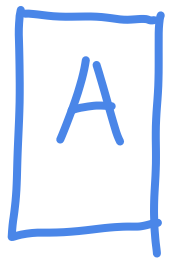
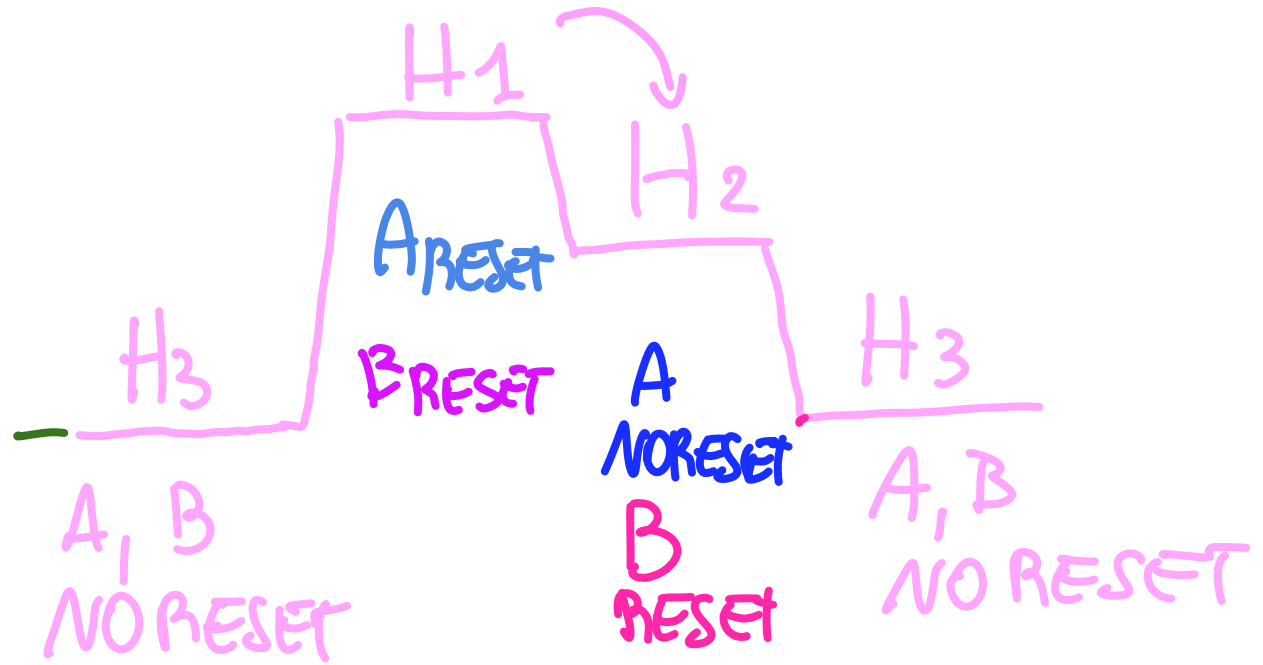
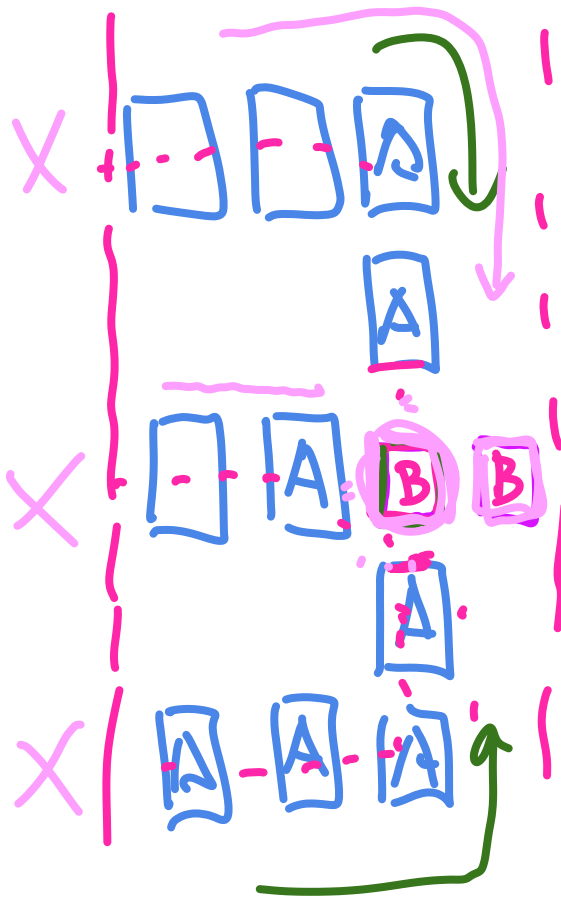


ACTIVE

VERIFY CASES β, γ, δ :

ARE THEY SAME AS α ? WHICH ONE IS BETTER?

M.V. WORKS BETTER IF VIRTUAL CLOCK IS USED



REQUIRES
SMALLER H FOR
RESET

DIFFERENTI-
A.R.

H₃ hold old values Π

H₁ MV all in RESET

H₂ B magnet RESET
A pos'n SWITCH

H₂ REL., H₃, B SWITCHES

MICROMAGNETIC SIMULATION OF VIRTUAL CLOCK - M.V.

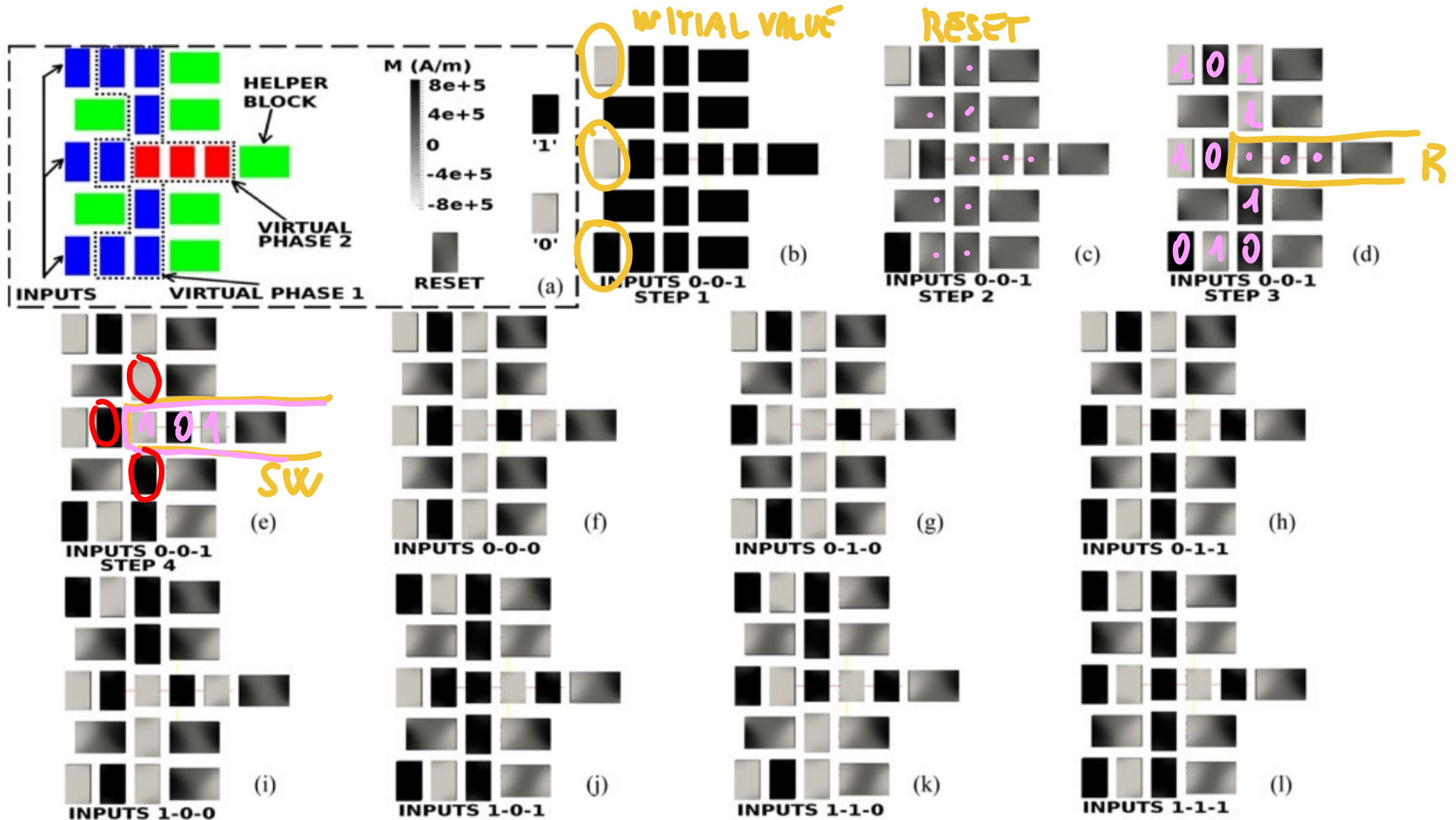
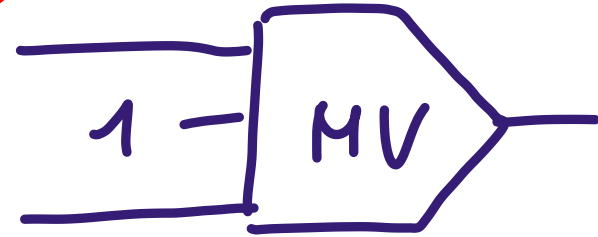


Fig. 5. Majority voter with Virtual Clock. a) Gate layout. The three input wires are in the first virtual clock phase, while the other magnets are in the second virtual clock phase. Helper blocks are required to assure a correct propagation of signals. b) Simulation with inputs equal to 0-0-1. Magnets are initialized to logic '1'. c) Magnets are then forced in the RESET state. d) When the magnetic field start to be removed, only the input wire magnets switch. e) Finally also the central and output magnets switch correctly. f) Final state with inputs equal to 0-0-0. g) Final state with inputs equal to 0-1-0. h) Final state with inputs equal to 0-1-1. i) Final state with inputs equal to 1-0-0. j) Final state with inputs equal to 1-0-1. k) Final state with inputs equal to 1-1-0. l) Final state with inputs equal to 1-1-1.

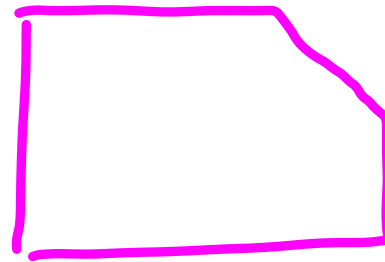
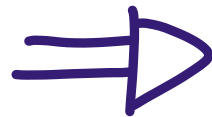
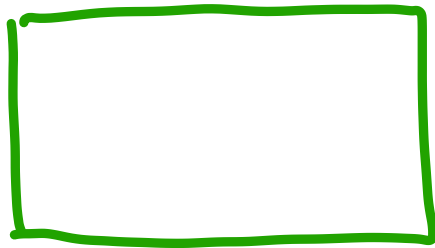
MV →

AND, OR

homework
↑
verify

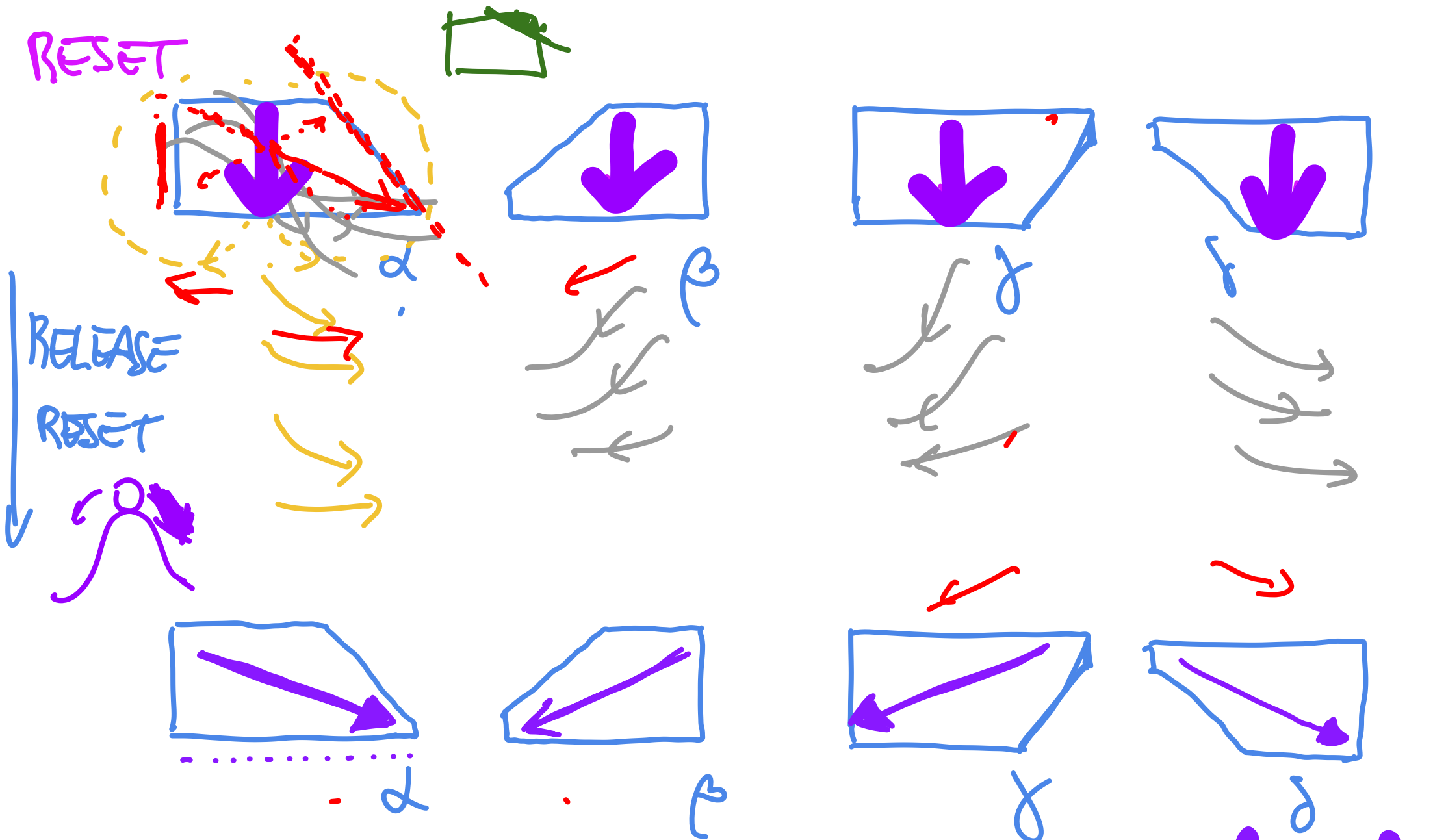


NOT THE ONLY WAY TO DO
AND, OR

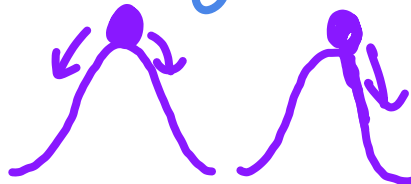


RECTANGULAR
MAGNETS
CUT IN ONE
CORNER TO


FAVOUR MAGNETIZATION



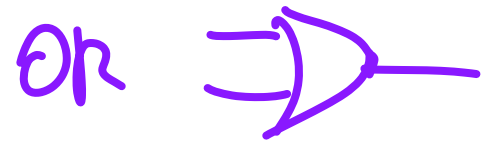
→ EASY AXYS WITH WCLINATION
 ONE DIRECTION FAVOURED By CUT



ANOTHER WAY TO DO LOGIC

IN1		1	0	1	
			1	1	
IN2			1	1	
IN1		1	0	1	0
					
IN2		0	1	1	0

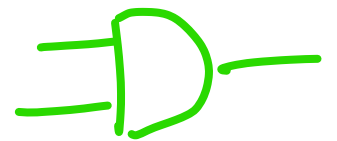
Verify the side of the CUT



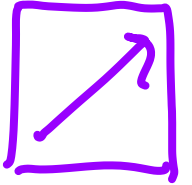
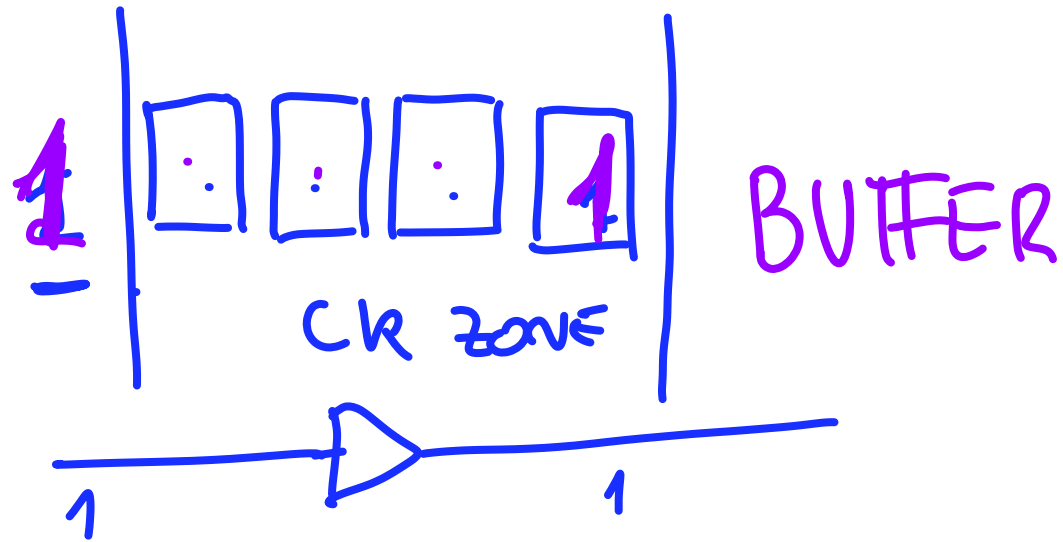
ACTIVE

VERIFY!

AND



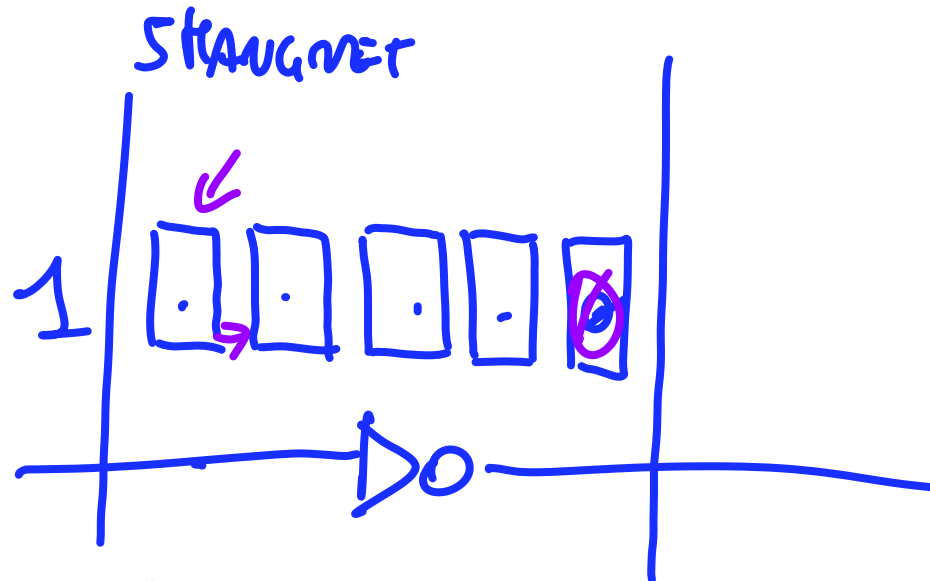
INVERTER



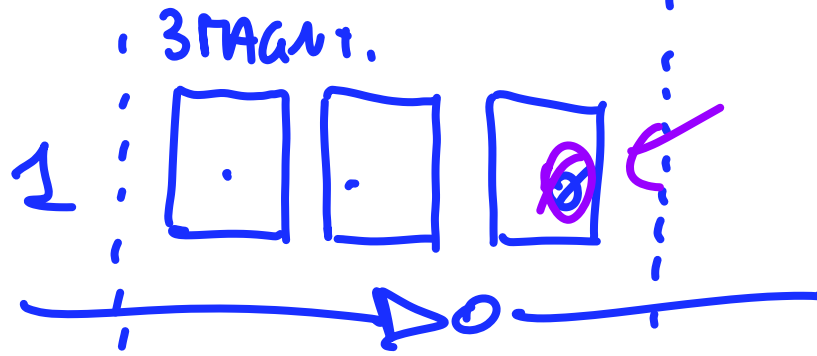
PLAY

-> D.A.R.

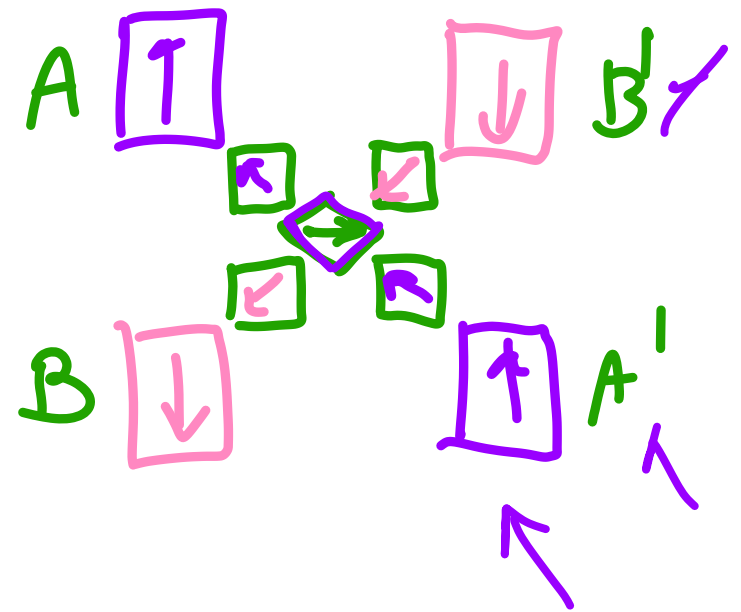
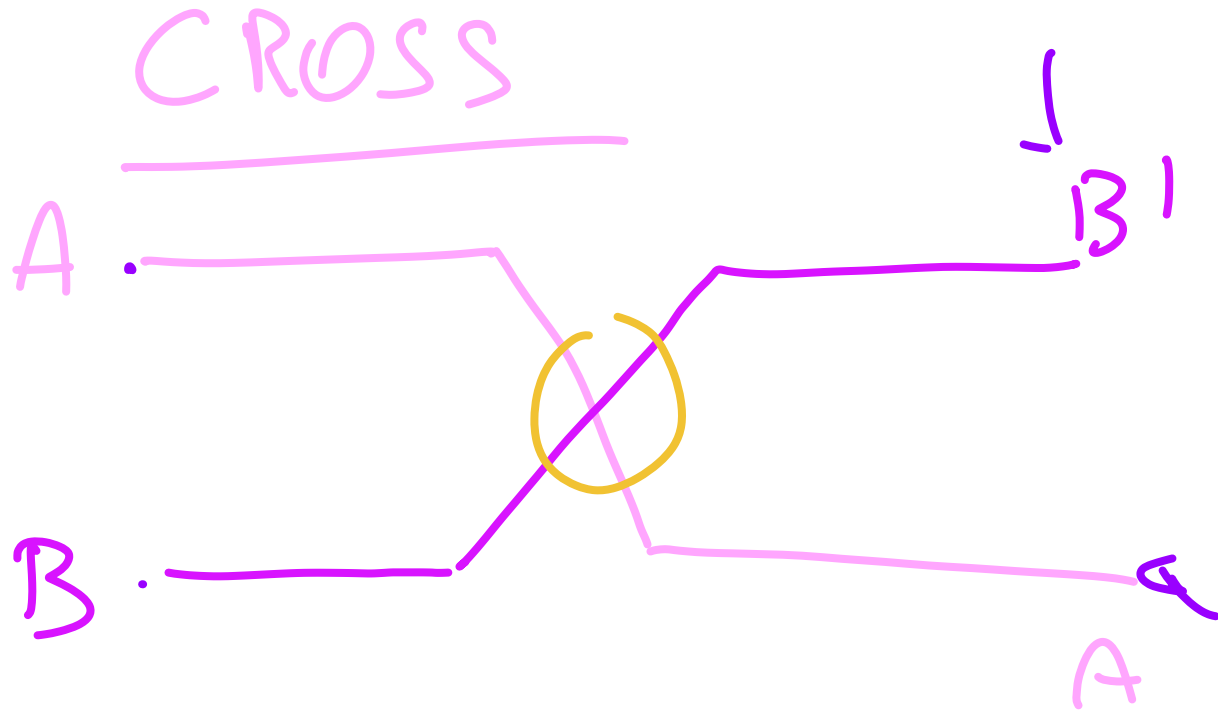
-> DISTANCES



BETTER

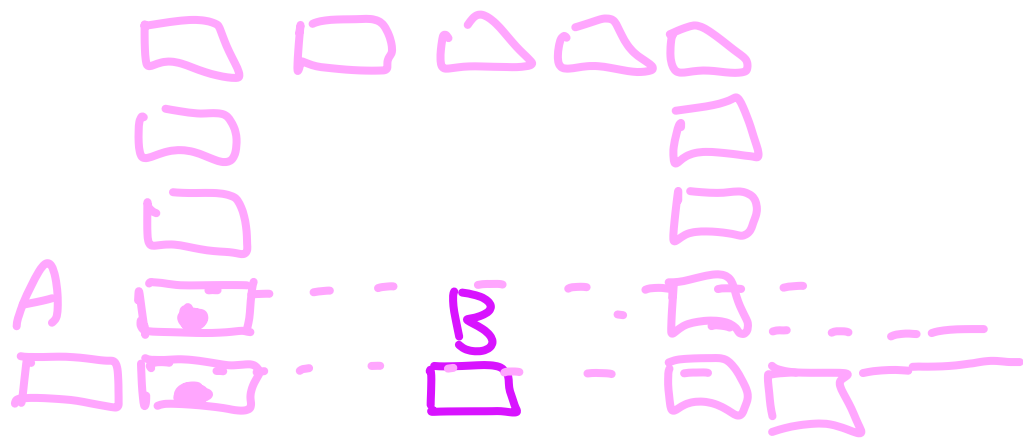


WAY 1

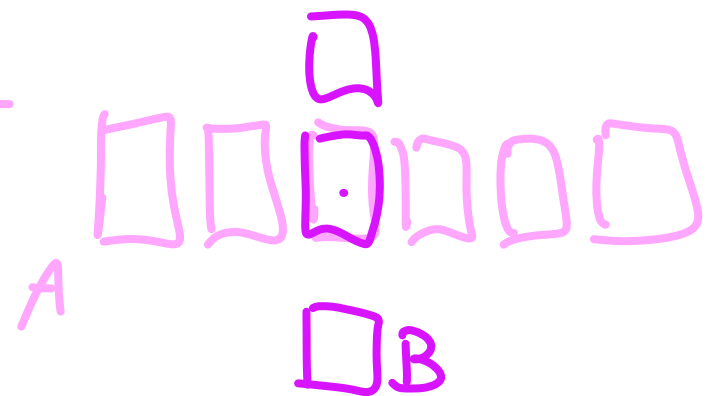


WAY 2

SECTION VIEW



TOP VIEW



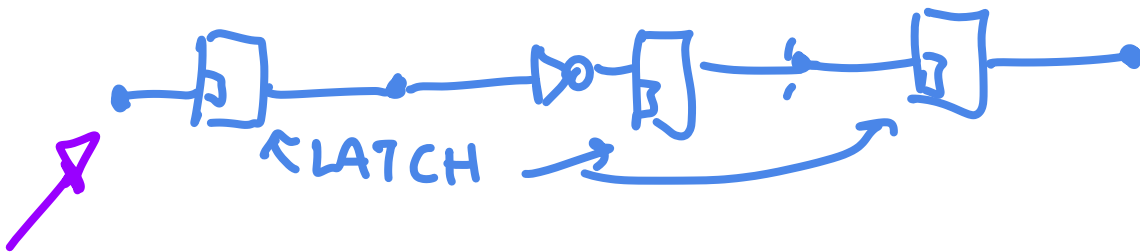
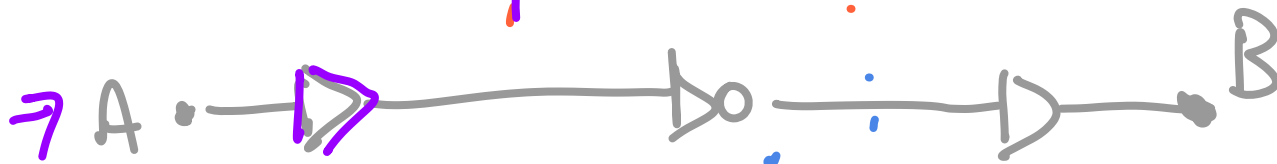
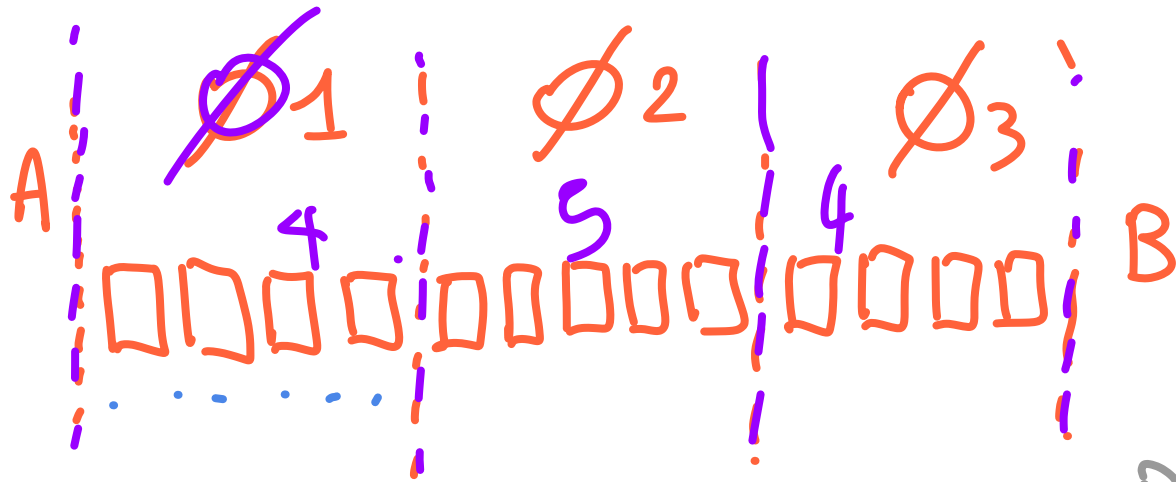
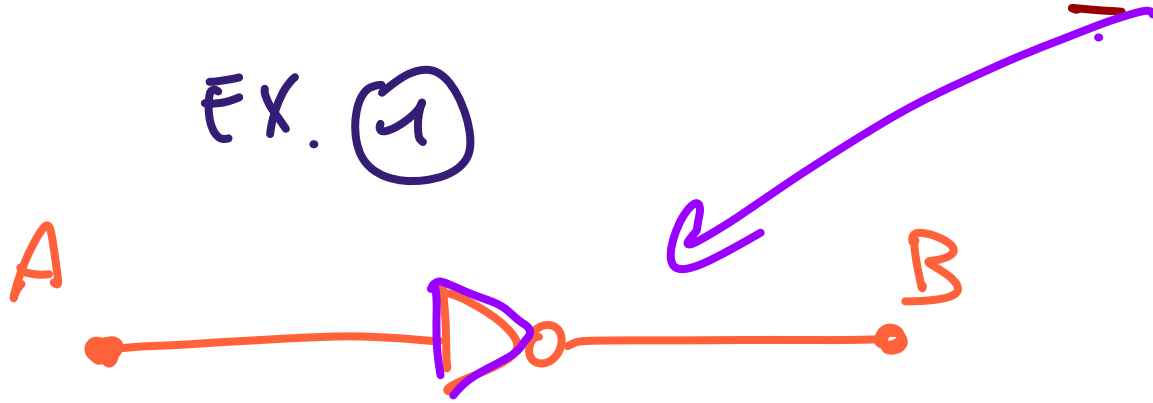
OBJECTIVES

I-NM L CIRCUITS

EXERCISES

EXAMPLES

EX. ①



DESIGN LAYOUT

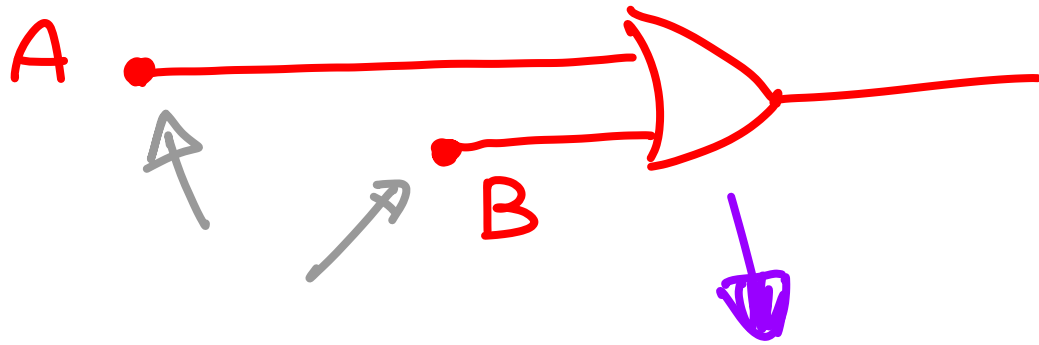
4 MAGNETS \checkmark
ZONE

3 ZONES

EQUIVALENT LOGIC
CIRCUIT

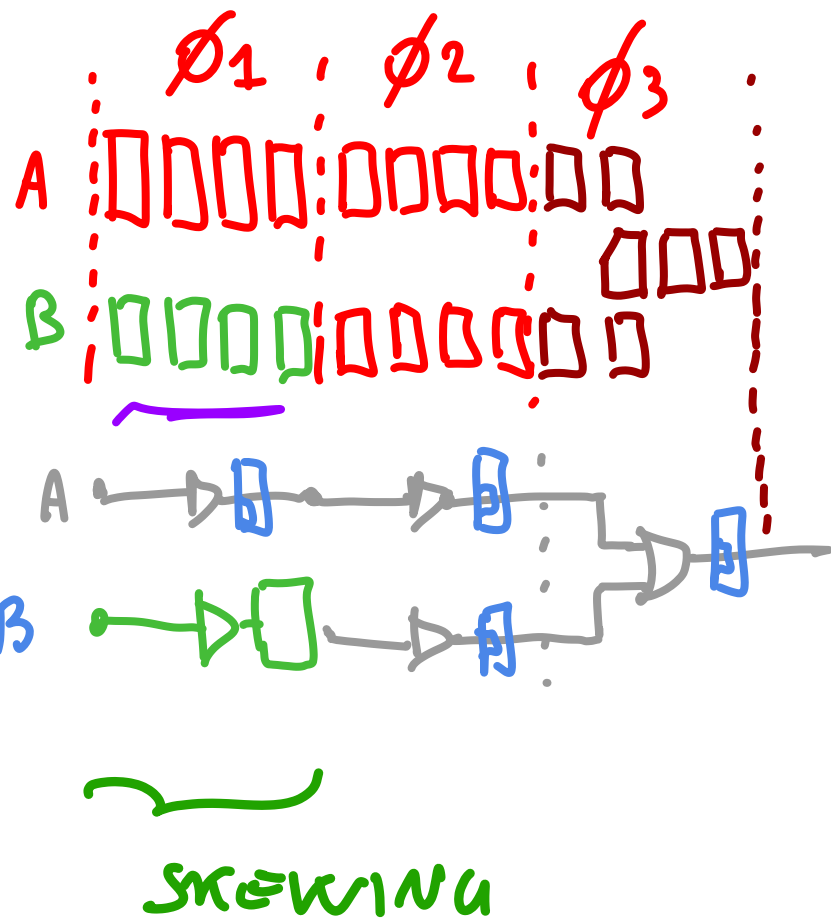
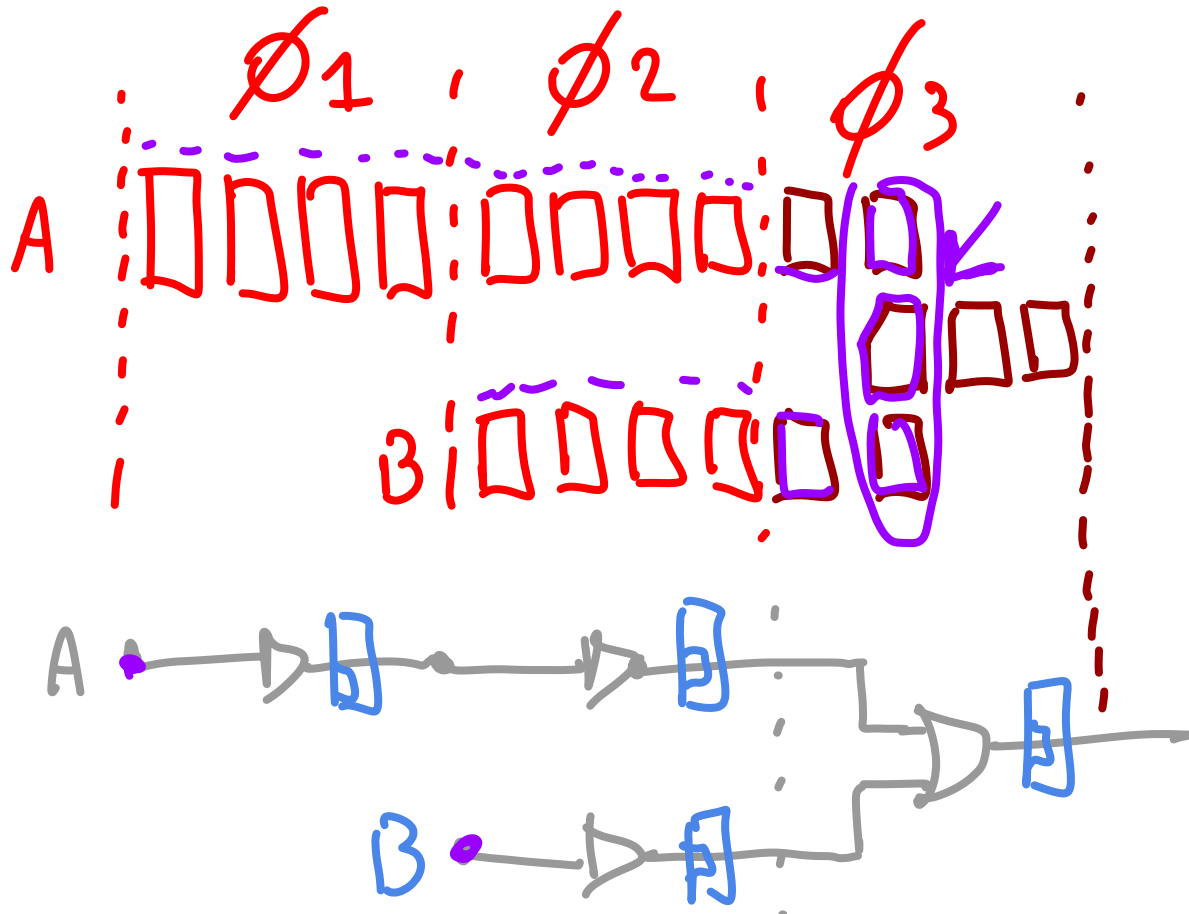
MORE CORRECT MODEL
TAKING INTO ACCOUNT
SYNCHRONIZATION

EXAMPLE 2



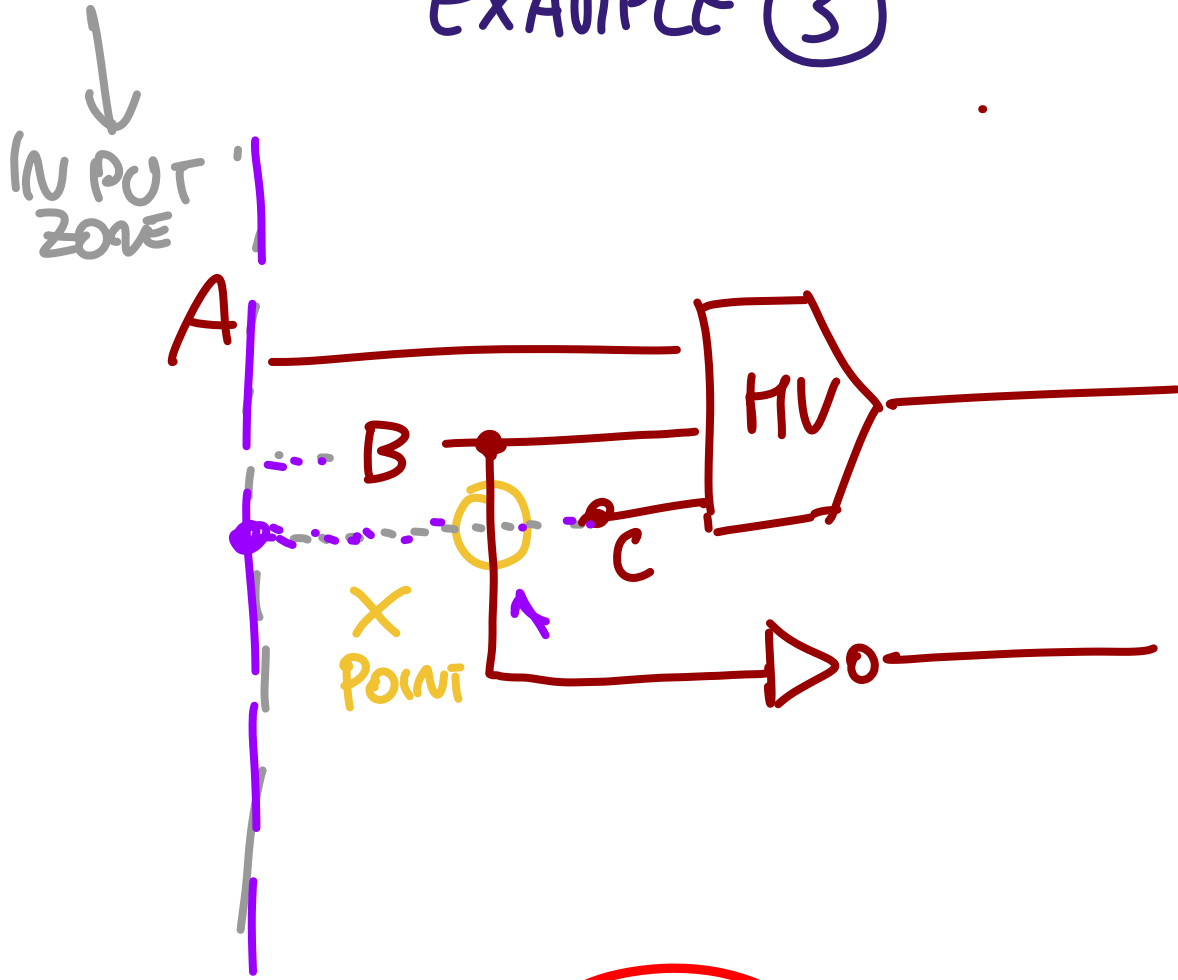
LAYOUT = TIMING

PAY ATTENTION TO SKEW / DESKEW NETS.



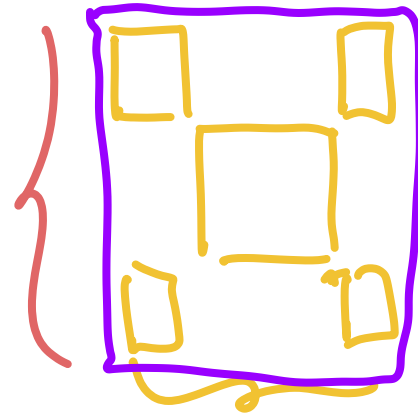
skewing

EXAMPLE (3)

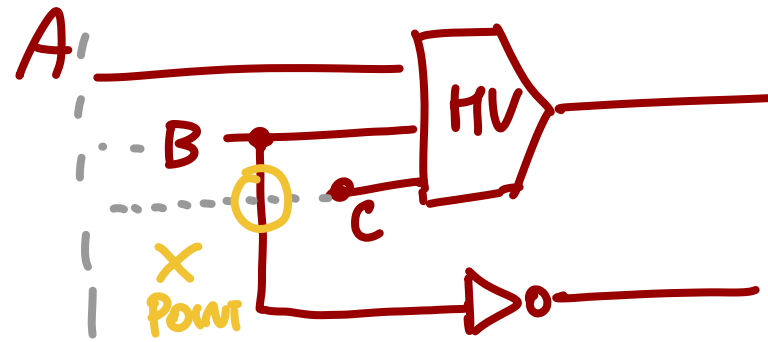


- COMPENSATE LATENCY (SKEW)

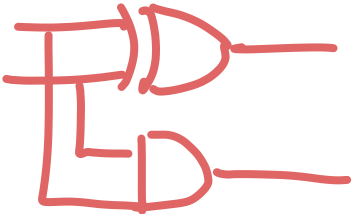
- USE CROSSWIRE



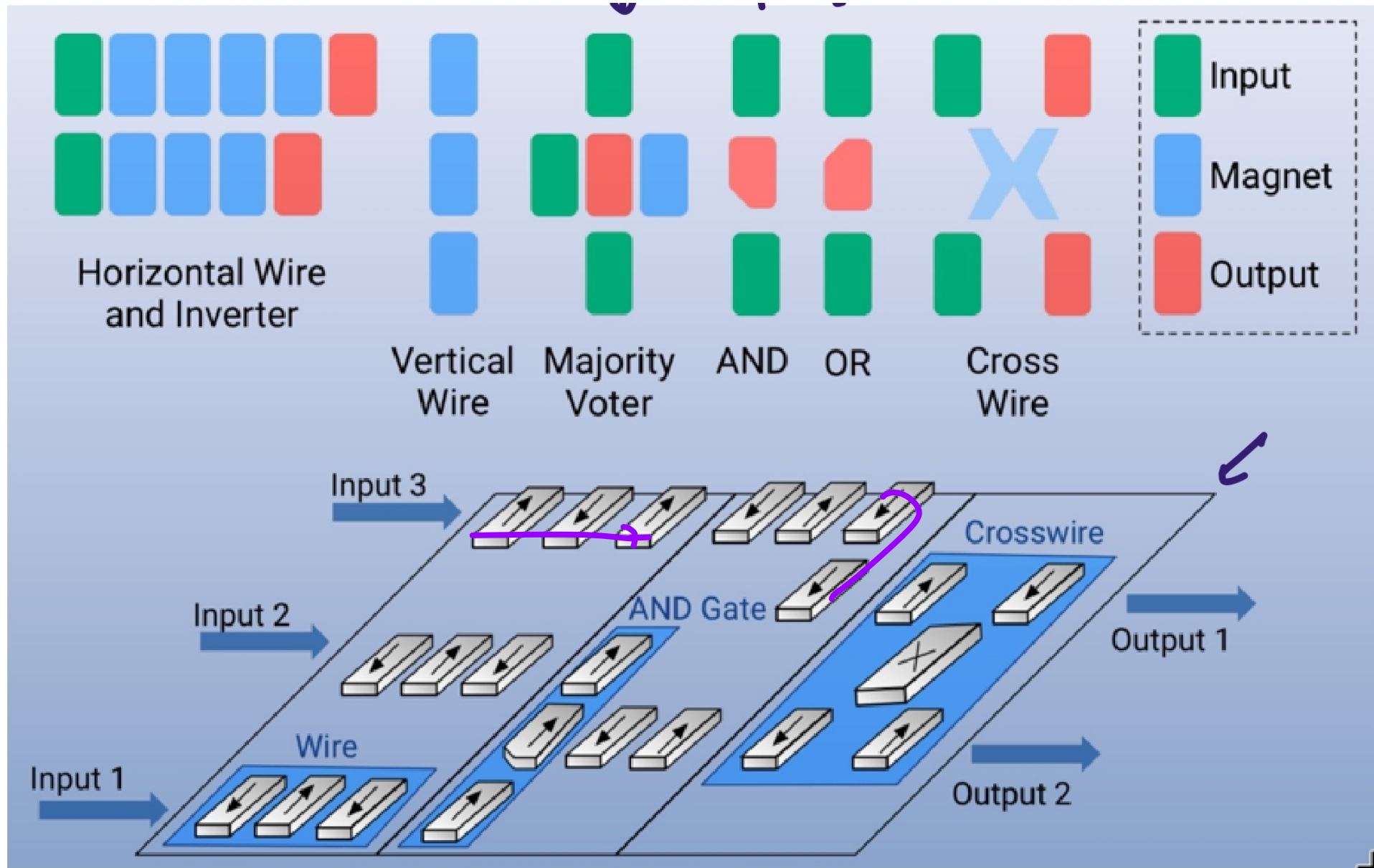
4 MAGNETS



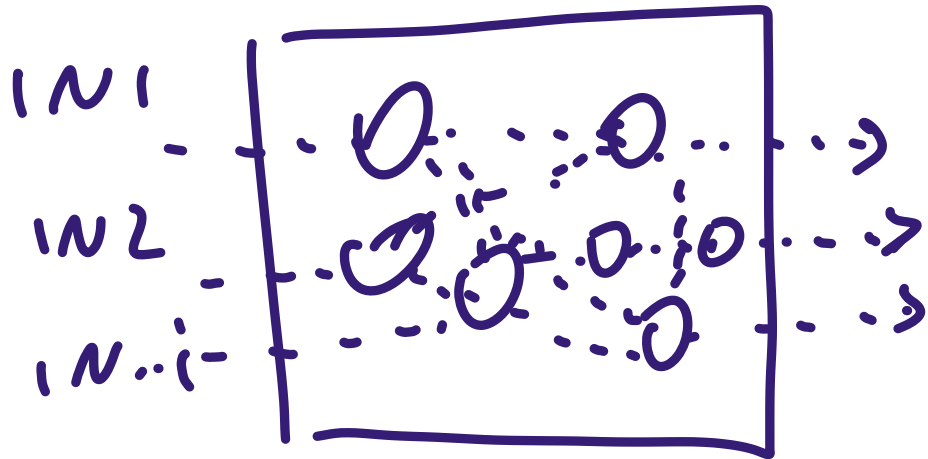
EXAMPLE (EXERCISES)

- ④ HALF-ADDER
H.A.
- 
- 4.1 WITH M.V.
4.2. WITH CUT
MAGNETS
- ⑤ FULL-ADDER (FA) USING 2 H.A.
- ⑥ 3 bits RIPPLE-CARRY-ADDER (RCA)
WITH INPUT FROM SAME ZONES

SCALING UP TO BIG CIRCUITS

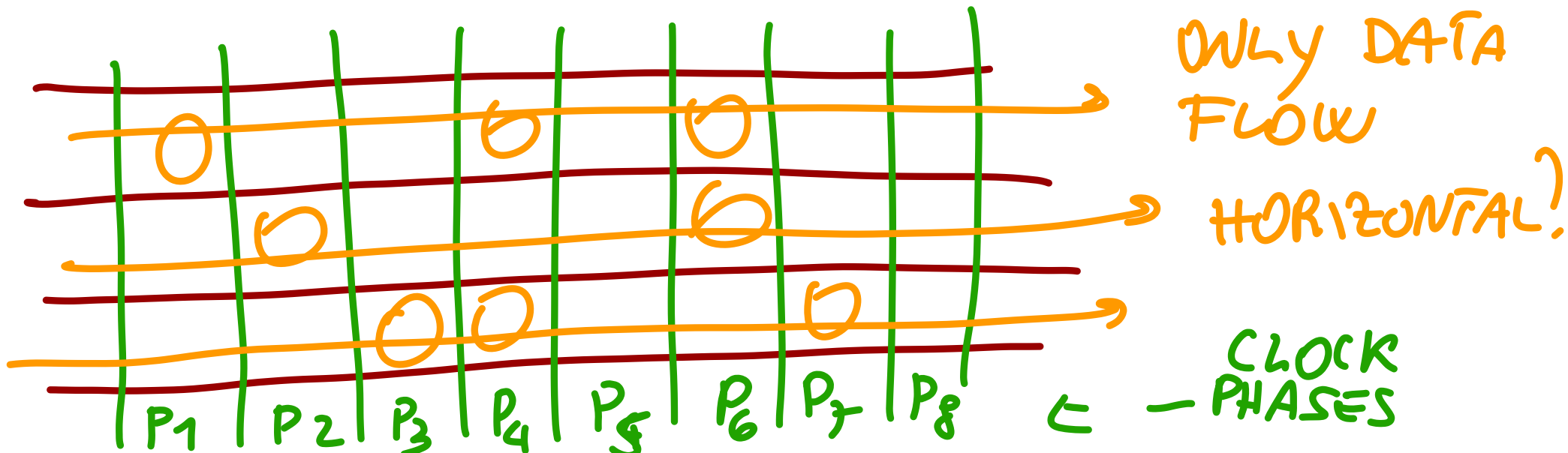


IN A STANDARD CIRCUIT

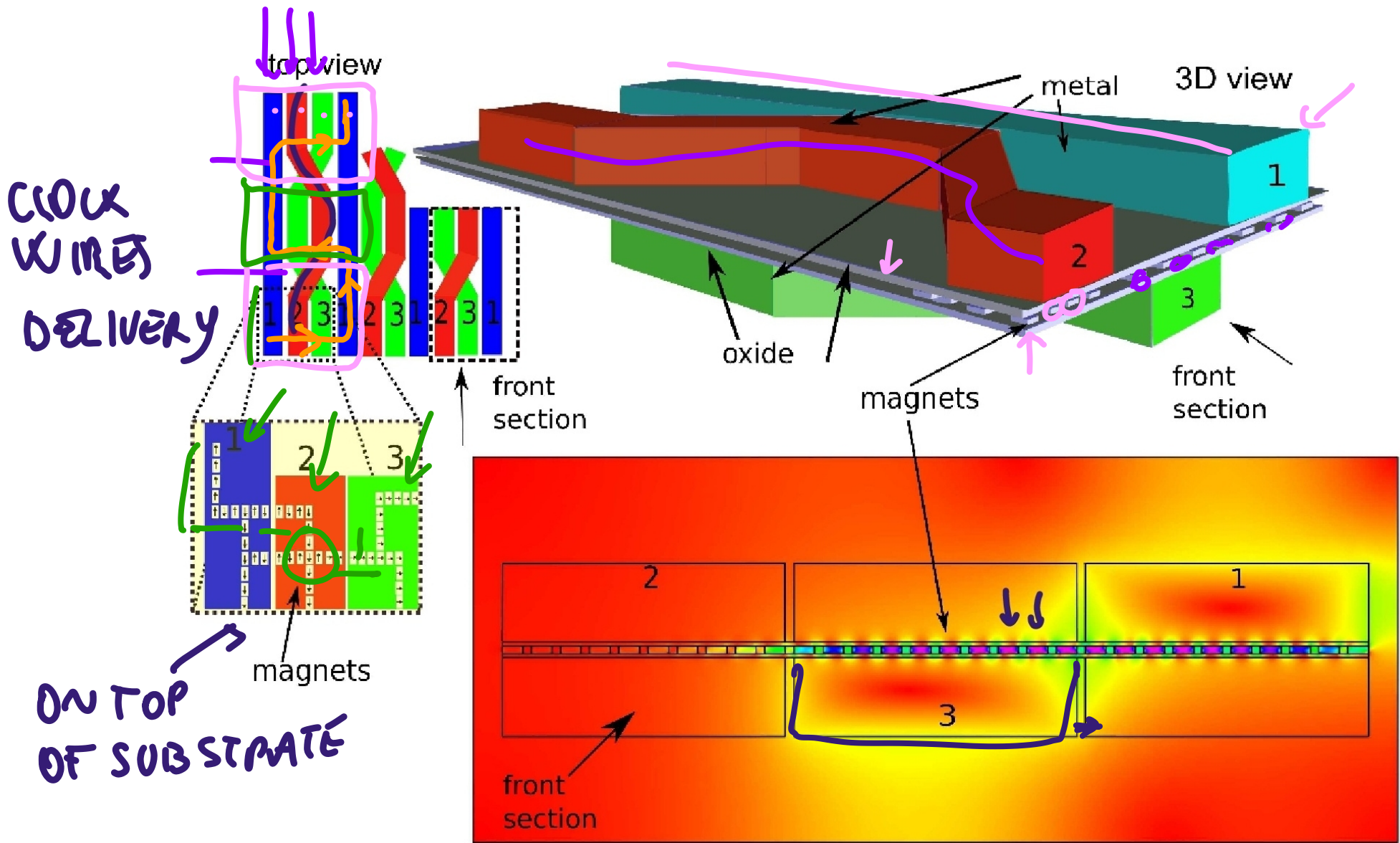


INFORMATION PROPAGATES
IN ALL DIRECTIONS
(NO α , WE HAVE 20
METAL LAYERS...
EASY GATE)

WHAT IN 1-NHL?

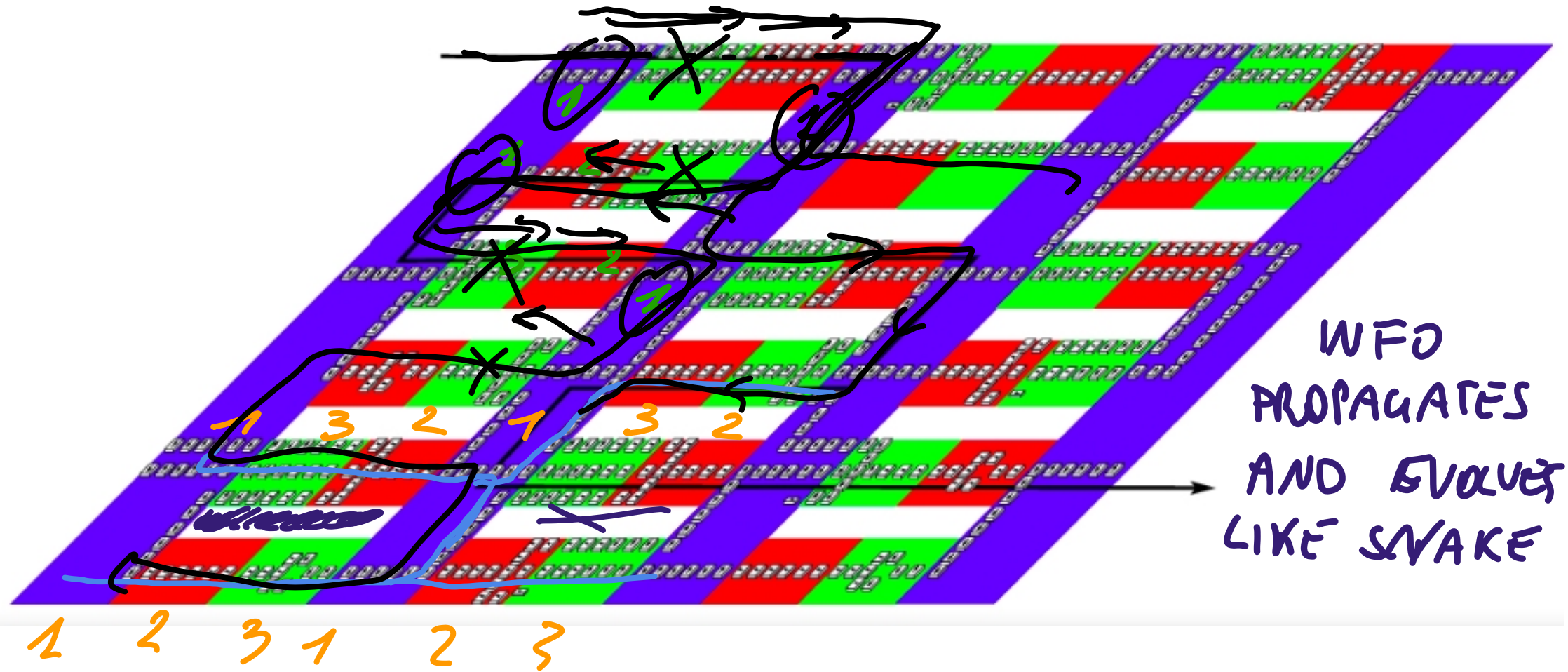


HOW TO DELIVER CLOCK IN BIGGER CIRCUITS : SNAKE CLOCK



→ Comsol Multiphysics simulation - clock distribution

A POSSIBILITY: SNAKE CLOCK AS
EXAMPLE TO ADAPT A TECH. LIMIT TO...

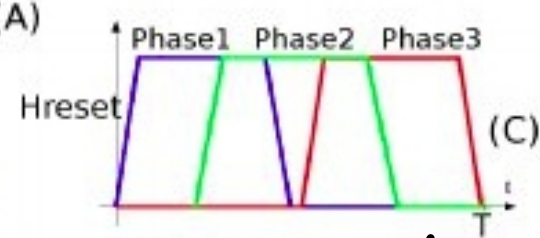
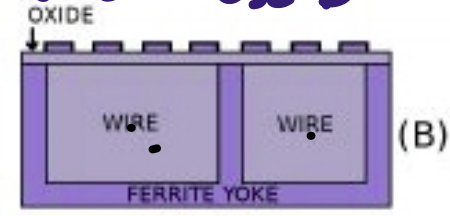
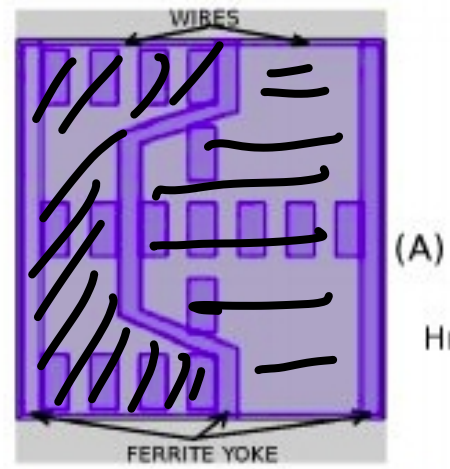


..... A REAL NECESSITY: BIGGER CIRCUITS
AND COMPLEX INFO PROPAGATION

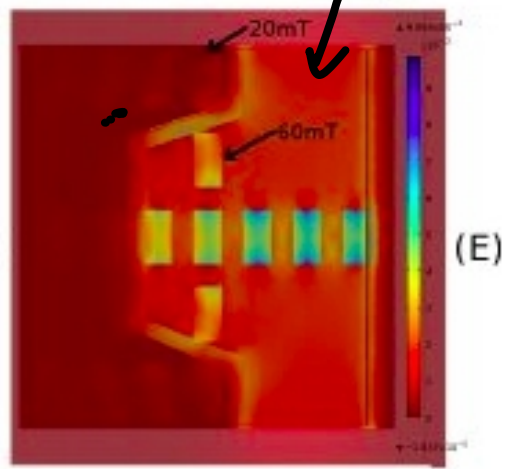
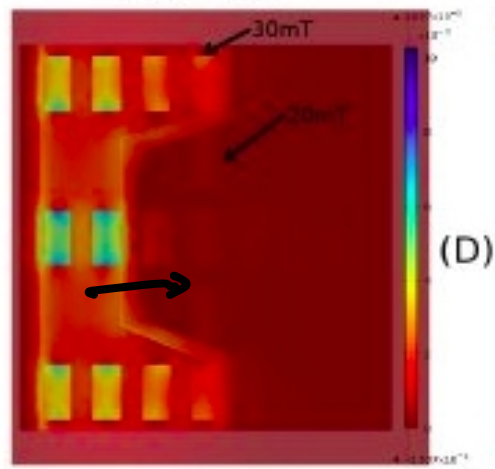
FEM ANALYSIS OF M.F. APPLIED

PHASES PARTIALLY SUPERPOSED

Control mutation impact on magnets of applied make clock

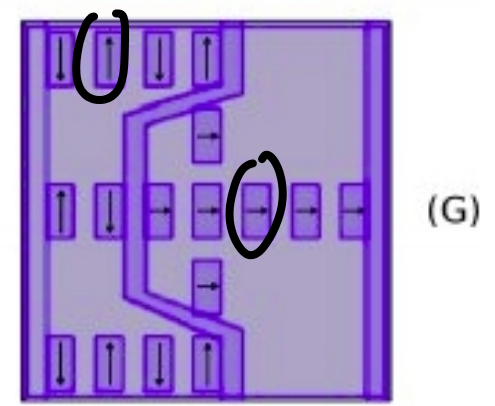
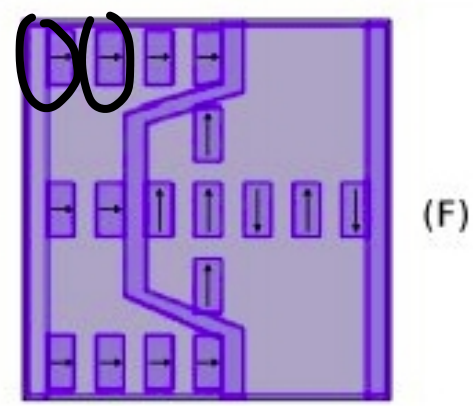


RESET APPLIED TO PHASE 1



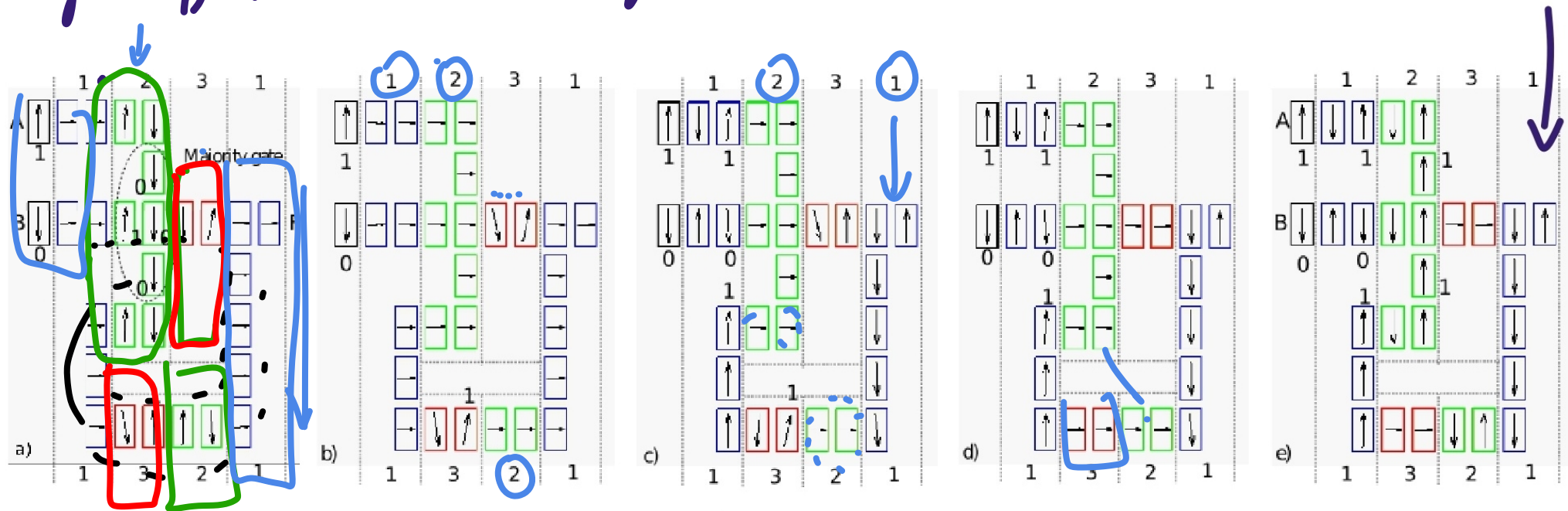
RESET APPLIED TO PHASE 2

MAGN. ALONG HARD AXIS IN P. 1 EVAL IN P. 2



MAGN. ALONG HARD AXIS IN P2, INFO IN P. 1

HOW TO DESIGN GATES AND SIMULATE THEM logic gates micromagnetic simulations (MAGSIMS)



Micromagnetic simulations (MAGSIMS) of a LOGIC GATE
....

➔ Null Convention Logic: a solution to layout=timing constraint which is associated to NanoMGneticLogic intrinsic micropipelining

Here NCL-TH22 $F = AB + F(A+B)$

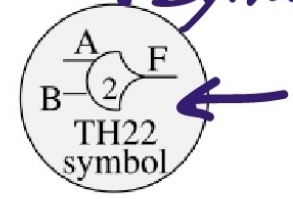
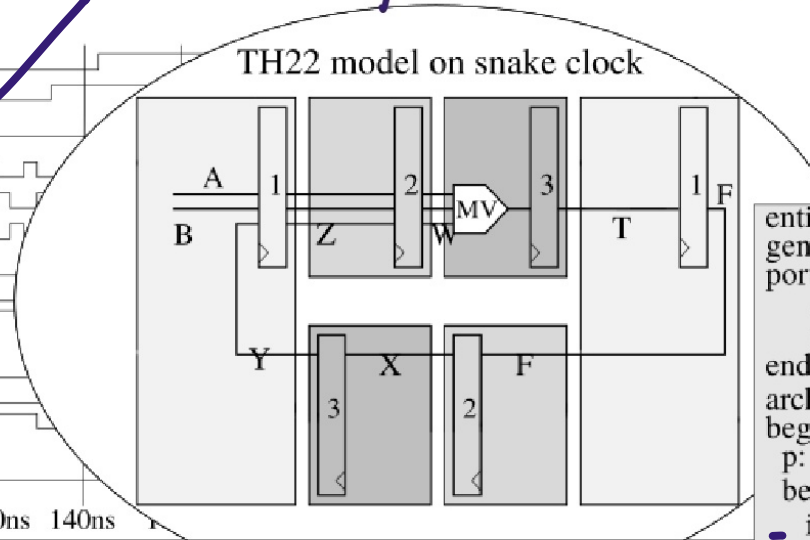
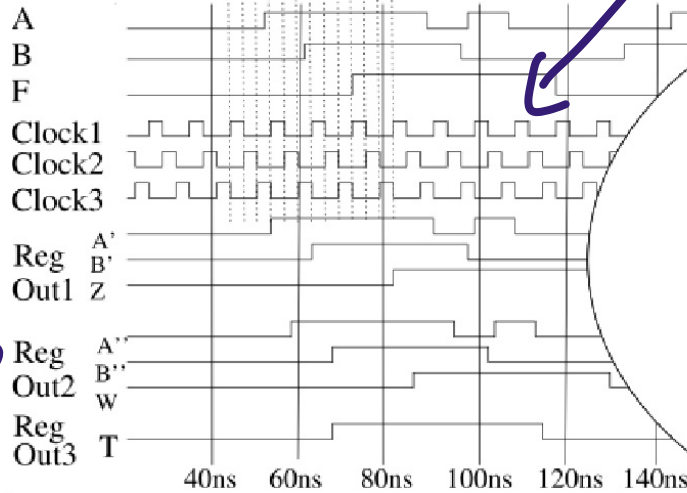
snake clock application, micromagnetic simulation in time

HOW TO DESIGN BIG CIRCUITS AND SIMULATE THEM

logic simulation

conceptual model

symbol



```
entity reg is
generic (nbit: integer :=32);
port (din: in std_logic_vector (nbit-1 downto 0);
      dout: out std_logic_vector (nbit-1 downto 0);
      reset, clock: in std_logic);
end reg;
architecture behav of reg is
begin
p: process (clock, reset)
begin
-- Register
if reset = '1' then
dout <= (others => '0');
elsif (clock'event and clock='1') then
dout <= din;
end if;
end process;
end behav;
```

```
entity TH22 is
port (A,B, clk1,clk2,clk3: in std_logic; F: out std_logic);
end TH22;
architecture behav of TH22 is
.....components declaration of MV and Register gates.....
signal MVO, T, P, X, Y : std_logic; signal Z, W : std_logic_vector(2 downto 0);
begin
R1 reg: generic map (nbit=>3) port map (din(0)=>A, din(1)=>B, din(2)=>Y, dout=>Z, reset='0', clk=>clk1);
R2 reg: generic map (nbit => 3) port map (din=>Z, dout=>W, reset = '0', clk=>clk2);
M1 mv: port map (a=>W(0), b=>W(1), c=>W(2), y=>MVO);
R3 reg: generic map (nbit => 1) port map (din=>MVO, dout=>T, reset = '0', clk=>clk3);
R4 reg: generic map (nbit => 1) port map (din=>T, dout=>P, reset = '0', clk=>clk1);
R5 reg: generic map (nbit => 1) port map (din=>P, dout=>X, reset = '0', clk=>clk2);
R6 reg: generic map (nbit => 1) port map (din=>X, dout=>Y, reset = '0', clk=>clk3);
F<=P;
end behav;
```

TH22 VHDL model

```
entity mv is
port(a,b,c: in std_logic);
end mv;
architecture behav of mv is
begin
y <= (a and b)or(a and c)or(b and c);
end behav;
```

VHDL model of TH22

RISC PROCESSOR SIMULATED

+

BIOSEQUENCE PROCESSOR DESIGNED

& SIMULATED



IT WORKS

~ 400 MHz

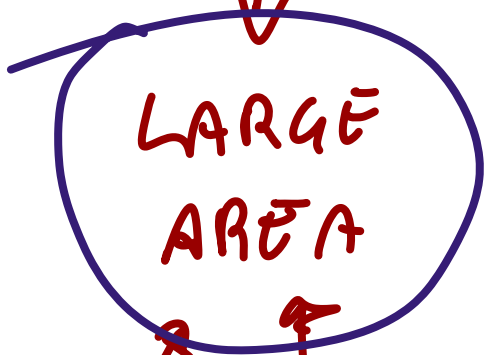


ARCH. TECHNIQUES
USED TO SOLVE

NO
MULTILAYER
YET



LARGE
AREA

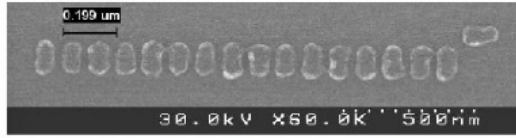


NO LEAKAGE
BUT

POWER FOR CLOCK
DUE TO

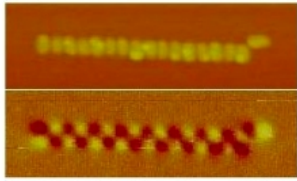
LESSONS LEARNED!

EXAMPLES



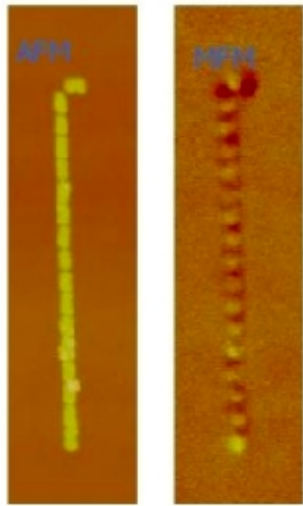
SEM

WIRE

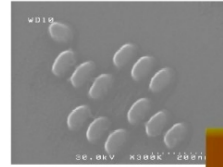


AFM

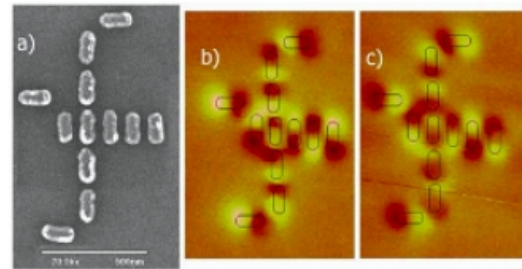
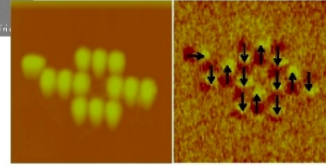
MFM



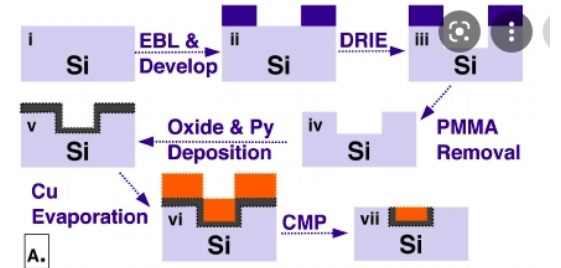
WIRE



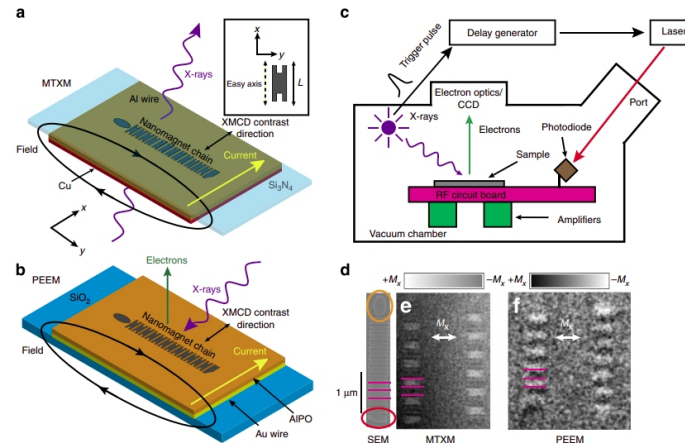
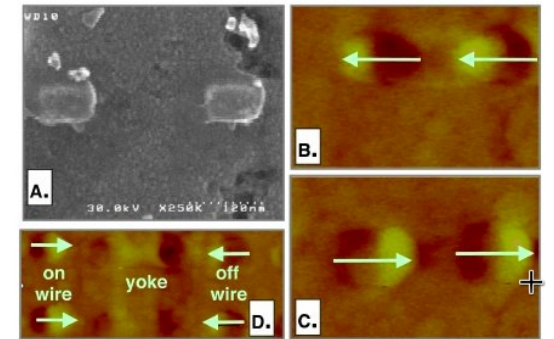
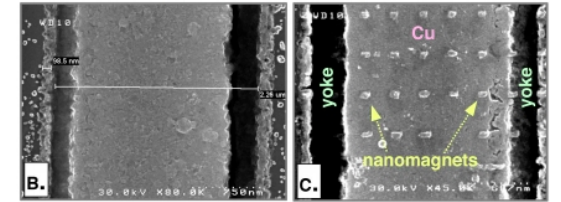
INV



MV

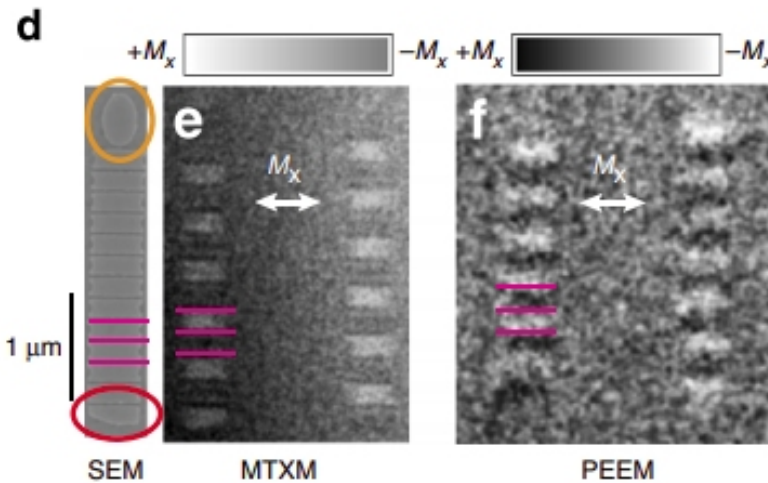
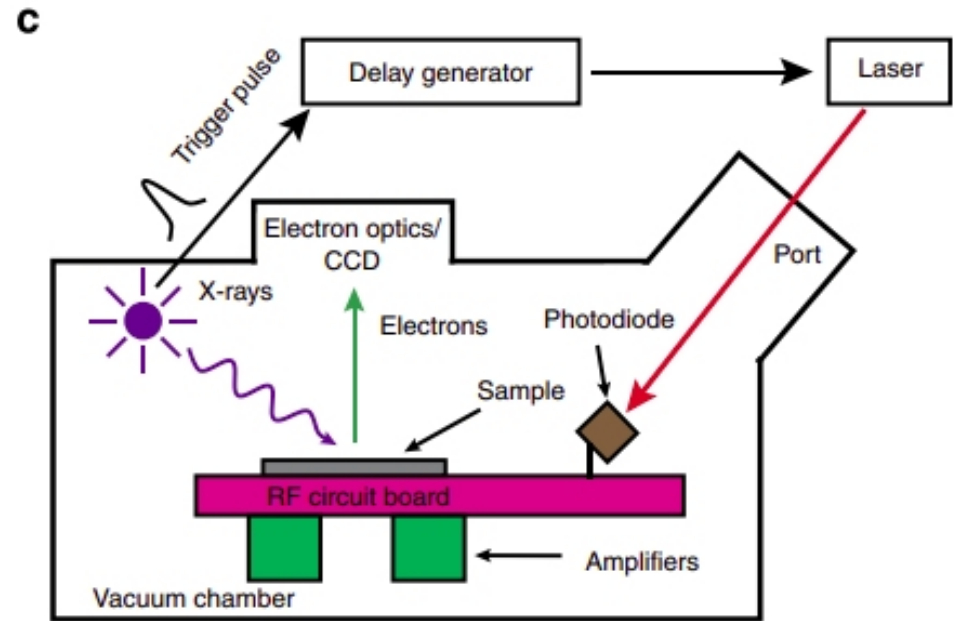
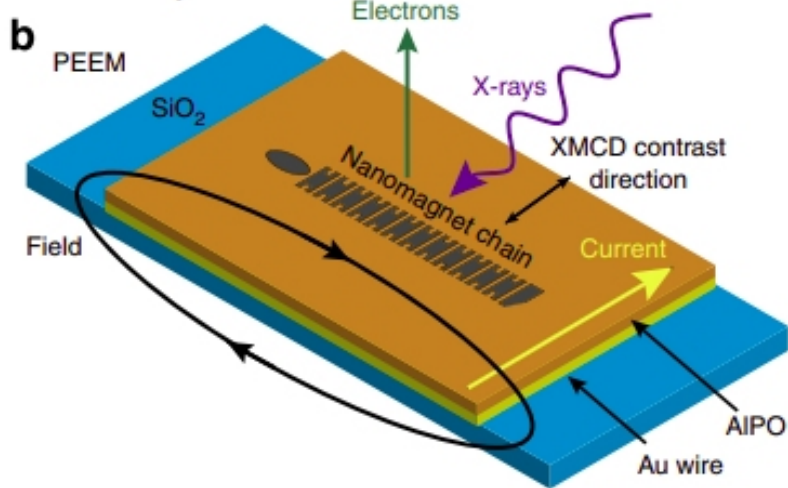
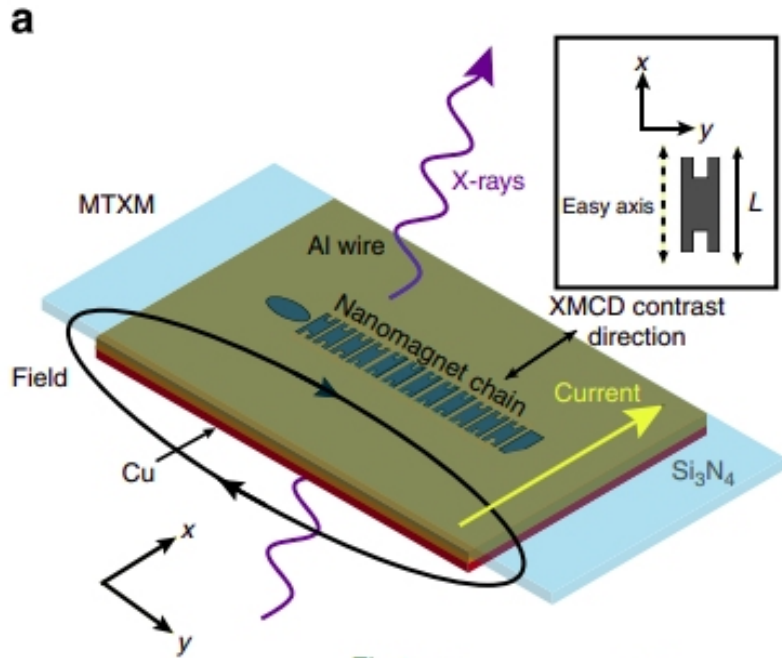


CLOCK

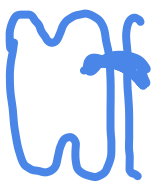


very recent (20)
picosecond switching
observed!

RECENT DEMONSTRATION OF SUBNANOSECOND SIGNAL PROPAGATION IN UCL

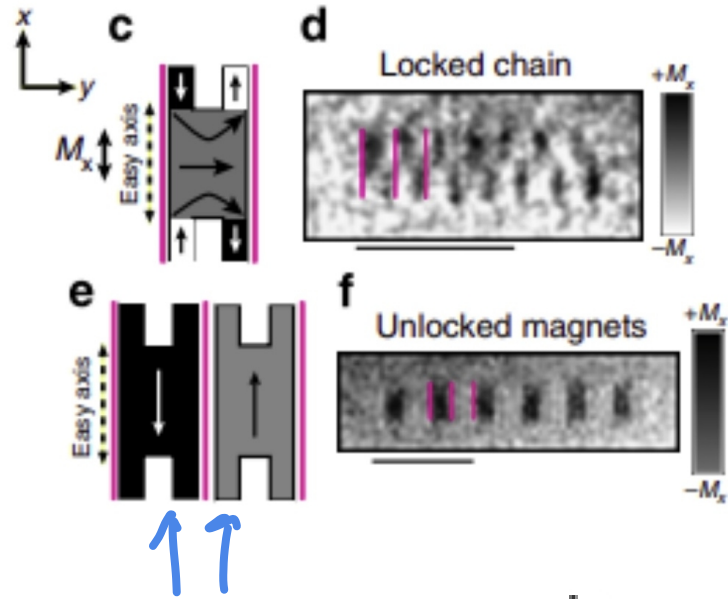


DOI 10.1038/ncomms557466



MODIFIED SHAPE

OBSERVED EVOLUTION OF SWITCH PROPAGATION



100ps per SWITCH
 ⇒ 5GHz
 2π rad / PHASE
 4 MAG → 2.5 GHz

