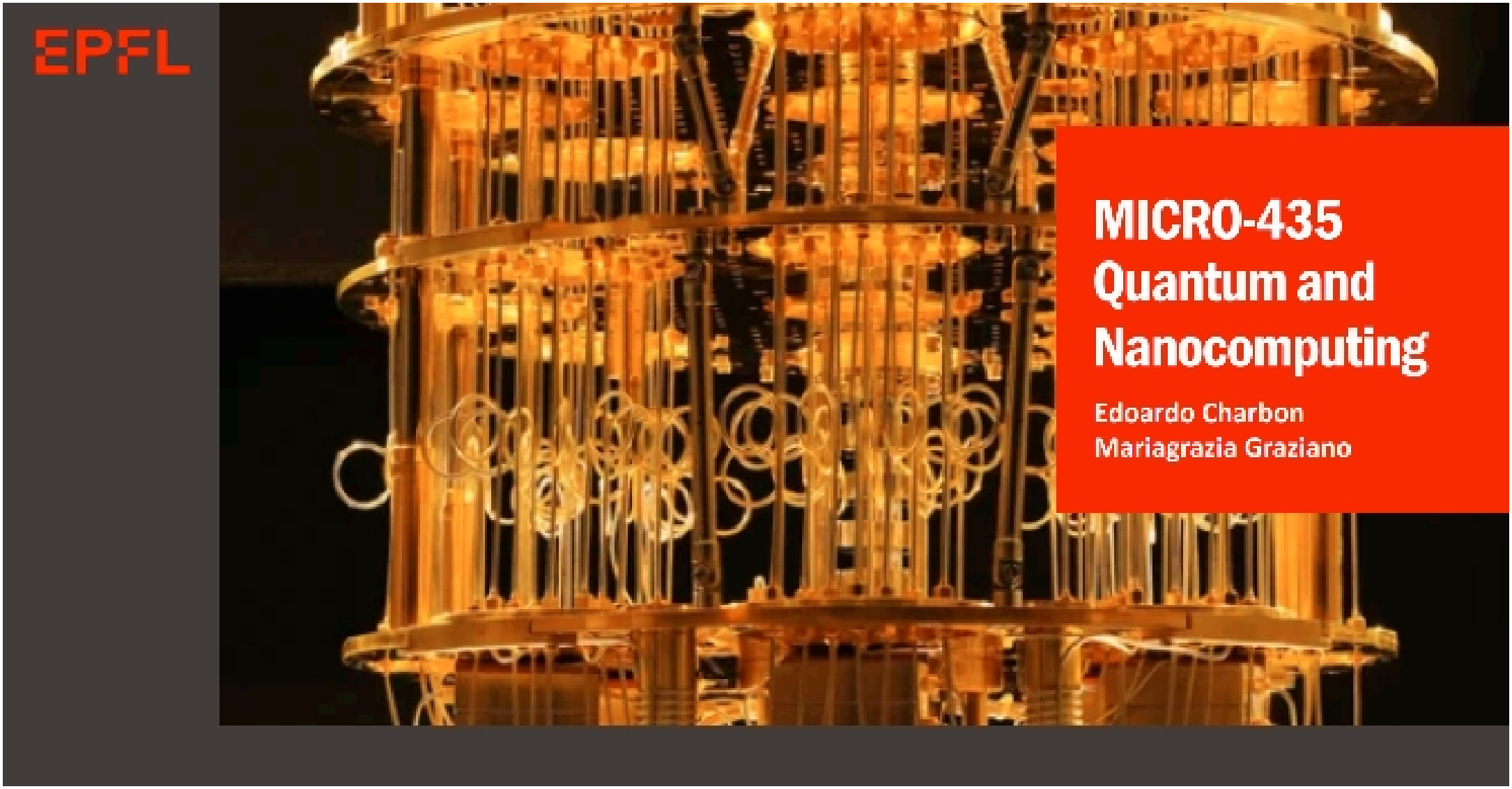


CIRCUITS BASED ON MT

CIRCUITS BASED ON MT

OBJECTIVES

a) → – SIMPLE CASES

b) → – ARRAY BASED LOGIC CIRCUITS

– OTHER ELEMENTS

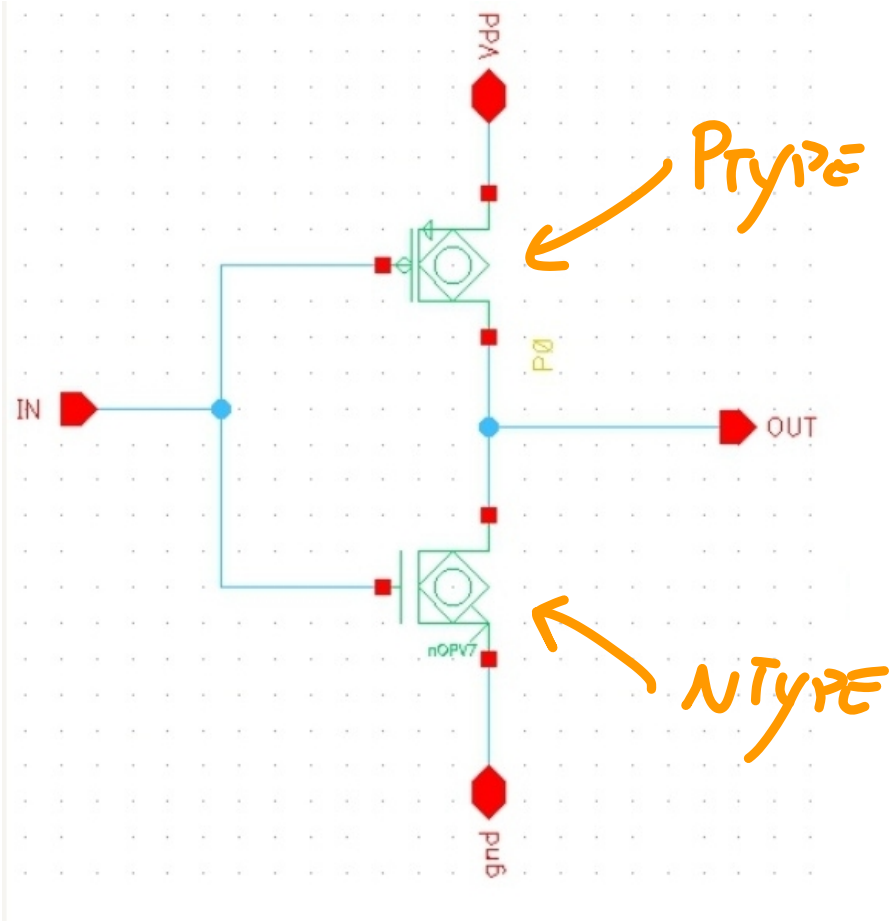
MEMORY ELEMENTS

NEURONS

SENSORS

OPTIONAL

USE OF MT FOR LOGIC COMPUTATION

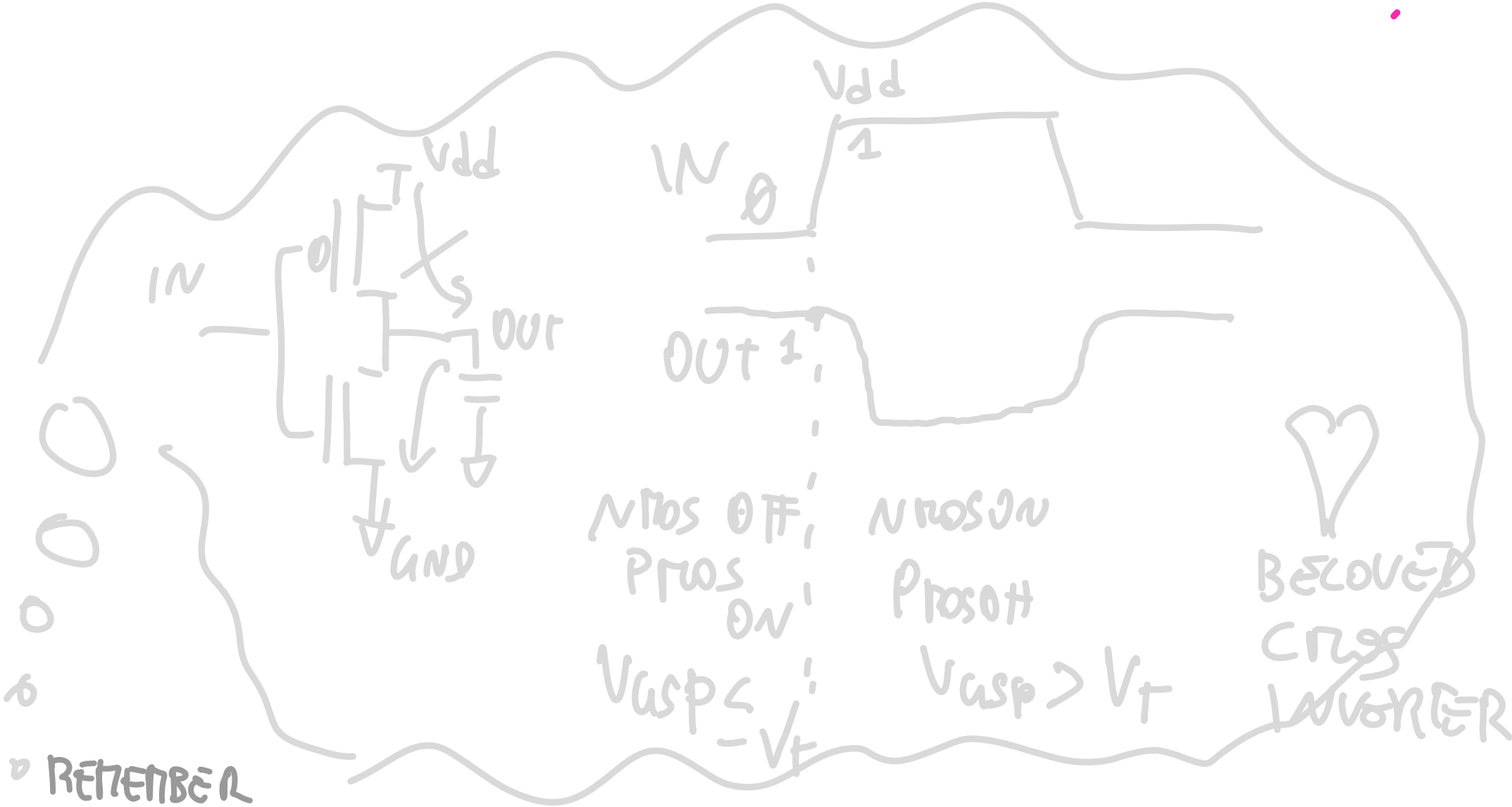


INVERTER

EVEN IF A M.T. WORKS CORRECTLY AND ASSURES GOOD CURRENT AND I_{ON}/I_{OFF} ALONE

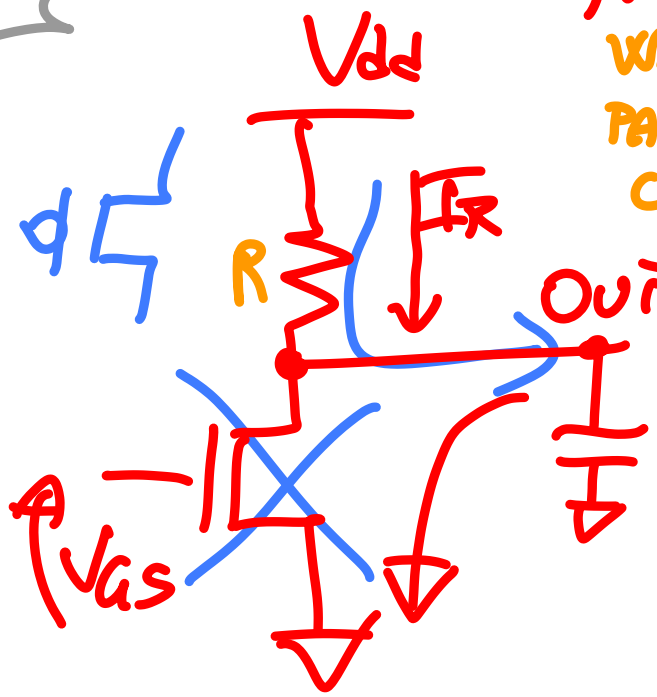
NOT NECESSARILY IT WORKS WELL IF CONNECTED TO OTHER M.T IN A LOGIC GATE

AN OLD GOOD FRIEND .... REMEMBER



- REMEMBER

... AND ALSO REMEMBER THAT ONCE UPON A TIME....
NMOS LOGIC ONLY COULD WORK - NO PMOS!



NMOS LOGIC
WAS COMMON IN THE PAST WHEN PMOS STILL COULD NOT BE FABRICATED

IF Vgs > 0
T. ON
Out → OFF

IF Vgs = 0
T OFF

POWER CONSUMPTION BECOUSE THE R IS ALWAYS "IN CONDUCTION"

COMPLEMENTARY BEHAVIOR WORKS WELL, LET'S KEEP IT!

How to Design & Simulate a MT. Logic Gate?

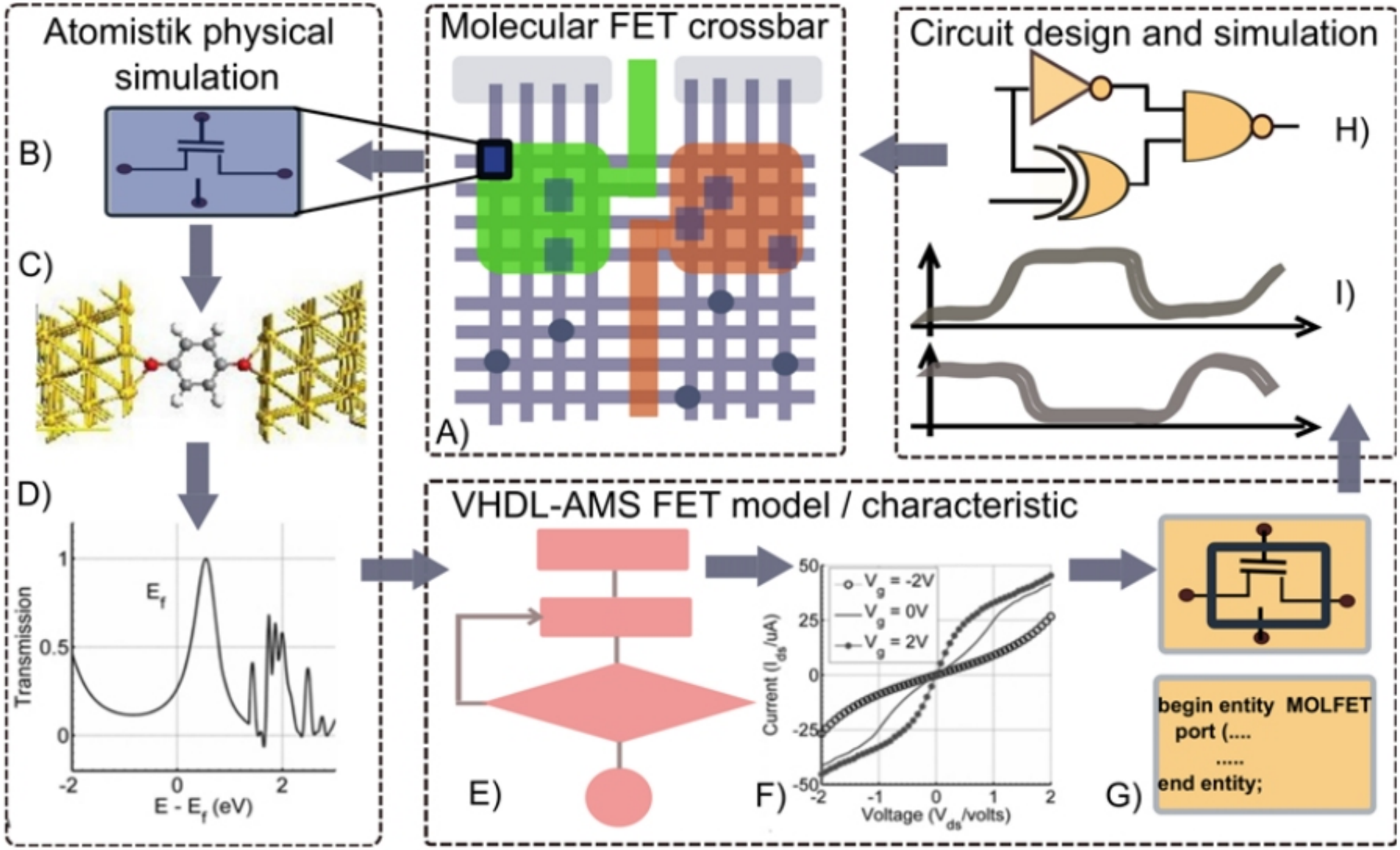
→ Quantum ATK and EEBESD are not suitable

→ In standard tech

→ Schematic entry

→ Each TR. has a symbol and a tech model

A METHOD FROM DEVICE PHYSICAL SIMULATION TO CIRCUIT DESIGN AND FUNCTIONAL VERIFICATION



credit Ali Zahir © POLITO

```
ENTITY MOLFET IS
Generic (----);
Port(-----);
End Entity MOLFET;
ARCHITECTURE behav OF MOLFET IS
--Declaration of Quantities
begin
-- DL_SCF (discrete molecular level- self consistent
field) function call.
I == DL_SCF(EF,E0,U0,G1,G2,A,V,VG1,VG1_back);
END ARCHITECTURE behav;

--- Function DL_SCF is defined in a package
FUNCTION DL_SCF (EF,E0,U0,G1,G2,A,Vds,Vg,Vg_back:REAL)
RETURN REAL IS VARIABLE Ids:REAL;
----Variable Declarations----------
---- Here all the variables used in the code are
declared
BEGIN
-- self consistent calculations--
G  := G1+G2; UL1 := -A*Vg; UL2 := -A*Vg_back; UL :=
UL1+UL2;
E1 := E0+UL;  F0 := 1.0/( 1.0 + exp((E0-EF)/KT));
N0 := 2.0 * F0;                    -- number of electrons
U1 := EF - ((1.0 - VDF)*Vds); U2 := EF + VDF*Vds;
while dU > 1.0e-6 loop
E1 := E0+Uscf+UL;       --- New molecular energy levels
F1 := 1.0/( 1.0 + exp((E1-U1)/KT));
F2:= 1.0/( 1.0 + exp((E1-U2)/KT));
N := 2.0*((G1*F1)+(G2*F2))/G;    -- Electron population
Uc := U0*(N-N0);                 -- SCF energy
dU := ABS(Uscf - Uc);
Uscf := Uscf + 0.1*(Uc-Uscf);
end loop;
-- shifting of transmission function--
 TQ_SHIFT = shift(TQ,N_SHIFT)  -- function for
calculating the shift in transmission function
-- calculating current--
for i in 0 to 100 loop
F11(i):= 1.0/(1.0+exp((E(i)-U1)/KT));
F22(i):= 1.0/(1.0+exp((E(i)-U2)/KT));
FT(i):= F22(i)-F11(i);
SUM1:= SUM1+ (TQ_SHIFT(i)*FT(i)); SUM := dE*SUM1;
Ids := (2.0*Q*Q/H)*SUM;
end loop;
-----------------------------------------------
RETURN Ids;
END FUNCTION DL_SCF;
```

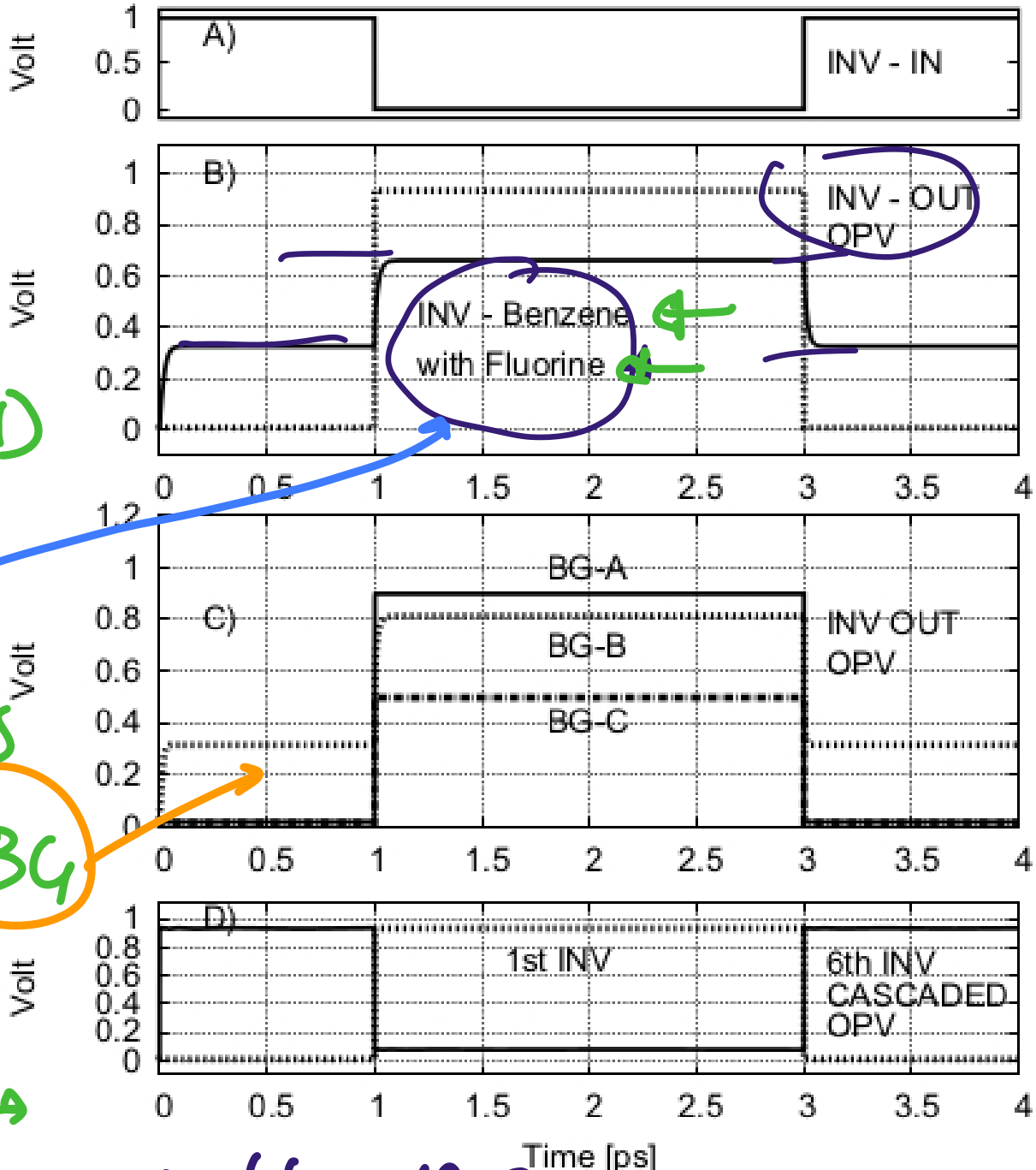
VHDL-AMS INCLUDES THE SCF LOOP

EEBESD METHOD

THE LANGUAGE IS USED TO DESCRIBE THE CIRCUIT AND AT EACH STEP, AND FOR EACH TRANSISTOR THE MODEL IS CALLED, THE SCF LOOP IS SOLVED FOR EACH CONDITION

VHDL-AMS SIMULATION OF GATES BASED ON BENZENE AND DIFFERENT ANCORING GROUPS AND DIFFERENT V_{BG}

6 CASCADED INV →



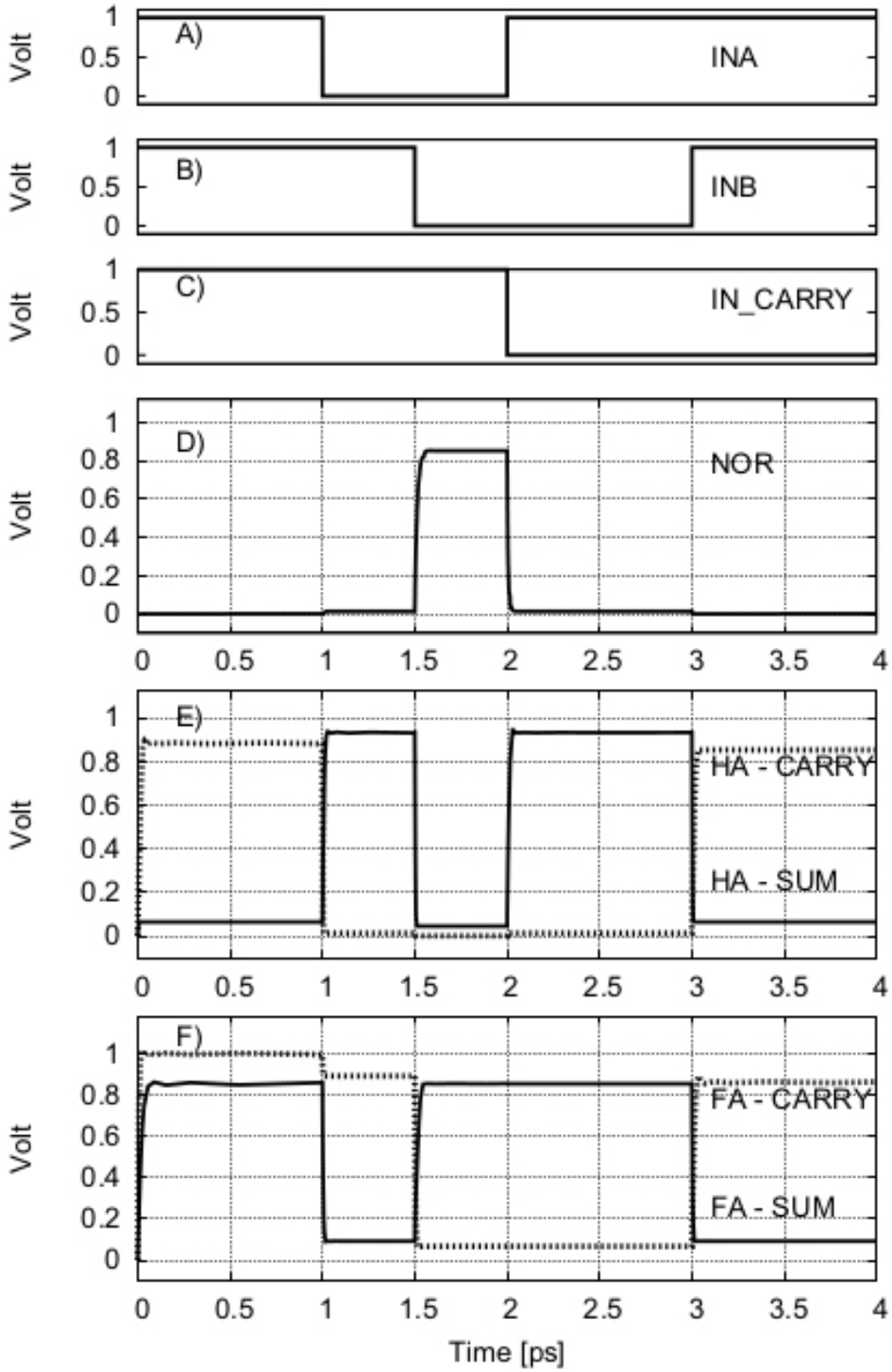
INV

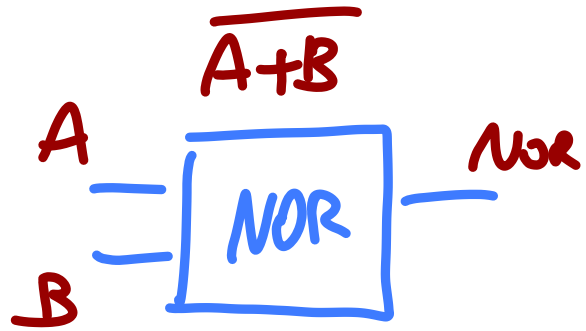
INV

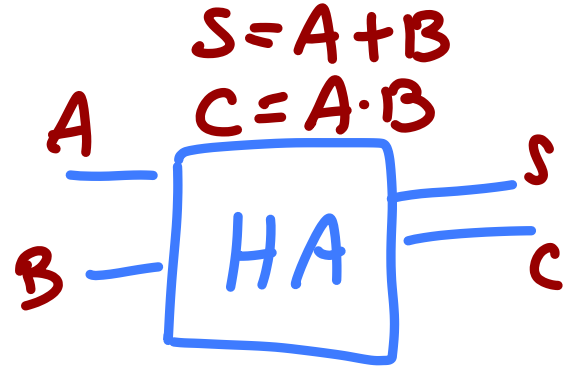
IN

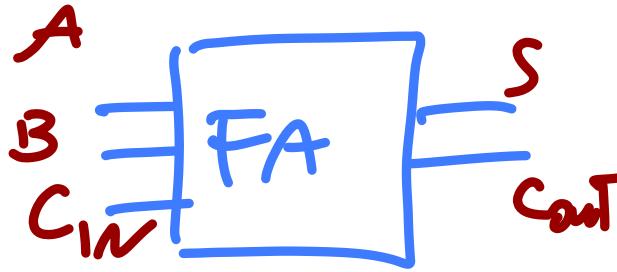
Credits : Ali Zahir

SAME METHOD ADOPTED FOR OTHER GATES









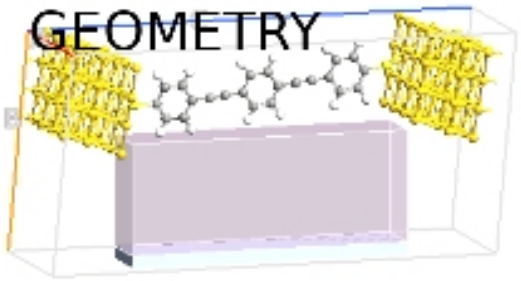
FROM PHD THESIS ALI ZAHIR. IEEE NANOARCH.

See in a next slide the T. Table

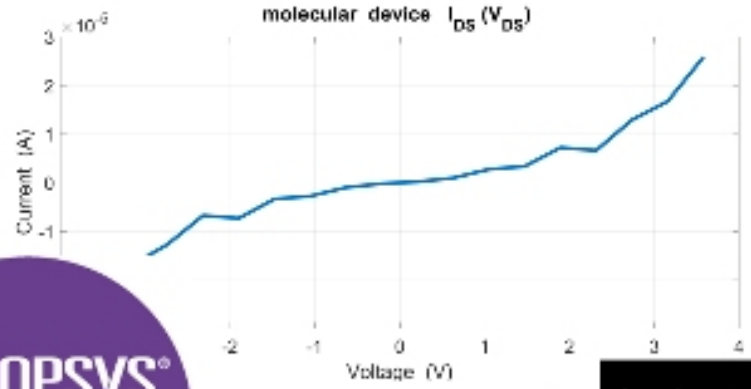
AN EVOLVED RECENT METHOD NOT BASED ON VHD-AMS

DESIGN & METHODS

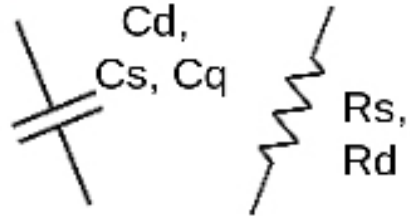
DEVICE GEOMETRY



Current-Voltage characteristics



MATLAB



(For dynamic power and transient analyses only)

SYNOPSYS® QUANTUMATK

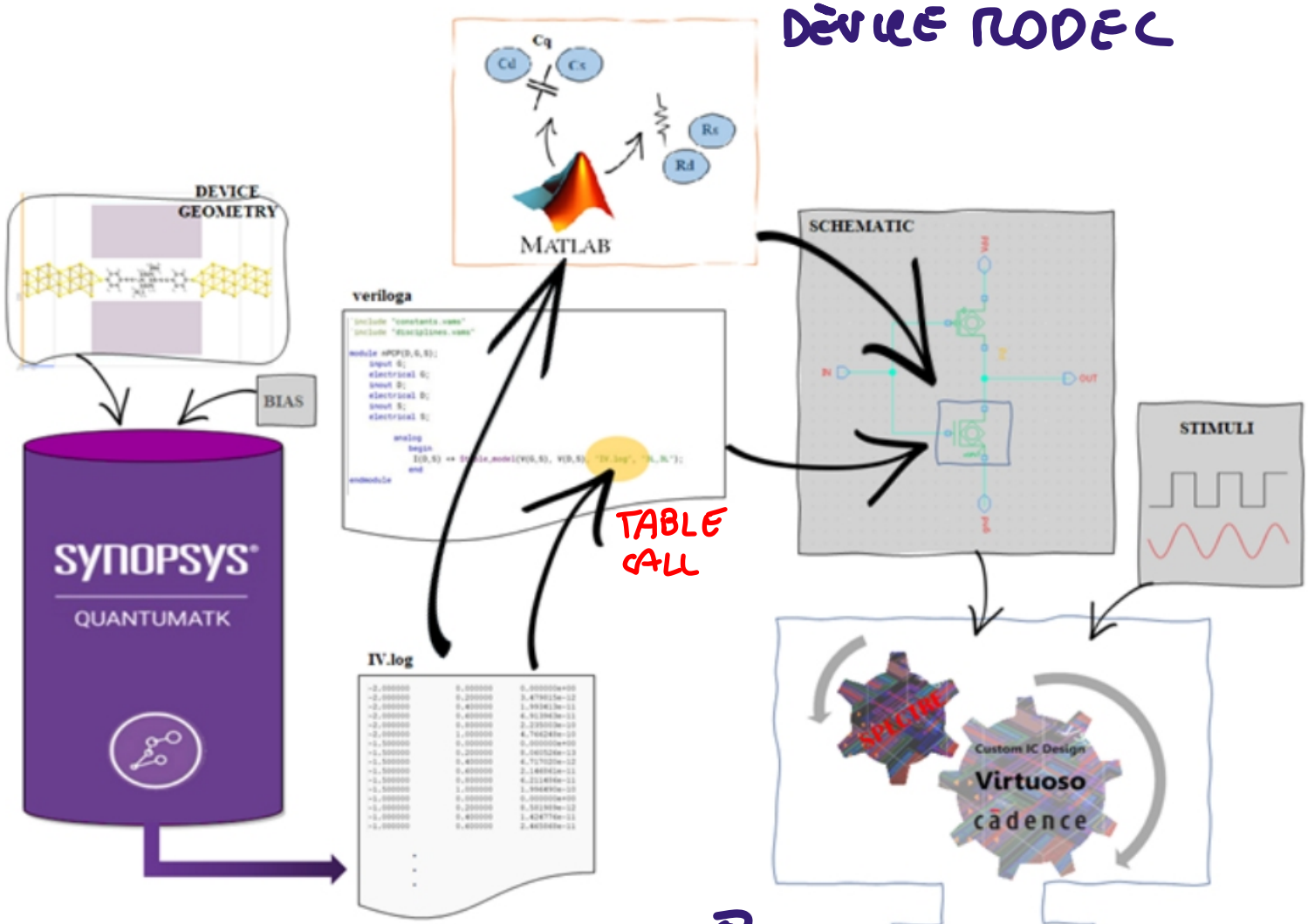
EHT + NEGF

$$I = \frac{2q}{h} \int_{-\infty}^{+\infty} T(E)\,[\,f_1(E) - f_2(E)\,]\,dE$$

Applied Voltages

LUT – BASED CIRCUIT

DEVICE MODEL



DEVICE PHYSICS

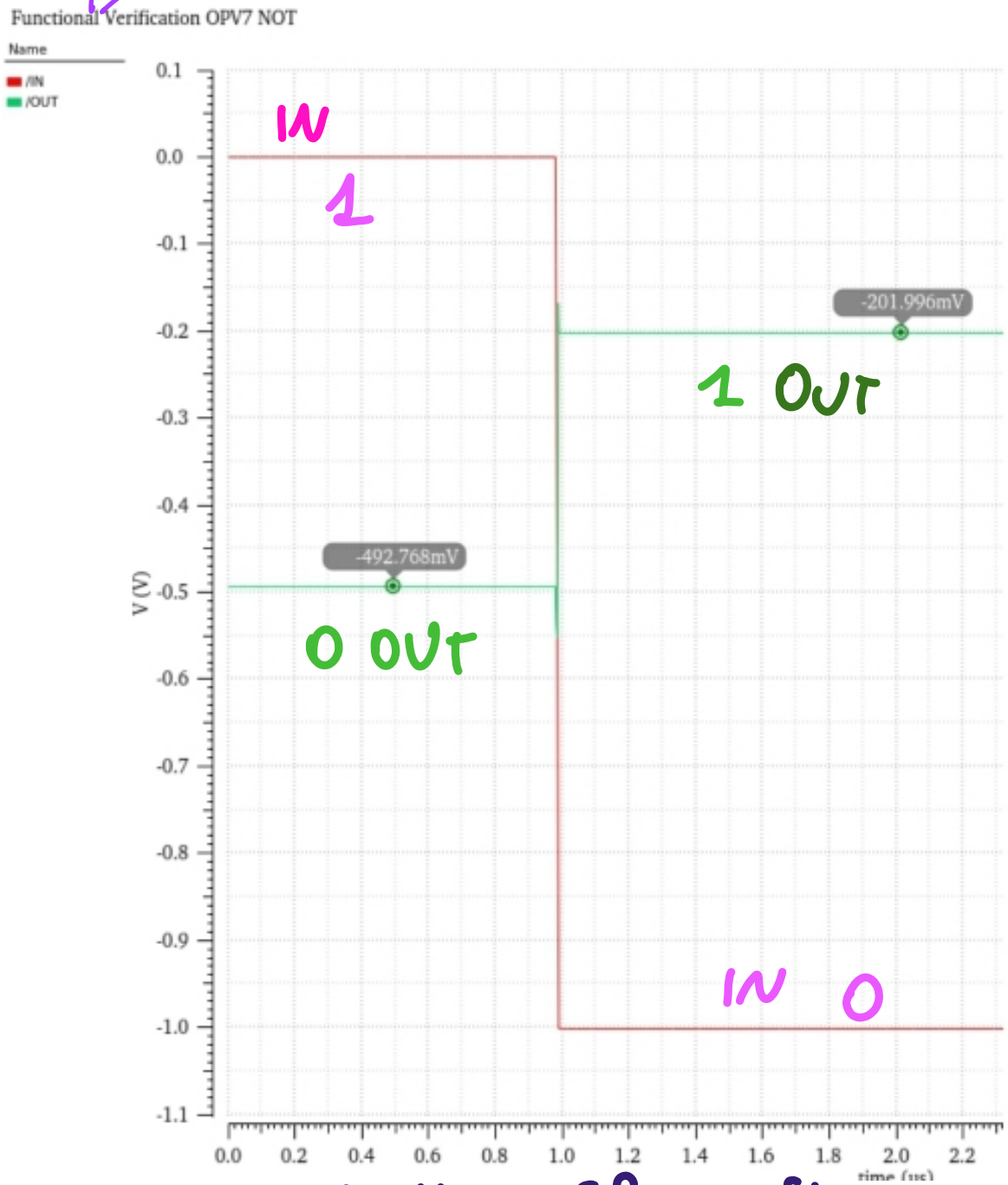
DEVICE MODEL

Geoh'ts Chiou Spano Fabrizio Ro

Paper accepted under consolitous

© IEEE TRANS. NANOELECTRONICS

IN OUT OPV7 INVERTER SIMULATION



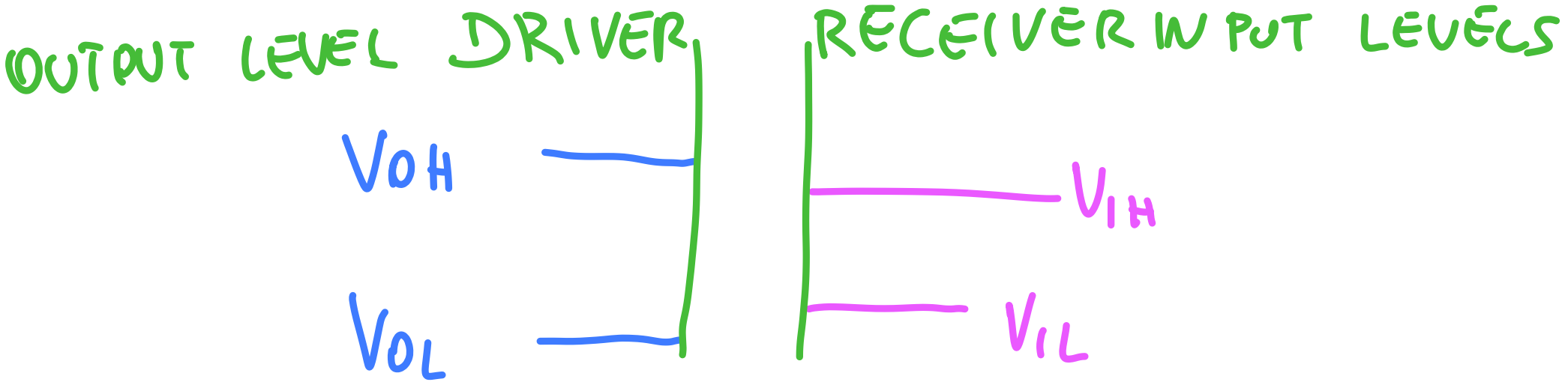
- BASED ON CADENCE VIRTUOSO
- VERILOG-A MODEL OF THE M.T.

- LOGICALLY IT WORKS CORRECTLY (INVERSION IS OK)

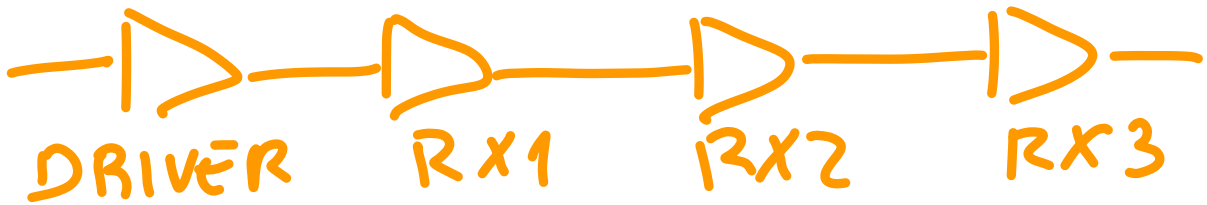
- FUNCTIONALLY IT DOES NOT VERY WELL.... WHY?

Credits : Chiara Sparo

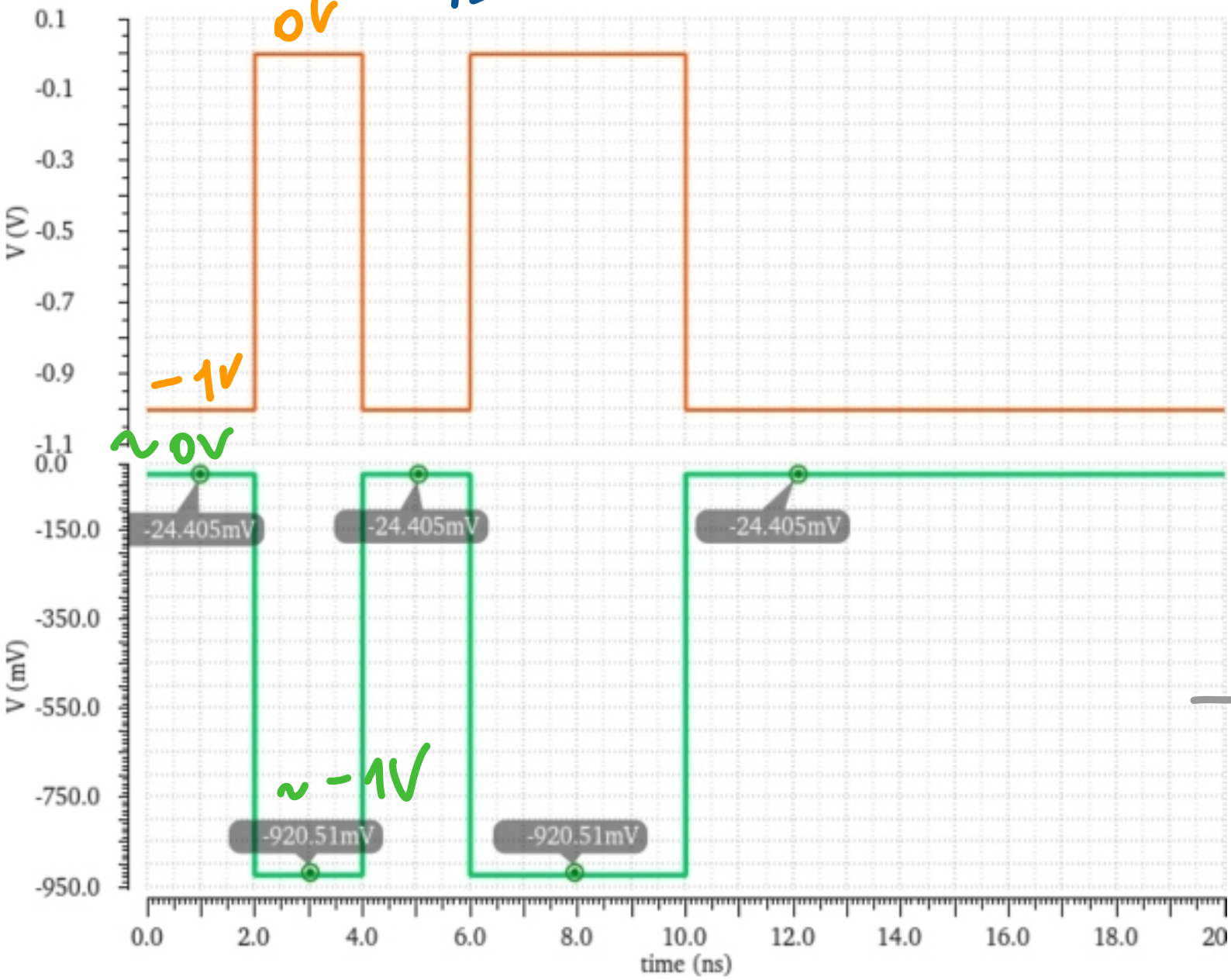
LOGIC INTERFACE



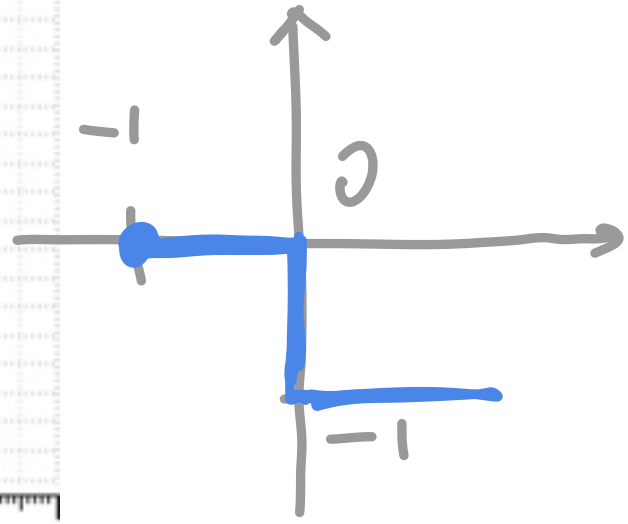
if the output levels reduce at each stage of receivers the logic values might not be recognized and only short chains work



2,2PCP INVERTER



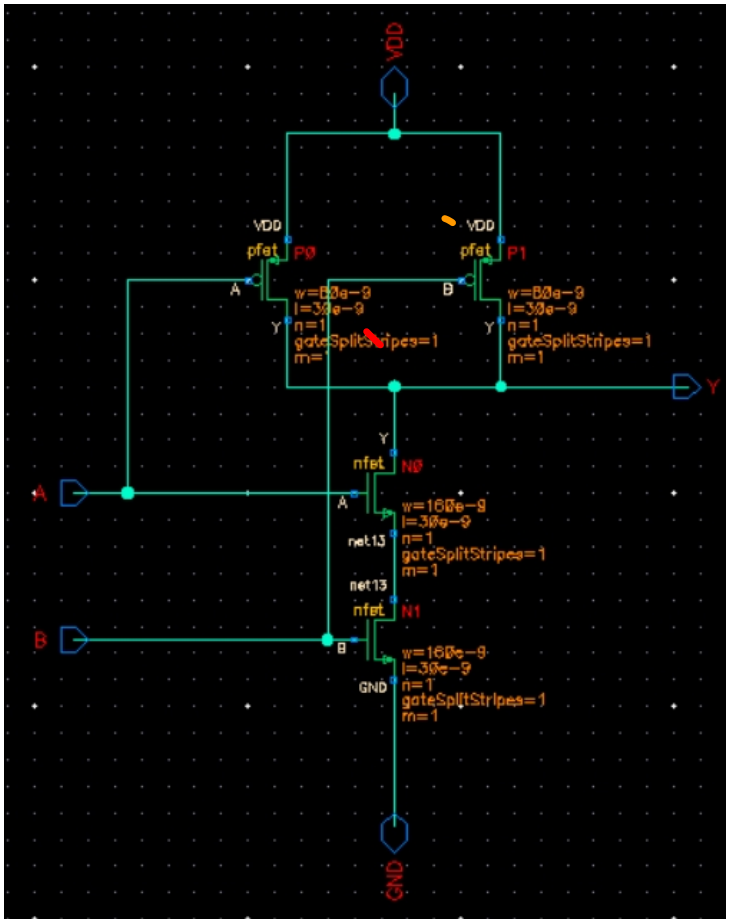
MUCH BETTER CHARACTERISTIC

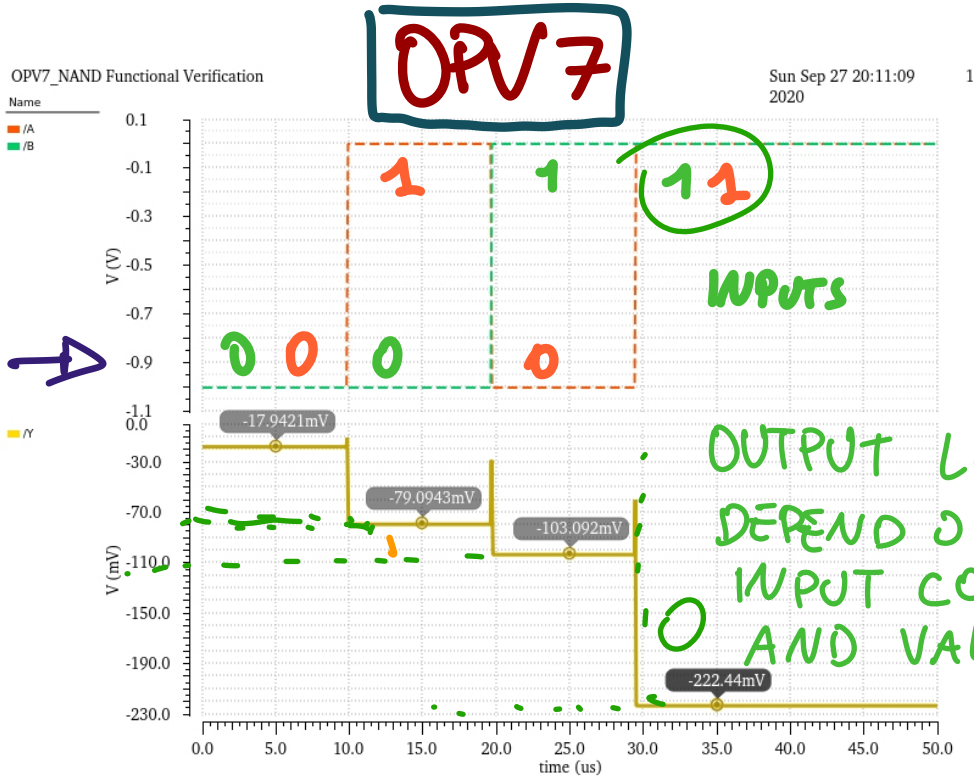


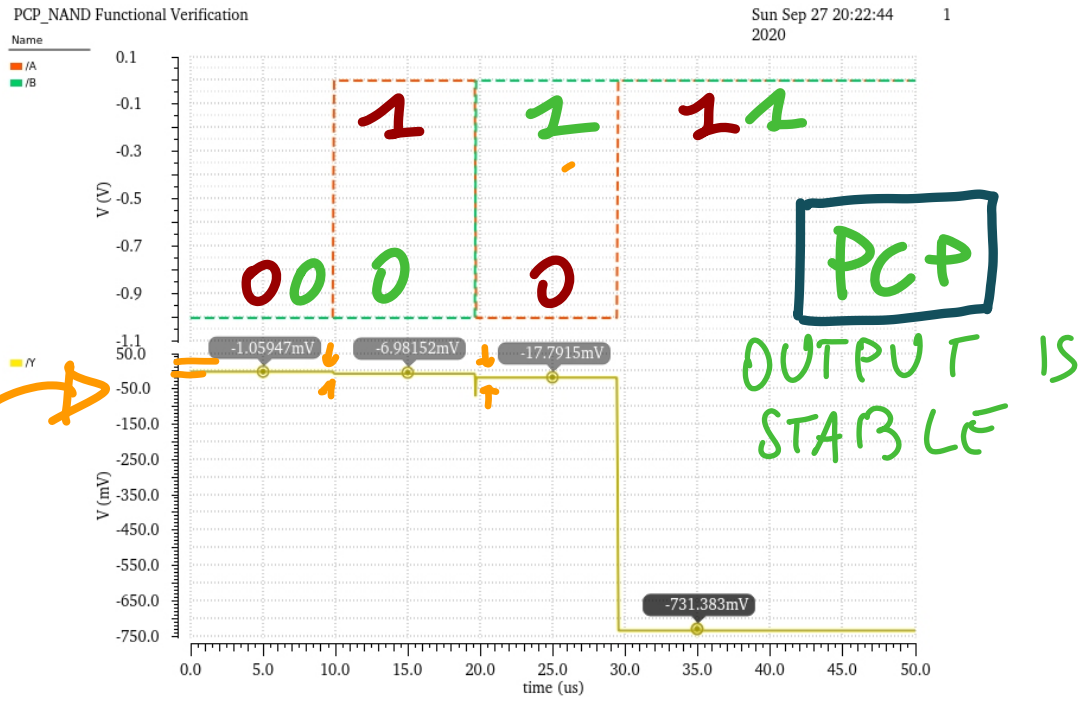
WE EXPECT THAT SEVERAL STAGES CAN BE CASCADED

OPV7 & PCP COMPARISON

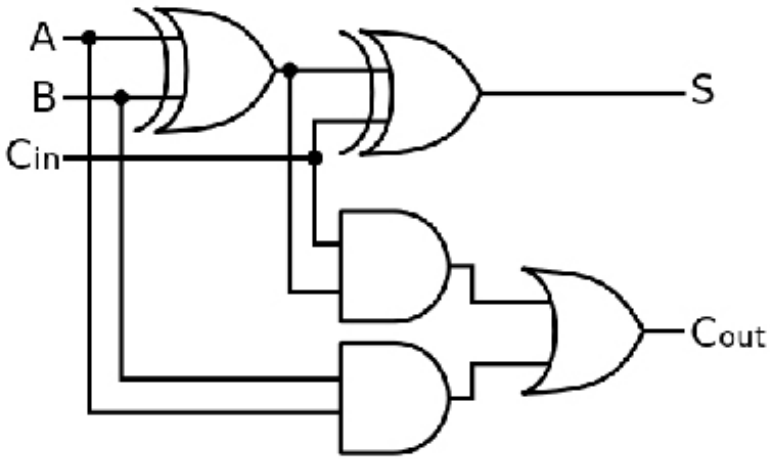
NAND $\overline{A \cdot B}$







FULL-ADDER

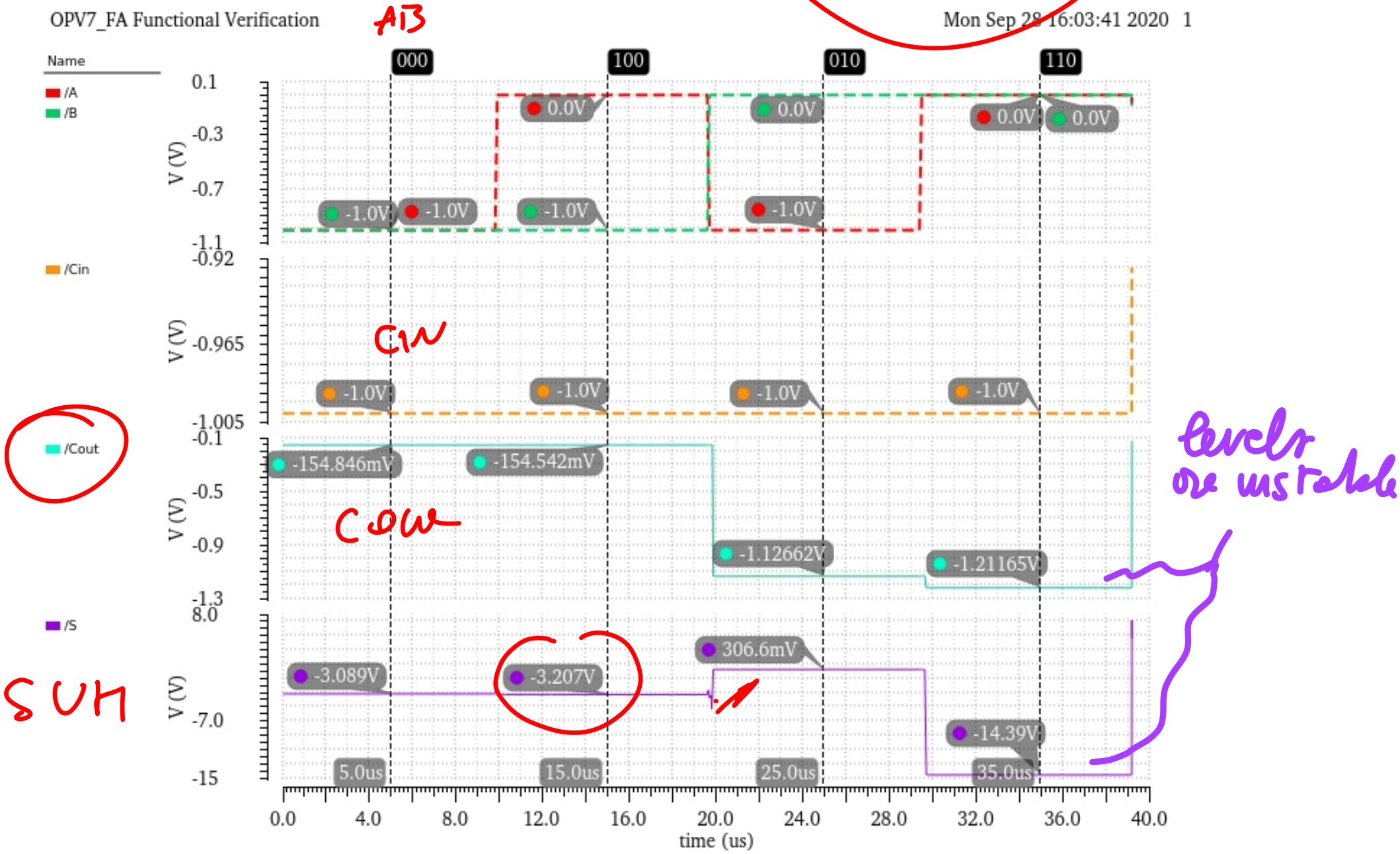


Full Adder				
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Very often it is considered a proof of promising behavior @ NANOCOMPUTING SCIENTIFIC COMMUNITY

FULL ADDER

OPV7



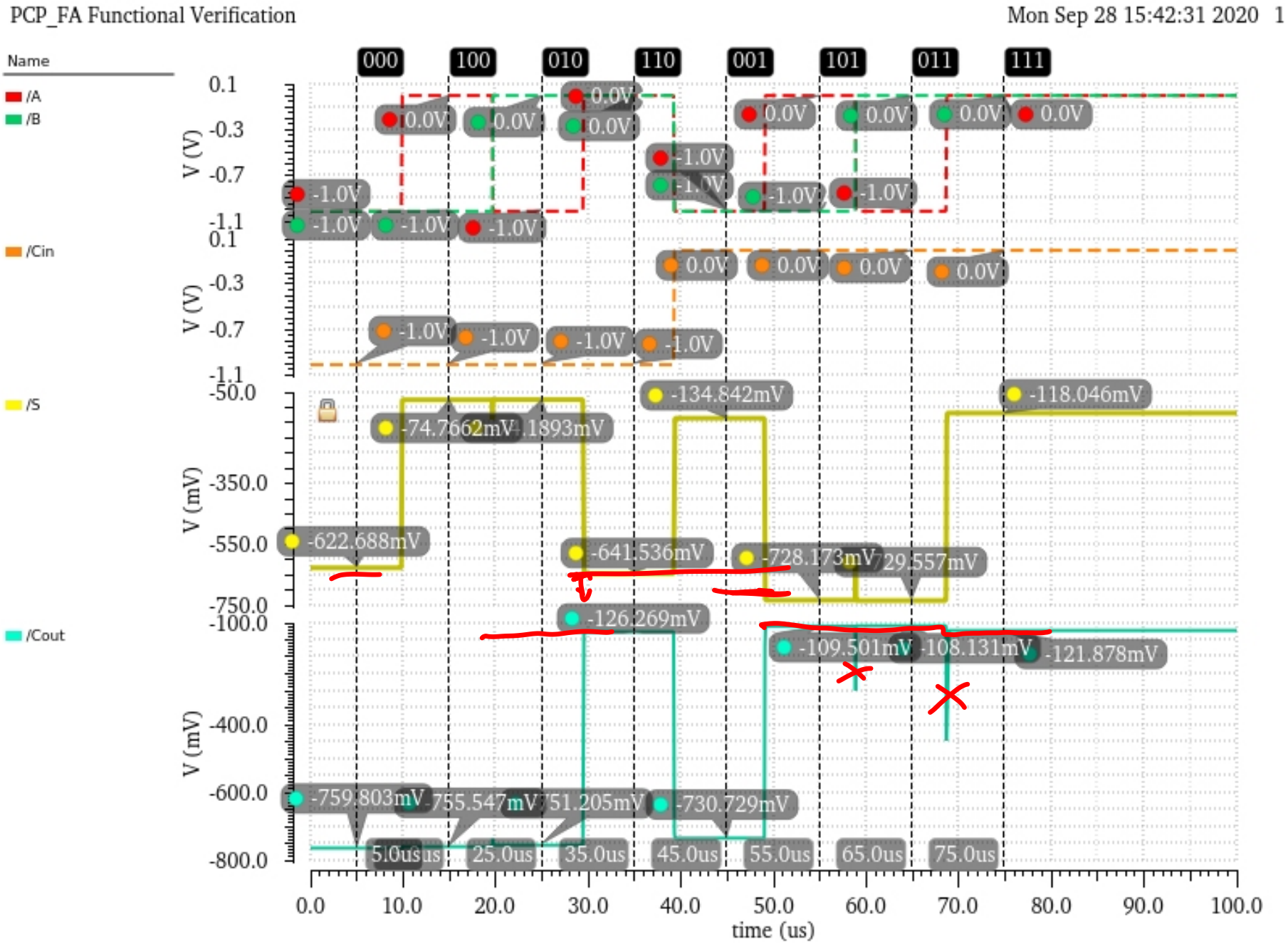
CIN

COUT

SUM

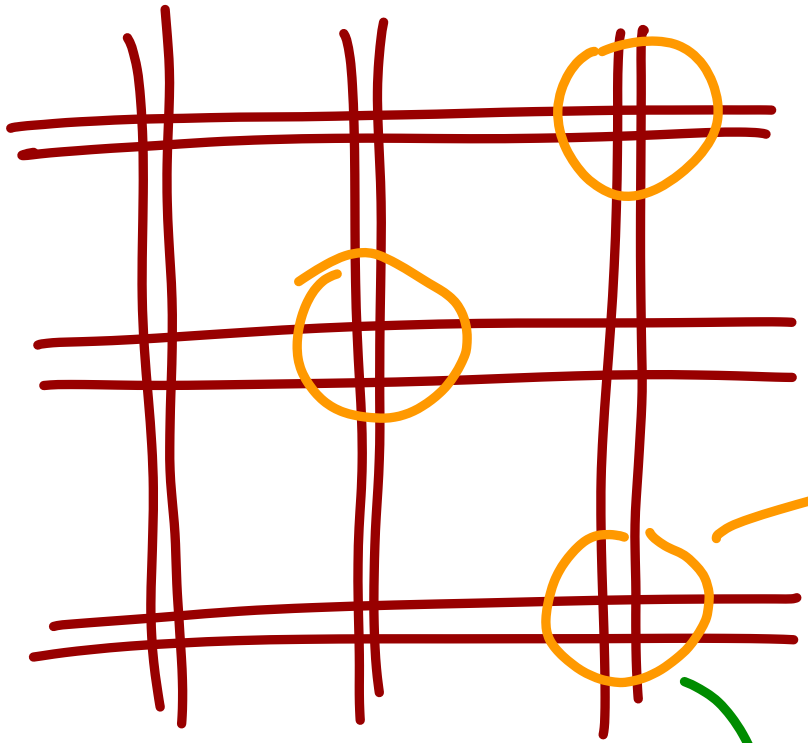
Carry one unstable

PCP FULLADDER



HOW CAN THE M.T. BE ORGANIZED?

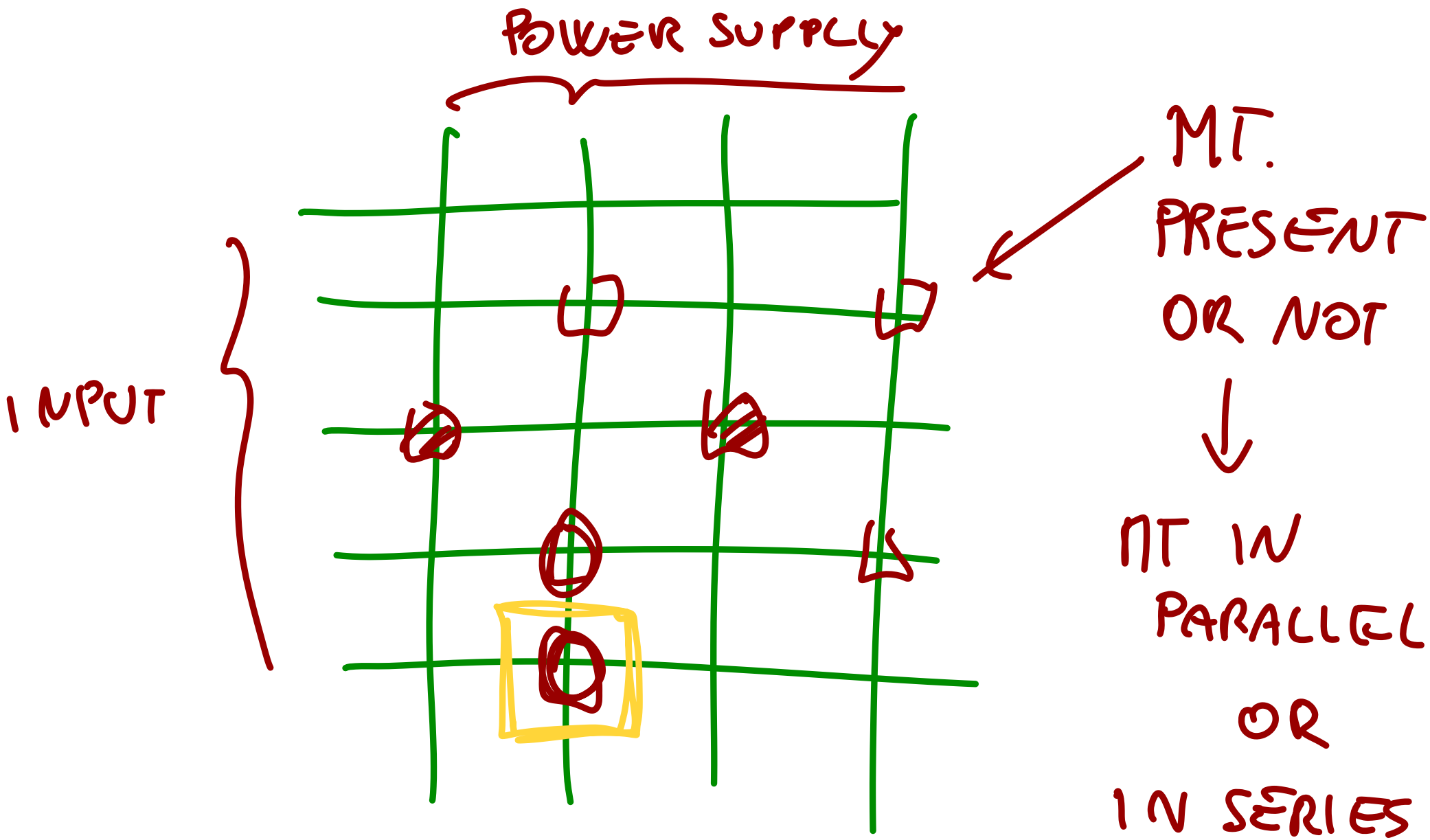
FOR ALL M.T. DEVICES



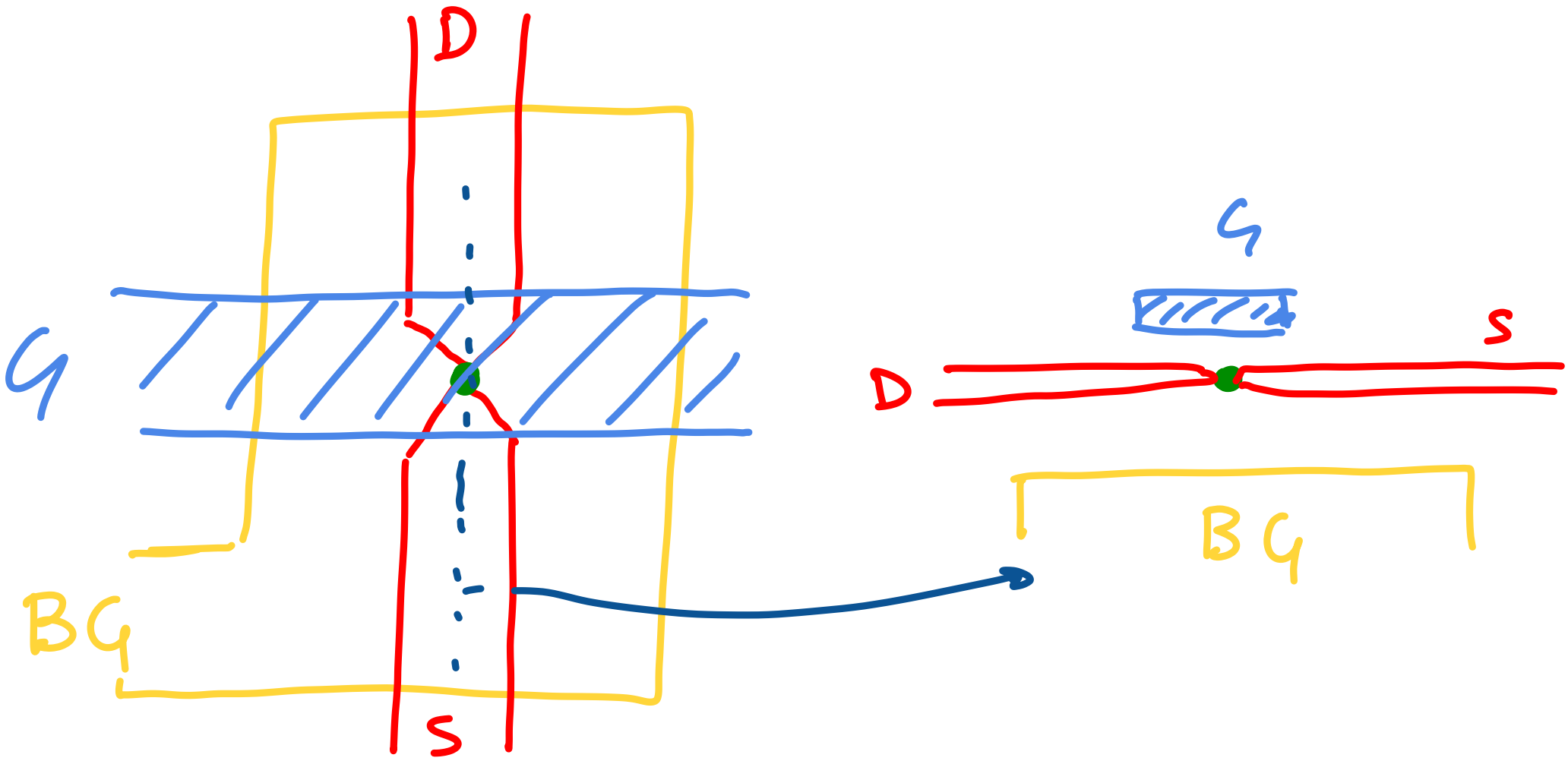
VERY REGULAR ARRAY - MATRIX

AT. INTERSECTION POINTS → GAPS AR FABRICATED

TR. CREATED SELECTIVELY


POWER SUPPLY
INPUT
MT.
PRESENT
OR NOT
↓
MT IN
PARALLEL
OR
IN SERIES

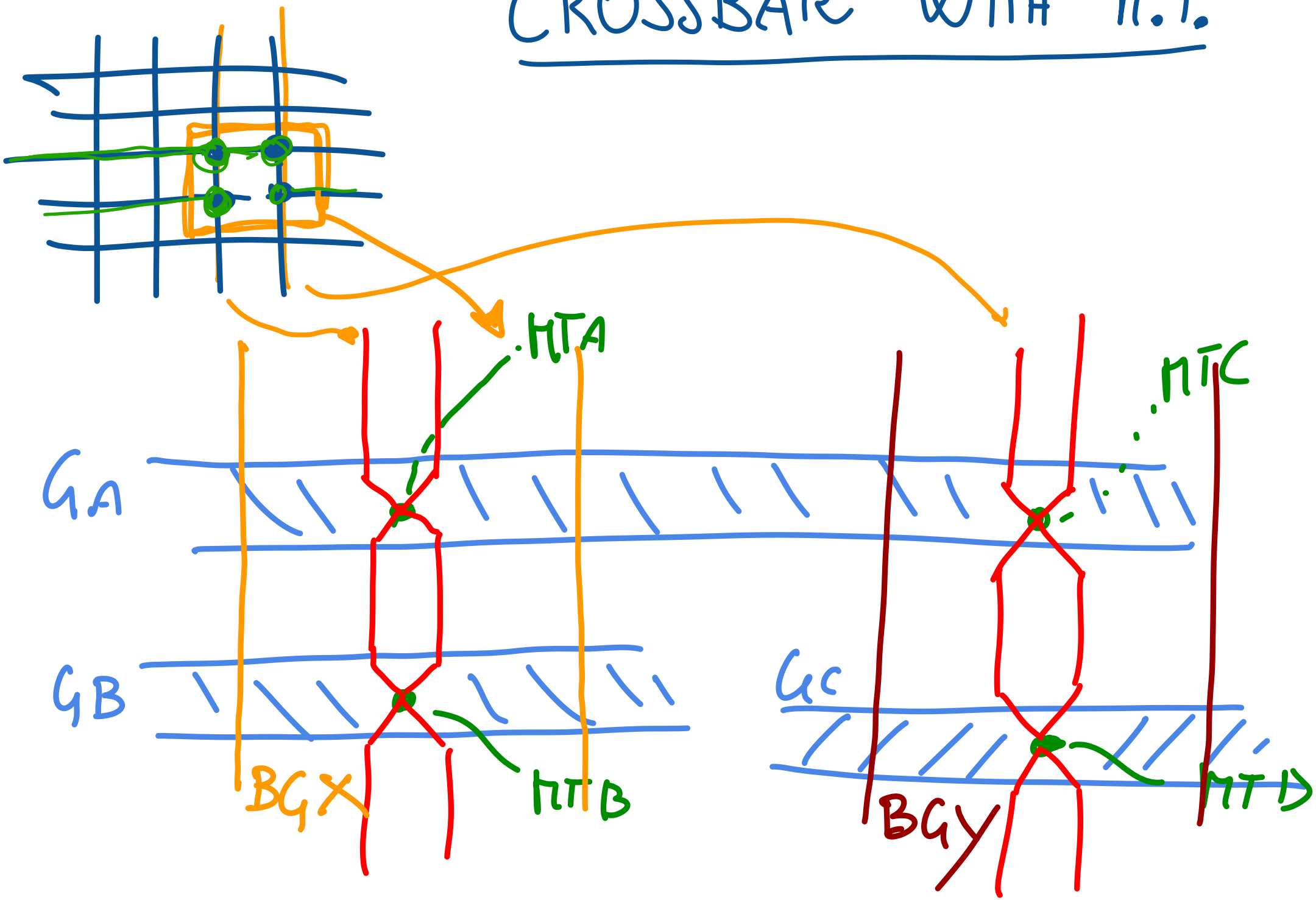
1 SINGLE MT



TOP VIEW

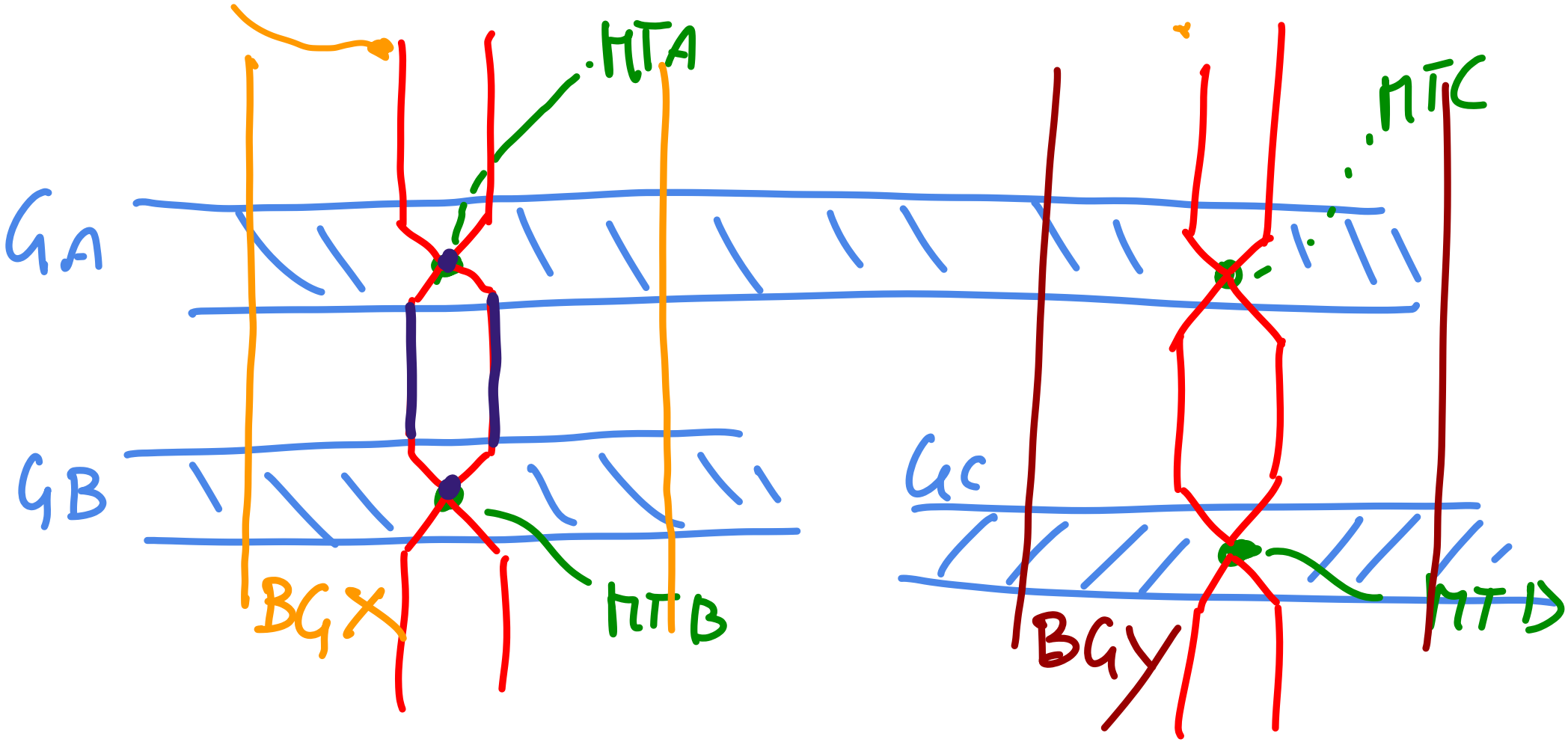
SECTION VIEW

CROSSBAR WITH M.T.

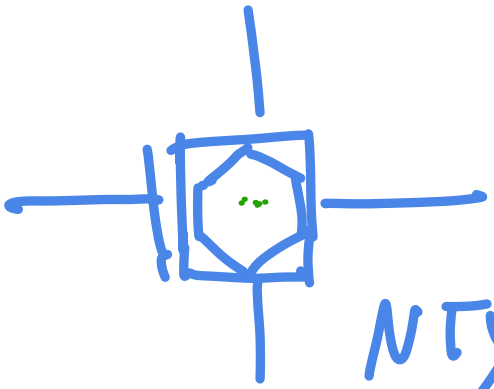


CONFIGURABLE BEHAVIOR

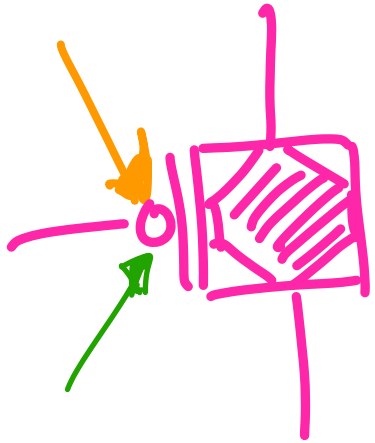
— SAME MOLECULE IN THE WHOLE CIRCUT BUT DIFFERENT V_{BG} TO CHANG THE BEHAVIOR (PEAK INCLUDED IN BW)



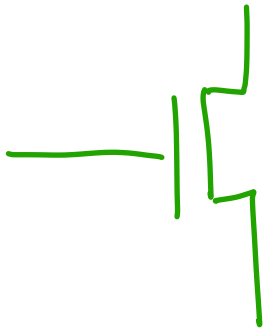
SYMBOLS



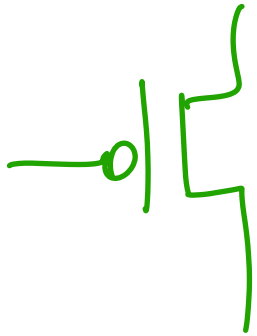
NTYPE
N.T



PTYPE
N.T.

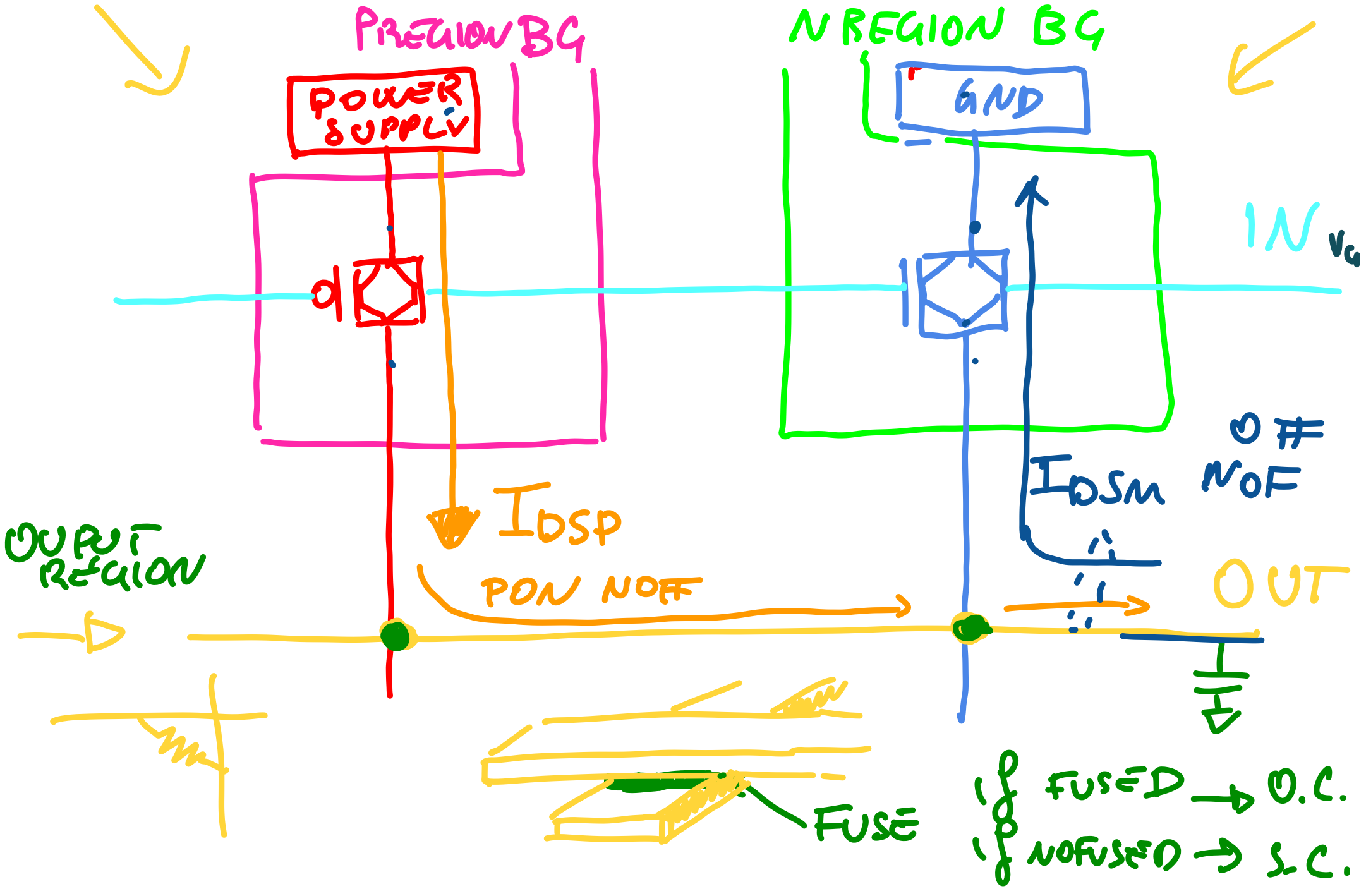


NMOS



PMOS

INVERTER BASED ON M.T.



NOTE: DIFFERENT ZONES FOR P&N FACILITATE DIFFERENT V_{BG} CONTROL & DIFFERENT β COUPLING FACTORS

ex OPV7

$V_G = 0V$ → N_{MT} OFF P_{MT} ON

OUT 0 → 1

V_{DSP} ACTIVE

I_{DSP} CHARGES OUTPUT

→ V_{OUT} ?

VALUE DEPENDS

CAP@OUT, R_{PATH}!

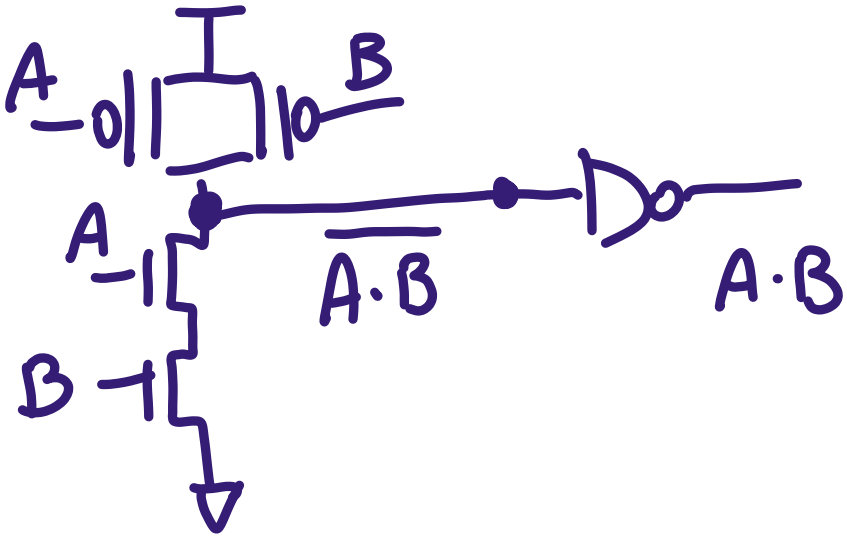
$V_G = 1V$

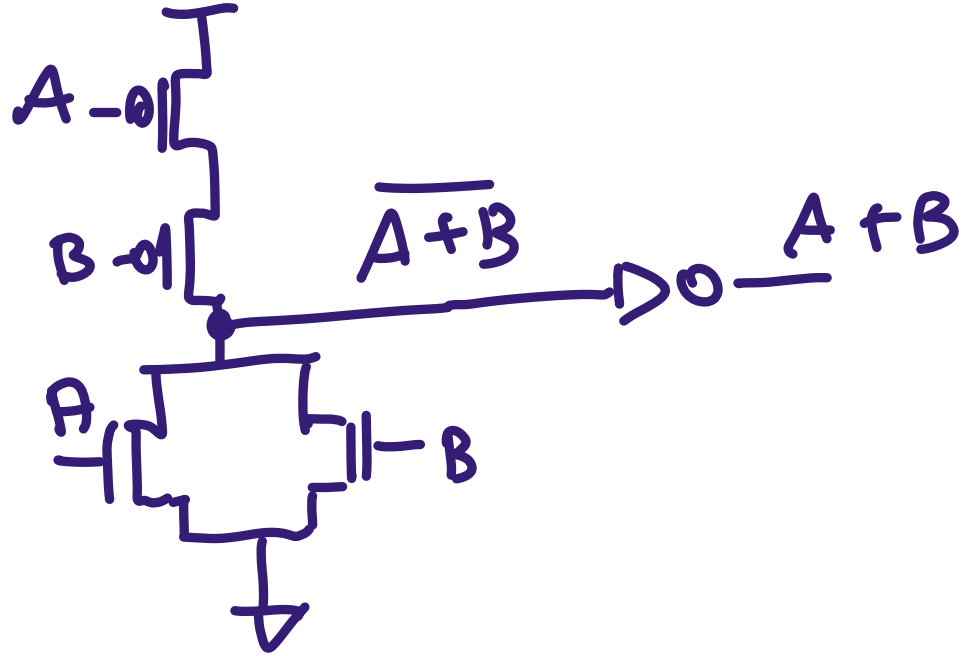
N_{MT} ON P_{MT} ~~OFF~~

OUT 1 → 0

I_{DN} DISCHARGES OUT

HOWTO FOR MORE COMPLEX LOGIC GATES?





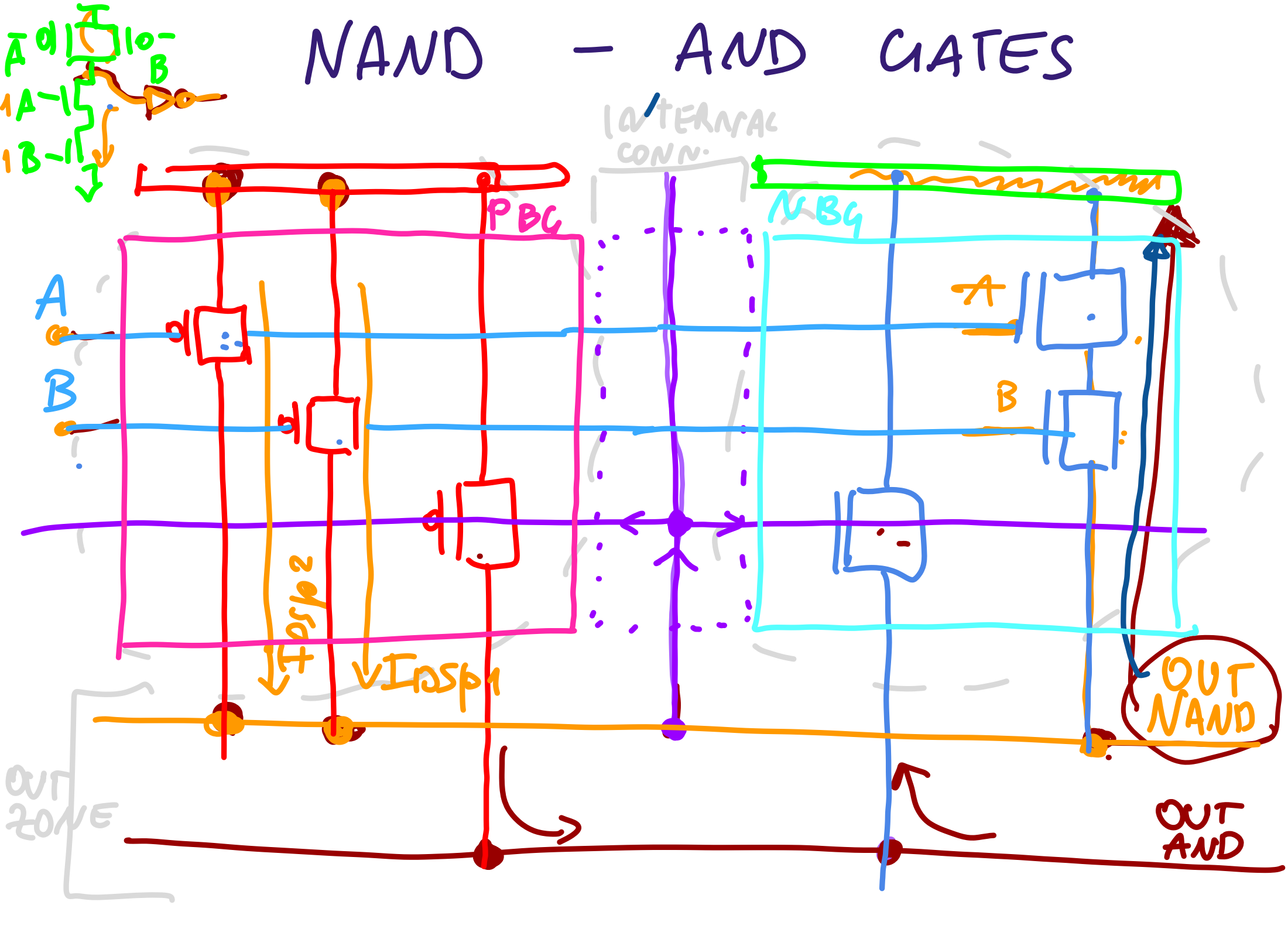
$A \oplus B$ HALF-ADDER

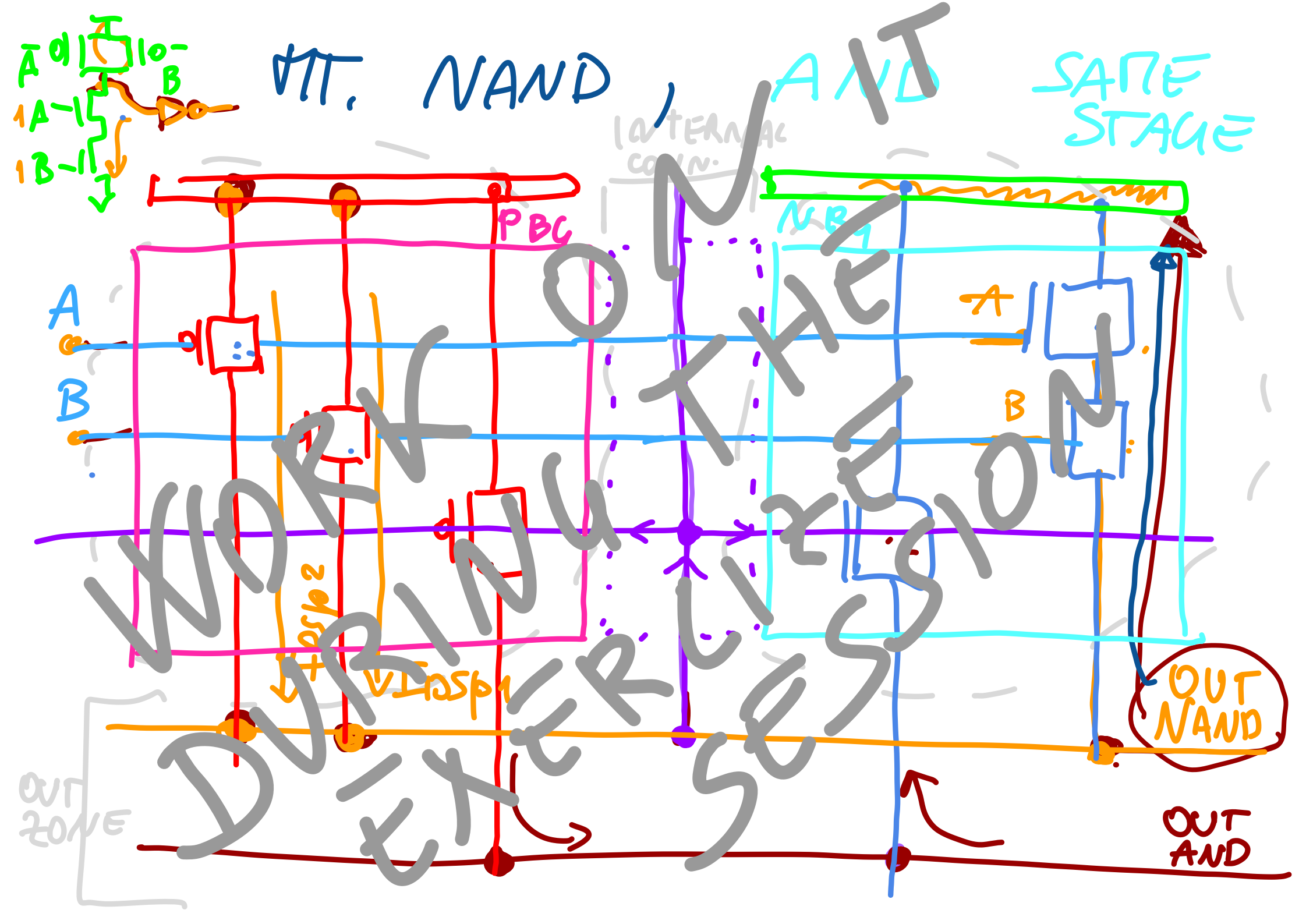
$A \overline{\oplus} B$ FULL ADDER

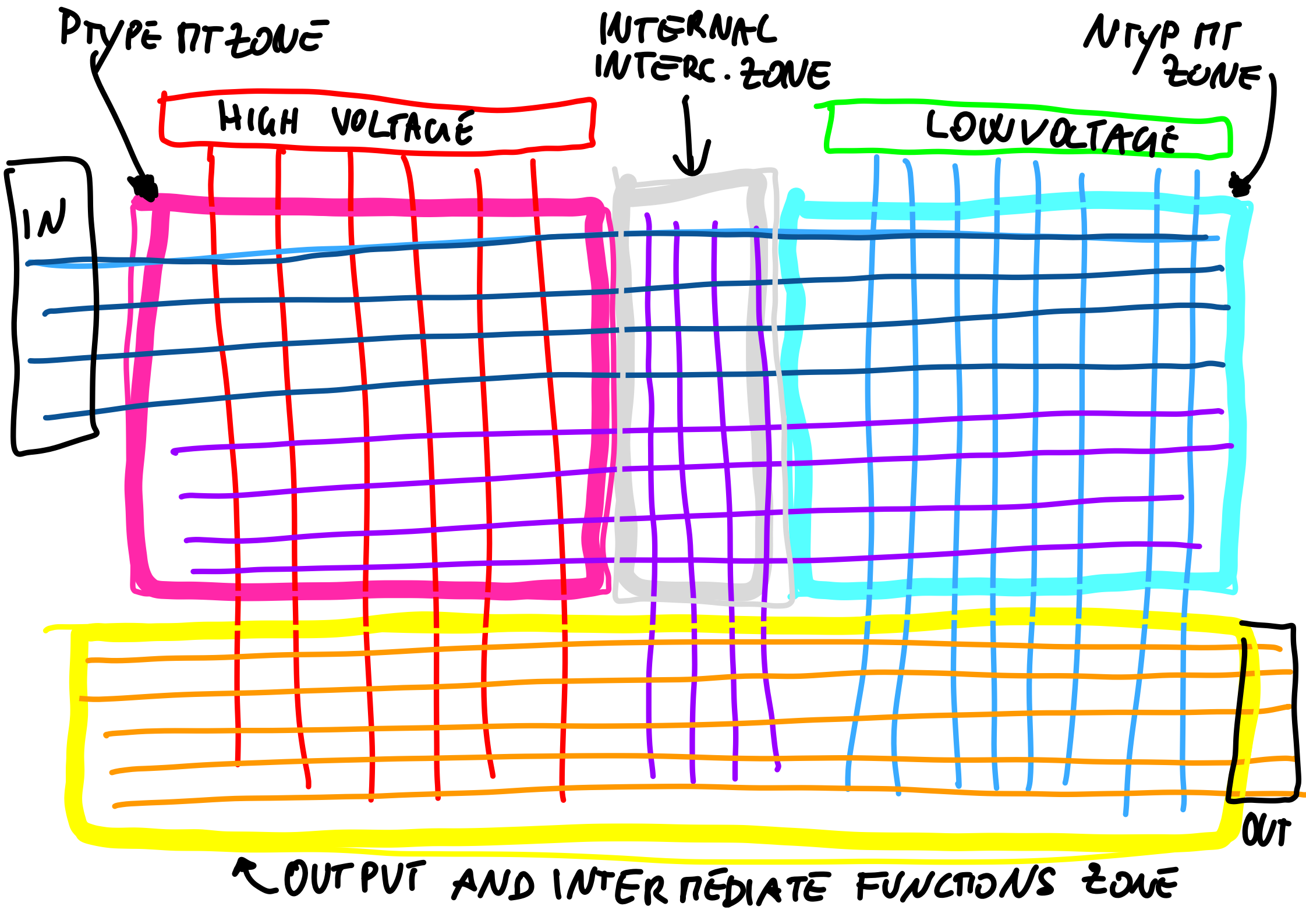
RIPPLE CARRY ADDER

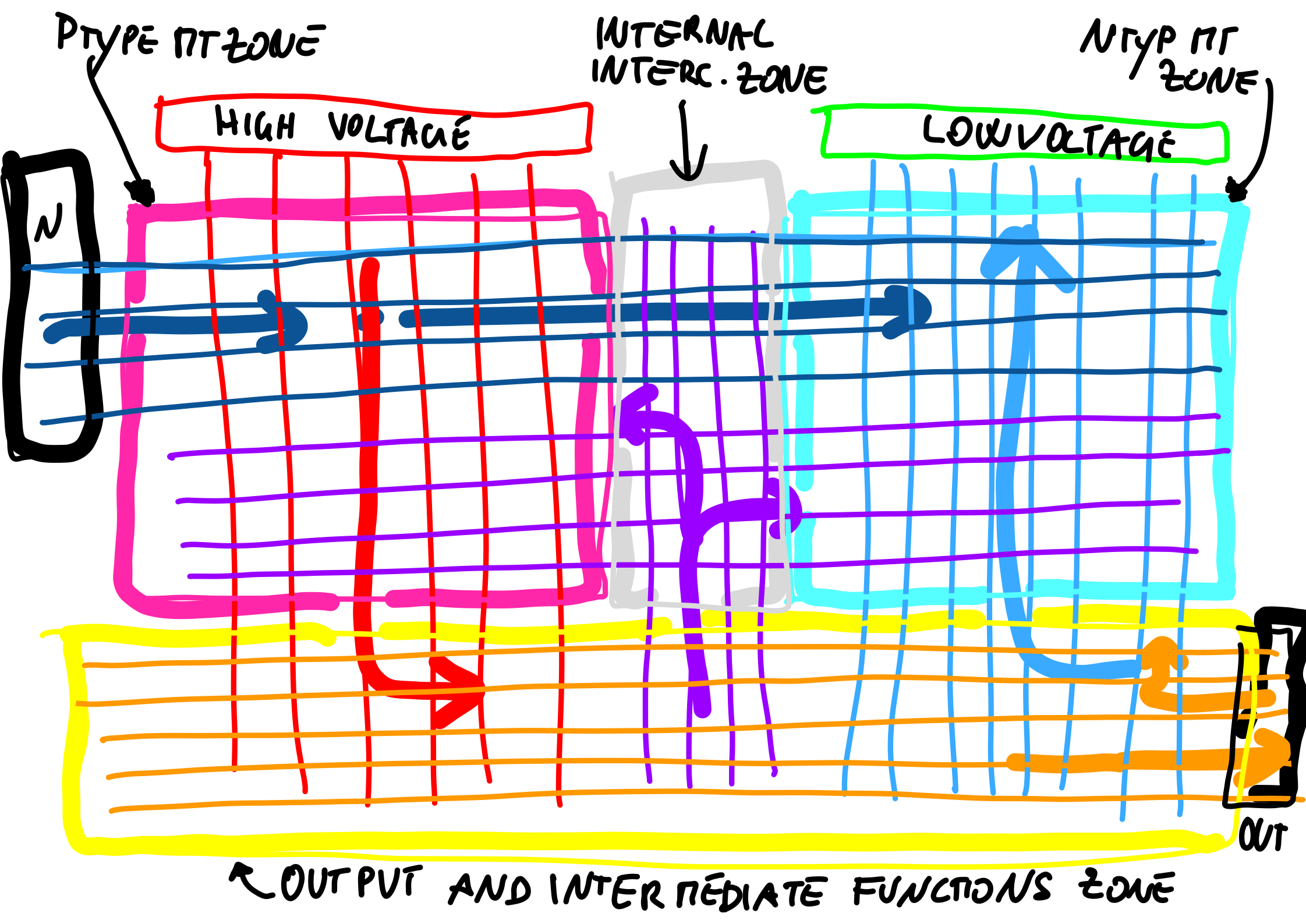
→ Work on them in the exercise section

NAND - AND GATES

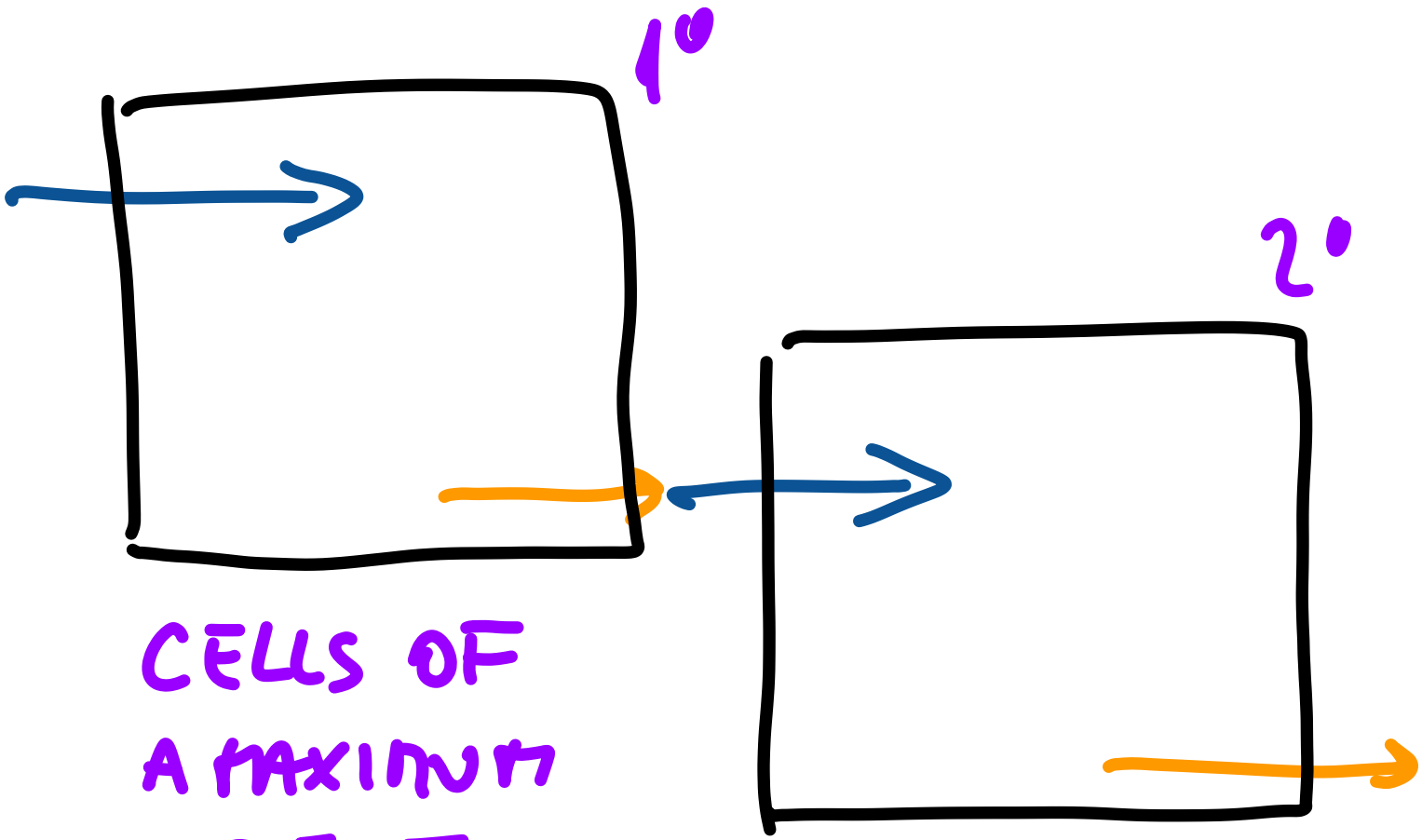



A
B
1A
1B
VT. NAND
AND
SAME STAGE
INTERNAL CONN.
PBC
NBC
A
B
A
B
VTPSP2
VTPSP1
OUT NAND
OUT AND
OUT ZONE
WORK ON THE DURING EXERCISE SESSION


P TYPE MT ZONE
INTERNAL INTERC. ZONE
N TYP MT ZONE
HIGH VOLTAGE
LOW VOLTAGE
IN
OUT
OUTPUT AND INTERMEDIATE FUNCTIONS ZONE


P TYPE MT ZONE
INTERNAL INTERC. ZONE
N TYP MT ZONE
HIGH VOLTAGE
LOW VOLTAGE
N
OUT
OUTPUT AND INTERMEDIATE FUNCTIONS ZONE

CASCADING IS POSSIBLE



CELLS OF A MAXIMUM SIZE FOR A CERTAIN N° OF TR & FUNCTIONS

WHAT ARE WE NEGLECTING?

- INTERCONNECT PARASITICS
  - RESISTANCES
  - CAPACITANCES
- DRIVING CAPABILITY OF GATES/TRANSISTORS
- NUMBER OF CASCADED GATES

CRISTALLIZATION

a) SCF LOOP

b) SIMPLE CIRCUITS BASED ON NT