PAB

COMPOSANTS SEMI-CONDUCTEURS

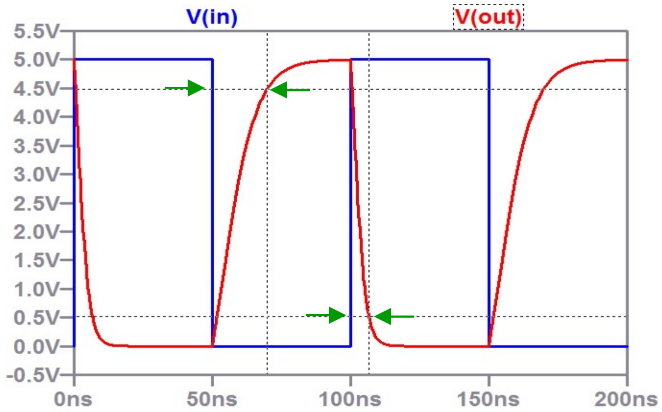
XII) Solutions S12

P.A. Besse

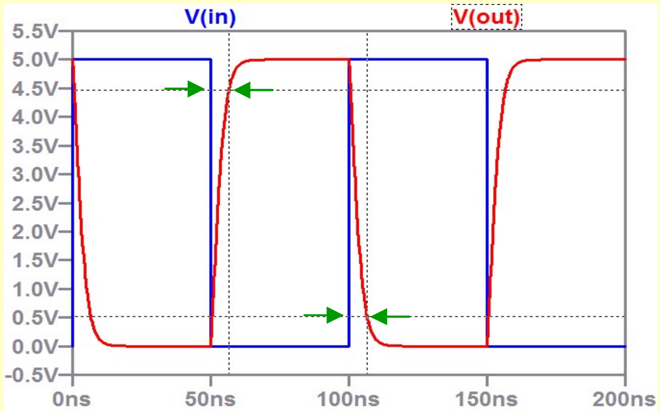
EPFL

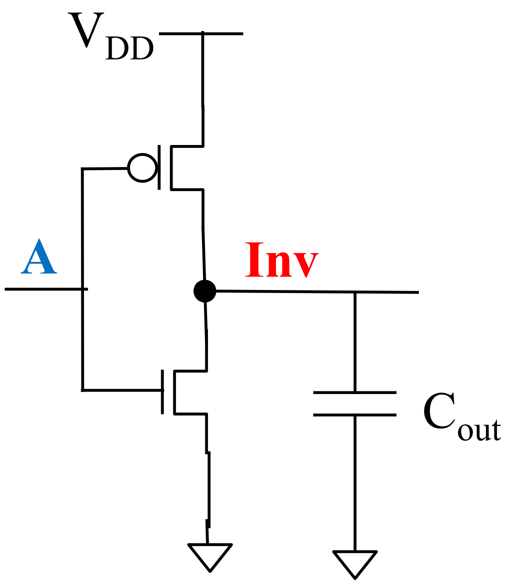
Exercice 12.3: dimensionnement (1)

Wp=Wn

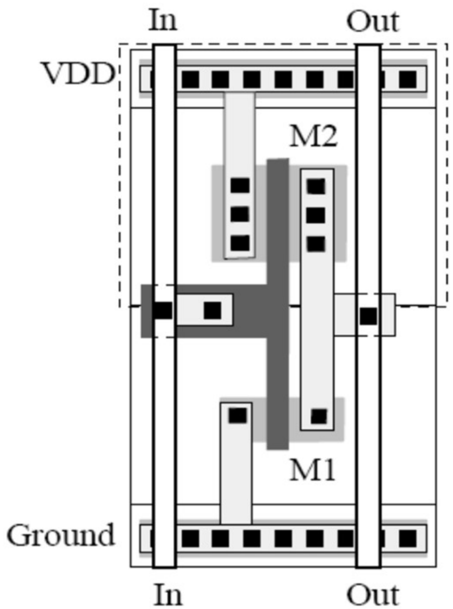


Wp= 3 Wn



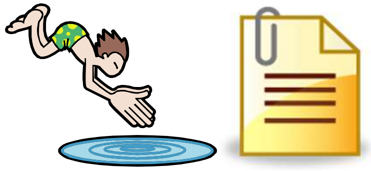


Inverseur

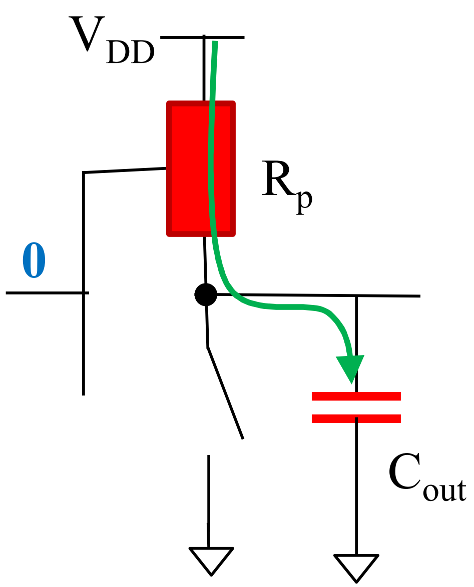


Wp= 3 Wn

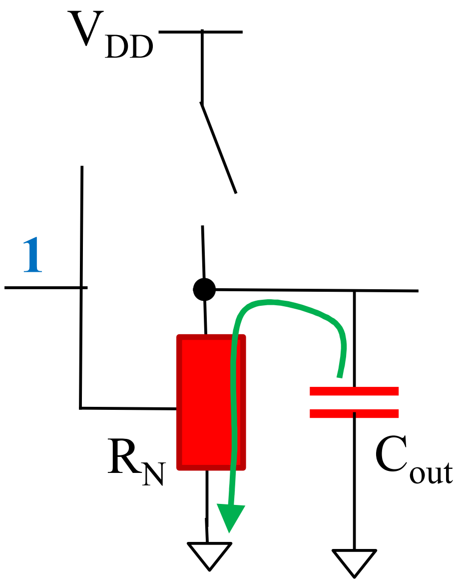
Exercice 12.3: dimensionnement (1)



Charge



Decharge



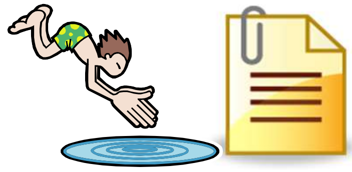
Condition:

$$R_p C_{out} = R_N C_{out} \quad \Rightarrow \quad \frac{C_{out}}{W_P \mu_p} = \frac{C_{out}}{W_N \mu_N}$$

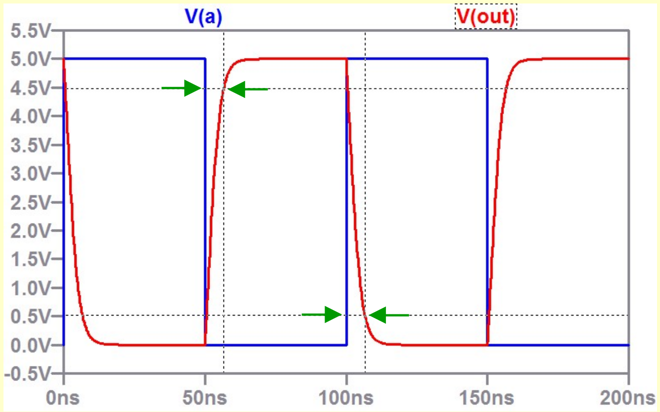
$$\Downarrow$$

$$\frac{W_P}{W_N} = \frac{\mu_n}{\mu_P} = 3$$

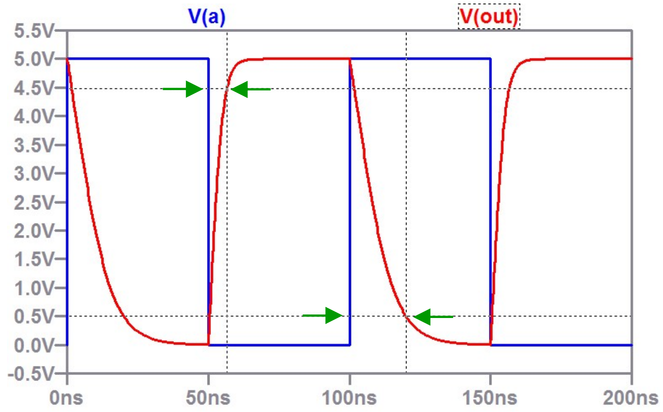
Exercice 12.3: dimensionnement (2)



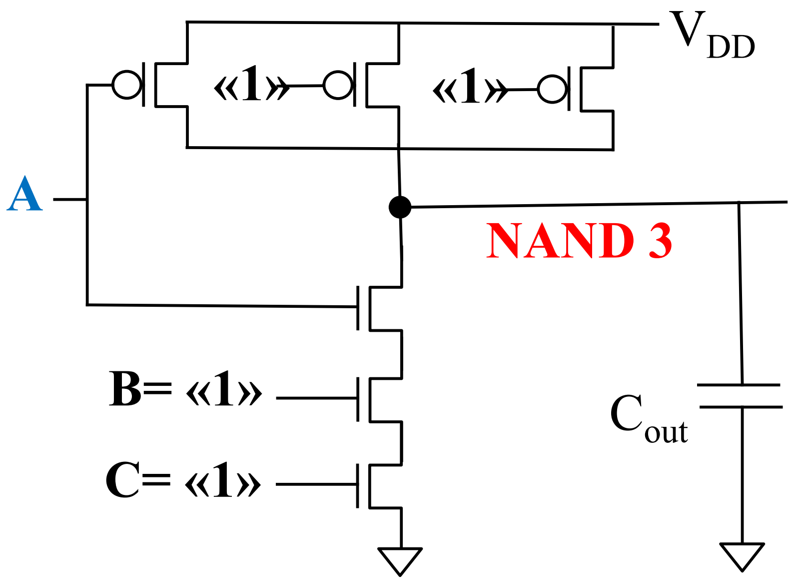
Wp= Wn

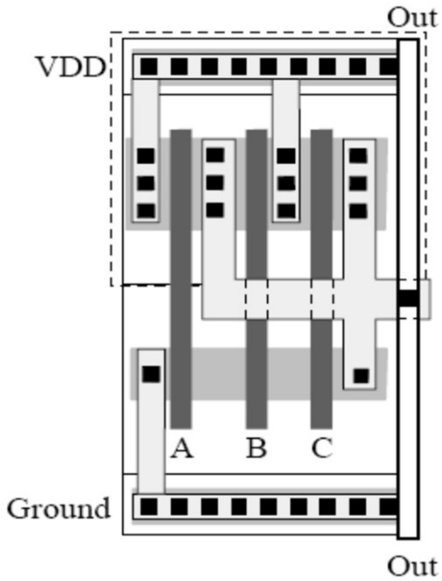


Wp= 3 Wn



NAND 3

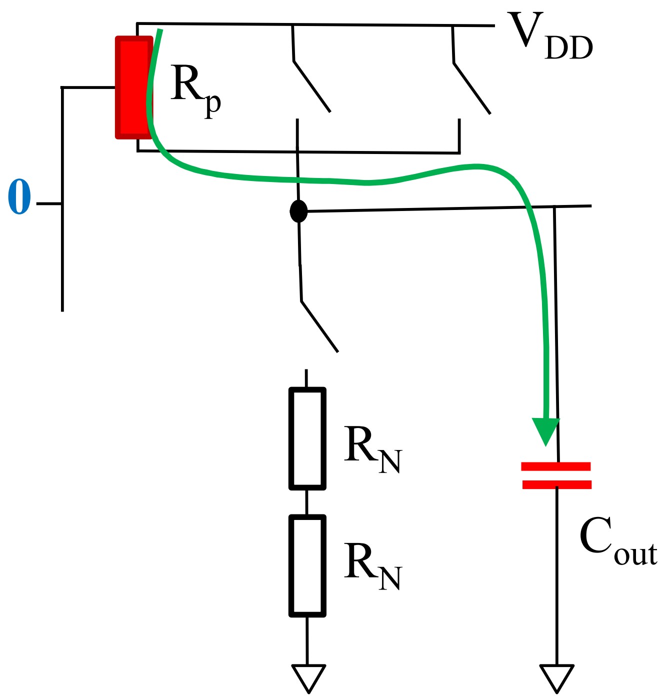




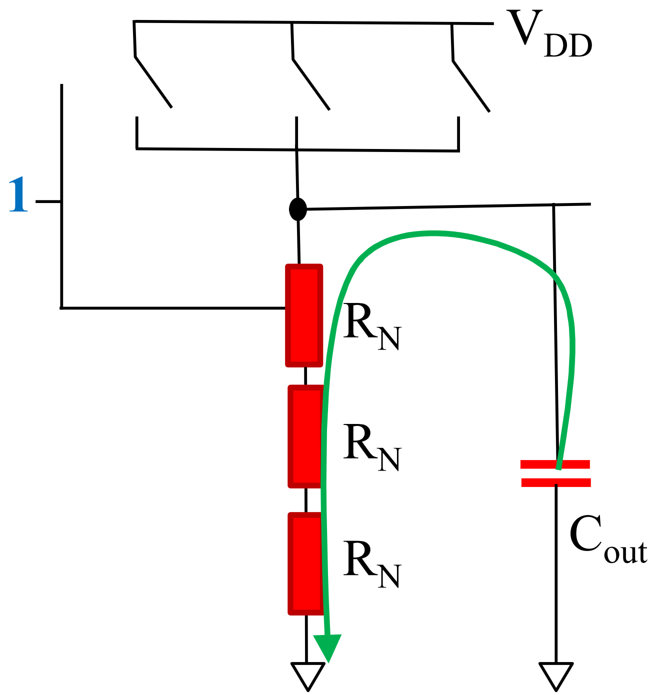
Wp= 3 Wn

Exercice 12.3: dimensionnement (2)

Charge



Decharge



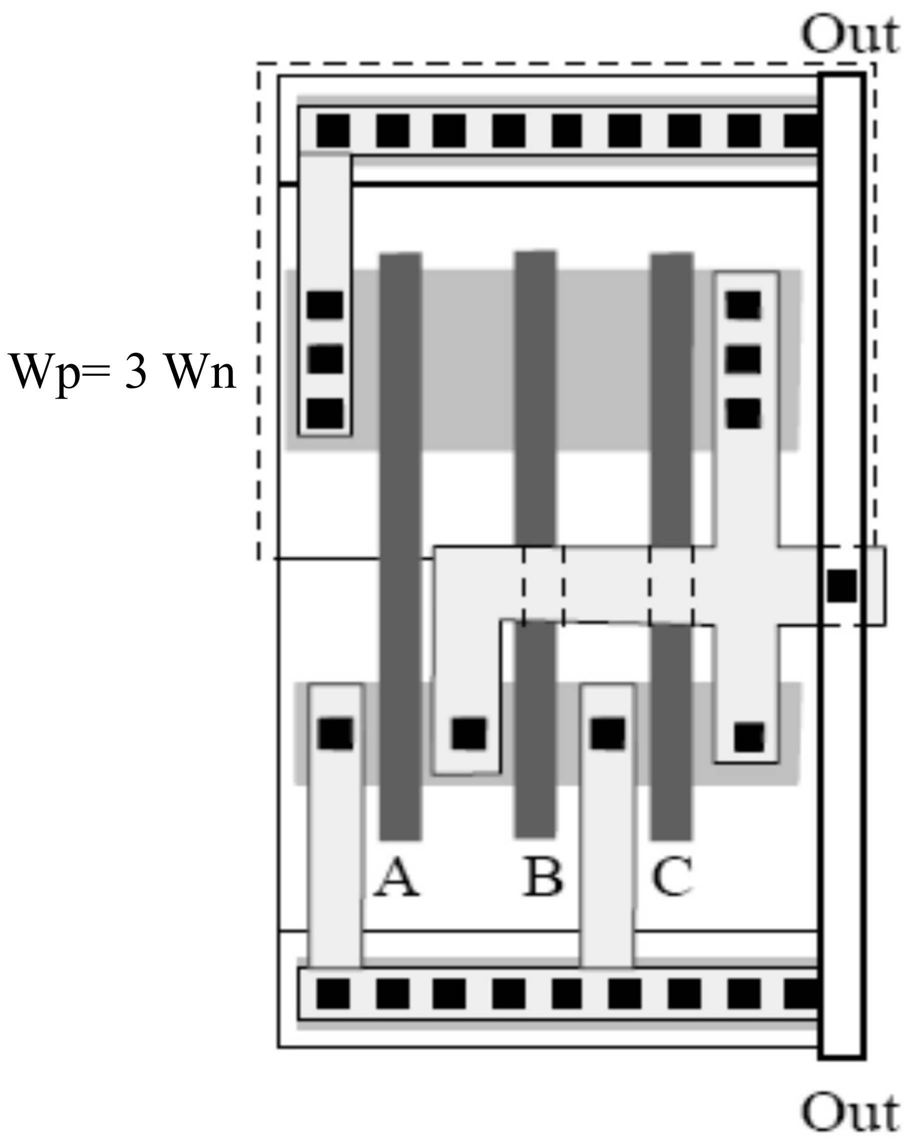
Condition:

$$R_p C_{out} = 3 R_N C_{out} \quad \Rightarrow \quad \frac{C_{out}}{W_P \mu_p} = \frac{3 \cdot C_{out}}{W_N \mu_N}$$

$$\Downarrow$$

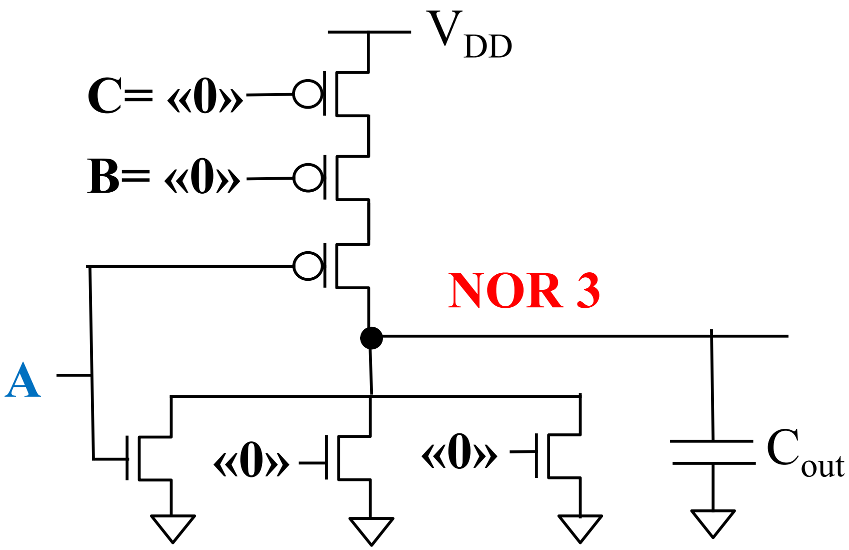
$$\frac{W_P}{W_N} = \frac{1}{3} \frac{\mu_n}{\mu_P} = 1$$

Ex. 12.3: Question supplémentaire

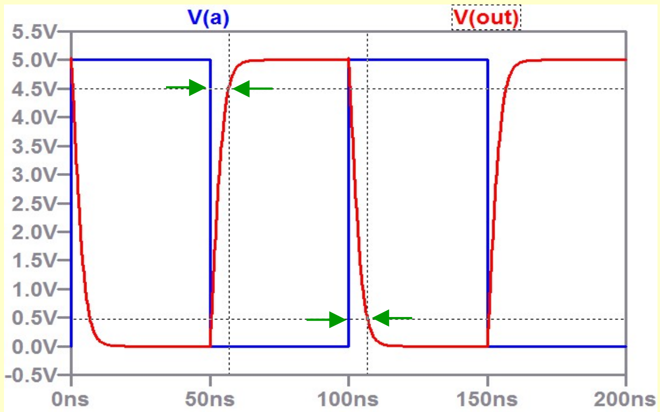


- Quelle est cette fonction ?
- Dessinez le circuit CMOS correspondant et analysez les temps de charge et de décharge pour le «worst case».
- En utilisant la même technologie ($\mu_p=\mu_n/3$), optimisez le rapport W_p/W_n.

NOR 3



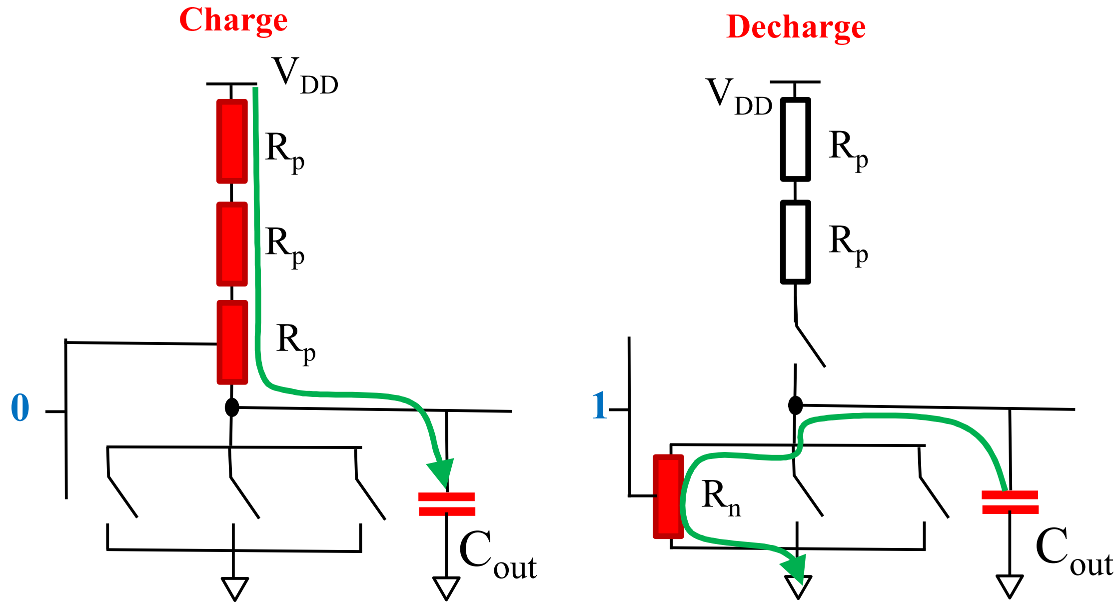
Wp= 9 Wn



$$3R_pC_{out} = R_NC_{out} \quad \Rightarrow \quad \frac{3\cdot C_{out}}{W_P\mu_p} = \frac{C_{out}}{W_N\mu_N}$$

⇓

$$\frac{W_P}{W_N} = 3\cdot\frac{\mu_n}{\mu_P} = 9$$



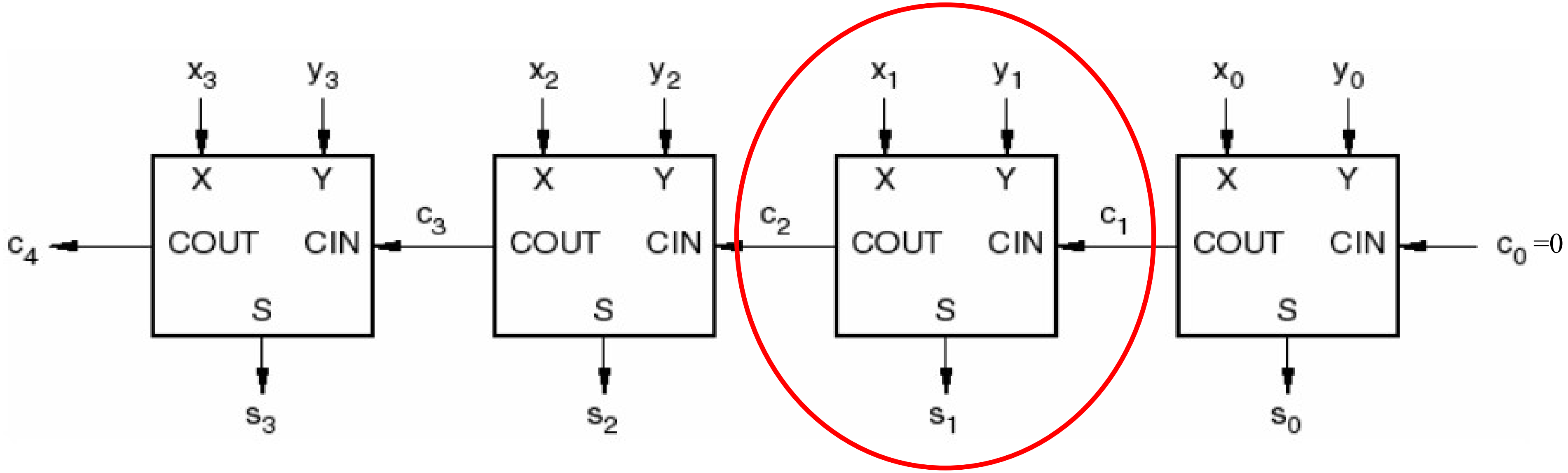
Exercice E12.2: Addition binaire

Principe

$$
\begin{array}{rl}
 & c_4\ c_3\ c_2\ c_1\ 0 \\
 & \quad x_3\ x_2\ x_1\ x_0 \\
+ & \quad y_3\ y_2\ y_1\ y_0 \\
\hline
= & c_4\ s_3\ s_2\ s_1\ s_0
\end{array}
$$

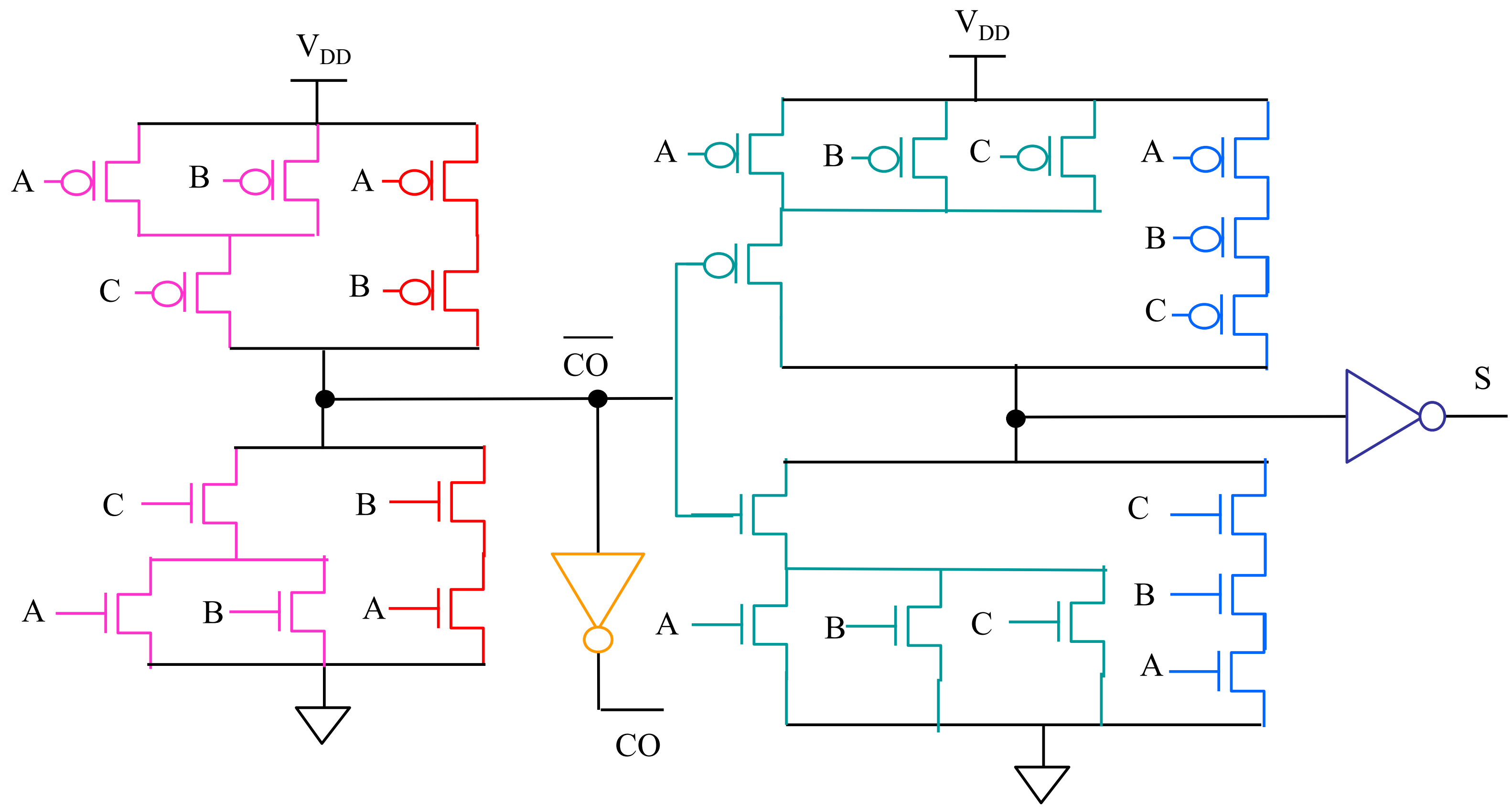
Exemple d'addition binaire: 1101 + 1001 = 10110

$$
\begin{array}{rll}
 & 1\,0\,0\,1\,0 & C \\
 & \ \ 1\,1\,0\,1 & A \\
+ & \ \ 1\,0\,0\,1 & B \\
\hline
= & 1\,0\,1\,1\,0 & S
\end{array}
$$



Exercice E12.2: « Full adder »

Calculez la table de vérité et montrez qu'elle correspond à une addition binaire



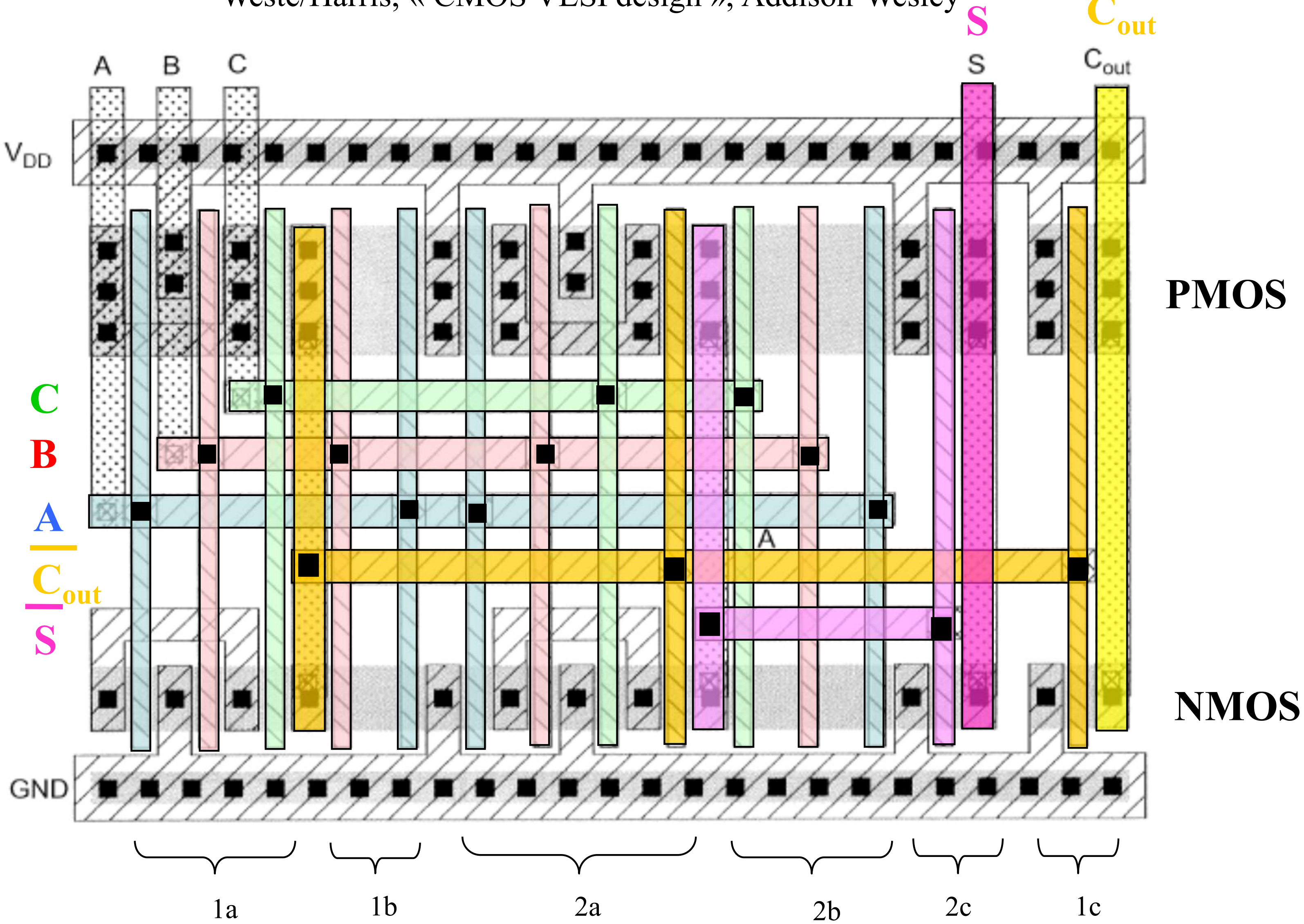
1a 1b 1c 2a 2b 2c

28 transistors

Zimmermann, Fichtner, IEEE journal of solid-state circuits, Vol. 32, No. 7, pp. 1-12.

Full Adder: layout

Weste/Harris, « CMOS VLSI design », Addison-Wesley



PAB

Table de vérité: « full adder » (1)

A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

retenue **somme**

Table de vérité: « full adder » (1)

A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

A =B=0 (rows 1–2)

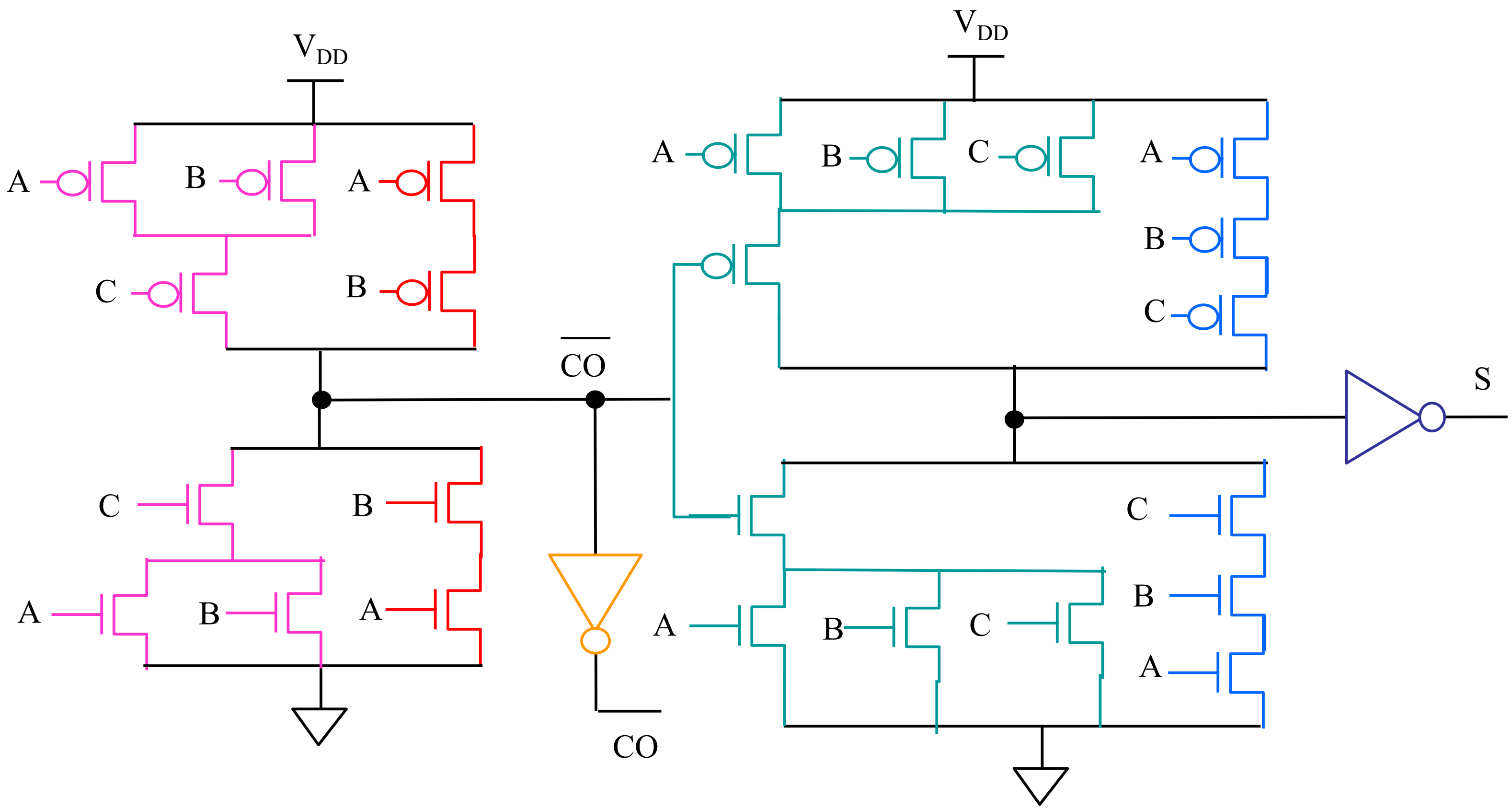
Au moins un «0» et un «1» →inverter (rows 3–6)

A =B=1 (rows 7–8)

retenue (CO) **somme** (S)

Exercice E12.2: « Full adder »

Calculez la table de vérité et montrez qu'elle correspond à une addition binaire



1a 1b 1c 2a 2b 2c

28 transistors

Zimmermann, Fichtner, IEEE journal of solid-state circuits, Vol. 32, No. 7, pp. 1-12.

PAB

Table de vérité: « full adder » (1)

	A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
A =B=0	0	0	0	1	0		
	0	0	1	1	0		
Au moins un «0» et un «1» →inverter	0	1	0	$\overline{C}$=1	0		
	0	1	1	$\overline{C}$=0	1		
	1	0	0	$\overline{C}$=1	0		
	1	0	1	$\overline{C}$=0	1		
A =B=1	1	1	0	0	1		
	1	1	1	0	1		

retenue **somme**

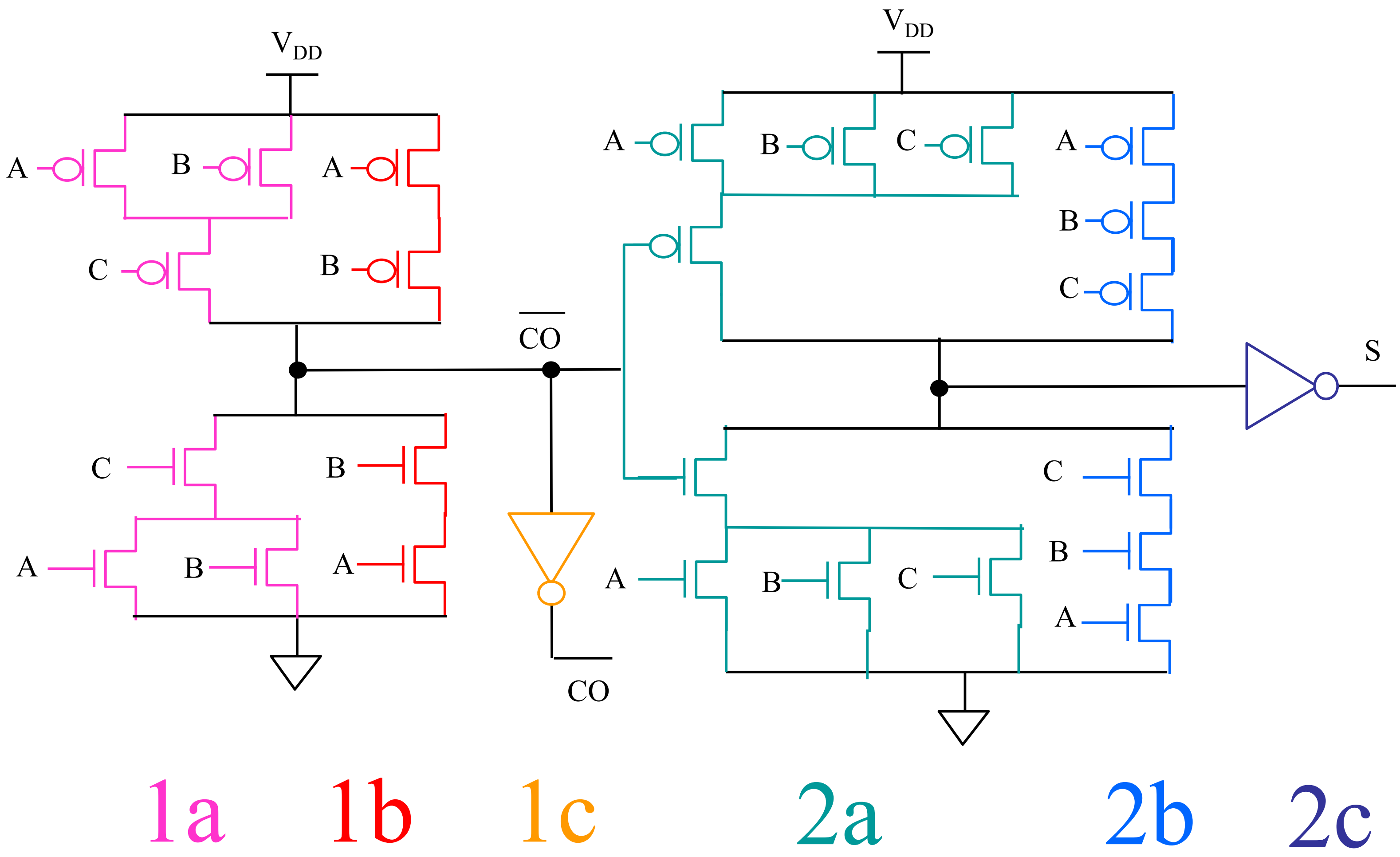
Table de vérité: « full adder » (1)

	A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
A=B=C=0	0	0	0	1	0		
	0	0	1	1	0		
	0	1	0	1	0		
Au moins un «0» et un «1» →inverter	0	1	1	0	1		
	1	0	0	1	0		
	1	0	1	0	1		
	1	1	0	0	1		
A=B=C=1	1	1	1	0	1		

retenue **somme**

Exercice E12.2: « Full adder »

Calculez la table de vérité et montrez qu'elle correspond à une addition binaire



28 transistors

Zimmermann, Fichtner, IEEE journal of solid-state circuits, Vol. 32, No. 7, pp. 1-12.

Table de vérité: « full adder » (1)

	A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
A=B=C=0	0	0	0	1	0	1	0
Au moins un «0» et un «1» →inverter	0	0	1	1	0	CO=0	1
	0	1	0	1	0	CO=0	1
	0	1	1	0	1	CO=1	0
	1	0	0	1	0	CO=0	1
	1	0	1	0	1	CO=1	0
	1	1	0	0	1	CO=1	0
A=B=C=1	1	1	1	0	1	0	1

retenue (CO) **somme** (S)

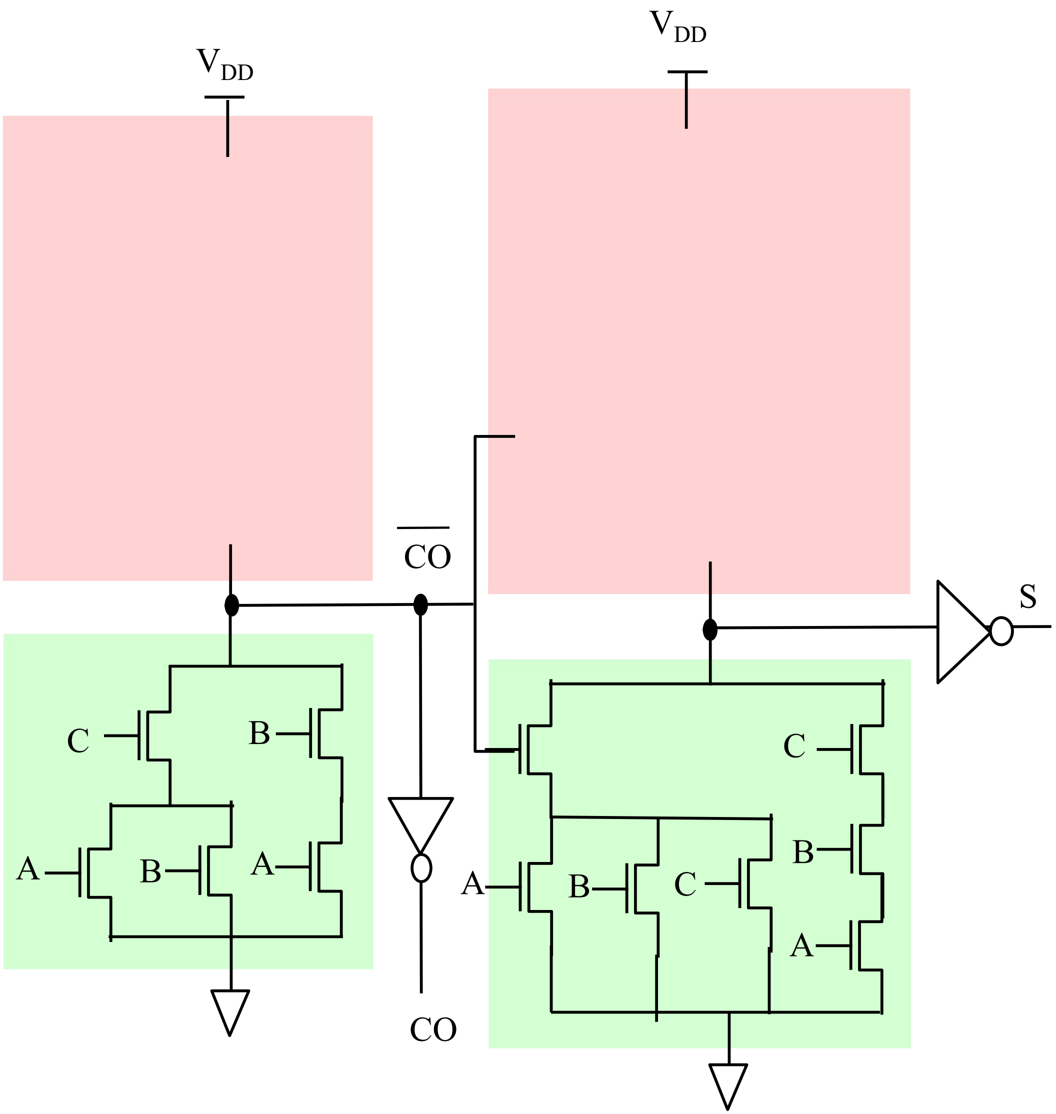
Table de vérité: « full adder » (2)

A	B	C	$\overline{CO}$	CO	$\overline{S}$	S
0	0	0	1	**0**	1	**0**
0	0	1	1	**0**	0	**1**
0	1	0	1	**0**	0	**1**
0	1	1	0	**1**	1	**0**
1	0	0	1	**0**	0	**1**
1	0	1	0	**1**	1	**0**
1	1	0	0	**1**	1	**0**
1	1	1	0	**1**	0	**1**

retenue **somme**

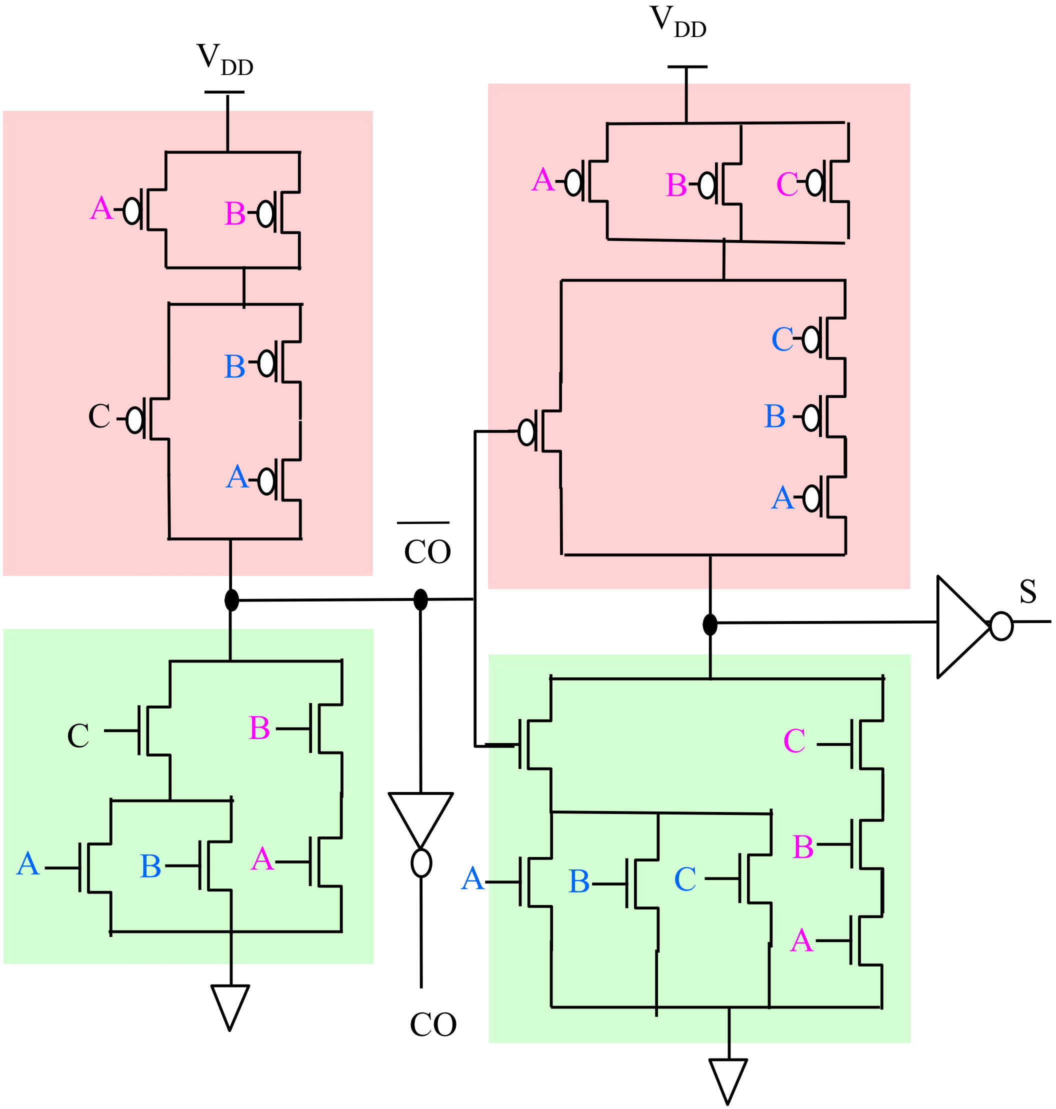
Exercice 12.6:
Full adder: alternative

Déterminez les boites correspondantes avec parallèle ←→ série



Exercice 12.6:
Full adder: alternative

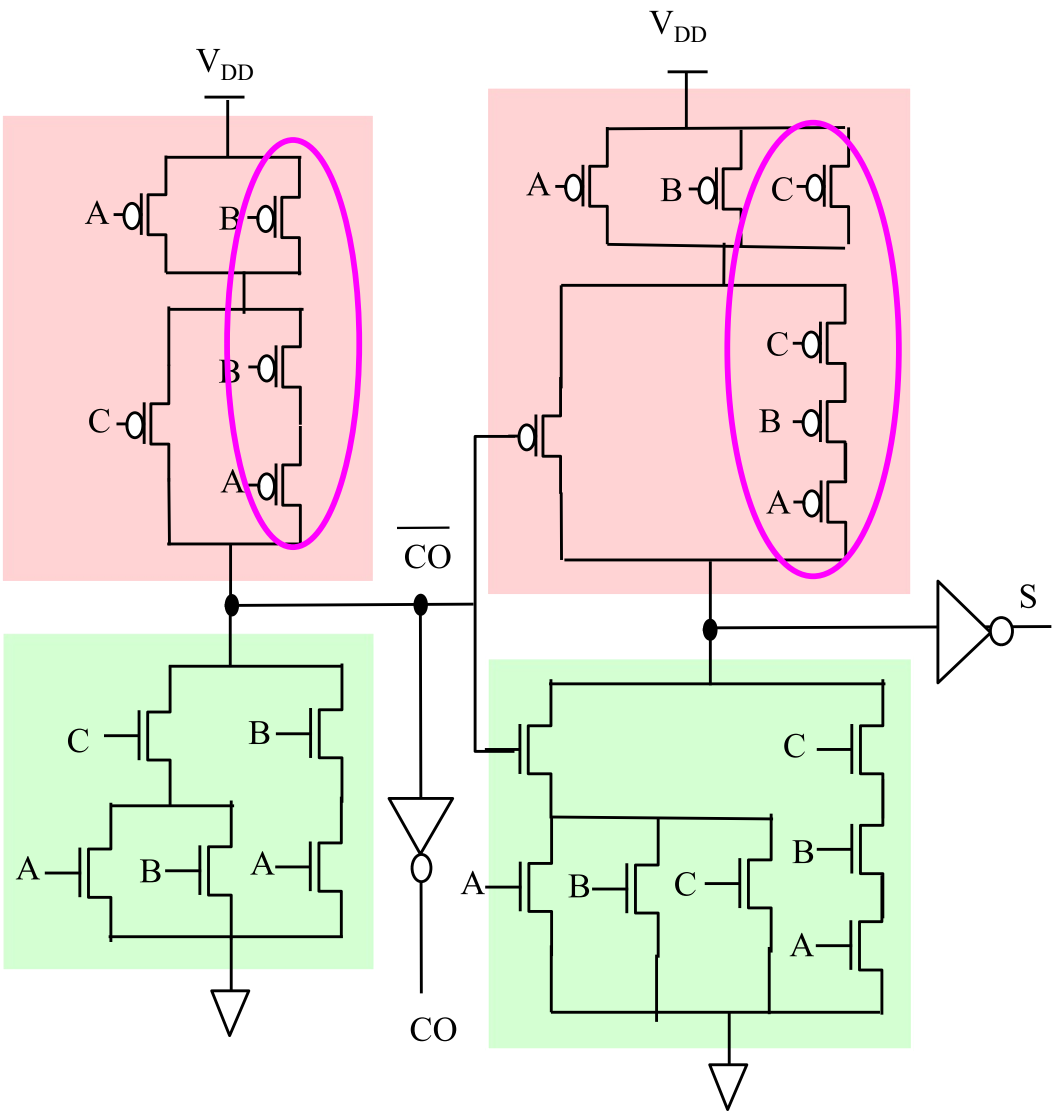
Déterminez les boites correspondantes avec parallèle ←→ série



PAB

Exercice 12.6:
Full adder: alternative

Longue chaine de transistors en série → Lent !



Version standard