

# Smart Sensors for IoT

## Exercise 5 (16.11.2022)

Christian Enz

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

### Problem 1 Input bias and offset currents

The circuit of Fig. 1 is to be used as an inverting amplifier with a gain of 10 V/V and is to employ the  $\mu\text{A}741$  op amp (the datasheet is appended at the end of the exercises).

- Specify suitable component values to ensure a maximum output error of 10 mV.

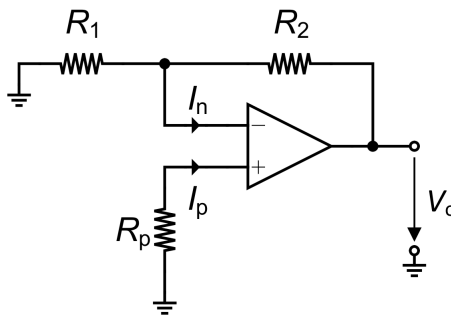


Figure 1: System to estimate the output error due to the input bias currents for the case of resistive feedback.

### Problem 2 Common-Mode Rejection Ratio (CMRR)

The difference amplifier of Fig. 2 uses a  $\mu\text{A}741$  op amp and a perfectly matched resistance set with  $R_1 = R_3 = 10\text{ k}\Omega$  and  $R_2 = R_4 = 100\text{ k}\Omega$ . Suppose the inputs are tied together and driven with a common signal  $V_I$ . Estimate the typical change in  $V_O$  if:

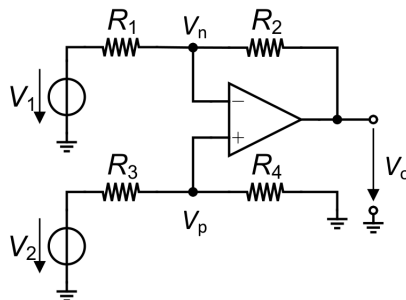


Figure 2: Difference amplifier.

- $V_I$  is slowly changed from 0 to 10 V;
- $V_I$  is a 10 kHz, 5 V 0-peak sine wave.

Hint: the output voltage can be rewritten as:

$$V_O = A_{dm} \left( V_{i+} - V_{i-} + \frac{A_{cm}}{A_{dm}} V_{ic} \right) \quad (1)$$

### Problem 3 Power-Supply Rejection Ratio (PSRR)

A  $\mu A741$  op amp is connected as in Fig. 1 with  $R_1 = 100 \Omega$  and  $R_2 = 100 \text{ k}\Omega$ .

- Predict the typical as well as the maximum ripple at the output for a power-supply ripple  $\Delta V_{DD}$  of 0.05 Vp at 120 Hz (assume ideal  $V_{SS}$ ).

Hint: The  $\mu A741$  datasheets do not show the PSRR rolloff with frequency, so let us use the ratings given at dc, keeping in mind that the results will be optimistic.

### Problem 4 Single-Pole Open-Loop Gain

With respect to the non-ideal op-amp frequency response, we shall make the simplifying assumption that the open-loop gain  $a(s)$  possesses just a single pole. Such a gain shall be expressed in the form:

$$a(s) = \frac{a_0}{1 + s/\omega_b} = \frac{a_0}{1 + jf/f_b}; \quad (2)$$

where  $s$  is the complex frequency,  $a_0$  is the open-loop dc gain, and  $-\omega_b$  is the  $s$ -plane pole location. Equivalently, in the second half of the equation, we express gain in terms of the frequency  $f$ , where  $j$  is the imaginary unit, and  $f_b = \omega_b/(2\pi)$  is the open-loop  $-3$ -dB frequency, also called the open-loop bandwidth. We calculate gain magnitude and phase as:

$$|a(jf)| = \text{mag } a(jf) = \frac{a_0}{\sqrt{1 + (f/f_b)^2}}; \quad (3)$$

$$\angle a(jf) = \text{ph } a(jf) = -\arctan(f/f_b). \quad (4)$$

Magnitude is plotted in Fig. 3. The gain is high and approximately constant only from dc up to  $f_b$ . Past  $f_b$  it rolls off at the rate of  $-20$  dB/dec, until it drops to 0 dB (or 1 V/V) at  $f = f_t$ .

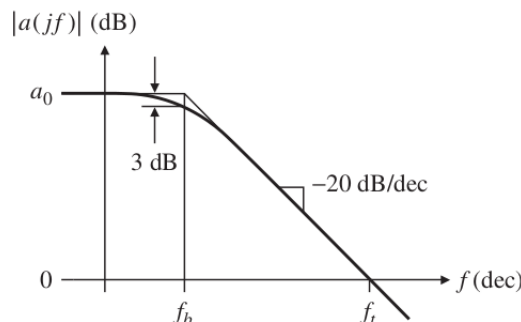


Figure 3: Single-pole open-loop gain. The frequency axis is on a logarithmic-base-10 scale.

- Calculate  $f_t$  by imposing  $1 = a_0/\sqrt{1 + (f_t/f_b)^2}$ . *Hint: notice that  $f_t \gg f_b$*
- According to the  $\mu\text{A}741$  datasheet, what are the typical  $a_0$  (called *large signal voltage gain*),  $f_b$  and  $f_t$  values?
- Calculate the module and phase of  $a(s)$  when  $f \ll f_b$ ,  $f = f_b$  and  $f \gg f_b$ .
- Consider another amplifier than the  $\mu\text{A}741$ , which has a magnitude of 80 dB at  $f = 10$  Hz and a phase angle of  $-58^\circ$  at  $f = 320$  Hz. Estimate  $a_0$ ,  $f_b$ , and  $f_t$ .

## Problem 5 Slew rate

Suppose a  $\mu\text{A}741$  op amp is configured as voltage follower (Fig. 4). We stress that  $SR$  is a nonlinear large-signal parameter, while  $t_R$  is a linear small-signal parameter. The critical output-step magnitude corresponding to the onset of slew-rate limiting is such that  $V_{om(\text{crit})}/\tau = SR$ . Since  $\tau = 1/(2\pi f_t)$ ,

$$V_{om(\text{crit})} = \frac{SR}{2\pi f_t}. \quad (5)$$

- What are the  $SR$ ,  $t_R$ ,  $\tau$  and  $V_{om(\text{crit})}$  for the  $\mu\text{A}741$  op amp?
- Investigate the response to an input step of 30 mV.
- Investigate the response to an input step of 0.8 V.

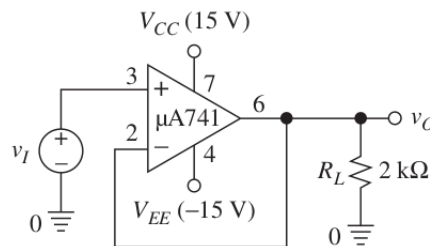


Figure 4: Voltage follower.

# μA741

## FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

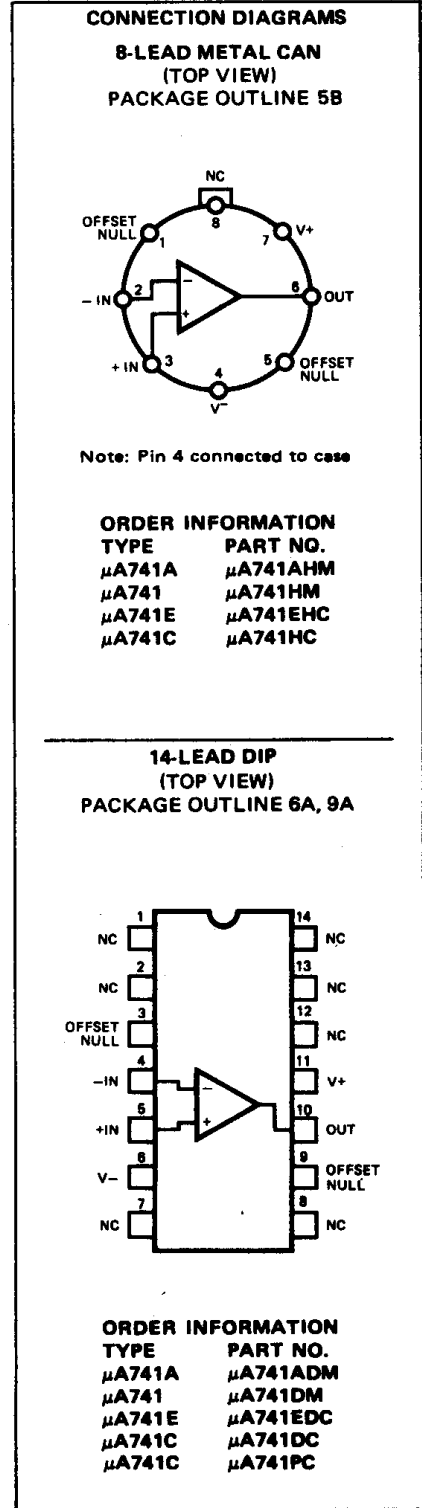
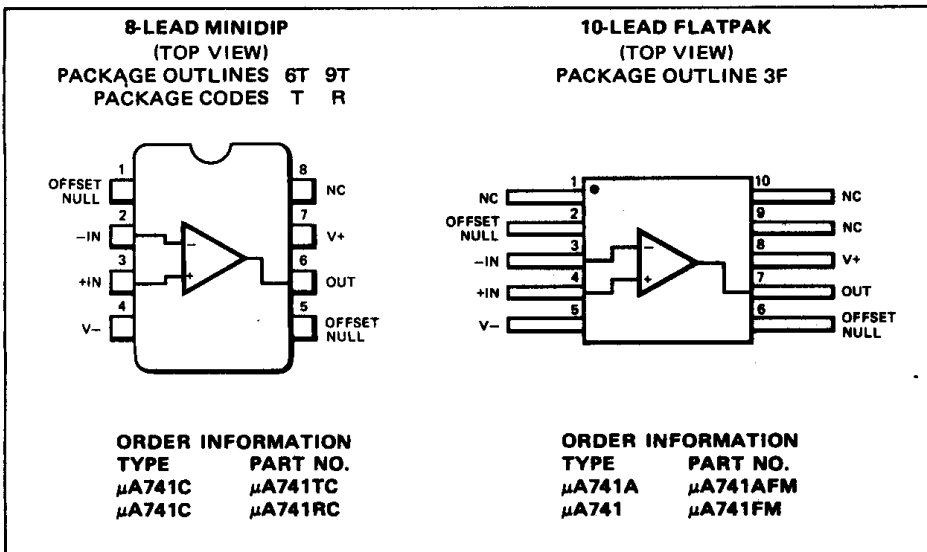
### FAIRCHILD LINEAR INTEGRATED CIRCUIT

**GENERAL DESCRIPTION** — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar\* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. Electrical characteristics of the μA741A and E are identical to MIL-M-38510/10101.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage		
μA741A, μA741, μA741E		±22 V
μA741C		±18 V
Internal Power Dissipation (Note 1)		
Metal Can	500 mW	
Molded and Hermetic DIP	670 mW	
Mini DIP	310 mW	
Flatpak	570 mW	
Differential Input Voltage		±30 V
Input Voltage (Note 2)		±15 V
Storage Temperature Range		
Metal Can, Hermetic DIP, and Flatpak	-65°C to +150°C	
Mini DIP, Molded DIP	-55°C to +125°C	
Operating Temperature Range		
Military (μA741A, μA741)	-55°C to +125°C	
Commercial (μA741E, μA741C)	0°C to +70°C	
Lead Temperature (Soldering)		
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C	
Molded DIPs (10 s)	260°C	
Output Short Circuit Duration (Note 3)		Indefinite



Notes on following pages.

\*Planar is a patented Fairchild process.

12

**FAIRCHILD LINEAR INTEGRATED CIRCUITS •  $\mu$ A741**

**$\mu$ A741**

**ELECTRICAL CHARACTERISTICS** ( $V_S = \pm 15$  V,  $T_A = 25^\circ$  C unless otherwise specified)

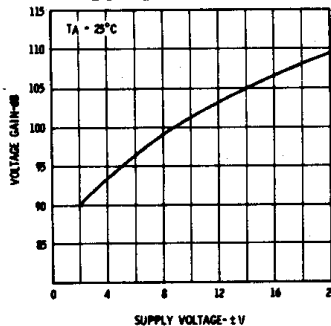
PARAMETERS (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S < 10$ k $\Omega$		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M $\Omega$
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			$\pm 15$		mV
Large Signal Voltage Gain	$R_L > 2$ k $\Omega$ , $V_{OUT} = \pm 10$ V	50,000	200,000		
Output Resistance			75		$\Omega$
Output Short Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain)	$V_{IN} = 20$ mV, $R_L = 2$ k $\Omega$ , $C_L < 100$ pF	Rise time	0.3		$\mu$ s
		Overshoot	5.0		%
Slew Rate	$R_L > 2$ k $\Omega$		0.5		V/ $\mu$ s

The following specifications apply for  $-55^\circ$  C  $< T_A < +125^\circ$  C:

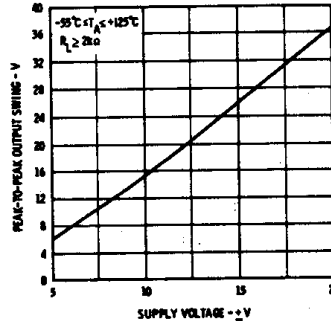
Input Offset Voltage	$R_S < 10$ k $\Omega$		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ$ C		7.0	200	nA
	$T_A = -55^\circ$ C		85	500	nA
Input Bias Current	$T_A = +125^\circ$ C		0.03	0.5	$\mu$ A
	$T_A = -55^\circ$ C		0.3	1.5	$\mu$ A
Input Voltage Range		$\pm 12$	$\pm 13$		V
Common Mode Rejection Ratio	$R_S < 10$ k $\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S < 10$ k $\Omega$		30	150	$\mu$ V/V
Large Signal Voltage Gain	$R_L > 2$ k $\Omega$ , $V_{OUT} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L > 10$ k $\Omega$	$\pm 12$	$\pm 14$		V
	$R_L > 2$ k $\Omega$	$\pm 10$	$\pm 13$		V
Supply Current	$T_A = +125^\circ$ C		1.5	2.5	mA
	$T_A = -55^\circ$ C		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ$ C		45	75	mW
	$T_A = -55^\circ$ C		60	100	mW

**TYPICAL PERFORMANCE CURVES FOR  $\mu$ A741A AND  $\mu$ A741**

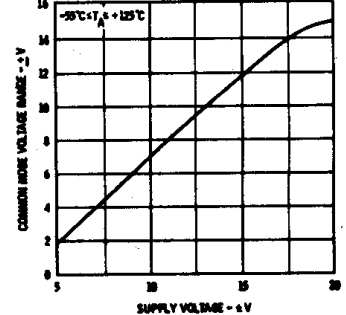
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE**



**OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE**



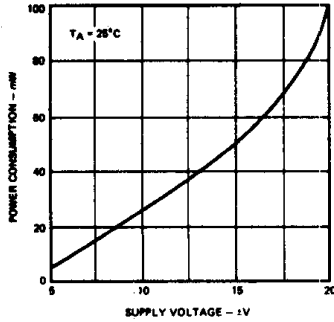
**INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



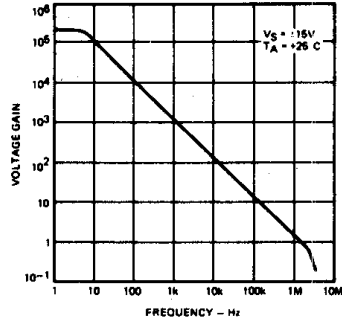
# FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu$ A741

## TYPICAL PERFORMANCE CURVES FOR $\mu$ A741A, $\mu$ A741, $\mu$ A741E AND $\mu$ A741C

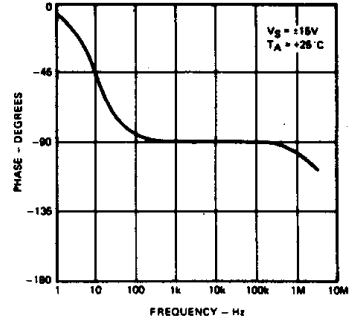
**POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE**



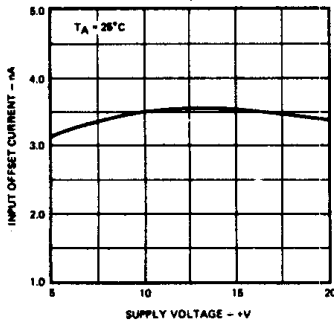
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**



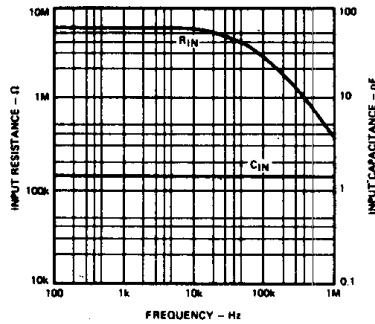
**OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY**



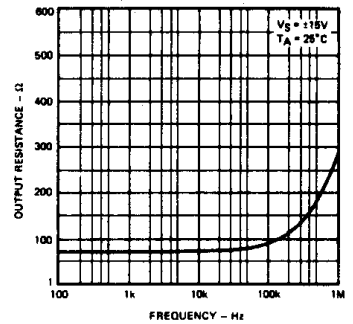
**INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



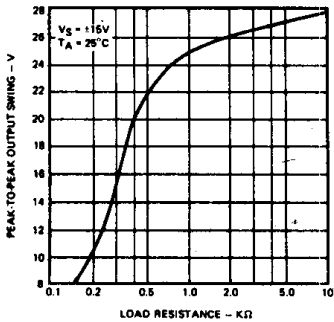
**INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY**



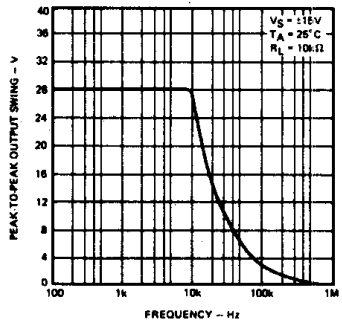
**OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY**



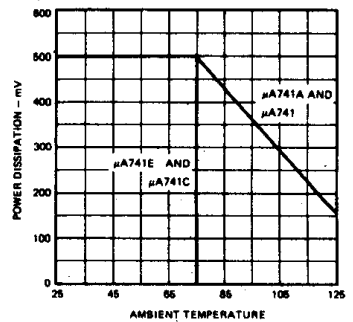
**OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE**



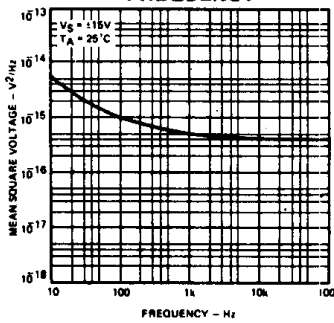
**OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY**



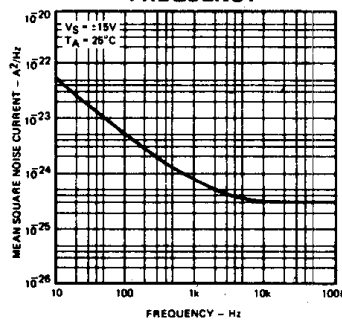
**ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE**



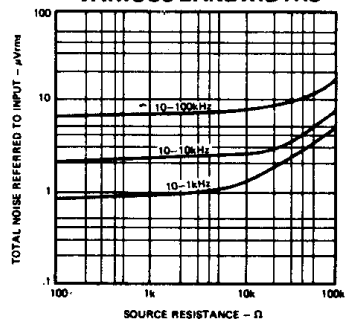
**INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY**



**INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY**

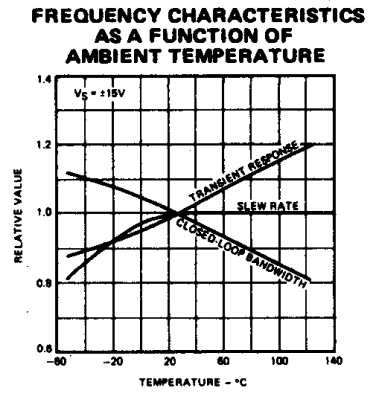
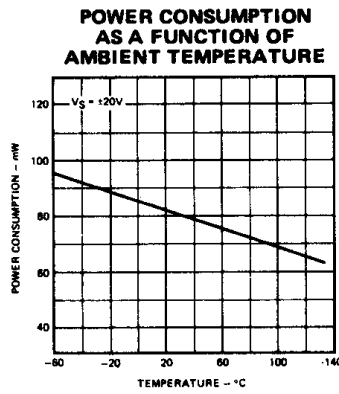
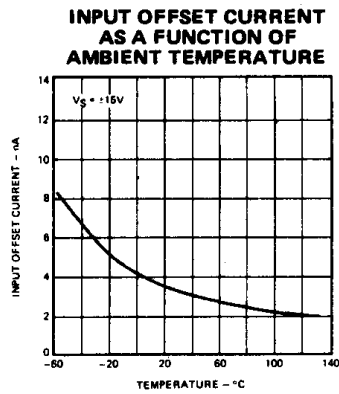
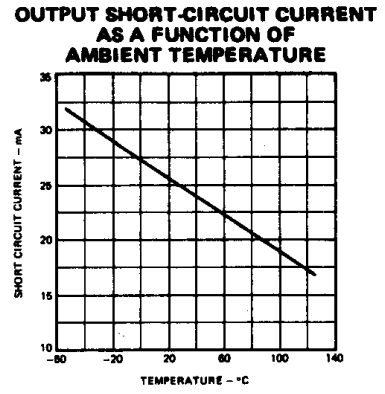
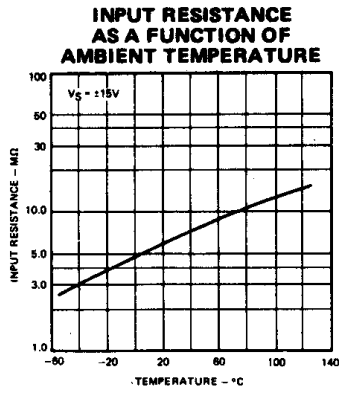
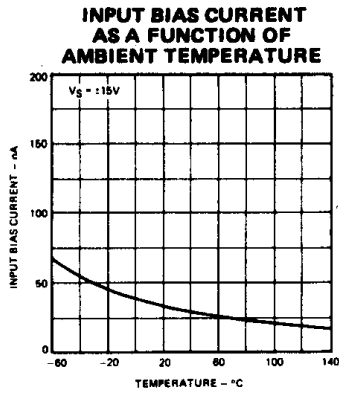


**BROADBAND NOISE FOR VARIOUS BANDWIDTHS**

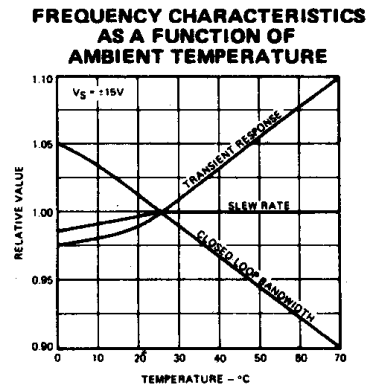
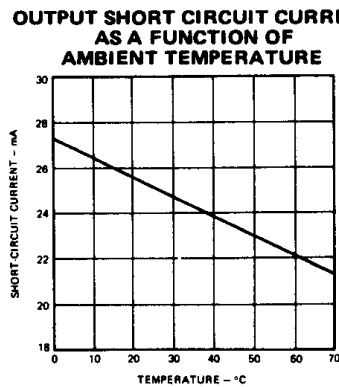
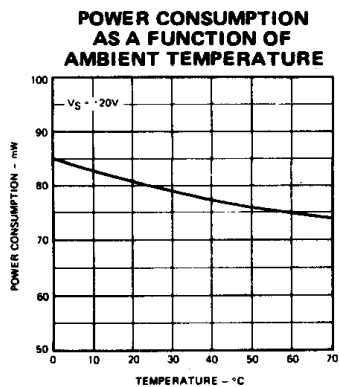
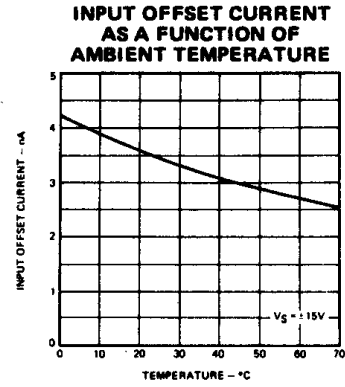
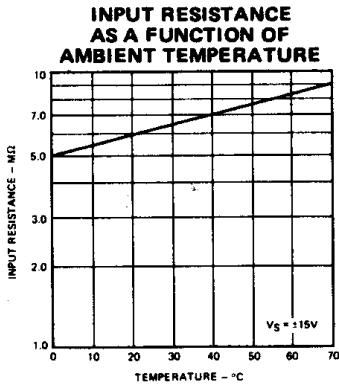
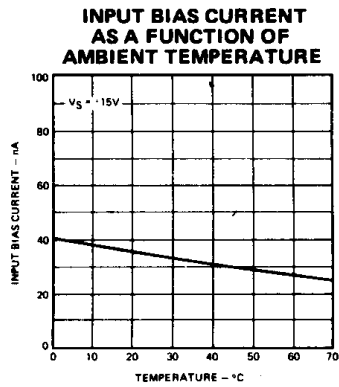


FAIRCHILD LINEAR INTEGRATED CIRCUITS •  $\mu$ A741

TYPICAL PERFORMANCE CURVES FOR  $\mu$ A741A AND  $\mu$ A741



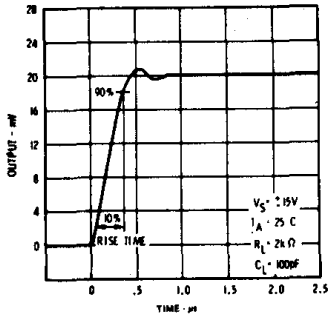
TYPICAL PERFORMANCE CURVES FOR  $\mu$ A741E AND  $\mu$ A741C



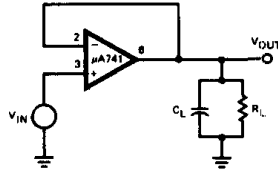
12

# FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A741$

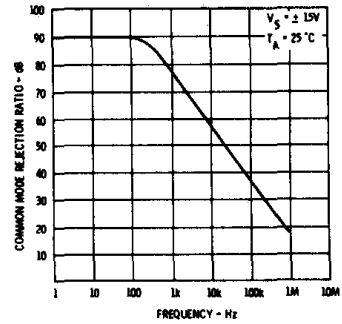
**TRANSIENT RESPONSE**



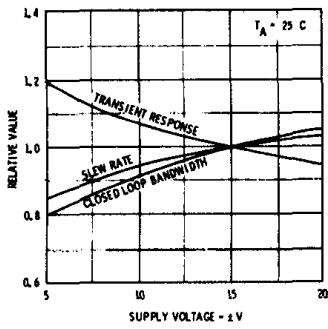
**TRANSIENT RESPONSE TEST CIRCUIT**



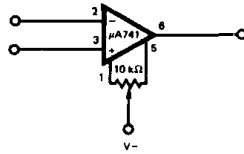
**COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY**



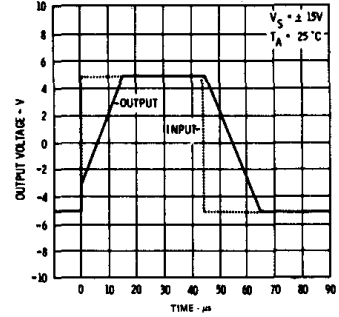
**FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE**



**VOLTAGE OFFSET NULL CIRCUIT**

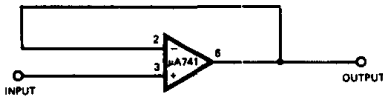


**VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE**



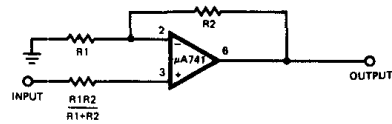
## TYPICAL APPLICATIONS

**UNITY-GAIN VOLTAGE FOLLOWER**



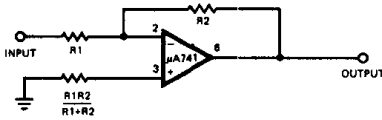
$R_{IN} = 400 \text{ M}\Omega$   
 $C_{IN} = 1 \text{ pF}$   
 $R_{OUT} \ll 1 \Omega$   
 $B.W. = 1 \text{ MHz}$

**NON-INVERTING AMPLIFIER**



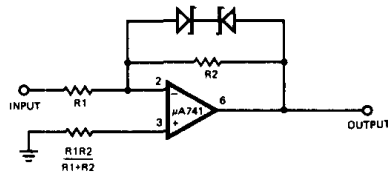
GAIN	R1	R2	BW	R <sub>IN</sub>
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

**INVERTING AMPLIFIER**



GAIN	R1	R2	BW	R <sub>IN</sub>
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

**CLIPPING AMPLIFIER**



$$\frac{E_{OUT}}{E_{IN}} = \frac{R_2}{R_1} \text{ if } |E_{OUT}| < V_Z + 0.7 \text{ V}$$

where  $V_Z$  = Zener breakdown voltage