Smart Sensors for IoT
Exercise 5 (17.11.2021)

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Problem 1 Input bias and offset currents

The circuit of Fig. 1 is to be used as an inverting amplifier with a gain of 10 V/V and is to employ the μA741 op amp (the datasheet is appended at the end of the exercises).

- Specify suitable component values to ensure a maximum output error of 10 mV.

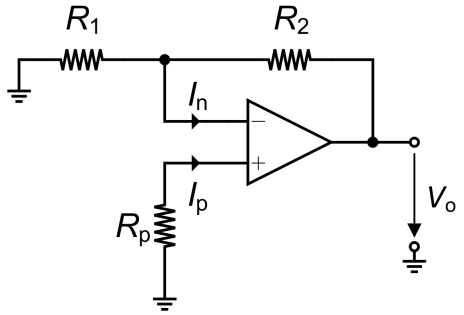


Figure 1: System to estimate the output error due to the input bias currents for the case of resistive feedback.

Problem 2 Common-Mode Rejection Ratio (CMRR)

The difference amplifier of Fig. 2 uses a μA741 op amp and a perfectly matched resistance set with $R_1 = R_3 = 10\,\text{k}\Omega$ and $R_2 = R_4 = 100\,\text{k}\Omega$. Suppose the inputs are tied together and driven with a common signal V_I . Estimate the typical change in V_O if:

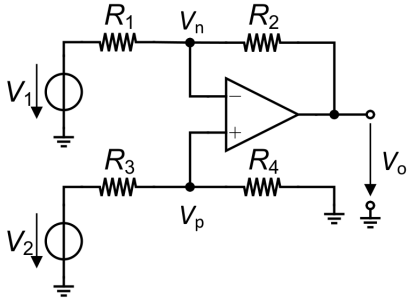


Figure 2: Difference amplifier.

- V_I is slowly changed from 0 to 10 V;

- V_I is a 10 kHz, 5 V 0-peak sine wave.

Hint: the output voltage can be rewritten as:

$$V_O = A_{dm}\left(V_{i+} - V_{i-} + \frac{A_{cm}}{A_{dm}}V_{ic}\right) \tag{1}$$

Problem 3 Power-Supply Rejection Ratio (PSRR)

A μA741 op amp is connected as in Fig. 1 with $R_1 = 100\,\Omega$ and $R_2 = 100\,\text{k}\Omega$.

- Predict the typical as well as the maximum ripple at the output for a power-supply ripple ΔV_{DD} of 0.05 Vp at 120 Hz (assume ideal V_{SS}).

Hint: The μA741 datasheets do not show the PSRR rolloff with frequency, so let us use the ratings given at dc, keeping in mind that the results will be optimistic.

Problem 4 Single-Pole Open-Loop Gain

With respect to the non-ideal op-amp frequency response, we shall make the simplifying assumption that the open-loop gain $a(s)$ possesses just a single pole. Such a gain shall be expressed in the form:

$$a(s) = \frac{a_0}{1 + s/\omega_b} = \frac{a_0}{1 + jf/f_b}; \tag{2}$$

where s is the complex frequency, a_0 is the open-loop dc gain, and $-\omega_b$ is the s-plane pole location. Equivalently, in the second half of the equation, we express gain in terms of the frequency f, where j is the imaginary unit, and $f_b = \omega_b/(2\pi)$ is the open-loop −3-dB frequency, also called the open-loop bandwidth. We calculate gain magnitude and phase as:

$$|a(jf)| = \text{mag}\, a(jf) = \frac{a_0}{\sqrt{1 + (f/f_b)^2}}; \tag{3}$$

$$\sphericalangle a(jf) = \text{ph}\, a(jf) = -\arctan(f/f_b). \tag{4}$$

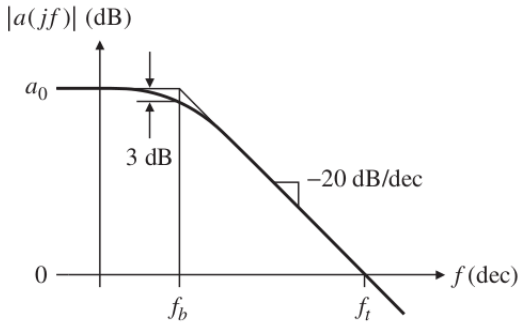


Figure 3: Single-pole open-loop gain.The frequency axis is on a logarithmic-base-10 scale.

Magnitude is plotted in Fig. 3. The gain is high and approximately constant only from dc up to f_b. Past f_b it rolls off at the rate of $-20\,\text{dB/dec}$, until it drops to $0\,\text{dB}$ (or $1\,\text{V/V}$) at $f = f_t$.

- Calculate f_t by imposing $1 = a_0/\sqrt{1 + (f_t/f_b)^2}$. *Hint: notice that* $f_t \gg f_b$
- According to the µA741 datasheet, what are the typical a_0 (called *large signal voltage gain*), f_b and f_t values?
- Calculate the module and phase of $a(s)$ when $f \ll f_b$, $f = f_b$ and $f \gg f_b$.
- Consider another amplifier than the µA741, which has a magnitude of $80\,\text{dB}$ at $f = 10\,\text{Hz}$ and a phase angle of $-58°$ at $f = 320\,\text{Hz}$. Estimate a_0, f_b, and f_t.

Problem 5 Slew rate

Suppose a µA741 op amp is configured as voltage follower (Fig. 4). We stress that SR is a nonlinear large-signal parameter, while t_R is a linear small-signal parameter. The critical output-step magnitude corresponding to the onset of slew-rate limiting is such that $V_{om(\text{crit})}/\tau = SR$. Since $\tau = 1/(2\pi f_t)$,

$$V_{om(\text{crit})} = \frac{SR}{2\pi f_t}. \tag{5}$$

- What are the SR, t_R, τ and $V_{om(\text{crit})}$ for the µA741 op amp?
- Investigate the response to an input step of $30\,\text{mV}$.
- Investigate the response to an input step of $0.8\,\text{V}$.

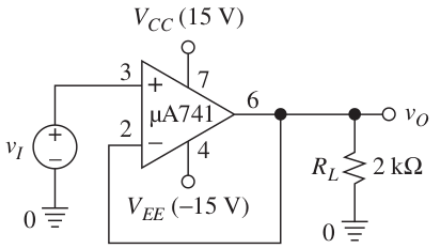


Figure 4: Voltage follower.

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

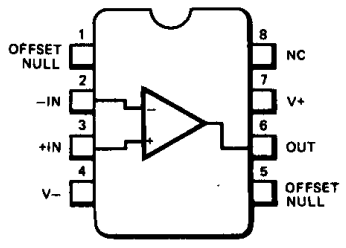
GENERAL DESCRIPTION — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. Electrical characteristics of the μA741A and E are identical to MIL-M-38510/10101.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Hermetic DIP, and Flatpak	−65°C to +150°C
Mini DIP, Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA741A, μA741)	−55°C to +125°C
Commercial (μA741E, μA741C)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

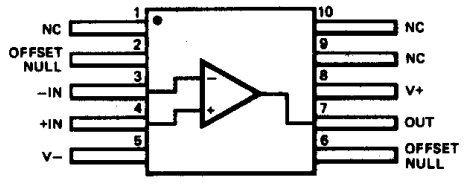
8-LEAD MINIDIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
μA741C	μA741TC
μA741C	μA741RC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F

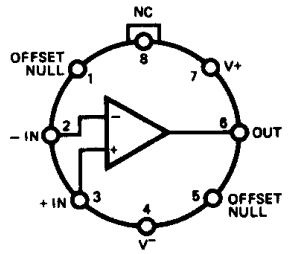


ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AFM
μA741	μA741FM

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B

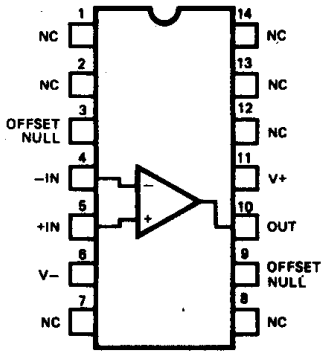


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AHM
μA741	μA741HM
μA741E	μA741EHC
μA741C	μA741HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741ADM
μA741	μA741DM
μA741E	μA741EDC
μA741C	μA741DC
μA741C	μA741PC

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Notes on following pages.

*Planar is a patented Fairchild process.

μA741

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	50,000	200,000		
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2\ k\Omega$		0.5		V/μs

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current	T_A = +125°C		7.0	200	nA
	T_A = −55°C		85	500	nA
Input Bias Current	T_A = +125°C		0.03	0.5	μA
	T_A = −55°C		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000			
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current	T_A = +125°C		1.5	2.5	mA
	T_A = −55°C		2.0	3.3	mA
Power Consumption	T_A = +125°C		45	75	mW
	T_A = −55°C		60	100	mW

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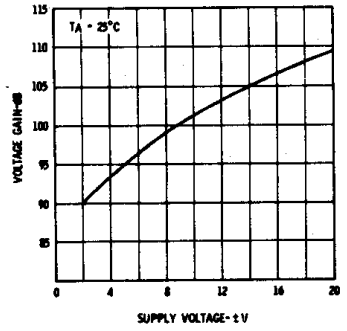
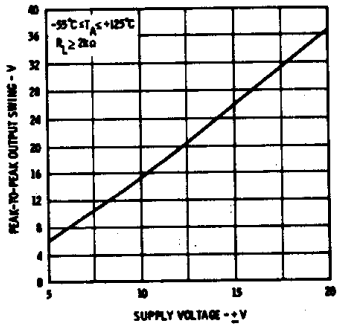
TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

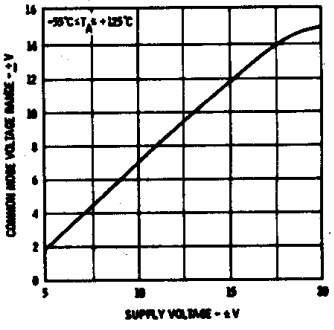
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

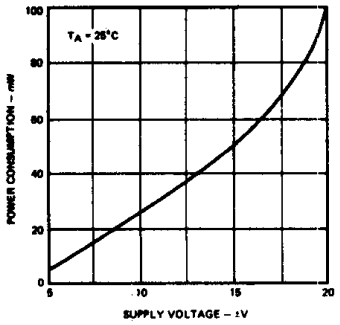


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

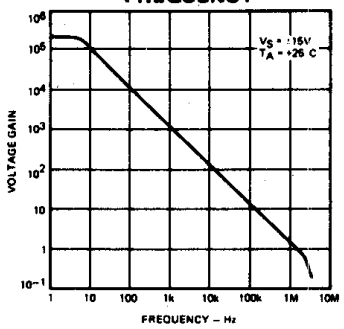


TYPICAL PERFORMANCE CURVES FOR μA741A, μA741, μA741E AND μA741C

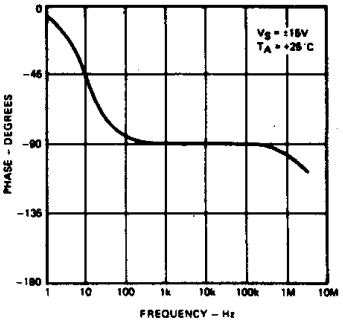
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



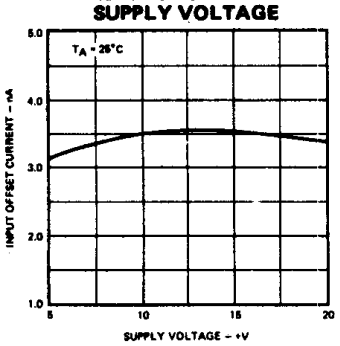
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



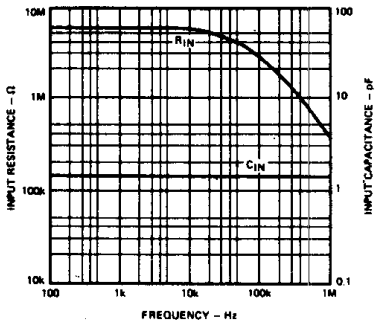
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



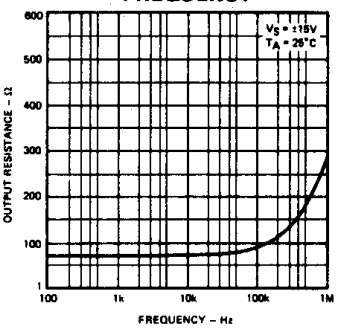
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



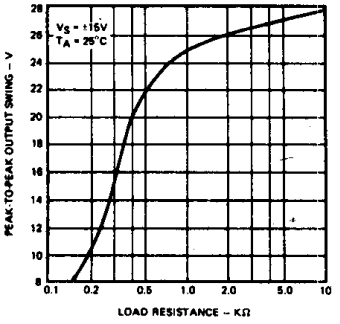
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



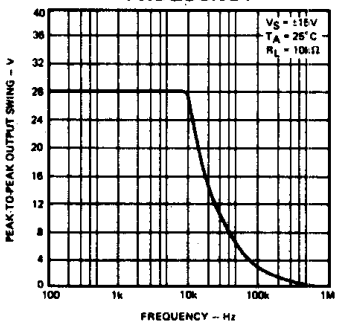
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



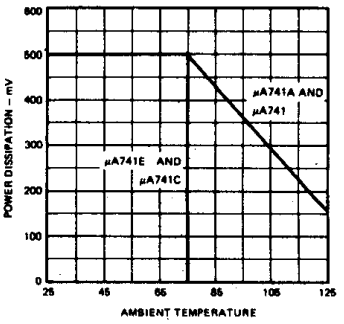
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



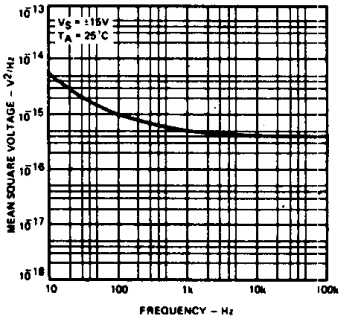
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



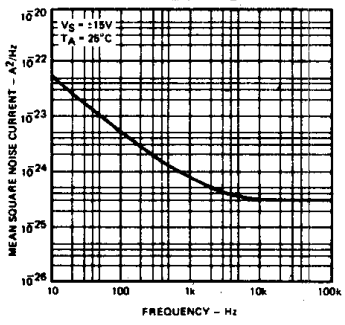
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



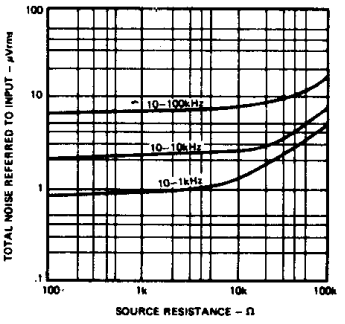
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

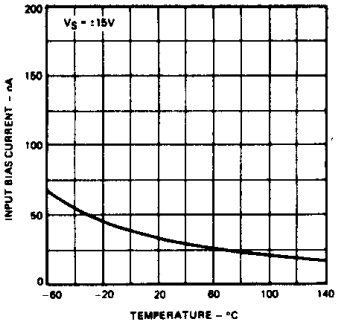


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

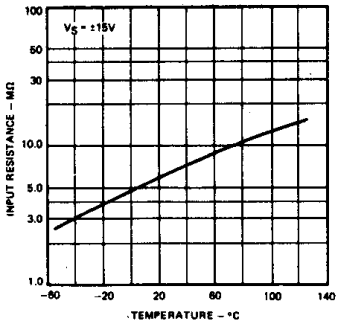


TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

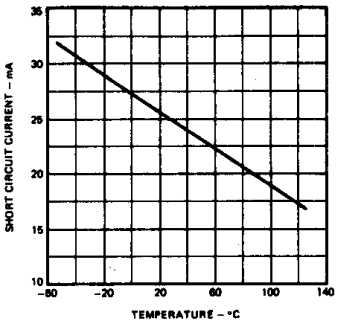
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



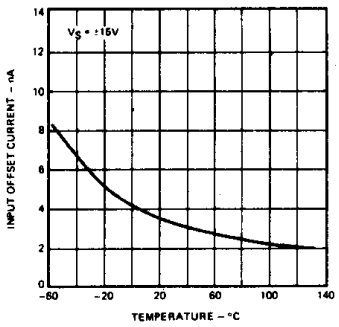
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



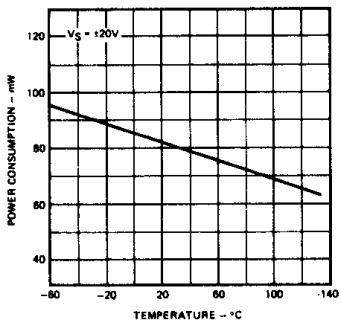
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



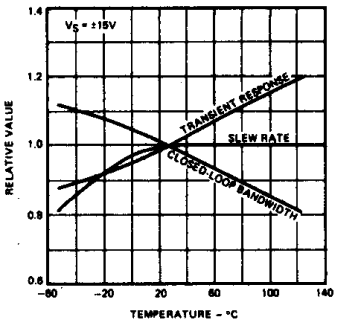
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

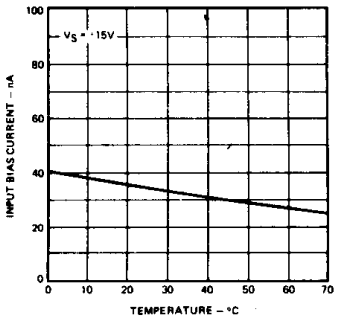


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

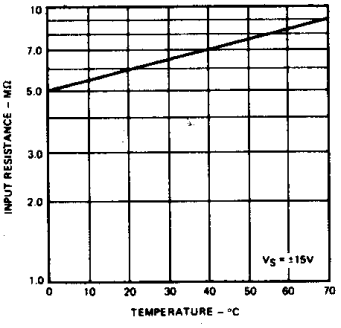


TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

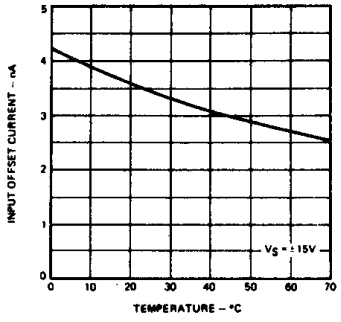
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



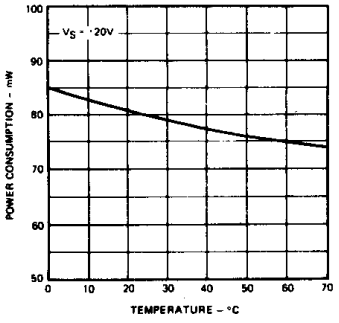
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



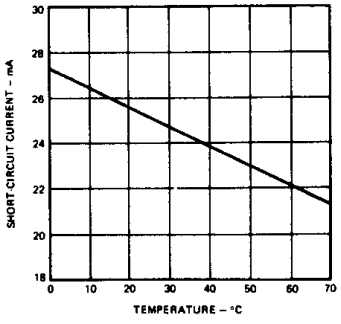
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



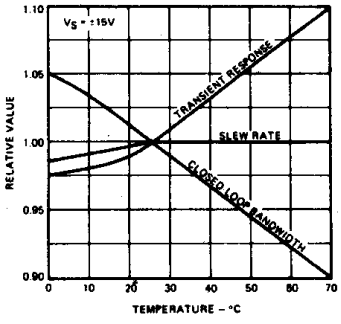
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



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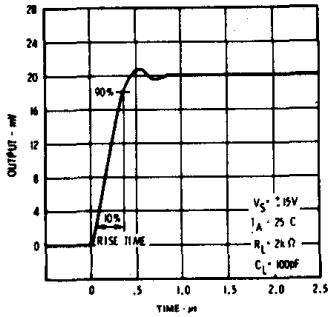
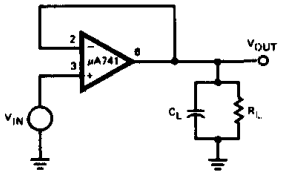
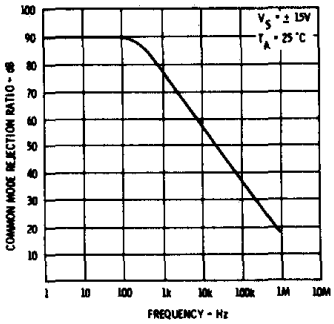
TRANSIENT RESPONSE



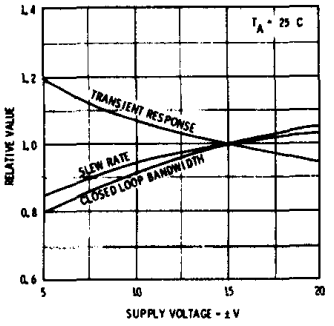
TRANSIENT RESPONSE TEST CIRCUIT



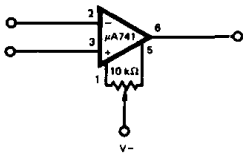
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



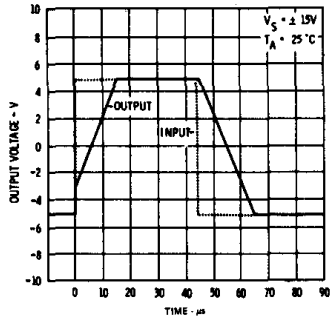
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

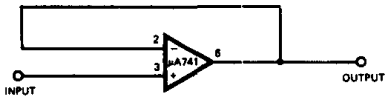


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



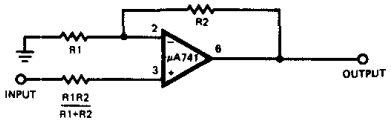
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



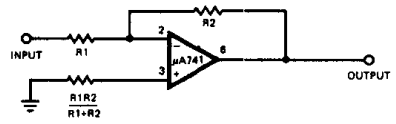
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{OUT} << 1 Ω
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



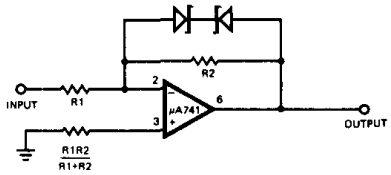
GAIN	R1	R2	B W	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R1	R2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER



$$\frac{E_{OUT}}{E_{IN}} = \frac{R2}{R1} \text{ if } |E_{OUT}| \leq V_Z + 0.7\ V$$

where V_Z = Zener breakdown voltage

Solutions to Exercise 5 (17.11.2021)

Problem 1 Input bias and offset currents

The circuit of Fig. 1 is to be used as an inverting amplifier with a gain of 10 V/V and is to employ the μA741 op amp (the datasheet is appended at the end of the exercises).

- Specify suitable component values to ensure a maximum output error of 10 mV.

In order to get a gain of 10 V/V, $R_2 = 10 \cdot R_1$ and $R_{12} = R_1 \parallel R_2 = 10/11 R_1$.

According to the course notes, output voltage is given by:

$$V_0 = \left(1 + \frac{R_2}{R_1}\right) \cdot [(R_{12} - R_p) \cdot I_B - (R_{12} + R_p) \cdot I_{os}/2]\,; \tag{6}$$

The effect of the bias current can be eliminated by choosing $R_p = R_1 \parallel R_2 = 0.91 R_1$ leaving only the effect of the input current mismatch I_{os}.

Based on the datasheet, the maximum I_{os} is 200 nA, therefore

$$V_0 = \left(1 + \frac{R_2}{R_1}\right) \cdot R_{12} I_{os} = 10\,\text{mV}; \tag{7}$$

which yields to $R_1 = 5\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$ and $R_p = 4.55\,\text{k}\Omega$

Problem 2 Common-Mode Rejection Ratio (CMRR)

The difference amplifier of Fig. 2 uses a μA741 op amp and a perfectly matched resistance set with $R_1 = R_3 = 10\,\text{k}\Omega$ and $R_2 = R_4 = 100\,\text{k}\Omega$. Suppose the inputs are tied together and driven with a common signal V_I . Estimate the typical change in V_O if:

- V_I is slowly changed from 0 to 10 V;

Since $R_4 = R_2$ and $R_3 = R_1$, then $V_o = R_2/R_1(V_2 - V_1)$. The unique characteristics of the difference amplifier are better appreciated if we introduce the differential-mode and the common-mode input components, defined as

$$V_{id} = V_2 - V_1 \qquad V_{ic} = \frac{V_1 + V_2}{2}. \tag{8}$$

Inverting these equations, we can express the actual inputs in terms of the newly defined components:

$$V_1 = V_{ic} - \frac{V_{id}}{2} \qquad V_2 = V_{ic} + \frac{V_{id}}{2}. \tag{9}$$

If we tie the inputs together to make $V_{id} = 0$, and we apply a common voltage $V_{ic} \neq 0$, a true difference amplifier will yield $V_o = 0$ regardless of the magnitude and polarity of V_{ic} . Conversely, this can serve as a test for finding how close a practical difference amplifier is to ideal. The smaller the output variation is because of a given variation of V_{ic}, the closer the amplifier is to ideal. The ratio between the differential-mode gain A_{dm} and the common-mode gain A_{cm} (ideally infinitive) is called the common-mode rejection ratio (CMRR).

Equation (1) can be rewritten as:

$$V_O = A_{dm}\left(V_{i+} - V_{i-} + \underbrace{\frac{V_{ic}}{\text{CMRR}}}_{V_{offset}}\right); \tag{10}$$

since op amps keep V_{i-} fairly close to V_{i+} , we can write $V_{ic} \approx V_{i+}$.

At dc we have $1/\text{CMRR} = 10^{-90/20} = 31.6\,\mu\text{V/V}$, typical. The common-mode change at the op amp input pins is:

$$\Delta V_{i+} = \frac{R_2}{R_1 + R_2}\Delta V_I = \frac{100}{10 + 100}10 = 9.09\,\text{V}. \tag{11}$$

Thus,

$$V_{offset} = \frac{V_{i+}}{\text{CMRR}} = 31.6 \cdot 9.09 = 287\,\mu\text{V}. \tag{12}$$

The dc gain is $1 + R_2/R_1 = 11\,\text{V/V}$. Hence, $V_O = 11 \cdot 287\,\mu\text{V} = 3.16\,\text{mV}$.

- V_I is a 10 kHz, 5 V 0-peak sine wave.

From the CMRR curve in the datasheet we find CMRR in dB at 10 kHz approximately 57 dB. Therefore

$$1/\text{CMRR} = 10^{-57/20} = 1.41\,\text{mV/V} \qquad V_{offset} = 1.41 \cdot 4.545 = 6.4\,\text{mVp} \qquad V_O = 11 \cdot 6.4 = 70.5\,\text{mVp} \tag{13}$$

The output error at 10 kHz is much worse than at dc.

Problem 3 Power-Supply Rejection Ratio (PSRR)

A µA741 op amp is connected as in Fig. 1 with $R_1 = 100\,\Omega$ and $R_2 = 100\,\text{k}\Omega$.

- Predict the typical as well as the maximum ripple at the output for a power-supply ripple ΔV_{DD} of 0.05 Vp at 120 Hz (assume ideal V_{SS}).

Hint: The µA741 datasheets do not show the PSRR rolloff with frequency, so let us use the ratings given at dc, keeping in mind that the results will be optimistic.

According to the datasheets, the Supply Voltage Rejection Ratio is typically 30 µV/V and maximum 150 µV/V. The induced ripple at the op amp input is:

$$V_{offset}|_{\text{typ}} = 30\,\mu\text{V/V} \cdot 0.05\,\text{Vp} = 1.5\,\mu\text{Vp typical}; \tag{14a}$$
$$V_{offset}|_{\text{max}} = 150\,\mu\text{V/V} \cdot 0.05\,\text{Vp} = 7.5\,\mu\text{Vp maximum}. \tag{14b}$$

The stage gain is $1 + R_2/R_1 \approx R_2/R_1 = 1000\,\mathrm{V/V}$, therefore:

$$V_O|_{\mathrm{typ}} = 1000\,\mathrm{V/V} \cdot 1.5\,\mu\mathrm{V} = 1.5\,\mathrm{mVp\ typical;} \tag{15a}$$
$$V_O|_{\mathrm{max}} = 1000\,\mathrm{V/V} \cdot 7.5\,\mu\mathrm{Vp} = 7.5\,\mathrm{mVp\ maximum.} \tag{15b}$$

Problem 4 Single-Pole Open-Loop Gain

- Calculate f_t by imposing $1 = a_0/\sqrt{1 + (f_t/f_b)^2}$. *Hint: notice that* $f_t \gg f_b$

Since $f_t \gg f_b$, $1 + (f_t/f_b)^2 \approx (f_t/f_b)^2$, therefore:

$$f_t = a_0 f_b. \tag{16}$$

- According to the μA741 datasheet, what are the typical a_0 (called *large signal voltage gain*), f_b and f_t values?

The typical gain given in the datasheet is $25\,000\,\mathrm{V/V}$, which translates to 88 dB. From the *OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF THE FREQUENCY* plot, $f_t \approx 1\,\mathrm{MHz}$, and $f_b \approx 190\,\mathrm{Hz}$ (verified by (16)).

- Calculate the module and phase of $a(s)$ when $f \ll f_b$, $f = f_b$ and $f \gg f_b$.

$$a(jf)|_{f \ll f_b} \to a_0 \underline{/0^\circ}; \tag{17a}$$
$$a(jf)|_{f = f_b} \to \frac{a_0}{\sqrt{2}} \underline{/-45^\circ}; \tag{17b}$$
$$a(jf)|_{f \gg f_b} \to \frac{f_t}{f} \underline{/-90^\circ}. \tag{17c}$$

- Consider another amplifier than the μA741, which has a magnitude of 80 dB at $f = 10\,\mathrm{Hz}$ and a phase angle of -58° at $f = 320\,\mathrm{Hz}$. Estimate a_0, f_b, and f_t.

By applying (4),

$$-\arctan\left(\frac{320}{f_b}\right) = -58^\circ \to f_b = 200\,\mathrm{Hz}. \tag{18}$$

Considering that $10\,\mathrm{Hz} \ll f_b$, $a_0 = 80\,\mathrm{dB} = 1 \times 10^4\,\mathrm{V/V}$, and therefore $f_t = a_0 f_b = 2\,\mathrm{MHz}$.

Problem 5 Slew rate

Suppose μA741 op amp is configured as voltage follower (Fig. 4).

- What are the *SR*, t_R, τ and $V_{om(\mathrm{crit})}$ for the μA741 op amp?

According to the datasheets, $SR = 0.5\,\mathrm{V/\mu s}$, $t_R = 0.3\,\mu\mathrm{s}$, $\tau = 1/(2\pi f_t) = 0.16\,\mu\mathrm{s}$ and $V_{om(\mathrm{crit})} = 80\,\mathrm{mV}$.

- Investigate the response to an input step of 30 mV.

Subjecting the voltage follower to an input voltage step smaller than $V_{om(\mathrm{crit})}$ will result in the well-known exponential response:

$$V_O = V_I \left(1 - e^{-t/\tau}\right); \tag{19}$$

which is plotted in Fig. 5

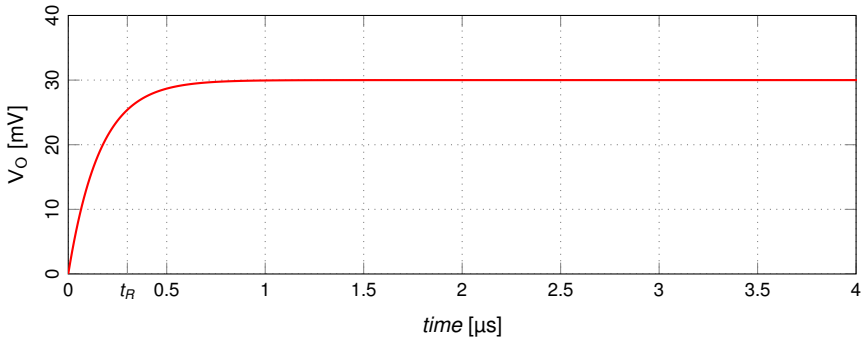


Figure 5: Voltage follower time response to a 30 mV step

- Investigate the response to an input step of 0.8 V.

Since the input step of 0.8 V exceeds $V_{om(\mathrm{crit})}$, the output slews at a constant rate of $0.5\,\mathrm{V/\mu s}$ until it comes within 80 mV of the final value, after which it performs the remainder of the transition in approximately exponential fashion. This is shown in Fig. 6.

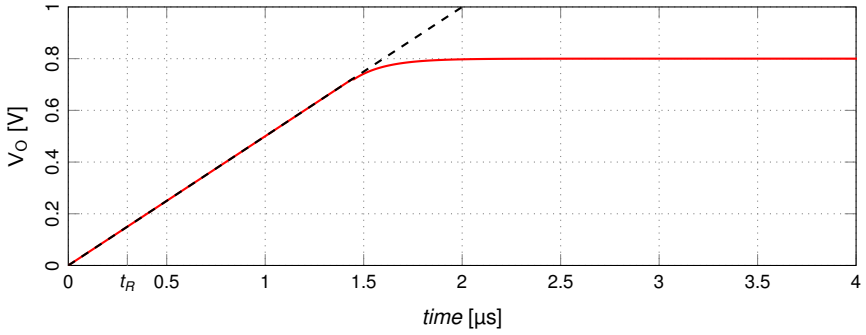


Figure 6: Voltage follower time response to a 800 mV step. The dashed line represents the slew-rate ramp.