Institute of Electrical and Microengineering
Biomedical and neuromorphic microelectronic systems

Test of VLSI Systems2025, MNIS-MA3, EL-MA1, EL-MA3. EE530-2025-FWEP-v1.1.fm
v1.0 A. Schmid 2024, November 5 v1.1 A. Schmid 2025, October 23

TEST OF VLSI SYSTEMS
FINAL WRITTEN EXAMINATION POLICIES

1. TIME AND PLACE

The duration of the final written examination is two hours.

The final written examination is scheduled by the Service Académique. Please check the web site of Service Académique prior to taking the exam, since the date and time may be changed.

http://is-academia.epfl.ch/

Provisionally, the examination has been scheduled by SAC on Wednesday, **January 21, 2025**, from 10:15 through 11:15, in classrooms GC A3 30 and GC A3 31.

It is your responsability to cross-check !

2. TOPICS

Full course, including the content of lectures, exercises, and practical laboratory sessions.

Following topics **are part** of the written examination.

Class #1 topics (full): Motivation for testing, economy of test, ATE, Yield and Defect level

Class #2 topics (full): Fault modeling

Class #3 topics (partial): Fault simulation, types of fault simulators, levelization, serial, parallel and deductive fault simulation

Class #4 topics (full): Testability measures, combinational and sequential SCOAP (the theory of sequential SCOAP is included !)

Class #5 topics (full): ATPG, combinational and sequential ATPG, search space abstractions, D-calculus and D-agorithm, concept of PODEM, time-frame expansion

Class #6 topics (full): Design for testability, scan-path design, JTAG boundary-scan

Class #7 topics (full): BIST I, LFSRs

Class #8 topics (full): BIST II, response/signature analysis, MISR, BILBO

Class #9 topics (full): memory faults, memory tests including march tests, Iddq.

Exercise #1, exercise #2, exercise #3, exercise #4, exercise #5, exercise#6, exercise#7.

Practical laboratory sessions are part of the written exam: be able to explain the concepts you have applied.

Following topics are **not** part of the written examination

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Station N° 11
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https://bnms.epfl.ch

Class #3 topics (partial): Concurrent fault simulation and fault sampling

Class #4 topics (partial): no exercise on sequential SCOAP will be proposed (the theory however, is in)

Class #9 topics (partial): slides 37-42 on delay-fault test generation.

(the class #, and exercise # refers to the number printed on the first page of the handout slides and exercises.)

3. EXAMINATION POLICIES

The final examination will be conducted as a closed-book examination. The examination will consist of theoretical questions to be answered (short and detailed), as well as exercises to be solved.

Student's ID card are controlled during the examination. Please place your student's ID on the forefront of the table.

No question will be answered during the examination time. Should you be in situation of uncertainty, please carefully formulate all hypothesis or assumptions you are stating.

4. DISTRIBUTED ITEMS

The examination documents including scratch paper (working sheets) will be distributed.

The formulary consisting of an arrangement of course transparencies, and provided with the Midterm Exam Policies document and the Midterm Exam will be distributed along with the examination documents.

5. RECOMMENDED ITEMS

Please make sure to bring pens, pencils.

6. FORBIDDEN ITEMS

No written document of any sort may be taken to the examination (no book, no transparencies, no handwritten notes, etc.). Blank paper will be provided.

Usage of information processing and telecommunication devices in a general sense is not permitted (no computer, no hand calculator, no electronic agenda, no cell phone, etc.).

7. GRADING

The final is graded, and accounts for 50% of the course grade.

8. COURSE WEB SITE

Please check the course web site on a regular basis.

URL: http://moodle.epfl.ch/course/view.php?id=293

Test of VLSI Systems
Final written examination

Formulary

This document must be returned along with the examination documents

Cost of production test (1)

$$\text{Testing cost} = N_c \cdot C_s \cdot T_m$$

N_c = total number of circuits
C_s = cost of testing per second
T_m = mean time of testing per circuit

$$T_m = \sum_{i=1}^{n} T_i (1 - P_{i-1})$$

n = number of test vectors
T_i = processing time for test number i
$P_{(i-1)}$ = probability of a defect to be detected during the application of tests prior to test i

Cost of production test (2)

$$C_s = ((D_t + D_h) + M_t + O_t) \cdot \left(\frac{1}{T_{test,per}}\right) \cdot \left(\frac{T_{prod,per} + T_{down,per} + T_{idle,per}}{T_{prod,per}}\right)$$

total annual cost | testing time (s) | occupation rate

C_s = cost of testing per second
D_t, D_h = depreciation of tester and handler over the period $T_{test,per}$:
$D_t + D_h = C_t / (T_{test,tot} / T_{test,per})$ (linear depreciation)
C_t = fixed cost of tester
M_t = maintenance cost
O_t = operating cost and personnel (building, facilities, auxiliary equipment)
$T_{test,tot}$ = total testing time (typically given in years
$T_{test,per}$ = testing time during period per (typically given in weeks)
$T_{prod,per}$ = usage time of tester during period per
$T_{down,per}$ = down time of tester during period per
$T_{idle,per}$ = idle time of tester during period per

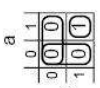
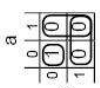
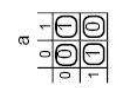
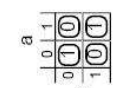
Fault list propagation rules

propagation rules for main Boolean gates in a deductive fault simulator

Gate	Input a	Input b	output z	output fault list L_z
AND	0	0	0	$[L_a \cap L_b] \cup z_1$
	0	1	0	$[L_a \cap \overline{L_b}] \cup z_1$
	1	0	0	$[\overline{L_a} \cap L_b] \cup z_1$
	1	1	1	$[L_a \cup L_b] \cup z_0$
OR	0	0	0	$[L_a \cup L_b] \cup z_1$
	0	1	1	$[\overline{L_a} \cap L_b] \cup z_0$
	1	0	1	$[L_a \cap \overline{L_b}] \cup z_0$
	1	1	1	$[L_a \cap L_b] \cup z_0$
NOT	0		1	$L_a \cup z_0$
	1		0	$L_a \cup z_1$

$\cup$ stands for union, $\cap$ represents intersection, and $\overline{\ }$ complementation

Singular cover tables

Function	Essential prime implicants: Karnaugh	Essential prime implicants: table
AND		Singular cover: AND a b z 0 X 0 X 1 0 1 1 1
NAND		Singular cover: NAND a b z 0 X 1 X 0 1 1 1 0
OR		Singular cover: OR a b z 1 X 1 X 1 1 0 0 0
NOR		Singular cover: NOR a b z 1 X 0 X 1 0 0 0 1
XOR		Singular cover: XOR a b z 1 0 1 0 1 1 1 1 0 0 0 0
XNOR		Singular cover: XNOR a b z 1 0 0 0 1 0 1 1 1 0 0 1
NOT		Singular cover: NOT a z 1 0 0 1

D-calculus (1)

D-intersection defines how different D-cubes coexist for different gates in the circuit

This set of rules is applied in the propagation phase, where D must be propagated to a primary output, and justification phase

∩	0	1	X	D	$\overline{D}$
0	0	ϕ	0	Ψ	Ψ
1	ϕ	1	1	Ψ	Ψ
X	0	1	X	D	$\overline{D}$
D	Ψ	Ψ	D	μ	λ
$\overline{D}$	Ψ	Ψ	$\overline{D}$	λ	μ

ϕ empty, Ψ undefined, λ or μ requires inversion of D and $\overline{D}$

D-calculus (2)

ϕ empty, Ψ undefined:

- the cubes are incompatible
- meeting a Ψ and ϕ during the progression of the algorithm means that the proposed solution is not viable → backtrack to another solution

example: intersection of cubes 0XX and 1XX

$0XX \cap 1XX = \phi\ XX$

these two cubes cannot coexist

λ or μ requires inversion of D and $\overline{D}$:

- if both λ and μ occur during D-intersection, then the cubes are incompatible
- if only μ occurs, then $D \cap D = D$ and $\overline{D} \cap \overline{D} = \overline{D}$
- if only λ occurs
  1. transform the second cube as follows: $D \rightarrow \overline{D}$ and $\overline{D} \rightarrow D$
  2. then, apply D-intersect again, considering the μ rule described above

March test notation (1)

Following notation is standard in the description of memory testing protocols

Notation	Action
r	read operation
w	write operation
r0	read a 0 from the memory location
r1	read a 1 from the memory location
w0	write a 0 to the memory location
w1	write a 1 to the memory location
↑	write a 1 to a cell containing a 0: the cell has a rising transition
↓	write a 0 to a cell containing a 1: the cell has a falling transition
↕	complement the cell contents
∀	any memory write operation
⇑	increase memory address
⇓	decrease memory address
⇕	addressing order can be either increasing or decreasing