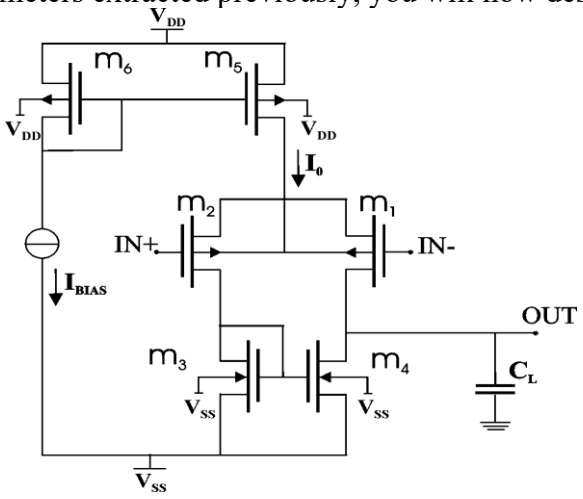
| Parameter | | Value Extracted | Unit | |
|---|---|---|---|---|
| $K_p$ | PMOS | 90 | $\mu A/V^2$ | 64nm CMOS Technology<br>$V_{DD}$= 1.2 V<br>$V_{ss}$ = 0V |
| | NMOS | 220 | | |
| $U_a$ | PMOS | 10 | V/µm | |
| | NMOS | 14 | | |
| $V_{T0}$ | | 0.4 | V | |
| n | PMOS | 1.25 | - | |
| | NMOS | 1.2 | | |
| $C_{ox}$ | | 13 | $fF/\mu m^2$ | |
| $C_{ov}$ | | 0.2 | fF/µm | |

# 1. OTA design

Using the technology parameters extracted previously, you will now design a simple OTA.




## 1.1. Specifications

The circuit will be designed to meet the following specifications, which will be verified by simulation.

| Parameter | Unit<br>Specification | |
|---|---|---|
| Open-loop: Gain: $\mathbf{A_0}$ | ≈ 35 dB (56) | dB |
| GBW: $\mathbf{f_{GBW}}$ | 25 | MHz |
| Slew rate: **SR** | 20 | V/µs |
| Load Cap: $\mathbf{C_L}$ | 1 | pF |
| $\mathbf{I_{F,5}}$ | 10 | |
| $\mathbf{I_{BIAS}}$ | 10 | µA |

## 1.2. Sizing:

The OTA will now be sized. Calculate the following parameters in the proposed order.

| | Parameter | Expression | Value | Unit | Guideline |
|---|---|---|---|---|---|
| Bias | $I_0$ | | | µA | |
| | $\frac{W_5}{L_5}$ | | | µm | $L_5 = 0.5\mu m$ |
| Differential pair | $g_{m2}$ | | | µS | *GBW* |
| | $\frac{g_{m2}}{I_{d2}}$ | | | $V^{-1}$ | |
| | $I_{F1,2}$ | | | - | $I_F = I_c$ *is the inversion factor* |
| | | | | | *Strong or weak inversion* |
| | $\frac{W_{1,2}}{L_{1,2}}$ | | | - | |
| | $R_{out}$ | | | kΩ | $A_o$ |
| | $L_{1,2}$ | | | µm | $R_{out}$, $L_4=L_2$ |
| | $W_{1,2}$ | | | µm | |
| | $\frac{W_4}{L_4}$ | | | - | $I_F = 10$ |
| | $L_4$ | | | µm | $L_2=L_4$ |
| | $W_4$ | | | µm | |
| | $g_{m4}$ | | | µS | $\frac{g_m}{I_D} =$ |

## 1.3. Determine analytically

- **the poles (dominant and non dominant)**
- **the phase margin PM**
- **the common mode input range $CMIR^+$/ $CMIR^-$**
- **the output swing**

| | Analytical expression | Numerical value |
|---|---|---|
| **A [dB]** | | |
| **$f_{dom}$ [Hz]** | | |
| **$f_{nondom}$ [Hz] (neglect junction cap $C_{SB}$, $C_{DB}$)** | | |
| **PM** [°] | | |
| **$CMIR^+$** [V] | | |
| **$CMIR^-$** [V] | | |
| **$V_{OUTmax}$** [V] | | |
| **$V_{OUTmin}$** [V] | | |
| **$\Delta V_{OUT}$** [V] | | |

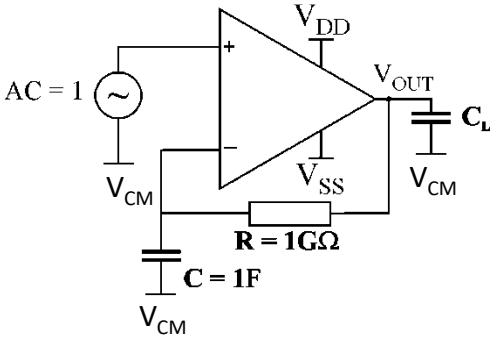
## 1.4. Design verification & Performance simulation

Using a prepared set of test-benches, the OTA performances will be verified by simulation.

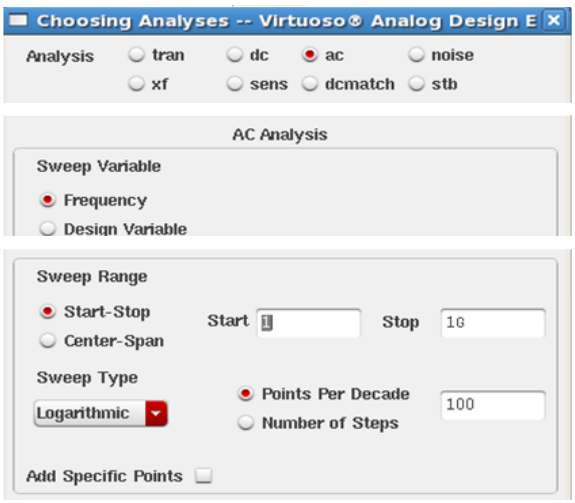
1. Open the OTA_65n schematic
2. Set all transistor sizes according to your design

### 1.4.1. Operating point and Open-loop gain

- The test-bench used to simulate the Dc and AC behavior of the OTA is the following:



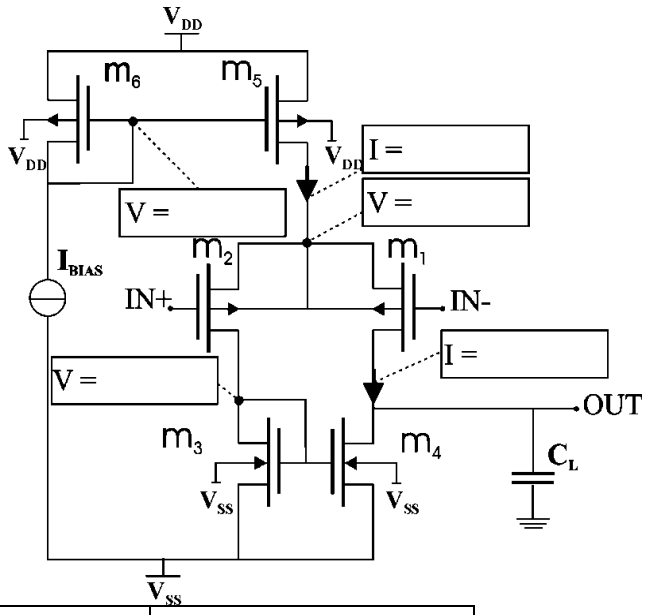

1. Open the Testbench TB_OTA_DC_AC schematic
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**
4. Create New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test choosing **DC_Analysis** and select **Save DC operation Point.** (you can change the default test name to **DC_Test**))
7. Define a new test choosing **AC_Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to **AC_Test**).
8. Define for AC_Test the following expression to be plotted:
   **open loop gain ? dB20(VF("/VOUT_OL"))**
   **open loop phase ? phase(VF("/VOUT_OL"))**
9. Save, Run and Report the values on the following schematic, and fill-in the tables below and verify that they correspond approximately to theory (your calculations).



**Note:** To display the simulation results

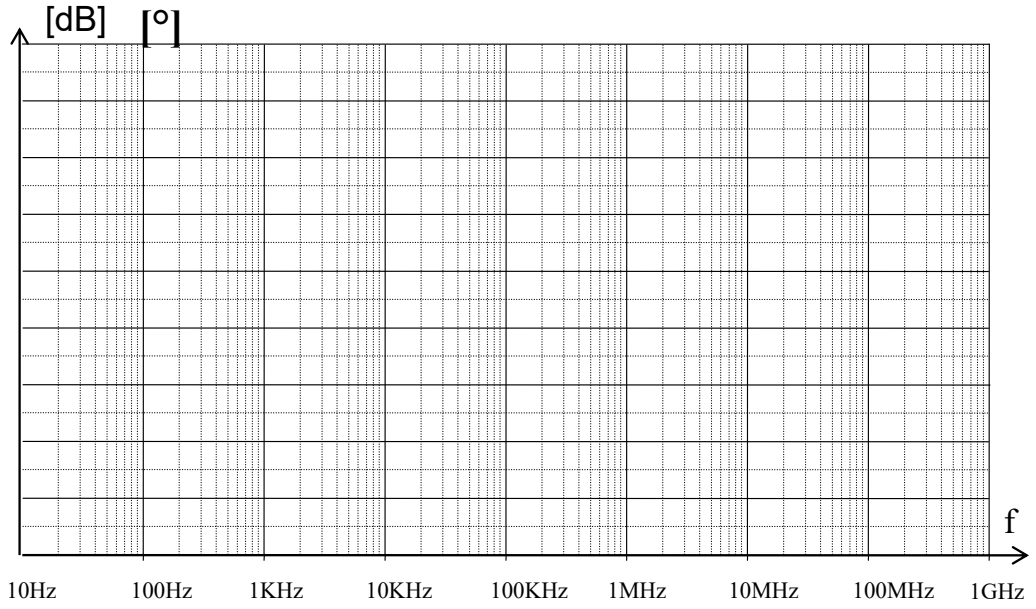
- Descend in the hierarchy to the schematic level of the OTA
- Select **maestro** tab
- Select **Results** tab
- Right click on **OP_Test** and select:

1. **Annotate→DC Node Voltages**
2. **Annotate→DC Operating Points**




| | calculated | simulated |
|---|---|---|
| **Dominant pole** [kHz] | | |
| **Non-Dom pole** [MHz] | | |
| **PM** [°] | | |
| **$A_0$** [dB] | | |
| **$f_{GBW}$** [MHz] | | |

**Provide the hand painted Bode plots for magnitude and phase:**

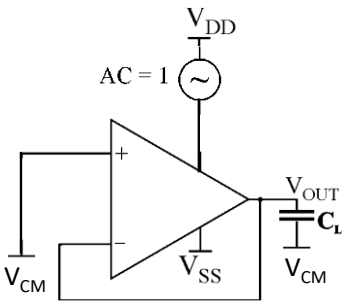


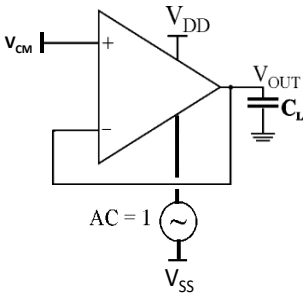

**Comment briefly on the stability:**

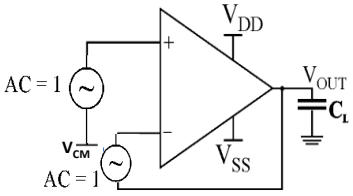
……
……
……

### 1.4.2. Power supply and Common mode rejections ratio (PSSR+, PSSr- & CMRR)

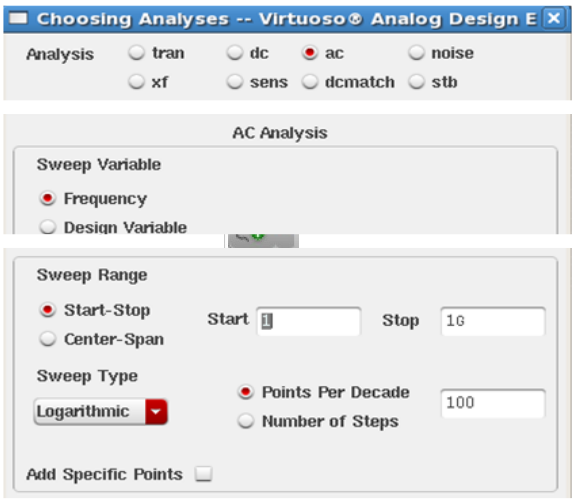
The test-bench for measuring the OTA PSSR + ; PSSR- and CMRR are:




1. Open the Testbench TB_OTA_PSRR_CMRR schematic
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**
4. Create New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test choosing **AC_Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to **AC_Test2**).
7. Define for AC_Test2 the following expression to be plotted:
   **(-dB20(VF("/VOUT_PSRR+")))**
   **(-dB20(VF("/VOUT_PSRR-")))**
   **(-dB20(VF("/VOUT_CMRR")))**
8. Save, run and report the values on the following schematic, and fill-in the tables below and verify that they correspond approximately to theory (your calculations).



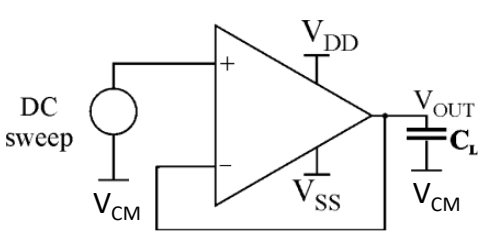

| | **Simulated @ low fréquency** |
|---|---|
| **PSRR$^+$** [dB] | |
| **PSRR$^-$** [dB] | |
| **CMRR** [dB] | |

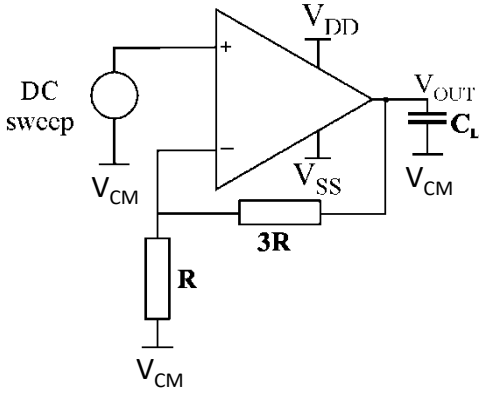
**Explain briefly the equations used:**

……
……
……
……
……
……

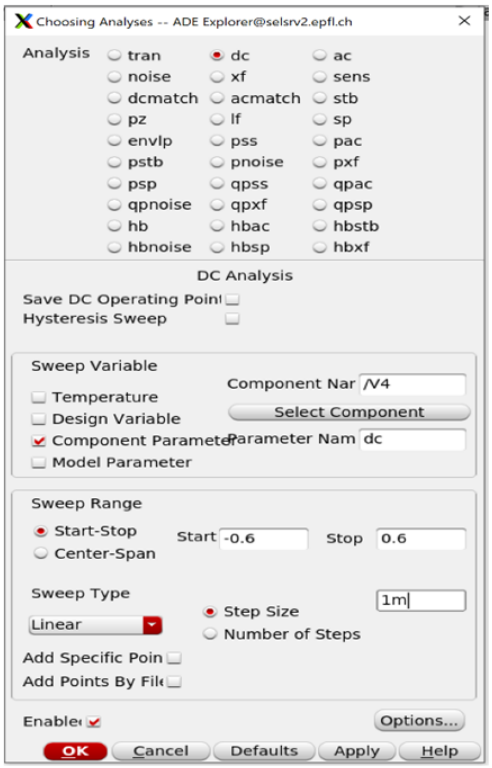
### 1.4.3. Input common-mode range

The test-bench for measuring the OTA input common-mode range and output range are :




1. Open the Testbench TB_OTA_CMIR_DVout
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**Create
4. New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test and choose **DC Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to *DC_Test*).
7. Define the following expression to be plotted:
   **Common mode input range → deriv(VDC ("/VOUT_CMIR"))**
   **VDC("/VOUT_SW")**
   **Output swing → deriv(VDC("/VOUT_SW"))**
8. Save, run the simulation and fill in the table below.




Measure the input and output ranges for a maximun gain variation of -10 %

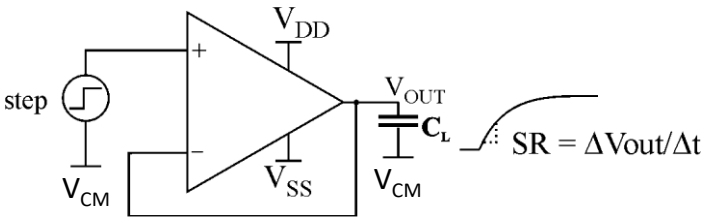
| Parameter | Value | | Unit |
|---|---|---|---|
| | Simulation | Optimized | |
| Input CMR+ | | | V |
| Input CMR- | | | V |
| Output Range+ | | | |
| Output Range- | | | |

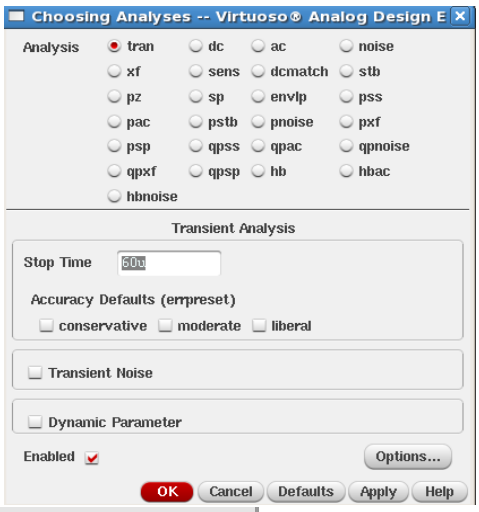
***NOTE:*** *For the Output Swing, group /VOUT_SW and deriv(VDC("/VOUT_SW")) plots in the same subwindow in Virtuoso and Analysis Waveform XL.*

- *Select the subwindow with the two signals*
- *select the deriv(VDC("/VOUT_SW")) signal and then select Axis →Y vs Y.*

### 1.4.4. Slew rate

The test-bench for measuring the slew-rate is:




1. Open the Testbench_OTA_SlewRate
2. Start the simulation environment: Launch ADE Assembler
3. Open Existing View
9. Load "maestro"
10. Define a new test and choose **tran Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to SR_*Test*)**.**
11. Define the following expression to be plotted:
    **Slew Rate → deriv(VT("/VOUT_SR"))**
12. Run the Simulation and fill in the table below.

| Parameter | Value | | Unit |
|---|---|---|---|
| | Simulation | Optimized | |
| SR+ | | | V/µs |
| SR- | | | V/µs |