Full-Custom Analog Design
Lab 1: Technology parameters extraction

1. Setting up your working environment

If you did not attend the EDA lab session of the course "Fundamentals of VLSI Design", you will need to create the file EE429_FULLCUSTOM and set up your working environment beforehand.

The detailed procedure is described in the document EDALAB2025_LAB01.pdf on Moodle.

Note: Executing commands and actions are enclosed in frames like this one.

1. Connect to the VDI workstation and to the jet cluster, go to the directory EE429_FULLCUSTOM and extract the library of your lab.

[1] username@jed.hpc.epfl.ch> cd EE429_FULLCUSTOM ↲

> gtar -xvf /softs/classroom/tutorials/2024-2025/EE435/Lab1_Techno_OTA.tar.gz

2. Run the cadence.

Run Virtuoso by typing: > virtuoso & ↲

3. Create a link to the lab1 library:

In the Library Manager (Tools→Library Manager), click Edit → Library Path Editor, add library Lab1_Techno_OTA

2. Technology parameters extraction

Before designing circuits, you will extract and verify the values of the most important technology parameters. A simulation setup has been prepared for each parameter. Your task is to understand them and run the corresponding simulations to familiarize yourself with the 64nm technology.
The values of all the 64nm technology parameters are presented in the table below. Report the average values you obtain through simulations.

Parameter		Value: Extracted	Value: Simulation	Unit	
K_p	PMOS	90		$\mu A/V^2$	V_{DD}= 1.2 V, V_{ss} = 0V
	NMOS	220			
U_a	PMOS	10		V/µm	
	NMOS	14			
V_{T0}		0.4		V	
n	PMOS	1.25		-	
	NMOS	1.2			
C_{ox}		13		$fF/\mu m^2$	
C_{ov}		0.2		fF/µm	

2.1. Normalized transconductance K_p

The K_p value will first be extracted for NMOS and PMOS transistors with W =10u and L = 400nm. Then, a large range of dimensions will be explored, and the variability of K_p will be verified.

1. Open the Kp schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Plot All → Explore and analyze the variability of Kpn and Kpp vs L and W

Write the equation used to simulate Kp and give its maximum value for W/L=10/0.4

Parameter	Equation	Value	Unit
k_{pn}			
k_{pp}			

2.2. g_m/I_d

The g_m/I_d curve will first be plotted for NMOS and PMOS transistors with W =10u L = 400nm. Then, a large range of dimensions will be explored.

1. Open the GmOverId schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Plot gm/Id → Explore and analyze the results
8. Verify the value given for the technology parameter "n".

Write the equation and values of is_n and is_p

Parameter	Equation	Value	Unit
is_n			
is_p			

2.3. Early voltage U_a

The Early voltage will first be extracted for NMOS and PMOS transistors with W =10u and L = 400nm at $I_F = 4$. Then, a large range of transistor lengths will be explored.

1. Open the U_a schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Extract Uan and Uap
8. Plot All → Explore and analyze the results

Observe the effect of increasing L on r_{on} and r_{op}. Does the output resistance increase when L increases, and how efficiently?

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