Your ALU-8 bit project Overview and Guidelines

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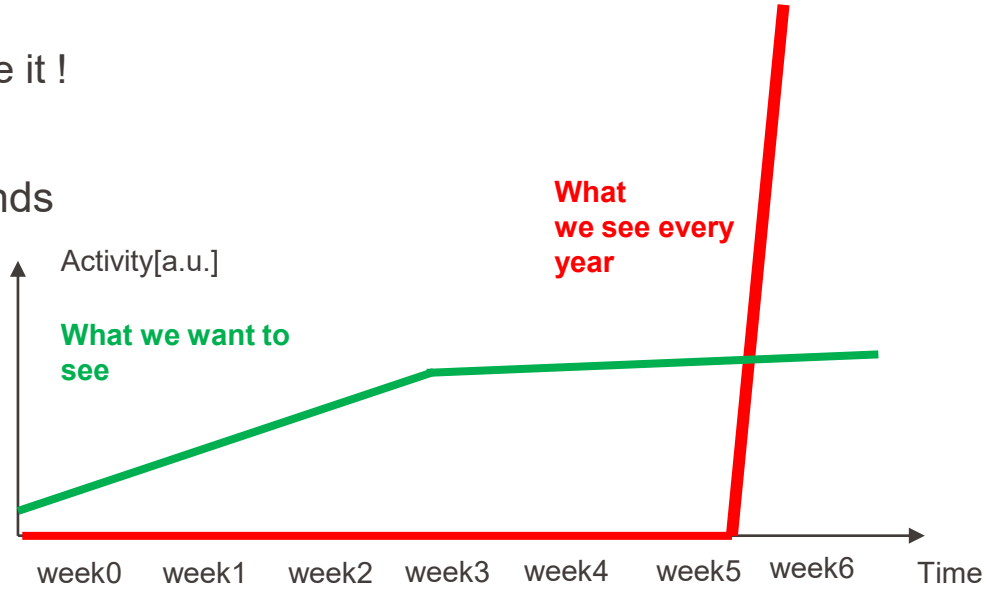
General Information

- During the sessions : Teaching assistants will be available for help and support.
  - Ask for help when you need some, but be mindful as you are a lot.
  - If the session is intense (i.e., TAs being extremely busy), and your question is not urgent, prioritize the forum.
- Use the forum !
  - **USE IT**
  - Don’t wait for the last week(end) to use it !
- We are here to help
  - But let us rest during nights and weekends



Deadline management

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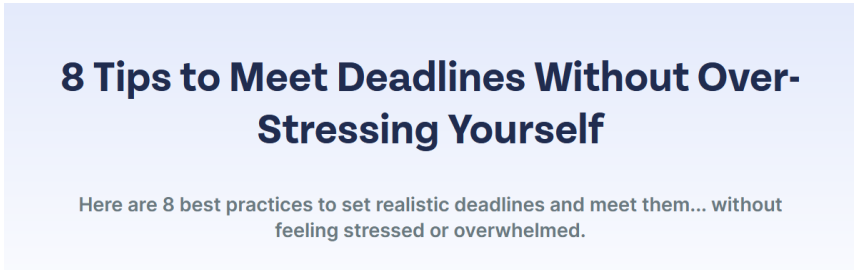
- You will always have to deal with deadlines in your life
- Deadline management is not innate

8 tips to meet your deadlines

1. Communicate a clear deadline
2. Break down the project
3. Have a start and completion date for each step
4. Block off time on your calendar
5. Focus on action (vs. motion)
6. Communicate progress with your team
7. Add a buffer time
8. Don’t overcommit



Basic Rules of Engineering

Four simple rules

- **Engineers are lazy**

If something takes too long, you are doing something wrong.

- **Divide and Conquer**

Divide complex problems into a collection of smaller simpler problems, solve one by one.

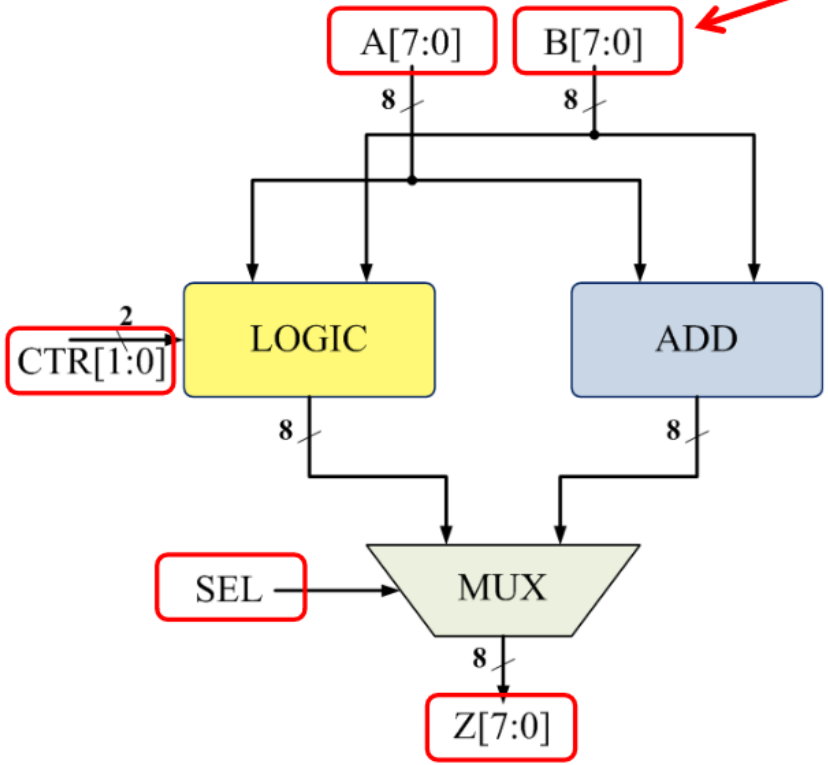
- **Simple and Regular**

Try simple and regular structures, they are easier to design and debug.

- **Engineering is not a religion**

Find the solution that best fits your problem

Our Project: ALU



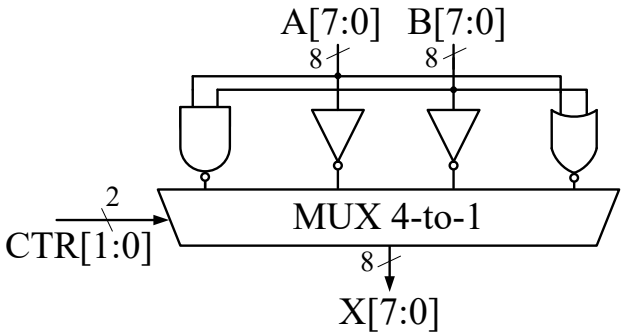
Please keep the pin naming as specified!!

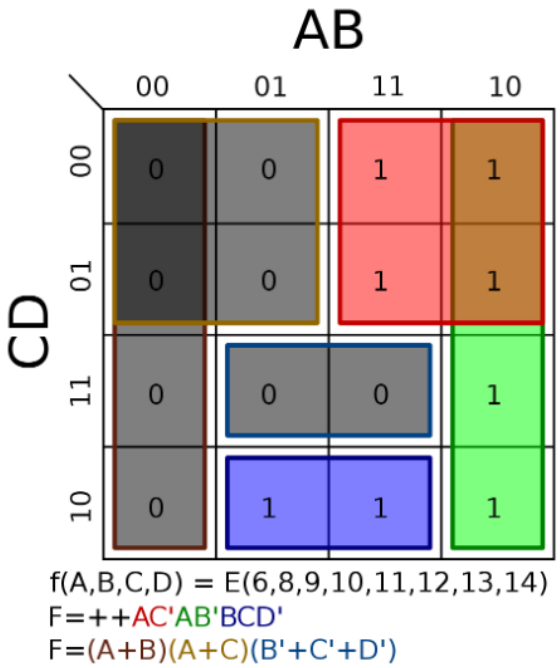
…in Cadence, use <> instead of []).

This will be graded!!!

Logic Block

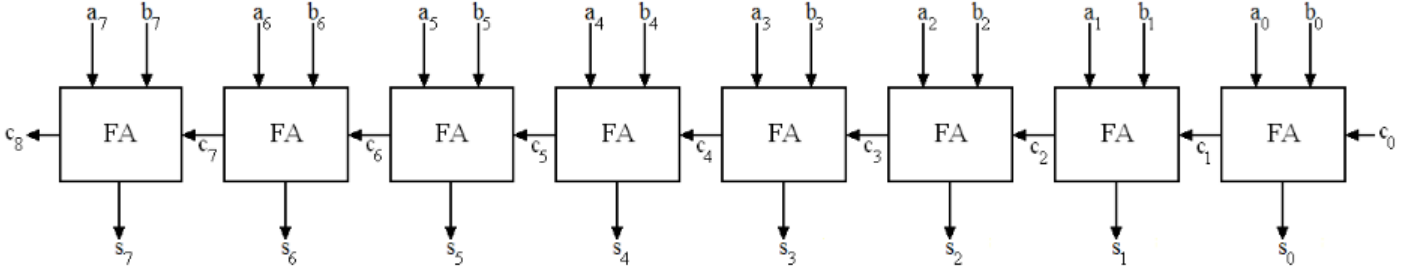
- Not in the critical path
- Use the Karnaugh table to optimize it.
- In CMOS quite simple:
  - MOS:
    - AND -> Parallel
    - OR -> Series
  - NMOS:
    - AND -> Series
    - OR -> Parallel





Adder

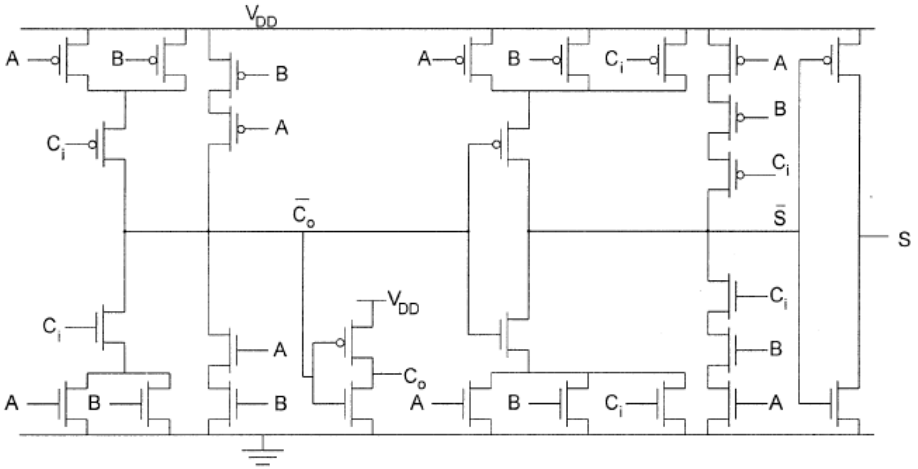
- Carry Ripple Adder



- Identify the critical path**s** and **Optimize THEM**
- Two approaches are possible

Adder

- Karnaugh-based approach
  - Mirror topology

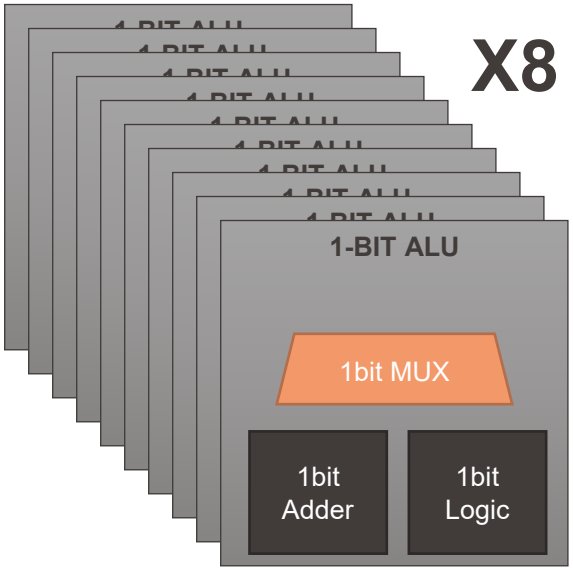


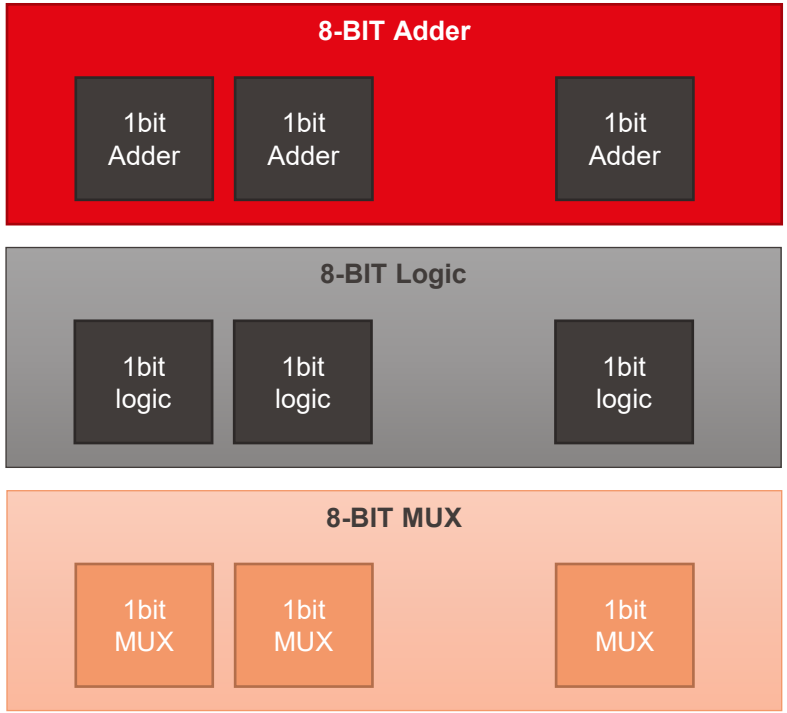
- Logic-based approach

OPTIMIZE IT !

Top – hierarchy – physical design

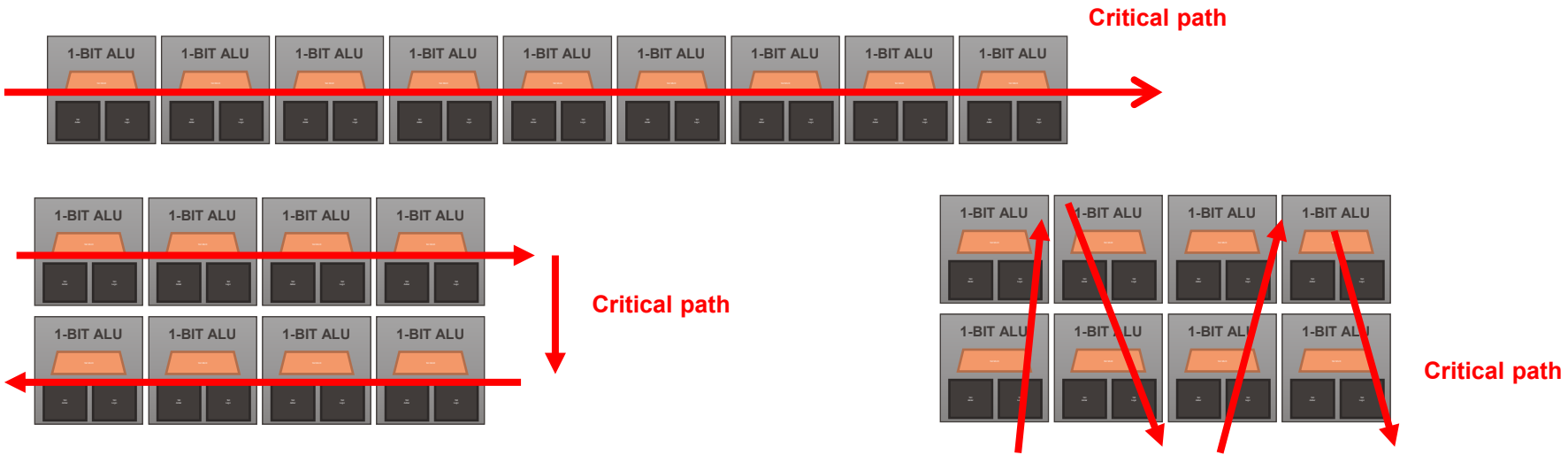
- Chose a hierarchy first !





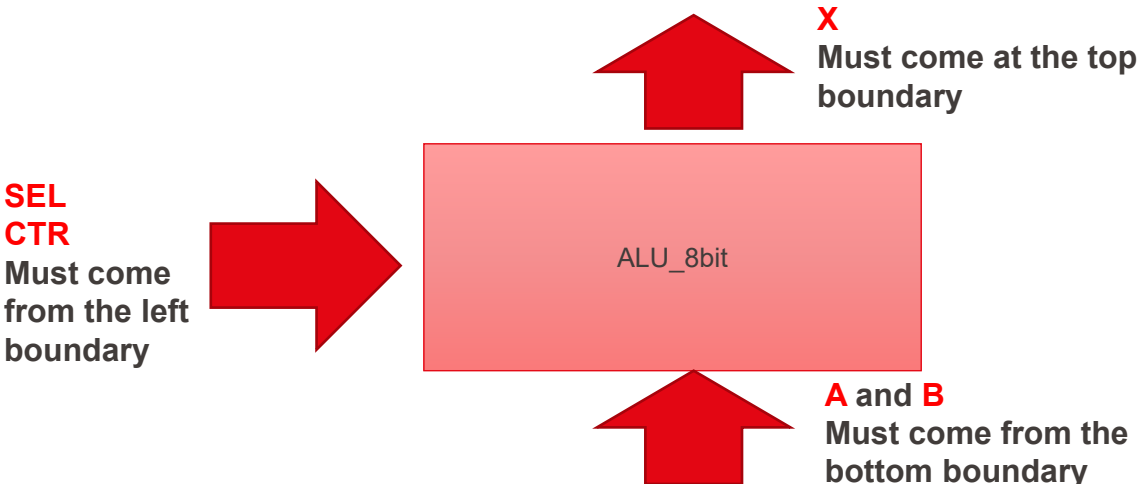
Top – hierarchy – physical design

- Chose a hierarchy first !
- Define a floorplan !



Top – hierarchy – physical design

- Chose a hierarchy first !
- Define a floorplan !
- Think about the input outputs !
  - This will have an impact on your floorplan

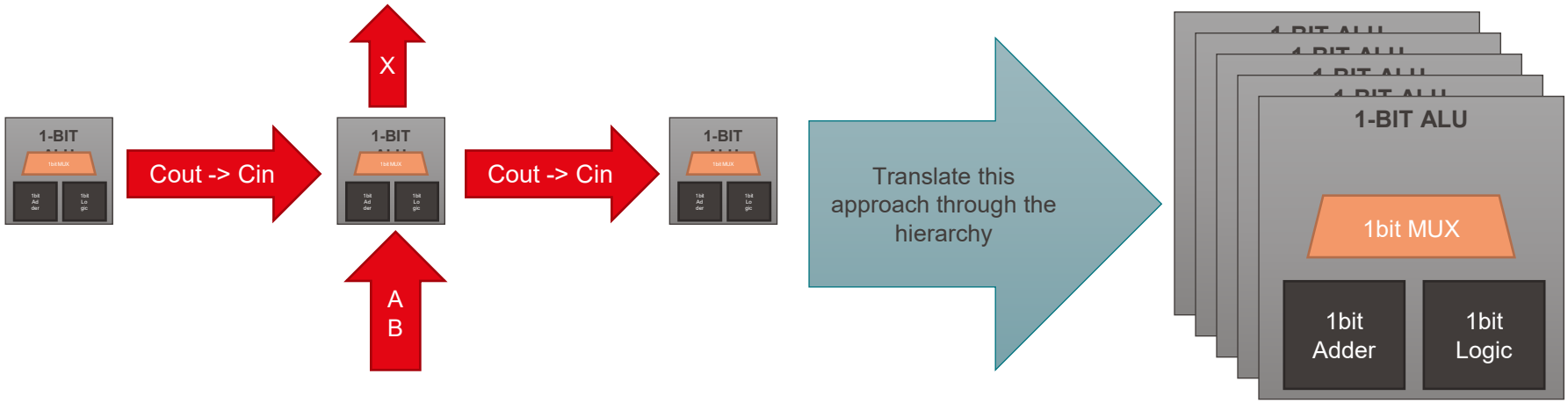


Top – hierarchy – physical design

- **Chose a hierarchy first !**
- **Define a floorplan !**
- **Think about the input outputs !**
  - This will have an impact on your floorplan
- **Think about properly placing your TAP cells**
  - Make sure you properly bias the cells substrates
- **Think about your power structure.**
  - Place your power pins on the boundary of Metal 4 for the 8bit ALU.

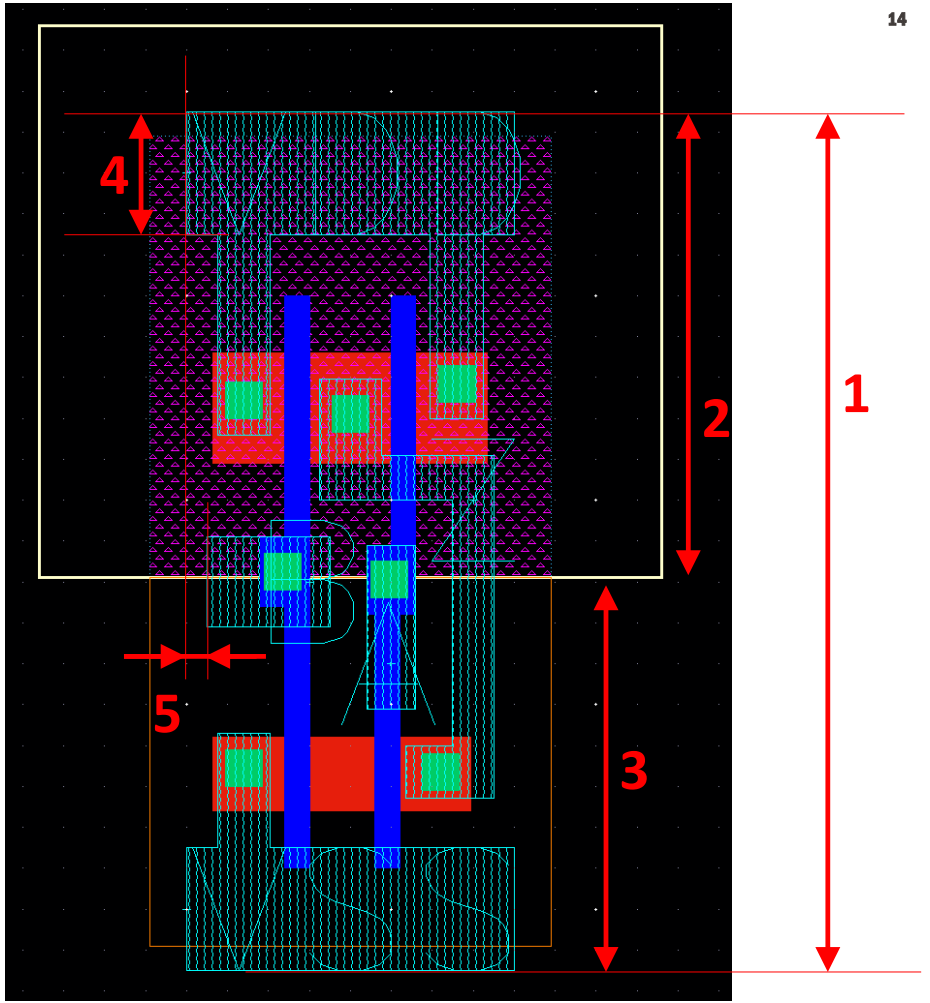
Signal flow ?

- Identify where signals come in, and where they need to come out.
- This will drive the design of the cells.



Layout ?

- Define the height of your cells
- Ease your life by making things generic
- Build everything with the same standards
- Keep your polysilicon vertical



Routing ?

- Make the routing hierarchical
  - Use low level wires to connect local connections
  - Use higher level wires for longer connections
- In the cells: keep local routing … local
  - In logic gates (NAND, NOR, etc)
    - Polysilicon and M1
  - In more complex transistor-based gates (Adder, Logic)
    - You can use M2
- Define a routing utilization case and a direction per metal
  - Polysilicon (PO) → only for gates. NEVER route using PO
  - Metal 1 → used for local connections. Can be used in all directions
  - Metal 2 → a good practice is to define an orientation and stick to it
  - Metal 3 → make its orientation orthogonal to ME2
  - Metal 4 → same wrt ME3 etc.

Power routing ?

- What about the IR drop ?

$$U = RI$$

  - A too resistive power grid leads to voltage drops
- Voltage drops make gates locally slower
- Leads to timing failures, accelerated aging etc.
- Limits the performances

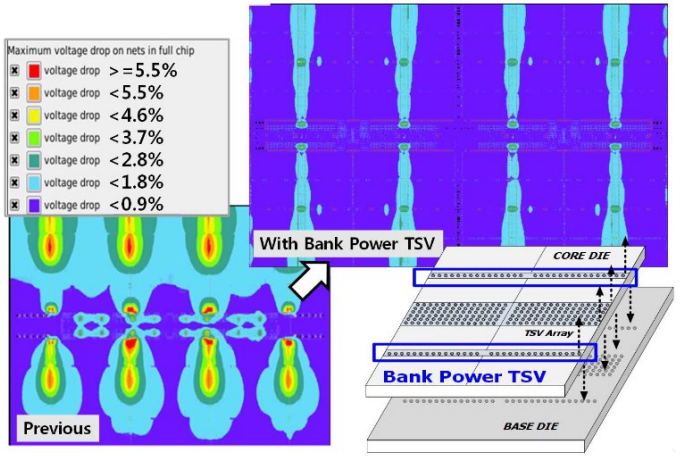
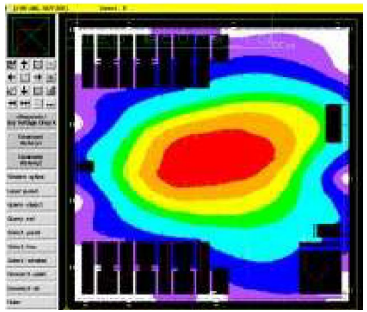


Figure 12.3.4: Power TSVs in the middle of banks and power distribution network simulation results.



https://ieeexplore.ieee.org/abstract/document/8310257
https://ieeexplore.ieee.org/document/1271098

Power routing ?

- What about the IR drop ?

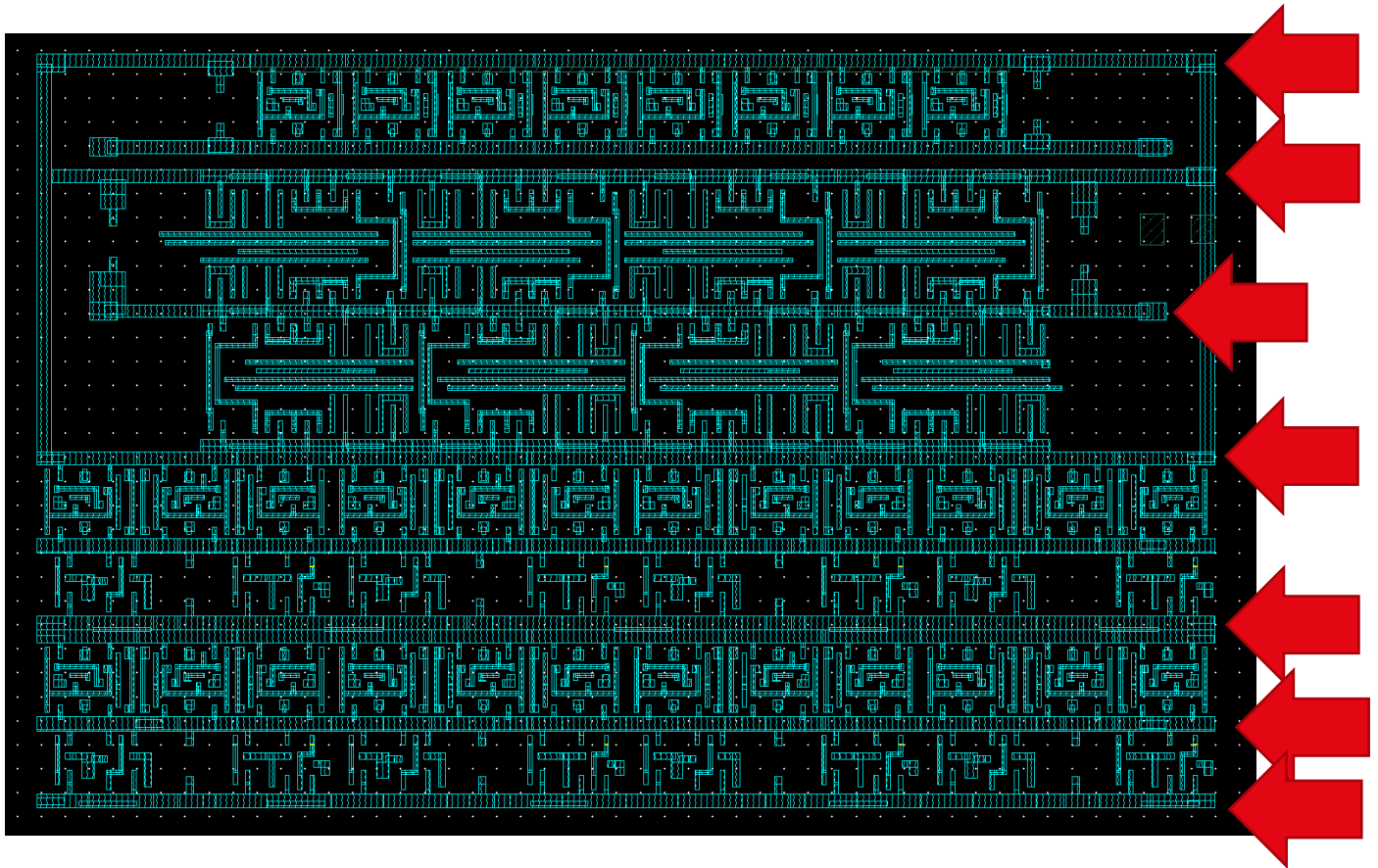
$$U = RI$$

- You can't do much about the current
- So… reduce R

https://ieeexplore.ieee.org/abstract/document/8310257
https://ieeexplore.ieee.org/document/1271098

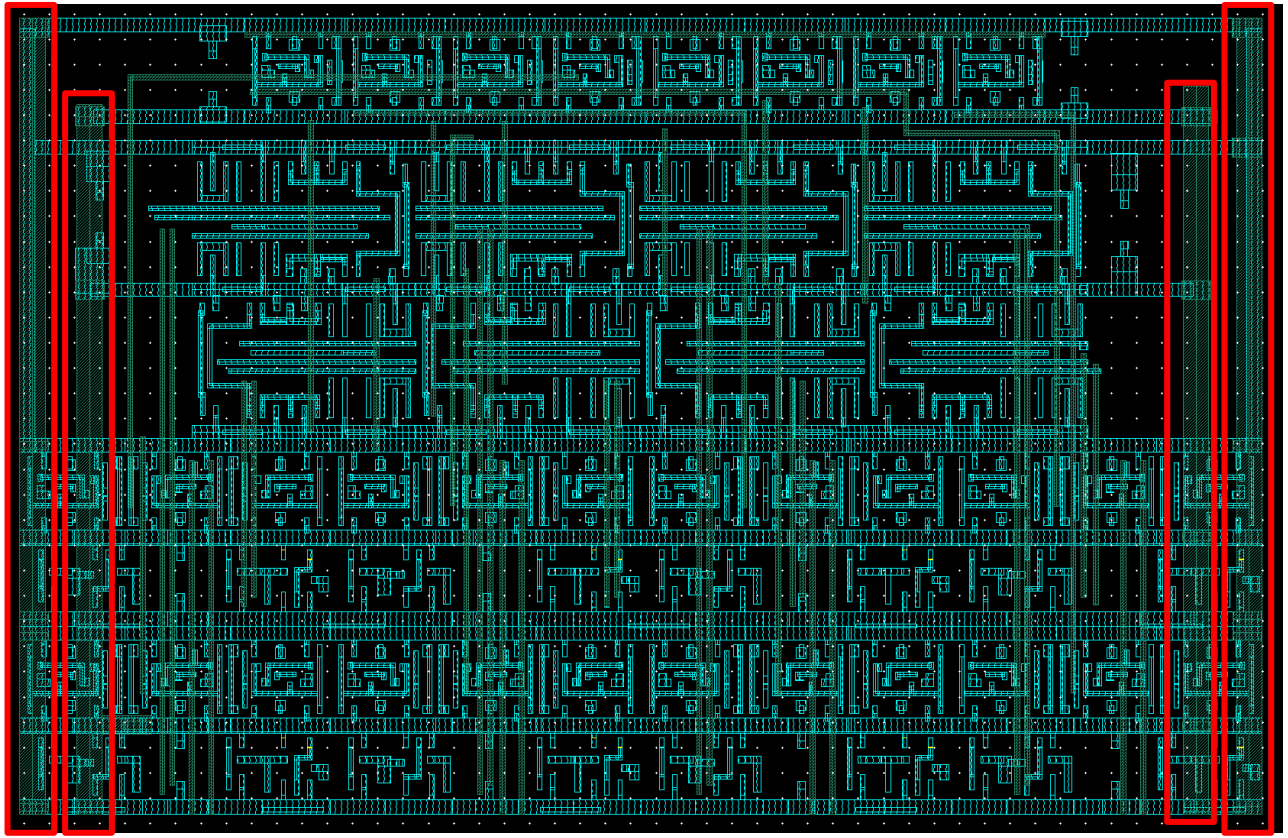
Power routing ?

LARGE M1 VDD and GND lines



Power routing ?

LARGE M3 VDD and GND lines

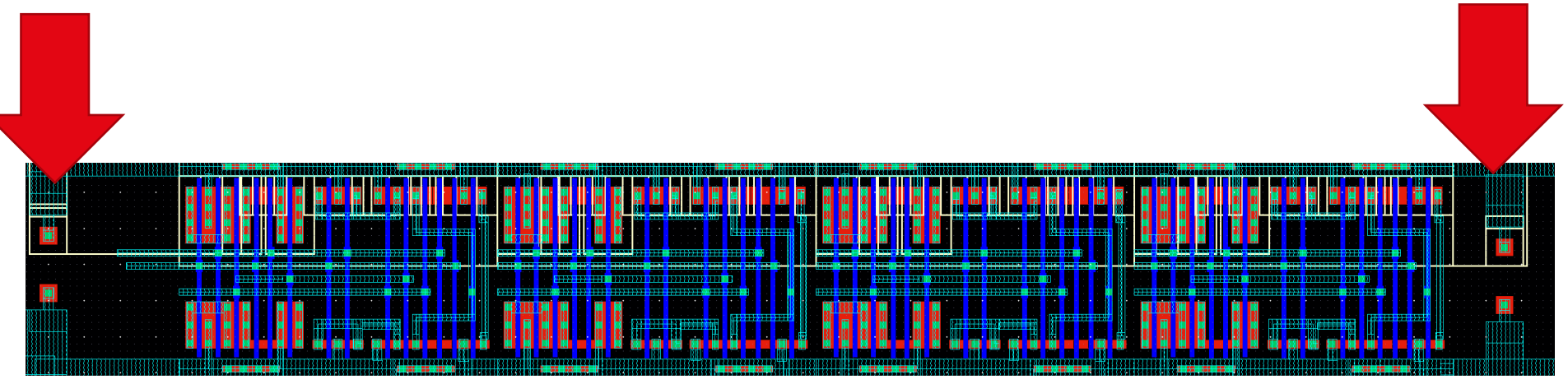


Power routing ?

- **Put your VDD and GND pins on ME4, on one of the edges of the circuit**
- Make sure you have designed a power grid which minimizes R (dense enough)
- Make it balanced.
  - If you have a long ME1 line, try connecting it on both ends
- Make it bigger and bigger
  - There is no absolute rule, it all depends on your circuit consumption. But we could consider that a 500nm wide ME4 line can be enough.
- Put enough vias (they are resistive)

Biasing the substrate – TAP cells

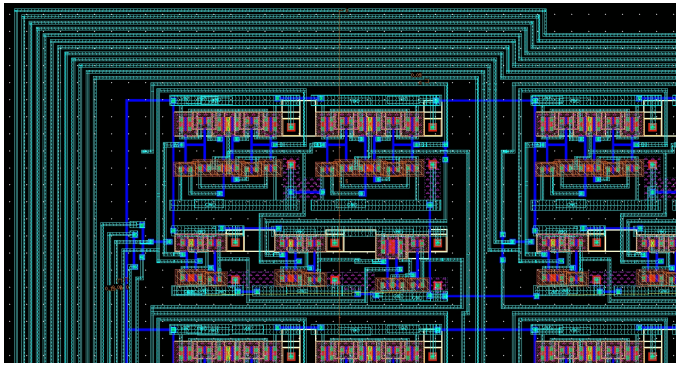
- Foundry guideline is 30um between two tap cells
- Good practice. If you have a row, put one tap cell on both ends.
- More tap cells means better protection to latch-up but… more area



General guidelines

- Keep the cell and pin naming and the functionality as agreed
- Do not flatten your blocks!!!
- Feel free to use Layout L or GXL (it might help you… or not)
- Perform DRC as often as you can
- Do LVS for every hierarchy level
- Extracted netlist must follow the rules described in the tutorial
- Try to size transistors, re-design and optimize, but do not over-do-it (You only have 3 weeks !!!)

General guidelines



Don’t do that !

- Don’t be afraid to use higher metal levels
  - Try to not go above m5
- Do not use poly to route signals
  - Only for gates
- Try to minimize poly length
- Vias are resistive, but if you have space, you can put 2 ?
- Better have an over-designed power grid than an under-designed one

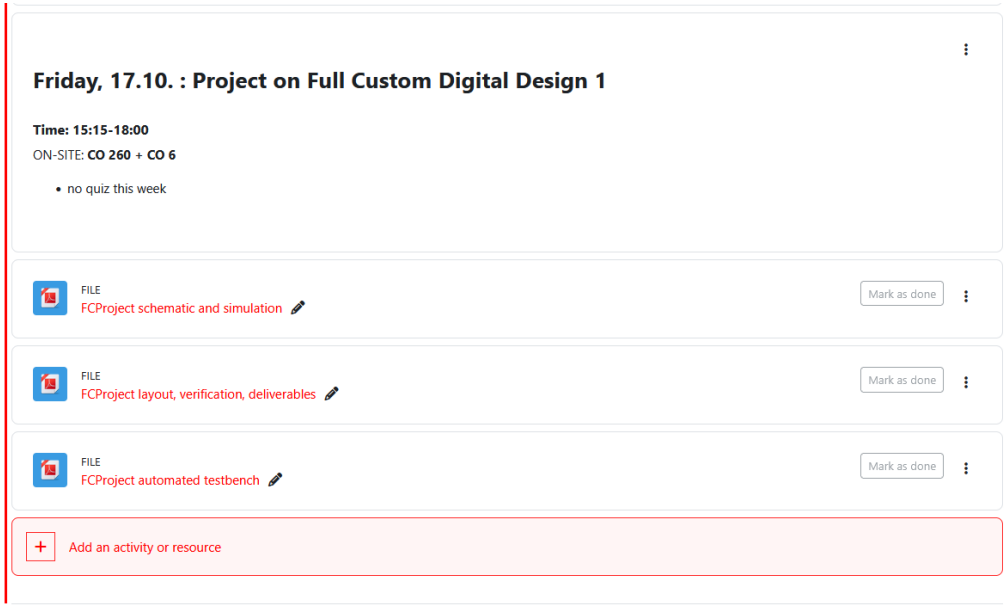
How can we help you ?

- We provide an automated testbench
- Verify the functionality
- Verify the speed of the circuit

- Your grading will be based off what the automated tester gives

Supporting documents

- Everything is available on moodle
- Supporting documents contain the same as these slides



Grading...

- Functionality (**should be correct, otherwise your project fails**)
- Area (500um2) and delay (1ns) specifications (**should be met, otherwise your project fails**)
- Circuit performance in terms of area and speed
- Cell names, pin names, file names, and top level symbol
  - The top view shall be called ALU_8BIT_PEX
- **No DRC and LVS errors in top level layout**
- Layout regularity, floorplan, and the width of the power supply lines
- **Read the supporting documents carefully!**

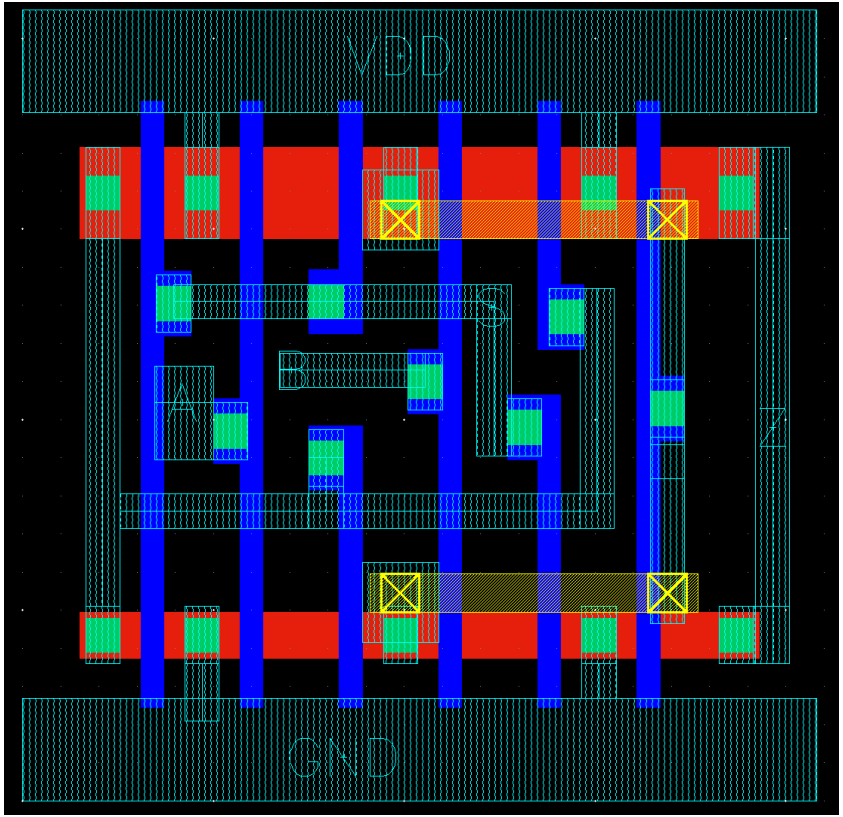
Deliverables...

- A set of slides explaining your design
  - Screenshots
  - Critical path identification
  - Speed
  - Area
- A tar.gz file (archive) of your design library
- The netlists of schematic and PEX circuits

MUX 2-1

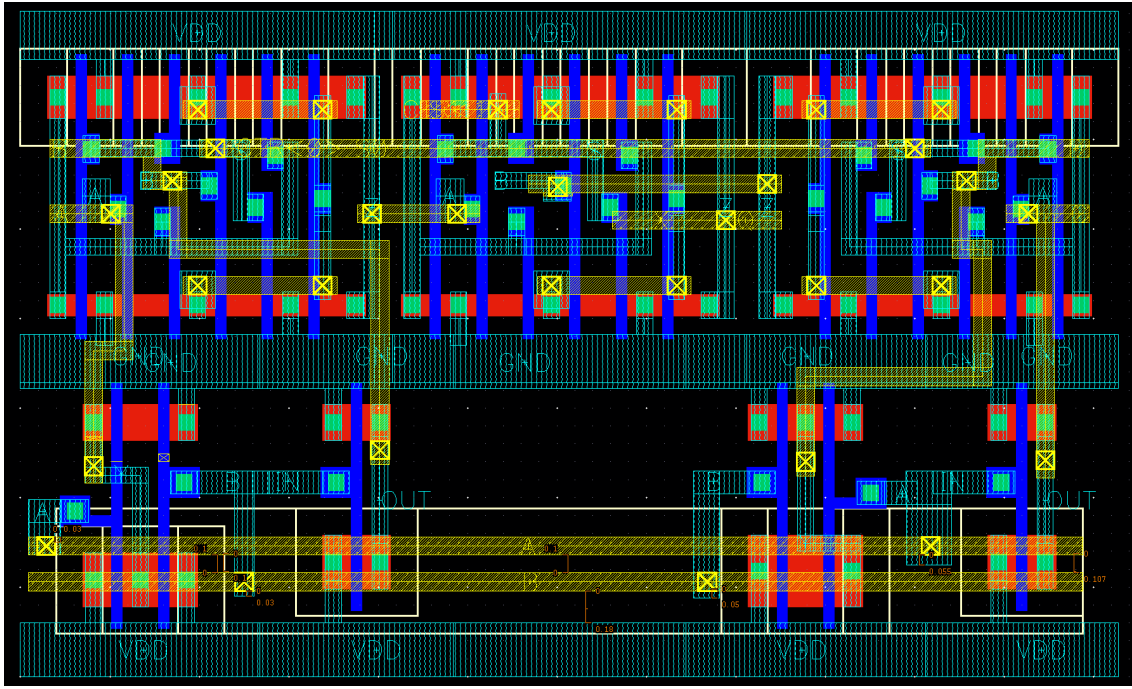
- Poly use only for the gates
- M1 in all directions fir local connections
- M2 used only horizontally here.

- Input pins A, B and S designed to cover for minimum area DRC check



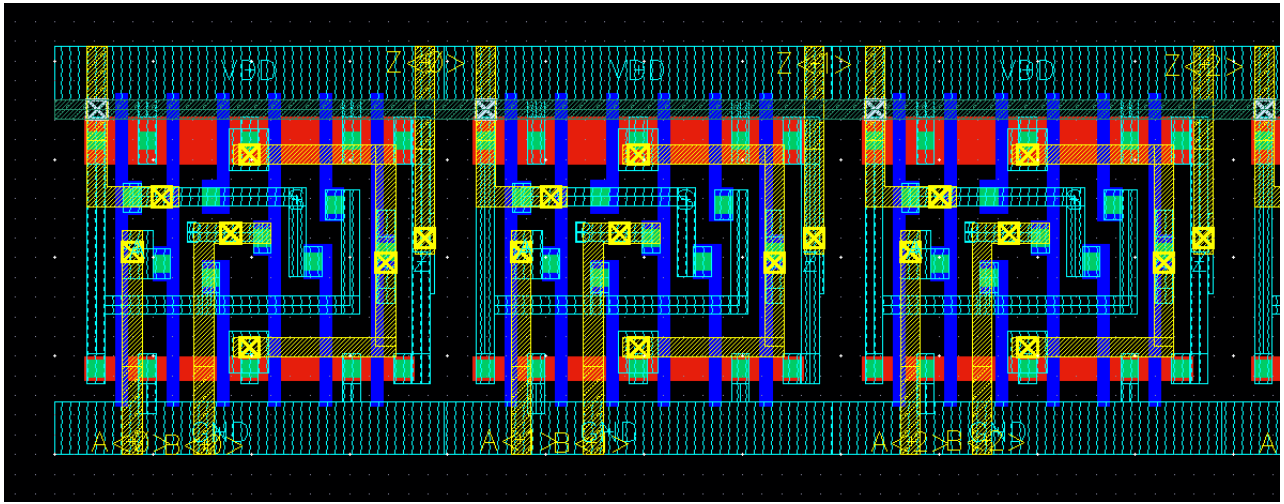
Logic gates with MUX

- This does not 100% follow the guidelines
- Generally M2 always in the same direction
- Here it would be difficult to connect from left to right through M2 because of the vertical M2
- Gates being vertically abutted
  - GND merged and VDD merged
  - One row over two is flipped
  - Merge NWELL

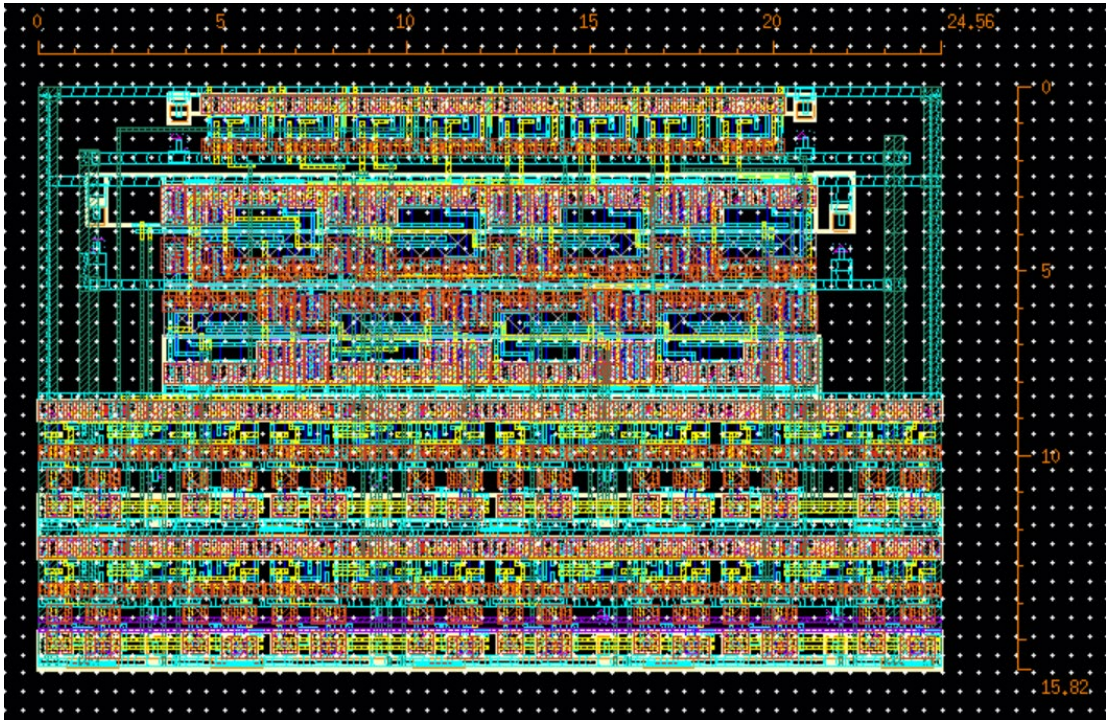


Some Muxes

- Inputs and outputs will drive your design
- You must take these into account !
- Here, A, B and Z are placed where expected to be used



My design



25um * 16um = 400um2

- Your goal for a 4 is 1ns.
  - Let's pass under 500ps ! (bonus points to take there)
- Your area must be lower than 500um2

- Challenge yourself, try to see how fast you can go with the logic-based adder.

Good luck and enjoy the project

Do You Have Questions?

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